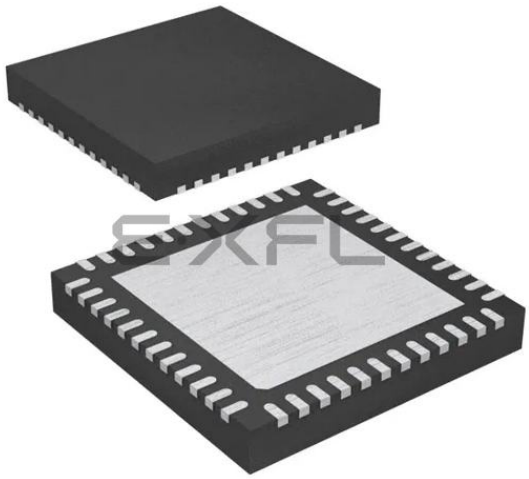

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Details	
Product Status	Obsolete
Applications	Battery Monitor
Core Processor	S12
Program Memory Type	FLASH (128kB)
Controller Series	HCS12
RAM Size	6K x 8
Interface	LIN, SCI, SPI
Number of I/O	8
Voltage - Supply	2.25V ~ 5.5V
Operating Temperature	-40°C ~ 105°C
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN-EP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mm912j637av1ep

Table of Contents

Table 4. MM912_637 Pin Description

Pin #	Pin Name	Formal Name	Description
28	VTEMP	Temperature Sensor Input	External temperature sensor input. See Section 5.6, “Temperature Measurement - TSENSE".
29	TSUP	Temperature Sensor Supply Output	Supply for the external temperature sensor. TSUP frequency compensation option to allow capacitor CTSUP. See Section 5.6, “Temperature Measurement - TSENSE".
30	GNDSUB	Substrate Ground	Substrate ground connection to improve EMC behavior.
31	ISENSEL	Current Sense L	Current sense input “Low”. This pin is used in combination with ISENSEH to measure the voltage drop across a shunt resistor. See Section 5.4, “Current Measurement - ISENSE".
32	ISENSEH	Current Sense H	Current sense input “high”. This pin is used in combination with ISENSEL to measure the voltage drop across a shunt resistor. See Section 5.4, “Current Measurement - ISENSE".
33	ADCGND	Analog Digital Converter Ground	Analog digital converter ground connection. See Section 5.2, “Analog Die - Power, Clock and Resets - PCR".
34	VSENSE	Voltage Sense	Precision battery voltage measurement input. This pin can be connected directly to the battery line for voltage measurements. The voltage preset at this input is scaled down by an internal voltage divider. The pin is self protected against reverse battery connections. An external resistor (R_{VSENSE}) is needed for protection. See Section 5.5, “Voltage Measurement - VSENSE".
35	VOPT	Optional Voltage Sense	Optional voltage measurement input. See Section 5.5, “Voltage Measurement - VSENSE".
36	PTB3 / L0	General Purpose Input 3 - High Voltage Input 0	This is the high voltage general purpose input pin 3, based on VDDX with the following shared functions: • Internal clamping structure to operate as a high voltage input (L0). When used as high voltage input, a series resistor (RL0) and capacitor to GND (C_{L0}) must be used to protect against automotive transients, when used to connect outside the PCB. • 5.0 V (VDDX) digital port input • Selectable internal pull-down resistor • Selectable wake-up input during low power mode. • Selectable timer channel input • Selectable connection to the LIN / SCI (Input only) See Section 5.10, “General Purpose I/O - GPIO".
37	PTB2	General Purpose I/O 2	This is the general purpose I/O pin 2 based on VDDX with the following shared functions: • Bidirectional 5.0 V (VDDX) digital port I/O • Selectable internal pull-up resistor • Selectable timer channel input/output • Selectable connection to the LIN / SCI See Section 5.10, “General Purpose I/O - GPIO".
38	PTB1	General Purpose I/O 1	This is the general purpose I/O pin 1, based on VDDX with the following shared functions: • Bidirectional 5.0 V (VDDX) digital port I/O • Selectable internal pull-up resistor • Selectable timer channel input/output • Selectable connection to the LIN / SCI See Section 5.10, “General Purpose I/O - GPIO".
39	PTB0	General Purpose I/O 0	This is the general purpose I/O pin 0 based on VDDX with the following shared functions: • Bidirectional 5.0 V (VDDX) digital port I/O • Selectable internal pull-up resistor • Selectable timer channel input/output • Selectable connection to the LIN / SCI See Section 5.10, “General Purpose I/O - GPIO".

Table 20. Static Electrical Characteristics - High Voltage Input - PTB3 / L0

Ratings	Symbol	Min	Typ	Max	Unit
Wake-up Threshold - Rising Edge	V_{WTHR}	1.3	2.6	3.4	V
Input High Voltage (digital Input)	V_{IH}	$0.7V_{DDX}$		V_{DDX}+0.3	V
Input Low Voltage (digital Input)	V_{IL}	V_{SS}-0.3		$0.35V_{DDX}$	V
Input Hysteresis	V_{HYS}	50	140	200	mV
Internal Clamp Voltage	V_{L0CLMP}	4.9	6.0	7.0	V
Input Current PTB3 / L0 (V_{IN} = 42 V; R_{L0}=47 kOhm)	I_{IN}			1.1	mA
Internal pull-down resistance[15]	R_{PD}	50	100	200	kOhm
PTB3 / L0 Series Resistor	R_{PTB3}	42.3	47	51.7	kOhm
PTB3 / L0 Capacitor	C_{L0}	42.3	47	51.7	nF

Notes
15.Disabled by default.

Table 21. Static Electrical Characteristics - General Purpose I/O - PTB[0...2]

Ratings	Symbol	Min	Typ	Max	Unit
Input High Voltage	V_{IH}	$0.7V_{DDX}$		V_{DDX}+0.3	V
Input Low Voltage	V_{IL}	V_{SS}-0.3		$0.35V_{DDX}$	V
Input Hysteresis	V_{HYS}	50	140	200	mV
Input Leakage Current (pins in high-impedance input mode) (V_{IN} = V_{DDX} or V_{SSX})	I_{IN}	-1.0		1.0	µA
Output High Voltage (pins in output mode) Full drive I_{OH} = –5.0 mA	V_{OH}	V_{DDX}-0.8			V
Output Low Voltage (pins in output mode) Full drive I_{OL} = 5.0 mA	V_{OL}			0.8	V
Internal Pull-up Resistance (V_{IH} min. > Input voltage > V_{IL} max)[16]	R_{PUL}	25	37.5	50	kOhm
Input Capacitance	C_{IN}		6.0		pF
Maximum Current All PTB Combined[17]	I_{BMAX}	-17		17	mA
Output Drive strength at 10 MHz	C_{OUT}			100	pF

Notes
16.Disabled by default.
17.Overall VDDR Regulator capability to be considered.

4.6 Dynamic Electrical Characteristics

Dynamic characteristics noted under conditions 3.5 V ≤ V_{SUP} ≤ 28 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

4.6.1 Dynamic Electrical Characteristics Analog Die

Table 28. Dynamic Electrical Characteristics - Modes of Operation

Ratings	Symbol	Min	Typ	Max	Unit
Low Power Oscillator Frequency	f_{OSCL}	—	512	—	kHz
Low Power Oscillator Tolerance over full temperature range	f_{TOL_A}				
Analog Option 2		-4.0	—	4.0	%
Analog Option 1		-5.0	—	5.0	
Low Power Oscillator Tolerance - synchronized ALFCLK[34]	f_{TOLC_A}				
ALF clock cycle = 1.0 ms		f_{TOL}-0.2	f_{TOL}	f_{TOL}+0.2	%
ALF clock cycle = 2.0 ms		f_{TOL}-0.1		f_{TOL}+0.1	
ALF clock cycle = 4.0 ms		f_{TOL}-0.05		f_{TOL}+0.05	
ALF clock cycle = 8.0 ms		f_{TOL}-0.025		f_{TOL}+0.025	

Notes
34.Parameter not tested. Guaranteed by design and characterization.

Table 29. Dynamic Electrical Characteristics - Die to Die Interface - D2D

Ratings	Symbol	Min	Typ	Max	Unit
Operating Frequency (D2DCLK, D2D[0:3])	f_{D2D}	—	—	32.768	MHz

Table 30. Dynamic Electrical Characteristics - Resets

Ratings	Symbol	Min	Typ	Max	Unit
Reset Deglitch Filter Time	t_{RSTDF}	1.0	2.0	3.2	µs
Reset Release Time for WDR and HWR	t_{RSTRT}	—	32	—	µs

Table 31. Dynamic Electrical Characteristics - Wake-up / Cyclic Sense

Ratings	Symbol	Min	Typ	Max	Unit
Cyclic Wake-up Time[35]	t_{WAKEUP}	ALFCLK	—	TIM4CH	ms
Cyclic Current Measurement Step Width[36]	t_{STEP}	ALFCLK	—	16Bit	ms

Notes
35.Cyclic wake-up on ALFCLK clock based 16 Bit TIMER with maximum 128x prescaler (min 1x)
36.Cyclic wake-up on ALFCLK clock with 16 Bit programmable counter

Table 32. Dynamic Electrical Characteristics - Window Watchdog

Ratings	Symbol	Min	Typ	Max	Unit
Initial Non-window Watchdog Timeout	t_{IWDTO}	see Figure 2			ms

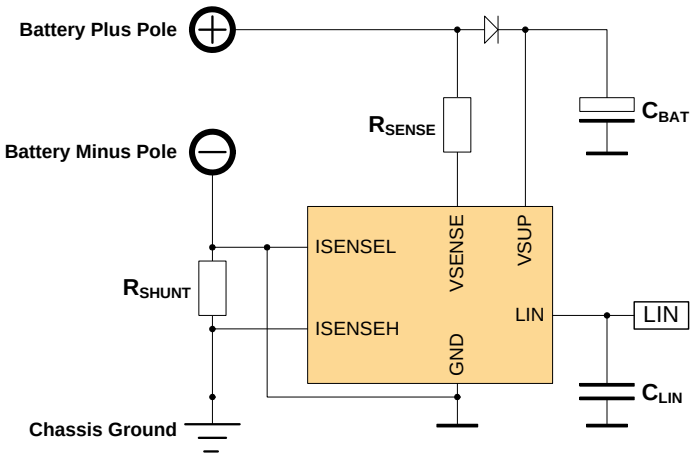


Figure 13. Typical IBS Application (Device GND = Battery Minus)

The vehicle power system needs actual measurement data from the battery, mainly voltage, current, and temperature. Out of these measurement data, it needs calculated characteristics, such as dynamic internal battery resistance. Therefore, an intelligent battery sensor (IBS) module is required.

To efficiently measure the battery voltage, current, and temperature, the IBS module is directly connected to and supplied from the battery. It is located directly on the negative pole of the battery; the supply of the IBS module comes from 'KL30'. The battery current is measured via a low-ohmic shunt resistor, connected between the negative pole of the battery and the chassis ground of the car. The battery voltage is measured at 'KL30'.

The data communication between the IBS module and the higher level ECU is done via a LIN interface.

The MM912_637 is able to measure its junction temperature. That temperature is the basis for a model in software that calculates the battery temperature out of the junction temperature. An optional external temperature sense input is provided as well.

5.0.2 Device Register Map

Table 49 shows the device register memory map overview.

Table 49. Device Register Memory Map Overview

Address	Module	Size (Bytes)
0x0000–0x0003	PIM (port integration module)	4
0x0004–0x0009	Reserved	6
0x000A–0x000B	MMC (memory map control)	2
0x000C–0x000D	PIM (port integration module)	2
0x000E–0x000F	Reserved	2
0x0010–0x0015	MMC (memory map control)	8
0x0016–0x0019	Reserved	2
0x001A–0x001B	Device ID register	2
0x001C–0x001E	Reserved	4
0x001F	INT (interrupt module)	1
0x0020–0x002F	DBG (debug module)	16
0x0030–0x0033	Reserved	4
0x0034–0x003F	CPMU (clock and power management)	12
0x0040–0x00D7	Reserved	152
0x00D8–0x00DF	D2DI (die 2 die initiator)	8

5.2.3 Power Management

To support the various operating modes and modules in the MM912_637, the following power management architecture has been implemented.

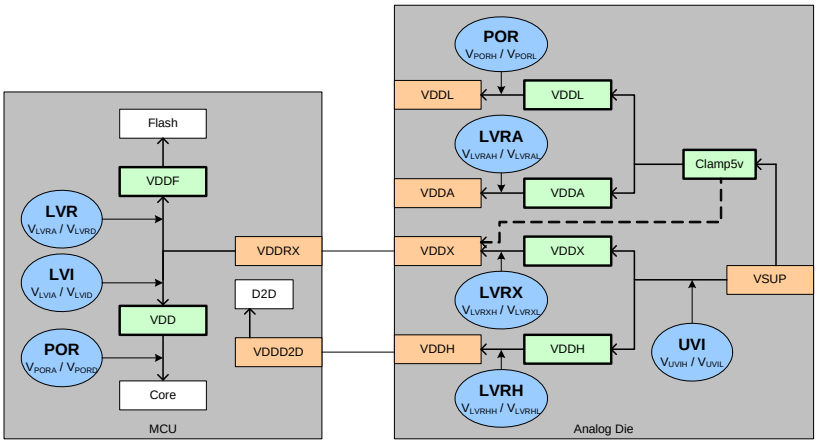


Figure 17. System Voltage Monitoring

5.2.3.1 Detailed Power Block Description

See recommended external components under Section 3.2, “Recommended External Components”.

5.2.3.1.1 VSUP

VSUP is the system power supply input, and must be reverse battery protected by an external diode. VSUP is monitored for under-voltage conditions (UVI). Once VSUP drops below V_{UVIL} an under-voltage interrupt (LVI) is issued.

NOTE

If the device has the cranking mode feature enabled, the under-voltage threshold would be V_{UVCIL} instead of V_{UVIL}.

5.2.3.1.2 VDDL

VDDL is the low power 2.5 V digital supply voltage, supplying the permanently active blocks. It is based on the internal Clamp5v voltage and always on. It is available externally, but must not be connected to any load.

5.2.3.1.3 VDDX

VDDX is the Normal mode 5.0 V regulator output, suppling the LIN block and the microcontroller via the VDDX pin. During STOP and SLEEP mode operation, the VDDX regulator is shut down (Clamp5v does supply the MCU during STOP mode).

5.2.3.1.4 VDDH

VDDH is the Normal mode 2.5 V regulator output, suppling only active blocks during Normal mode and the MCU Die to Die Interface, via the VDDH terminal. The VDDH regulator is shut down during both low power modes.

5.2.3.1.5 VDDA

VDDA is the 2.5 V analog supply voltage, active during Normal mode and I/T acquisitions. No external load must be connected to the VDDA terminal.

Figure 22 and Figure 23 show the different clock sources for normal and low power mode.

NOTE

D2DFCLK has to be set to match 512 kHz, resulting in D2DSCLK being 1.0, 2.0, 4.0, or 8.0 kHz, based on PF[1:0]

The minimum value for PRESC[15:0] has to be 0x0400. Any value lower than 0x0400 will result in faulty behavior and is not recommended. Values of 0x0003 or less are not stored by the internal logic.

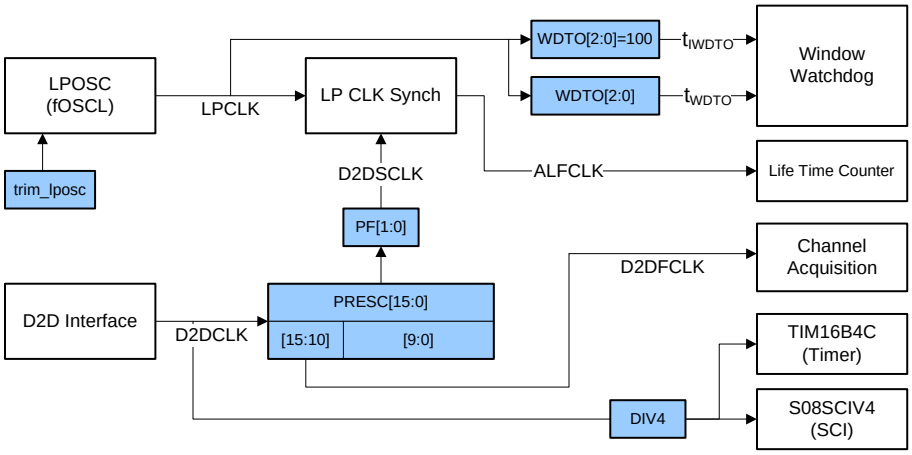


Figure 22. Clock Tree Overview - Normal Mode

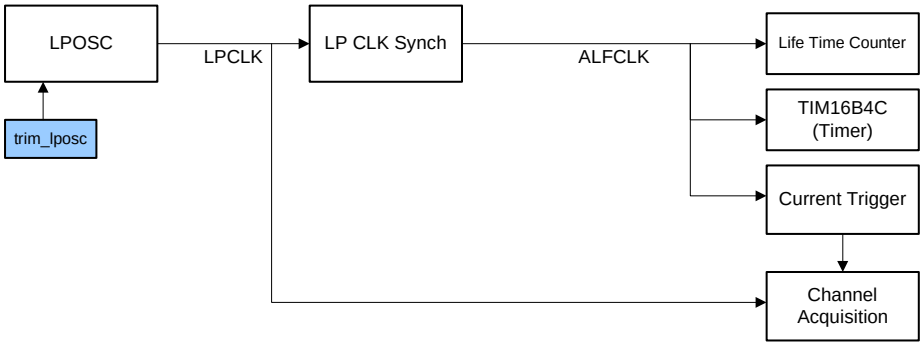


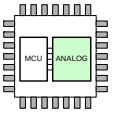
Figure 23. Clock Tree Overview - Low Power Modes

5.2.5.2 ALFCLK Calibration

To increase the accuracy of the 1.0 kHz (or 2.0, 4.0, 8.0 7kHz based on PF[1:0]) system clock (ALFCLK), the low power oscillator (LPCLK) is synchronized to the more precise D2DCLK, via the D2DSCLK signal. The “Calibrated Low Power Clock” (ALFCLK) could be trimmed to the D2DCLK accuracy plus a maximum error adder of 1 LPCLK period, by internally counting the number of periods of the LPCLK (512 kHz) during a D2DSCLK period. The APRESC[12:0] register will represent the calculated internal prescaler. The PRDF bit (Prescaler Ready flag) will indicate the synchronization complete after a power up or prescaler (PRESC/PF) change.

The adjustment is continuously performed during Normal mode. During low power mode (STOP or SLEEP), the last adjustment factor would be used.

5.3 Interrupt Module - IRQ



5.3.1 Introduction

Several interrupt sources are implemented on the analog die to indicate important system conditions. Those Interrupt events are signalized via the D2DINT signal to the microcontroller. See Section 5.17, “MCU - Interrupt Module (S12SINTV1)".

5.3.2 Interrupt Source Identification

Once an Interrupt is signalized, there are two options to identify the corresponding source(s).

NOTE

The following Interrupt source registers (Interrupt Source Mirror and Interrupt Vector Emulation by Priority) are indicators only. After identifying the interrupt source, the acknowledgement of the interrupt has to be performed in the corresponding block.

5.3.2.1 Interrupt Source Mirror

All Interrupt sources in the MM912_637 analog die are mirrored to a special Interrupt Source Register (INT_SRC). This register is read only and will indicate all currently pending Interrupts. Reading this register will not acknowledge any interrupt. An additional D2D access is necessary to serve the specific module.

5.3.2.2 Interrupt Vector Emulation by Priority

To allow a vector based interrupt handling by the MCU, the number of the highest prioritized interrupt pending is returned in the Interrupt Vector Register (INT_VECT). Reading this register will not acknowledge an interrupt. An additional D2D access is necessary to serve the specific module.

5.3.3 Interrupt Global Mask

The Global Interrupt mask registers INT_MSK (hi) and INT_MSK (lo) are implemented to allow a global enable / disable of all analog die Interrupt sources. The individual blocks mask registers should be used to control the individual sources.

5.3.4 Interrupt Sources

The following Interrupt sources are implemented on the analog die.

Table 87. Interrupt Sources

IRQ	Description
UVI	Under-voltage Interrupt (or wake-up from Cranking mode)
HTI	High Temperature Interrupt
LTI	LIN Driver Over-temperature Interrupt
CH0	TIM Channel 0 Interrupt
CH1	TIM Channel 1 Interrupt
CH2	TIM Channel 2 Interrupt
CH3	TIM Channel 3 Interrupt
TOV	TIM Timer Overflow Interrupt
ERR	SCI Error Interrupt
TX	SCI Transmit Interrupt
RX	SCI Receive Interrupt

Table 87. Interrupt Sources

IRQ	Description
CVMI	Current / Voltage Measurement Interrupt
LTC	Lifetime Counter Interrupt
CAL	Calibration Request Interrupt

5.3.4.1 Under-voltage Interrupt (UVI)

This maskable interrupt signalizes a under-voltage condition on the VSUP supply input.

Acknowledge the interrupt by writing a 1 into the UVF Bit in the PCR Status Register (PCR_SR (hi)). The flag cannot be cleared as long as the condition is present. To issue a new interrupt, the condition has to vanish and occur again. The UVF Bit represents the current condition, and might not be set after an interrupt was signalized by the interrupt source registers.

See Section 5.2, “Analog Die - Power, Clock and Resets - PCR" for details on the PCR Status Register (PCR_SR (hi)), including masking information.

NOTE

The under-voltage interrupt is not active in devices with the Cranking mode enabled. For those devices, the under-voltage threshold is used to enable the high precision low voltage threshold during Stop/Sleep mode.

Once the device wakes up from cranking mode, the UVI flag is indicating the wake-up source.

5.3.4.2 High Temperature Interrupt (HTI)

This maskable interrupt signalizes a high temperature condition on the analog die. The sensing element is located close to the major thermal contributors, the system voltage regulators.

Acknowledge the interrupt by writing a 1 into the HTF Bit in the PCR Status Register (PCR_SR (hi)). The flag cannot be cleared as long as the condition is present. To issue a new interrupt, the condition has to vanish and occur again. The HTF Bit represents the current condition and might not be set after an interrupt was signalized by the interrupt source registers.

See Section 5.2, “Analog Die - Power, Clock and Resets - PCR" for details on the PCR Status Register (PCR_SR (hi)), including masking information.

5.3.4.3 LIN Driver Over-temperature Interrupt (LTI)

Acknowledge the interrupt by reading the LIN Register - LINR. The flag cannot be cleared as long as the condition is present. To issue a new interrupt, the condition has to vanish and occur again. See Section 5.11, “LIN" for details on the LIN Register, including masking information.

5.3.4.4 TIM Channel 0 Interrupt (CH0)

See Section 5.9, “Basic Timer Module - TIM (TIM16B4C)".

5.3.4.5 TIM Channel 1 Interrupt (CH1)

See Section 5.9, “Basic Timer Module - TIM (TIM16B4C)".

5.3.4.6 TIM Channel 2 Interrupt (CH2)

See Section 5.9, “Basic Timer Module - TIM (TIM16B4C)".

5.7.5.1.2 Gain Compensation Look Up Table

In order to prepare the system for the optional calibration interrupt service during operation, it is be beneficial to create a look up table for the voltage and current channel gain compensation over temperature.

For all current and voltage channel gain buffers, there are corresponding ROOM temperature optimum trim values stored in the IFR FLASH. For HOT (125 °C) and COLD (-40 °C) temperature, the adjustment towards the ROOM value is stored.

Note: This table is partially populated for Analog Option 1 devices (populated from 0x0_40C0 to 0x0_40E1). Only Default (room temperature) Gain Compensation values applicable. For ISENSE, see Table 22 (IGAINERR). For VSENSE, see Table 23 (VGAINERR).

Table 105. Gain Compensation Buffer Optimum

Global Address (IFRON)	OFFSET		Byte Description								Content
	HEX	DEC	7	6	5	4	3	2	1	0	
0x0_40C0	00	00							IGC4[9:8]		Current Channel Gain (4) Compensation - Room Temp
0x0_40C1	01	01	IGC4[7:0]								
0x0_40C2	02	02							IGC8[9:8]		Current Channel Gain (8) Compensation - Room Temp
0x0_40C3	03	03	IGC8[7:0]								
0x0_40C4	04	04							IGC16[9:8]		Current Channel Gain (16) Compensation - Room Temp
0x0_40C5	05	05	IGC16[7:0]								
0x0_40C6	06	06							IGC32[9:8]		Current Channel Gain (32) Compensation - Room Temp
0x0_40C7	07	07	IGC32[7:0]								
0x0_40C8	08	08							IGC64[9:8]		Current Channel Gain (64) Compensation - Room Temp
0x0_40C9	09	09	IGC64[7:0]								
0x0_40CA	0A	10							IGC128[9:8]		Current Channel Gain (128) Compensation - Room Temp
0x0_40CB	0B	11	IGC128[7:0]								
0x0_40CC	0C	12							IGC256[9:8]		Current Channel Gain (256) Compensation - Room Temp
0x0_40CD	0D	13	IGC256[7:0]								
0x0_40CE	0E	14							IGC512[9:8]		Current Channel Gain (512) Compensation - Room Temp
0x0_40CF	0F	15	IGC512[7:0]								
0x0_40DE	1E	30							VSGC[9:8]		VSENSE Channel Gain Compensation - Room Temp
0x0_40DF	1F	31	VSGC[7:0]								
0x0_40E0	20	32							VOGC[9:8]		VOPT Channel Gain Compensation - Room Temp
0x0_40E1	21	33	VOGC[7:0]								
0x0_40EC	2C	44	COMP_VSG_COLD[7:0]								VSENSE Channel Gain Compensation - COLD Temp[108]
0x0_40ED	2D	45	COMP_VSG_HOT[7:0]								VSENSE Channel Gain Compensation - HOT Temp[108]
0x0_40EE	2E	46	COMP_VOG_COLD[7:0]								VOPT Channel Gain Compensation - COLD Temp[108]
0x0_40EF	2F	47	COMP_VOG_HOT[7:0]								VOPT Channel Gain Compensation - HOT Temp[108]
0x0_40F0	30	48	IGC4_COLD[7:0]								Current Channel Gain (4) Compensation - COLD Temp[108]
0x0_40F1	31	49	IGC4_HOT[7:0]								Current Channel Gain (4) Compensation - HOT Temp[108]
0x0_40F2	32	50	IGC8_COLD[7:0]								Current Channel Gain (8) Compensation - COLD Temp[108]
0x0_40F3	33	51	IGC8_HOT[7:0]								Current Channel Gain (8) Compensation - HOT Temp[108]

Table 108. Module Memory Map

Offset	Name		7	6	5	4	3	2	1	0
0x6A	ACQ_CURR0 Current measurement result	R	CURR[15:8]							
		W								
		R	CURR[7:0]							
		W								
0x6C	ACQ_VOLT Voltage measurement result	R	VOLT[15:8]							
		W								
		R	VOLT[7:0]							
		W								
0x6E	ACQ_LPFC	R	0	0	0	0	LPFC[3:0]			
	Low pass filter coefficient number	W								
0x6F	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x70	ACQ_TCMP Low power trigger current measurement period	R	TCMP[15:0]							
		W								
		R								
		W								
0x72	ACQ_THF	R	THF[7:0]							
	Low power current threshold filtering period	W								
0x73	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x74	ACQ_CVCR (hi)	R	0	0	0	0	0	0	0	0
	I and V chopper control register	W			DBTM[1:0]		IIRCM[2:0]			PGAFM
0x75	ACQ_CVCR (lo)	R	0	0	DBT[1:0]		IIRC[2:0]			PGAF
	I and V chopper control register	W								
0x76	ACQ_CTH	R	CTH[7:0]							
	Low power current threshold	W								
0x77	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x78	ACQ_AHTH1 (hi)	R	0							
	Low power Ah counter threshold	W				AHTH[30:16]				
0x79	ACQ_AHTH1 (lo)	R								
	Low power Ah counter threshold	W								
0x7A	ACQ_AHTH0 (hi)	R	AHTH[15:0]							
	Low power Ah counter threshold	W								
0x7B	ACQ_AHTH0 (lo)	R								
	Low power Ah counter threshold	W								
0x7C	ACQ_AHC1 (hi)	R	AHC[31:24]							
	Low power Ah counter	W								
0x7D	ACQ_AHC1 (lo)	R	AHC[23:16]							
	Low power Ah counter	W								

Table 118. Acquisition Chain Control 0 (ACQ_ACC0) - Register Field Descriptions

Field	Description
11 CADCGM	Current ADC Gain Select - Mask 0 - writing the CADCG bit will have no effect 1 - writing the CADCG bit will be effective
10 TDENM	100ns Clock delay - Internal Temperature - Mask 0 - writing the TDEN bit will have no effect 1 - writing the TDEN bit will be effective
9 VDENM	100ns Clock delay - Voltage - Mask 0 - writing the VDEN bit will have no effect 1 - writing the VDEN bit will be effective
8 CDENM	100ns Clock delay - Current - Mask 0 - writing the CDEN bit will have no effect 1 - writing the CDEN bit will be effective
7 ZERO	Current and Voltage Sigma Delta Input Short (to perform Offset Compensation measurement) 0 - Sigma delta inputs not shorted 1 - Current and voltage sigma delta inputs shorted
6 ECAP	TSUP External Capacitor select 0 - TSUP frequency compensation disabled. No capacitor at pin. 0 - TSUP frequency compensation enabled. Capacitor C_{TSUP} allowed at pin.
5 TADCG	Temperature ADC Gain Select; Test purpose only, Default value (1) must be used 0 - Temperature ADC - gain adjustment 1 - Temperature ADC - standard gain (default)
4 VADCG	Voltage ADC Gain Select; Test purpose only; Default value (1) must be used 0 - Voltage ADC - gain adjustment 1 - Voltage ADC - standard gain (default)
3 CADCG	Current ADC Gain Select; Test purpose only; Default value (1) must be used 0 - Current ADC - gain adjustment 1 - Current ADC - standard gain (default)
2 TDEN	Timing delay - Temperature 0 - standard timing for temperature measurement channel 1 - additional SD converter input delay (typ. 100 ns) for temperature measurement channel
1 VDEN	Timing delay - Voltage 0 - standard timing for Voltage measurement channel 1 - additional SD converter input delay (typ. 100 ns) for voltage measurement channel
0 CDEN	Timing delay - Current 0 - standard timing for current measurement channel 1 - additional SD converter input delay (typ. 100 ns) for current measurement channel

5.7.6.3.6 Decimation Rate (ACQ_DEC)

Table 119. Decimation Rate (ACQ_DEC)

Offset[122] 0x60 — Access: User read/write

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	DEC[2:0]		
W								
Reset	0	0	0	0	0	1	0	0

Notes

122.Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

5.9.3.3.13 Main Timer Interrupt Flag 2 (TFLG2)

Table 218. Main Timer Interrupt Flag 2 (TFLG2)

Offset[188] 0x2D — Access: User read/write

	7	6	5	4	3	2	1	0
R	TOF	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

Notes
188.Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 219. TFLG2 - Register Field Descriptions

Field	Description
7 TOF	Timer Overflow Flag 1 = Indicates that an interrupt has occurred (Set when 16-bit free-running timer counter overflows from $FFFF to $0000) 0 = Flag indicates an interrupt has not occurred.

NOTE

The TFLG2 register indicates when an interrupt has occurred. Writing a one to the TOF bit will clear it. Any access to TCNT will clear TOF bit of TFLG2 register if the TFFCA bit in TSCR register is set.

5.9.3.3.14 Timer Input Capture/Output Compare Registers (TC3 - TC0)

Table 220. Timer Input Capture/Output Compare Register 0 (TC0)

Offset[189] 0x2E, 0x2F — Access: User read/write

	15	14	13	12	11	10	9	8
R	tc0_15	tc0_14	tc0_13	tc0_12	tc0_11	tc0_10	tc0_9	tc0_8
W								
Reset	0	0	0	0	0	0	0	0
	7	6	5	4	3	2	1	0
R	tc0_7	tc0_6	tc0_5	tc0_4	tc0_3	tc0_2	tc0_1	tc0_0
W								
Reset	0	0	0	0	0	0	0	0

Notes
189.Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 335. DBGC2 Field Descriptions

Field	Description
1–0 ABCM[1:0]	**A and B Comparator Match Control** — These bits determine the A and B comparator match mapping as described in Table 336.

Table 336. ABCM Encoding

ABCM	Description
00	Match0 mapped to comparator A match: Match1 mapped to comparator B match.
01	Match 0 mapped to comparator A/B inside range: Match1 disabled.
10	Match 0 mapped to comparator A/B outside range: Match1 disabled.
11	Reserved(250)

Notes
250.Currently defaults to Comparator A, Comparator B disabled

5.19.3.2.5 Debug Trace Buffer Register (DBGTBH:DBGTBL)

Table 337. Debug Trace Buffer Register (DBGTB)

Address: 0x0024, 0x0025

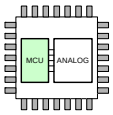
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
POR	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Other Resets	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

Read: Only when unlocked AND unsecured AND not armed AND TSOURCE set
Write: Aligned word writes when disarmed unlock the trace buffer for reading but do not affect trace buffer contents

Table 338. DBGTB Field Descriptions

Field	Description
15–0 Bit[15:0]	**Trace Buffer Data Bits** — The Trace Buffer Register is a window through which the 20-bit wide data lines of the Trace Buffer may be read 16 bits at a time. Each valid read of DBGTB increments an internal trace buffer pointer which points to the next address to be read. When the ARM bit is set the trace buffer is locked to prevent reading. The trace buffer can only be unlocked for reading by writing to DBGTB with an aligned word write when the module is disarmed. The DBGTB register can be read only as an aligned word, any byte reads or misaligned access of these registers return a 0, and do not cause the trace buffer pointer to increment to the next trace buffer address. Similarly reads while the debugger is armed or with the TSOURCE bit clear, return a 0, and do not affect the trace buffer pointer. The POR state is undefined. Other resets do not affect the trace buffer contents.

5.20 MCU - Security (S12XS9SECV2)



5.20.1 Introduction

This specification describes the function of the security mechanism in the S12I chip family (9SEC).

NOTE

No security feature is absolutely secure. However, Freescale's strategy is to make reading or copying the FLASH and/or EEPROM difficult for unauthorized users.

5.20.1.1 Features

The user must be reminded that part of the security must lie with the application code. An extreme example would be application code that dumps the contents of the internal memory. This would defeat the purpose of security. At the same time, the user may also wish to put a backdoor in the application program. An example of this is the user downloads a security key through the SCI, which allows access to a programming routine that updates parameters stored in another section of the Flash memory.

The security features of the S12I chip family (in secure mode) are:

- Protect the content of non-volatile memories (Flash, EEPROM)
- Execution of NVM commands is restricted
- Disable access to internal memory via background debug module (BDM)

5.20.1.2 Modes of Operation

Table 388 gives an overview over availability of security relevant features in unsecure and secure modes.

Table 388. Feature Availability in Unsecure and Secure Modes on S12XS

	Unsecure Mode						Secure Mode					
	NS	SS	NX	ES	EX	ST	NS	SS	NX	ES	EX	ST
Flash Array Access	4	4					4	4				
EEPROM Array Access	4	4					4	4				
NVM Commands	(254)	4					(254)	(254)				
BDM	4	4					—	(255)				
DBG Module Trace	4	4					—	—				

Notes

254.Restricted NVM command set only. Refer to the NVM wrapper block guides for detailed information.

255.BDM hardware commands restricted to peripheral registers only.

5.20.1.3 Securing the Microcontroller

Once the user has programmed the Flash and EEPROM, the chip can be secured by programming the security bits located in the options/security byte in the Flash memory array. These non-volatile bits will keep the device secured through reset and power-down.

The options/security byte is located at address 0xFF0F (= global address 0x7F_FF0F) in the Flash memory array. This byte can be erased and programmed like any other Flash location. Two bits of this byte are used for security (SEC[1:0]). On devices which have a memory page window, the Flash options/security byte is also available at address 0xBF0F by selecting page 0x3F with the PPAGE register. The contents of this byte are copied into the Flash security register (FSEC) during a reset sequence.

Table 389. Flash Options/Security Byte

	7	6	5	4	3	2	1	0
0xFF0F	KEYEN1	KEYEN0	NV5	NV4	NV3	NV2	SEC1	SEC0

The default state of the BDM after reset is hardware handshake protocol disabled.

All the read commands will ACK (if enabled) when the data bus cycle has completed and the data is then ready for reading out by the BKGD serial pin. All the write commands will ACK (if enabled) after the data has been received by the BDM through the BKGD serial pin, and when the data bus cycle is complete. See Section 5.21.4.3, “BDM Hardware Commands" and Section 5.21.4.4, “Standard BDM Firmware Commands" for more information on the BDM commands.

The ACK_ENABLE sends an ACK pulse when the command has been completed. This feature could be used by the host to evaluate if the target supports the hardware handshake protocol. If an ACK pulse is issued in response to this command, the host knows that the target supports the hardware handshake protocol. If the target does not support the hardware handshake protocol the ACK pulse is not issued. In this case, the ACK_ENABLE command is ignored by the target since it is not recognized as a valid command.

The BACKGROUND command issues an ACK pulse when the CPU changes from normal to background mode. The ACK pulse related to this command could be aborted using the SYNC command.

The GO command issues an ACK pulse when the CPU exits from background mode. The ACK pulse related to this command could be aborted using the SYNC command.

The GO_UNTIL(262) command is equivalent to a GO command with exception that the ACK pulse, in this case, is issued when the CPU enters into background mode. This command is an alternative to the GO command and should be used when the host wants to trace if a breakpoint match occurs and causes the CPU to enter active background mode. Note that the ACK is issued whenever the CPU enters BDM, which could be caused by a breakpoint match or by a BGND instruction being executed. The ACK pulse related to this command could be aborted using the SYNC command.

The TRACE1 command has the related ACK pulse issued when the CPU enters background active mode after one instruction of the application program is executed. The ACK pulse related to this command could be aborted using the SYNC command.

5.21.4.9 SYNC — Request Timed Reference Pulse

The SYNC command is unlike other BDM commands, because the host does not necessarily know the correct communication speed to use for BDM communications until after it has analyzed the response to the SYNC command. To issue a SYNC command, the host should perform the following steps:

1. Drive the BKGD pin low for at least 128 cycles at the lowest possible BDM serial communication frequency (The lowest serial communication frequency is determined by the settings for the VCO clock (CPMUSYNR). The BDM clock frequency is always VCO clock frequency divided by 8.)
2. Drive BKGD high for a brief speedup pulse to get a fast rise time (this speedup pulse is typically one cycle of the host clock.)
3. Remove all drive to the BKGD pin so it reverts to high-impedance.
4. Listen to the BKGD pin for the sync response pulse.

Upon detecting the SYNC request from the host, the target performs the following steps:

1. Discards any incomplete command received or bit retrieved.
2. Waits for BKGD to return to a logic one.
3. Delays 16 cycles to allow the host to stop driving the high speedup pulse.
4. Drives BKGD low for 128 cycles at the current BDM serial communication frequency.
5. Drives a one-cycle high speedup pulse to force a fast rise time on BKGD.
6. Removes all drive to the BKGD pin so it reverts to high-impedance.

The host measures the low time of this 128 cycle SYNC response pulse and determines the correct speed for subsequent BDM communications. Typically, the host can determine the correct communication speed within a few percent of the actual target speed, and the communication protocol can easily tolerate speed errors of several percent.

As soon as the SYNC request is detected by the target, any partially received command or bit retrieved is discarded. This is referred to as a soft-reset, equivalent to a time-out in the serial communication. After the SYNC response, the target will consider the next negative edge (issued by the host) as the start of a new BDM command or the start of new SYNC request.

Another use of the SYNC command pulse is to abort a pending ACK pulse. The behavior is exactly the same as in a regular SYNC command. Note that one of the possible causes for a command to not be acknowledged by the target is a host-target synchronization problem. In this case, the command may not have been understood by the target, so an ACK response pulse will not be issued.

5.22.4.2 Startup from Reset

An example of startup of clock system from Reset is given in Figure 94.

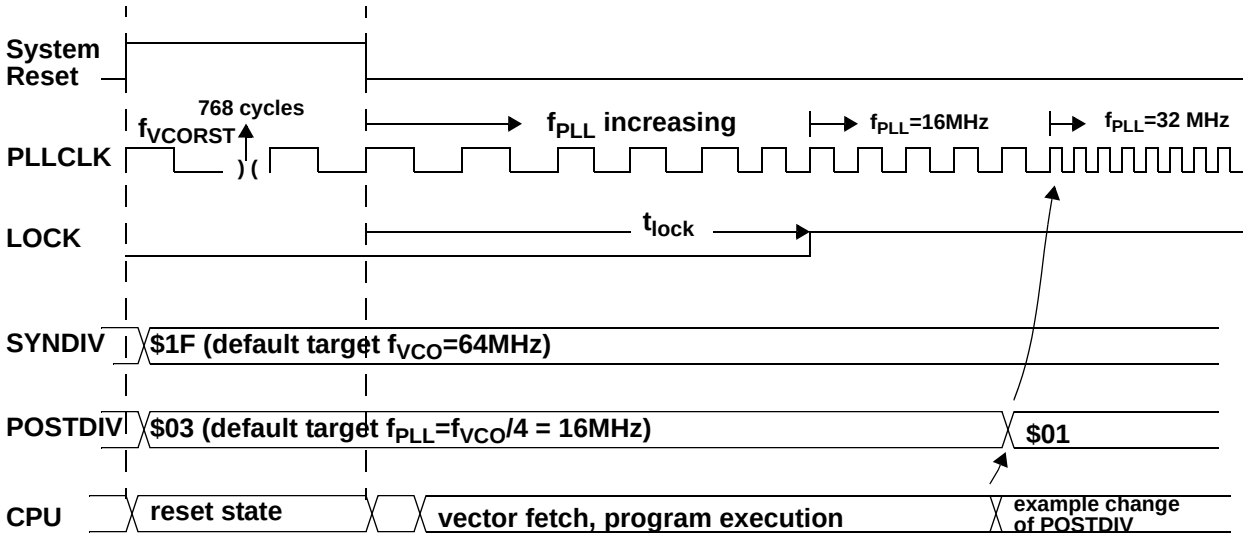


Figure 94. Startup of Clock System After Reset

5.22.4.3 Stop Mode using PLLCLK as Bus Clock

An example of what happens going into Stop mode and exiting Stop mode after an interrupt is shown in Figure 95. Disable PLL Lock interrupt (LOCKIE=0) before going into Stop mode.

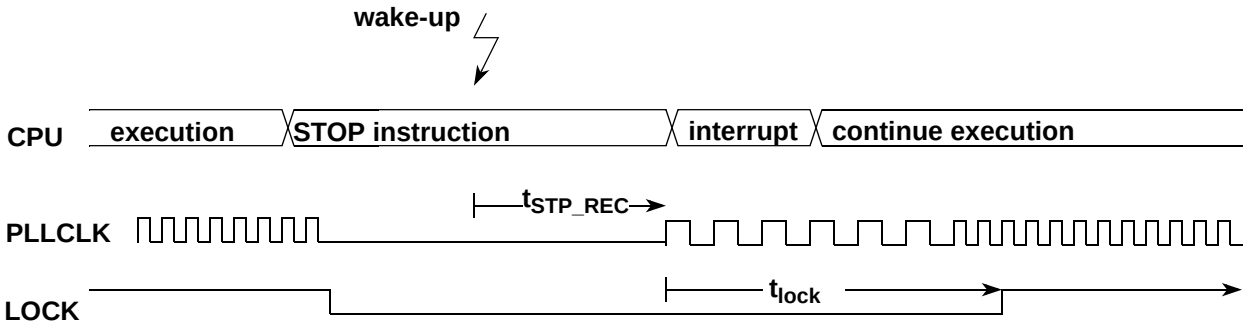


Figure 95. Stop Mode using PLLCLK as Bus Clock

5.22.4.4 Full Stop Mode Using Oscillator Clock as Bus Clock

An example of what happens going into Full Stop mode and exiting Full Stop mode after an interrupt is shown in Figure 96. Disable PLL Lock interrupt (LOCKIE=0) and oscillator status change interrupt (OSCIE=0) before going into Full Stop mode.

This mode fault error also sets the mode fault (MODF) flag in the SPI status register (SPISR). If the SPI interrupt enable bit (SPIE) is set when the MODF flag becomes set, then an SPI interrupt sequence is also requested.

When a write to the SPI data register in the master occurs, there is a half SCK-cycle delay. After the delay, SCK is started within the master. The rest of the transfer operation differs slightly, depending on the clock format specified by the SPI clock phase bit, CPHA, in SPI control register 1 (see Section 5.23.4.3, “Transmission Formats").

NOTE

A change of the bits CPOL, CPHA, SSOE, LSBFE, XFRW, MODFEN, SPC0, or BIDIROE with SPC0 set, SPPR2-SPPR0, and SPR2-SPR0 in master mode, will abort a transmission in progress and force the SPI into idle state. The remote slave cannot detect this, therefore the master must ensure that the remote slave is returned to idle state.

5.23.4.2 Slave Mode

The SPI operates in slave mode when the MSTR bit in SPI control register 1 is clear.

- Serial clock
  In slave mode, SCK is the SPI clock input from the master.
- MISO, MOSI pins
  In slave mode, the function of the serial data output pin (MISO) and serial data input pin (MOSI) is determined by the SPC0 bit and BIDIROE bit in SPI control register 2.
- $\overline{SS}$ pin
  The $\overline{SS}$ pin is the slave select input. Before a data transmission occurs, the $\overline{SS}$ pin of the slave SPI must be low. $\overline{SS}$ must remain low until the transmission is complete. If $\overline{SS}$ goes high, the SPI is forced into idle state.
  The $\overline{SS}$ input also controls the serial data output pin. If $\overline{SS}$ is high (not selected), the serial data output pin is high impedance, and, if $\overline{SS}$ is low, the first bit in the SPI data register is driven out of the serial data output pin. Also, if the slave is not selected ($\overline{SS}$ is high), then the SCK input is ignored and no internal shifting of the SPI shift register occurs.
  Although the SPI is capable of duplex operation, some SPI peripherals are capable of only receiving SPI data in a slave mode. For these simpler devices, there is no serial data out pin.

NOTE

When peripherals with duplex capability are used, take care not to simultaneously enable two receivers whose serial outputs drive the same system slave’s serial data output line.

As long as no more than one slave device drives the system slave’s serial data output line, it is possible for several slaves to receive the same transmission from a master, although the master would not receive return information from all of the receiving slaves.

If the CPHA bit in SPI control register 1 is clear, odd numbered edges on the SCK input cause the data at the serial data input pin to be latched. Even numbered edges cause the value previously latched from the serial data input pin to shift into the LSB or MSB of the SPI shift register, depending on the LSBFE bit.

If the CPHA bit is set, even numbered edges on the SCK input cause the data at the serial data input pin to be latched. Odd numbered edges cause the value previously latched from the serial data input pin to shift into the LSB or MSB of the SPI shift register, depending on the LSBFE bit.

When CPHA is set, the first edge is used to get the first data bit onto the serial data output pin. When CPHA is clear and the $\overline{SS}$ input is low (slave selected), the first bit of the SPI data is driven out of the serial data output pin. After the nth[(276)] shift, the transfer is considered complete and the received data is transferred into the SPI data register. To indicate transfer is complete, the SPIF flag in the SPI status register is set.

Notes

276.n depends on the selected transfer width, refer to Section 5.23.3.2.2, “SPI Control Register 2 (SPICR2)"

NOTE

A change of the bits CPOL, CPHA, SSOE, LSBFE, MODFEN, SPC0, or BIDIROE with SPC0 set in slave mode, will corrupt a transmission in progress and must be avoided.

5.25.3.4 D2DI Control Register 1 (D2DCTL1)

This register is used to enable the D2DI interrupt and set number of D2DCLK cycles before a timeout error is asserted.

Table 553. D2DI Control Register 1 (D2DCTL1)

Offset 0x1 Access: User read/write

	7	6	5	4	3	2	1	0
R	D2DIE	0	0	0	TIMOUT[3:0]			
W								
Reset	0	0	0	0	0	0	0	0

Table 554. D2DCTL1 Register Field Descriptions

Field	Description
7 D2DIE	**D2D Interrupt Enable** — Enables the external interrupt 0 External Interrupt is disabled 1 External Interrupt is enabled
6:4	Reserved, should be written to 0 to ensure compatibility with future versions of this interface.
3:0 TIMOUT	**Time-out Setting** — Defines the number of D2DCLK cycles to wait after the last transaction cycle until a timeout is asserted. In case of a timeout the TIMEF flag in the D2DSTAT0 register will be set. These bits are write-once in normal modes and can always be written in special modes. 0000 The acknowledge is expected directly after the last transfer, i.e. the target must not insert a wait cycle. 0001 - 1111: The target may insert up to TIMOUT wait states before acknowledging a transaction until a timeout is asserted

NOTE

"Write-once" means that after writing D2DCNTL0.D2DEN=1 the write accesses to these bits have no effect.

5.25.3.5 D2DI Status Register 0 (D2DSTAT0)

This register reflects the status of the D2DI transactions.

Table 555. D2DI Status Register 0 (D2DSTAT0)

Offset 0x2 Access: User read/write

	7	6	5	4	3	2	1	0
R	ERRIF	ACKERF	CNCLF	TIMEF	TERRF	PARF	PAR1	PAR0
W								
Reset	0	0	0	0	0	0	0	0

Table 556. D2DI Status Register 0 Field Descriptions

Field	Description
7 ERRIF	**D2DI error interrupt flag** — This status bit indicates that the D2D initiator has detected an error condition (summary of the following five flags).This interrupt is not locally maskable. Write a 1 to clear the flag. Writing a 0 has no effect. 0 D2DI has not detected an error during a transaction. 1 D2DI has detected an error during a transaction.
6 ACKERF	**Acknowledge Error Flag**— This read-only flag indicates that in the acknowledge cycle not all data inputs are sampled high, indicating a potential broken wire. This flag is cleared when the ERRIF bit is cleared by writing a 1 to the ERRIF bit.
5 CNCLF	**CNCLF** — This read-only flag indicates the initiator has canceled a transaction and replaced it by an IDLE command due to a pending error flag (ERRIF). This flag is cleared when the ERRIF bit is cleared by writing a 1 to the ERRIF bit.
4 TIMEF	**Time Out Error Flag** — This read-only flag indicates the initiator has detected a time-out error. This flag is cleared when the ERRIF bit is cleared by writing a 1 to the ERRIF bit.

5.25.4.8 Low Power Mode Options

5.25.4.8.1 D2DI in Run Mode

In run mode, with the D2D Interface enable (D2DEN) bit in the D2D control register 0 clear, the D2DI system is in a low-power, disabled state. D2D registers remain accessible, but clocks to the core of this module are disabled. On D2D lines the GPIO function is activated.

5.25.4.8.2 D2DI in Wait Mode

D2DI operation in wait mode depends upon the state of the D2DSWAI bit in D2D control register 0.

- If D2DSWAI is clear, the D2DI operates normally when the CPU is in the wait mode
- If D2DSWAI is set and the CPU enters the wait mode, any pending transmission is completed. When the D2DCLK output is driven low then the clock generation is stopped, all internal clocks to the D2DI module are stopped as well and the module enters a power saving state.

5.25.4.8.3 D2DI in Stop Mode

If the CPU enters the STOP mode, the D2DI shows the same behavior as for the wait mode with an activated D2DSWAI bit.

5.25.4.8.4 Reset

In case of reset any transaction is immediately stopped and the D2DI module is disabled.

5.25.4.8.5 Interrupts

The D2DI only originates interrupt requests when D2DI is enabled (D2DIE bit in D2DCTL0 set). There are two different interrupt requests from the D2D module. The interrupt vector offset and interrupt priority are chip dependent.

5.25.4.8.5.1 D2D External Interrupt

This is a level sensitive active high external interrupt driven by the D2DINT input. This interrupt is enabled if the D2DIE bit in the D2DCTL1 register is set. The interrupt must be cleared using an target specific clearing sequence. The status of the D2D input pin can be observed by reading the D2DIF bit in the D2DSTAT1 register.

The D2DINIT signal is also asserted in the wait and stop mode; it can be used to leave these modes.

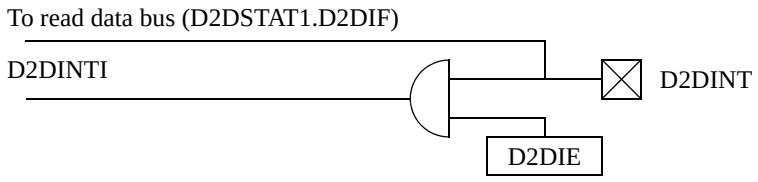


Figure 119. D2D External Interrupt Scheme

5.25.4.8.5.2 D2D Error Interrupt

Those D2D interface specific interrupts are level sensitive and are all cleared by writing a 1 to the ERRIF flag in the D2DSTAT0 register. This interrupt is not locally maskable and should be tied to the highest possible interrupt level in the system, on an S12 architecture to the XIRQ. See the chapter “Vectors” of the MCU description for details.