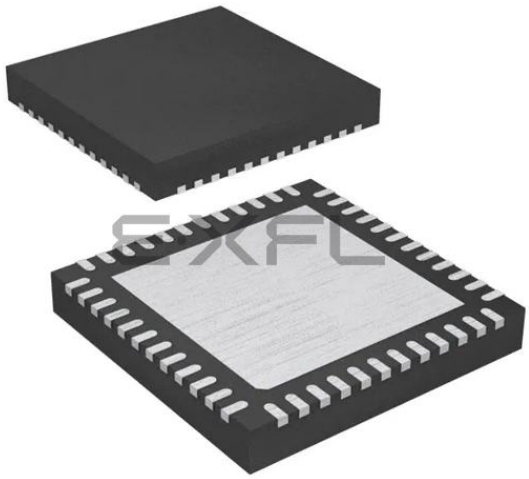

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Product Status	Obsolete
Applications	Battery Monitor
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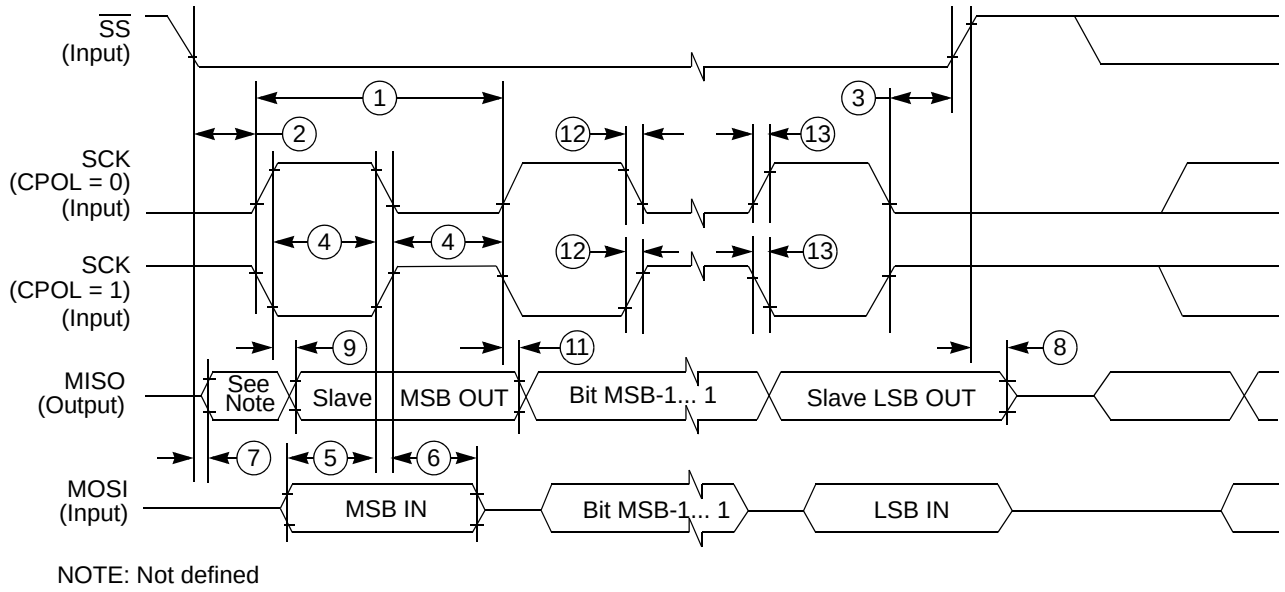
Controller Series	HCS12
RAM Size	6K x 8
Interface	LIN, SCI, SPI
Number of I/O	8
Voltage - Supply	2.25V ~ 5.5V
Operating Temperature	-40°C ~ 105°C
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN-EP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mm912j637av1epr2

Table of Contents

Table 4. MM912_637 Pin Description

Pin #	Pin Name	Formal Name	Description
40	TCLK	Test Clock Input	Test mode clock input pin for Test mode only. This pin must be grounded in user mode.
41	GNDSUB	Substrate Ground	Substrate ground connection to improve EMC behavior.
42	VDDL	Low Power Voltage Regulator Output	2.5 V low power voltage regulator output pin. See Section 5.2, “Analog Die - Power, Clock and Resets - PCR".
43	TEST_A	Test Mode	Analog die Test mode pin for Test mode only. This pin must be grounded in user mode.
44	DGND	Digital Ground	This pin is the device digital ground connection. See Section 5.2, “Analog Die - Power, Clock and Resets - PCR".
45	$\overline{\text{RESET\_A}}$	Reset I/O	Reset output pin of the analog die. Active low signal with internal pull-up. V_{DDX} based. See Section 5.2, “Analog Die - Power, Clock and Resets - PCR".
46	$\overline{\text{RESET}}$	MCU Reset	Bidirectional reset I/O pin of the MCU die. Active low signal with internal pull-up. V_{DDRX} based. See Section 5.2, “Analog Die - Power, Clock and Resets - PCR".
47	BKGD	MCU Background Debug and Mode	The BKGD/MODC pin is used as a pseudo-open-drain pin for the background debug communication. It is used as an MCU operating mode select pin during reset. The state of this pin is latched to the MODC bit at the rising edge of $\overline{\text{RESET}}$. The BKGD pin has a pull-up device. See Section 5.19, “MCU - Debug Module (S12SDBG)".
48	PA7	MCU PA7	General purpose port A input or output pin 7. See Section 5.16, “MCU - Port Integration Module (9S12I128PIMV1)".



NOTE: Not defined

Figure 11. SPI Slave Timing (CPHA = 1)

The timing characteristics for slave mode are listed in Table 46.

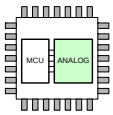
Table 46. SPI Slave Mode Timing Characteristics

Num	C	Characteristic	Symbol	Min	Typ	Max	Unit
1	D	SCK Frequency	f_{SCK}	DC	—	1/4	f_{BUS}
1	D	SCK Period	t_{SCK}	4.0	—	∞	f_{BUS}
2	D	Enable Lead Time	t_{LEAD}	4.0	—	—	f_{BUS}
3	D	Enable Lag Time	t_{LAG}	4.0	—	—	f_{BUS}
4	D	Clock (SCK) High or Low Time	t_{WSCK}	4.0	—	—	f_{BUS}
5	D	Data Setup Time (inputs)	t_{SU}	8.0	—	—	ns
6	D	Data Hold Time (inputs)	t_{HI}	8.0	—	—	ns
7	D	Slave Access Time (time to data active)	t_{A}	—	—	20	ns
8	D	Slave MISO Disable Time	t_{DIS}	—	—	22	ns
9	D	Data Valid After SCK Edge	t_{VSCK}	—	—	$29 + 0.5 \cdot t_{BUS}$ (63)	ns
10	D	Data Valid After $\overline{SS}$ Fall	t_{VSS}	—	—	$29 + 0.5 \cdot t_{BUS}$ (63)	ns
11	D	Data Hold Time (outputs)	t_{HO}	20	—	—	ns
12	D	Rise and Fall Time Inputs	t_{RFI}	—	—	8.0	ns
13	D	Rise and Fall Time Outputs	t_{RFO}	—	—	8.0	ns

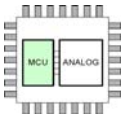
Notes
63.0.5 t_{BUS} added due to internal synchronization delay

5 Functional Description and Application Information

This chapter describes the MM912_637 dual die device functions on a block by block base. The following symbols are shown on all module cover pages to distinguish between the module location being the MCU die or the analog die:



The documented module is physically located on the Analog die. This applies to Section 5.1, “MM912_637 - Analog Die Overview" through Section 5.14, “Die to Die Interface - Target".



The documented module is physically located on the Microcontroller die. This applies to Section 5.1, “MM912_637 - Analog Die Overview" through Section 5.25, “MCU - Die-to-Die Initiator (D2DIV1)".

Sections concerning both die or the complete device will not have a specific indication (e.g. Section 6, “MM912_637 - Trimming").

5.0.1 Introduction

Many types of electronic control units (ECUs) are connected to and supplied from the main car battery in modern cars. Depending on the cars mode of operation (drive, start, stop, standby), the battery must deliver different currents to the different ECUs. The vehicle power management has several sub-functions, like control of the set-point value of the power generator, dynamic load management during drive, start, stop, and standby mode.

The Application Specific Integrated Circuit (ASIC) allows for two application circuits, depending on whether the bias current of the MM912_637 itself shall be included into the current measurement.

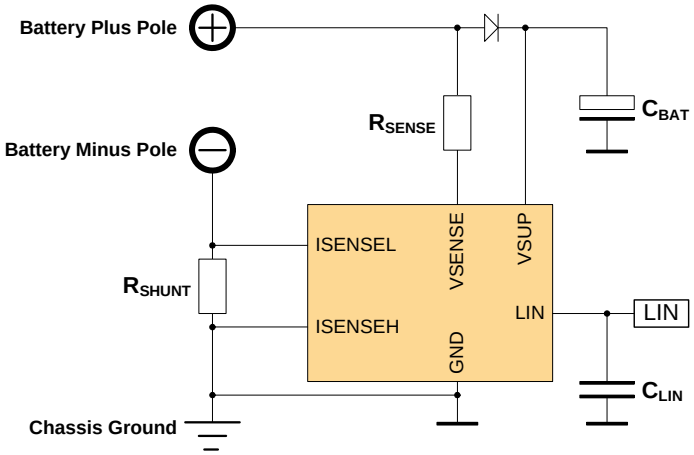


Figure 12. Typical IBS Application (Device GND = Chassis GND)

Table 63. Analog die Registers - 0x0200–0x02FF D2D Blocking Access (D2DI) 2 of 3/ 0x0300–0x03FF D2D Non Blocking Access (D2DI) 3 of 3

Offset[71]	Name		15 7	14 6	13 5	12 4	11 3	10 2	9 1	8 0
0x96	LPF_A11 (hi)	R	A11[15:0]							
	A11 filter coefficient	W								
0x97	LPF_A11 (lo)	R								
	A11 filter coefficient	W								
0x98	LPF_A12 (hi)	R	A12[15:0]							
	A12 filter coefficient	W								
0x99	LPF_A12 (lo)	R								
	A12 filter coefficient	W								
0x9A	LPF_A13 (hi)	R	A13[15:0]							
	A13 filter coefficient	W								
0x9B	LPF_A13 (lo)	R								
	A13 filter coefficient	W								
0x9C	LPF_A14 (hi)	R	A14[15:0]							
	A14 filter coefficient	W								
0x9D	LPF_A14 (lo)	R								
	A14 filter coefficient	W								
0x9E	LPF_A15 (hi)	R	A15[15:0]							
	A15 filter coefficient	W								
0x9F	LPF_A15 (lo)	R								
	A15 filter coefficient	W								
0xA0	COMP_CTL Compensation control register	R	0	0	0	0	0	0		0
		W	BGCALM[1:0]		PGAZM	PGAOM	DIAGVM	DIAGIM		CALIEM
		R	BGCAL[1:0]		PGAZ	PGAO	DIAGV	DIAGI		CALIE
		W								
0xA2	COMP_SR	R	0	BGRF	0	PGAOF	0	0	0	CALF
	Compensation status register	W	Write 1 will clear the flags							
0xA3	COMP_TF	R	0	0	0	0	0	TMF[2:0]		
	Temperature filtering period	W								
0xA4	COMP_TMAX Max temp before recalibration	R	TCMAX[15:0]							
		W								
		R								
		W								
0xA6	COMP_TMIN Min temp before recalibration	R	TCMIN[15:0]							
		W								
		R								
		W								
0xA8	Reserved	R	0	0	0	0	0	0	0	0
		W								
0xA9	Reserved	R	0	0	0	0	0	0	0	0
		W								
0xAA	COMP_VO	R	VOC[7:0]							
	Offset voltage compensation	W								

Table 97. Interrupt Mask Register (INT_MSK (hi)) - Register Field Descriptions

Field	Description
7 TOVM	Timer overflow interrupt mask 0 - Interrupt enabled 1 - Interrupt disabled
6 CH3M	Timer channel 3 interrupt mask 0 - Interrupt enabled 1 - Interrupt disabled
5 CH2M	Timer channel 2 interrupt mask 0 - Interrupt enabled 1 - Interrupt disabled
4 CH1M	Timer channel 1 interrupt mask 0 - Interrupt enabled 1 - Interrupt disabled
3 CH0M	Timer channel 1 interrupt mask 0 - Interrupt enabled 1 - Interrupt disabled
2 LTIM	LIN driver over-temperature interrupt mask 0 - Interrupt enabled 1 - Interrupt disabled
1 HTIM	High temperature interrupt mask 0 - Interrupt enabled 1 - Interrupt disabled
0 UVIM	Under-voltage interrupt mask 0 - Interrupt enabled 1 - Interrupt disabled

5.3.5.3.5 Interrupt Mask Register (INT_MSK (lo))

Table 98. Interrupt mask register (INT_MSK (lo))

Offset[104] 0x0D — Access: User read/write

	7	6	5	4	3	2	1	0
R	0	0	CALM	LTCM	CVMM	RXM	TXM	ERRM
W								
Reset	0	0	0	0	0	0	0	0

Notes
104.Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 99. Interrupt Mask Register (INT_MSK (lo)) - Register Field Descriptions

Field	Description
5 CALM	Calibration request interrupt mask 0 - Interrupt enabled 1 - Interrupt disabled
4 LTCM	Life time counter interrupt mask 0 - Interrupt enabled 1 - Interrupt disabled
3 CVMM	Current / Voltage measurement interrupt mask 0 - Interrupt enabled 1 - Interrupt disabled

Table 104. Offset Compensation - Temperature Channel[106]

ITOC[7:0] ETOC[7:0]	Temperature Channel Offset Compensation[107]
0x7F	+9.689
0x7E	+9.613
0x7D	+9.537
.	.
.	.
0x03	+0.229
0x02	+0.153
0x01	+0.076
0x00 (default)	0
0xFF	-0.076
0xFE	-0.153
0xFD	-0.229
.	.
.	.
0x82	-9.613
0x81	-9.689
0x80	-9.766

Notes
106.Typical values based on default gain setting
107.SD input related (mV)

NOTE

Factory trimmed compensation values are only available for the internal temperature channel.

5.7.5 Calibration

To ensure the maximum precision of the current and voltage sense module, several stages of calibration are implemented to compensate temperature effects. The calibration concept combines the availability of FLASH and the temperature information to guarantee the measurement accuracy under all functional conditions.

The trimming and calibration procedures are split in three different categories: Power On-, Calibration Request-, and Optional Verification Procedures.

5.7.5.1 System Power On Procedure

Several device parameters are guaranteed with full precision after system trimming only. During final test of the device, trim values are computed, verified, and stored into the system FLASH memory.

To ensure optimum system performance, the following power on procedure has to be performed during power on. As the device is typically constantly powered during its operation, this operation has to be performed typically one time only.

During a system power loss or low power reset condition, the application software has to ensure the procedure executes again.

Table 108. Module Memory Map

Offset	Name		7	6	5	4	3	2	1	0
0x58	ACQ_CTL Acquisition control register	R	0	0	0	0	0	0	0	0
		W	AHCRM	OPTEM	OPENEM	CVMIEM	ETMENM	ITMENM	VMENM	CMENM
		R	0	OPTE	OPENE	CVMIE	ETMEN	ITMEN	VMEN	CMEN
		W	AHCR							
0x5A	ACQ_SR (hi)	R	AVRF	PGAG	VMOW	CMOW	ETM	ITM	VM	CM
	Acquisition status register	W	Write 1 will clear the flags							
0x5B	ACQ_SR (lo)	R	OPEN	0	0	VTH	ETCHOP	ITCHOP	VCHOP	CCHOP
	Acquisition status register	W								
0x5C	ACQ_ACC1 Acquisition chain control 1	R	0	0	0	0	0	0	0	0
		W	TCOMPM	VCOMPM	CCOMPM	LPFENM	ETCHOPM	ITCHOPM	CVCHOPM	AGENM
		R	TCOMP	VCOMP	CCOMP	LPFEN	ETCHOP	ITCHOP	CVCHOP	AGEN
		W								
0x5E	ACQ_ACC0 Acquisition chain control 0	R	0	0	0	0	0	0	0	0
		W	ZEROM	ECAPM	TADCGM	VADCGM	CADCGM	TDENM	VDENM	CDENM
		R	ZERO	ECAP	TADCG	VADCG	CADCG	TDEN	VDEN	CDEN
		W								
0x60	ACQ_DEC	R	0	0	0	0	0	DEC[2:0]		
	Decimation Rate	W								
0x61	ACQ_BGC	R	0	0	BGADC[1:0]		BGLDO	BG3EN	BG2EN	BG1EN
	BandGap control	W								
0x62	ACQ_GAIN	R	0	0	0	0	0	IGAIN[2:0]		
	PGA gain	W								
0x63	ACQ_GCB	R	D[7:0]							
	GCB threshold	W								
0x64	ACQ_ITEMP (hi)	R	ITEMP[15:8]							
	Internal temp. measurement result	W								
0x65	ACQ_ITEMP (lo)	R	ITEMP[7:0]							
	Internal temp. measurement result	W								
0x66	ACQ_ETEMP (hi)	R	EEMP[15:8]							
	External temp. measurement result	W								
0x67	ACQ_ETEMP (lo)	R	EEMP[7:0]							
	External temp. measurement result	W								
0x68	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x69	ACQ_CURR1	R	CURR[23:16]							
	Current measurement result	W								

5.9.4.2 Prescaler

The prescaler divides the bus clock by 1, 2, 4, 8,16, 32, 64, or 128. The prescaler select bits, PR[2:0], select the prescaler divisor. PR[2:0] are in the timer system control register 2 (TSCR2).

5.9.4.3 Input Capture

Clearing the I/O (input/output) select bit, IOSn, configures channel n as an input capture channel. The input capture function captures the time at which an external event occurs. When an active edge occurs on the pin of an input capture channel, the timer transfers the value in the timer counter into the timer channel registers, TCn.

The minimum pulse width for the input capture input is greater than two bus clocks. An input capture on channel n sets the CnF flag. The CnI bit enables the CnF flag to generate interrupt requests.

5.9.4.4 Output Compare

Setting the I/O select bit, IOSn, configures channel n as an output compare channel. The output compare function can generate a periodic pulse with a programmable polarity, duration, and frequency. When the timer counter reaches the value in the channel registers of an output compare channel, the timer can set, clear, or toggle the channel pin. An output compare on channel n sets the CnF flag. The CnI bit enables the CnF flag to generate interrupt requests.

The output mode and level bits, OMn and OLn, select set, clear, toggle on output compare. Clearing both OMn and OLn disconnects the pin from the output logic. Setting a force output compare bit, FOCn, causes an output compare on channel n. A forced output compare does not set the channel flag.

A successful output compare on channel 3 overrides output compares on all other output compare channels. The output compare 3 mask register masks the bits in the output compare 3 data register. The timer counter reset enable bit, TCRE, enables channel 3 output compares to reset the timer counter.Writing to the timer port bit of an output compare pin does not affect the pin state. The value written is stored in an internal latch. When the pin becomes available for general-purpose output, the last value written to the bit appears at the pin.

5.9.5 Resets

5.9.5.1 General

The reset state of each individual bit is listed within the Register Description Section 5.9.3, “Memory Map and Registers", which details the registers and their bit-fields.

5.9.6 Interrupts

5.9.6.1 General

This section describes interrupts originated by the TIM16B4C block. Table 225 lists the interrupts generated by the TIM16B4C to communicate with the MCU.

Table 225. TIM16B4C Interrupts

Interrupt	Offset	Vector	Priority	Source	Description
C[3:0]F	-	-	-	Timer Channel 3-0	Active high timer channel interrupts 3-0
TOF	-	-	-	Timer Overflow	Timer Overflow interrupt

5.9.6.2 Description of Interrupt Operation

The TIM16B4C uses a total of 5 interrupt vectors. The interrupt vector offsets and interrupt numbers are chip dependent. More information on interrupt vector offsets and interrupt numbers can be found in Section 5.3, “Interrupt Module - IRQ".

5.10.5.3.3 GPIO Port Data Register (GPIO_DATA)

Table 231. GPIO Port Data Register (GPIO_DATA)

Offset[199] 0x43 Access: User read

	7	6	5	4	3	2	1	0
R	0	0	0	0	PD3[200]	PD2	PD1	PD0
W								

Notes
199.Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.
200.Due the different implementation of the L0/PTB3, PTWU needs to be set in the GPIO_IN3 to read the PD3 port status during normal mode.

Table 232. GPIO Port Data Register (GPIO_DATA)

Field	Description
3 PD3	PTB3 Data Register A read returns the value of the PTB3 buffer.
2 PD2	PTB2 Data Register A read returns the value of the PTB2 buffer.
1 PD1	PTB1 Data Register A read returns the value of the PTB1 buffer.
0 PD0	PTB0 Data Register A read returns the value of the PTB0 buffer.

5.10.5.3.4 Port 0 Input Configuration (GPIO_IN0)

Table 233. Port 0 Input Configuration (GPIO_IN0)

Offset[201] 0x44 Access: User read/write

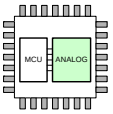
	7	6	5	4	3	2	1	0
R	0	TCAP3	TCAP2	TCAP1	TCAP0	SCIRX	LINTX	0
W								
Reset	0	0	0	0	0	0	0	0

Notes
201.Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 234. Port 0 input configuration (GPIO_IN0)

Field	Description
6 TCAP3	PTB0 - Timer Input Capture Channel 3 0 - PTB0 Input buffer disconnected from Timer Channel 3 - Input Capture 1 - PTB0 Input buffer routed to Timer Channel 3 - Input Capture
5 TCAP2	PTB0 - Timer Input Capture Channel 2 0 - PTB0 Input buffer disconnected from Timer Channel 2 - Input Capture 1 - PTB0 Input buffer routed to Timer Channel 2 - Input Capture
4 TCAP1	PTB0 - Timer Input Capture Channel 1 0 - PTB0 Input buffer disconnected from Timer Channel 1 - Input Capture 1 - PTB0 Input buffer routed to Timer Channel 1 - Input Capture
3 TCAP0	PTB0 - Timer Input Capture Channel 0 0 - PTB0 Input buffer disconnected from Timer Channel 0 - Input Capture 1 - PTB0 Input buffer routed to Timer Channel 0 - Input Capture

5.12 Serial Communication Interface (S08SCIV4)



5.12.1 Introduction

5.12.1.1 Features

Features of SCI module include:

- Full-duplex, standard non-return-to-zero (NRZ) format
- Double-buffered transmitter and receiver with separate enables
- Programmable baud rates (13-bit modulo divider)
- Interrupt-driven or polled operation:
  - Transmit data register empty and transmission complete
  - Receive data register full
  - Receive overrun, parity error, framing error, and noise error
  - Idle receiver detect
  - Active edge on receive pin
  - Break detect supporting LIN
- Hardware parity generation and checking
- Programmable 8-bit or 9-bit character length
- Receiver wake-up by idle-line or address-mark
- Optional 13-bit break character generation / 11-bit break character detection
- Selectable transmitter output polarity

5.12.1.2 Modes of Operation

See Section 5.12.3, “Functional Description", for details concerning SCI operation in these modes:

- 8- and 9-bit data modes
- Loop mode
- Single-wire mode

5.12.1.3 Block Diagram

Figure 46 shows the transmitter portion of the SCI.

5.15.8.2 Low Power Operation

The MM912_637 has two static low-power modes Pseudo Stop and Stop mode. For a detailed description refer to the S12CPMU section.

5.15.9 Security

The MCU security mechanism prevents unauthorized access to the Flash memory. Refer to Section 5.20, “MCU - Security (S12XS9SECV2)", Section 5.21.4.1, “Security", and Section 5.24.5, “Security". Resets and Interrupts

Consult the S12 CPU manual and the S12SINT section for information on exception processing.

5.15.9.1 Resets

Table 287 lists all Reset sources and the vector locations. Resets are explained in detail in Section 5.22, “S12 Clock, Reset, and Power Management Unit (S12CPMU)".

Table 287. Reset Sources and Vector Locations

Vector Address	Reset Source	CCR Mask	Local Enable
$FFFE	Power-On Reset (POR)	None	None
$FFFE	Low Voltage Reset (LVR)	None	None
$FFFE	External pin $\overline{\text{RESET}}$	None	None
$FFFE	Illegal Address Reset	None	None
$FFFC	Clock monitor reset	None	OSCE Bit in CPMUOSC register
$FFFA	COP watchdog reset	None	CR[2:0] in CPMUCOP register

5.15.9.2 Interrupt Vectors

Table 288 lists all interrupt sources and vectors in the default order of priority. The interrupt module (see Section 5.17, “MCU - Interrupt Module (S12SINTV1)") provides an interrupt vector base register (IVBR) to relocate the vectors.

Table 288. Interrupt Vector Locations (Sheet 1 of 2)

Vector Address[236]	Interrupt Source	CCR Mask	Local Enable	Wake-up from STOP	Wake-up from WAIT
Vector base + $F8	Unimplemented instruction trap	None	None	-	-
Vector base+ $F6	SWI	None	None	-	-
Vector base+ $F4	D2DI Error Interrupt	X Bit	None	Yes	Yes
Vector base+ $F2	D2DI External Interrupt	I bit	D2DCTL (D2DIE)	Yes	Yes
Vector base+ $F0	RTI timeout interrupt	I bit	CPMUINT (RTIE)	3.22.6 Interrupts	
Vector base + $EE to Vector base + $DA	Reserved				
Vector base + $D8	SPI	I bit	SPICR1 (SPIE, SPTIE)	No	Yes
Vector base + $D6 to Vector base + $CA	Reserved				
Vector base + $C8	Oscillator status interrupt	I bit	CPMUINT (OSCIE)	No	No
Vector base + $C6	PLL lock interrupt	I bit	CPMUINT (LOCKIE)	No	No
Vector base + $C4 to Vector base + $BC	Reserved				

Table 310. Interrupt Vector Base Register (IVBR)

Address: 0x001F

	7	6	5	4	3	2	1	0
R W	IVB_ADDR[7:0]							
Reset	1	1	1	1	1	1	1	1

Read: Anytime.
Write: Anytime.

Table 311. IVBR Field Descriptions

Field	Description
7–0 IVB_ADDR[7:0]	**Interrupt Vector Base Address Bits** — These bits represent the upper byte of all vector addresses. Out of reset, these bits are set to 0xFF (i.e., vectors are located at 0xFF80–0xFFFE) to ensure compatibility to HCS12. **Note:** A system reset will initialize the interrupt vector base register with “0xFF” before it is used to determine the reset vector address. Therefore, changing the IVBR has no effect on the location of the three reset vectors (0xFFFA–0xFFFE). **Note:** If the BDM is active (i.e., the CPU is in the process of executing BDM firmware code), the contents of IVBR are ignored and the upper byte of the vector address is fixed as “0xFF”. This is done to enable handling of all non-maskable interrupts in the BDM firmware.

5.17.4 Functional Description

The INT module processes all exception requests to be serviced by the CPU module. These exceptions include interrupt vector requests and reset vector requests. Each of these exception types and their overall priority level is discussed in the following subsections.

5.17.4.1 S12S Exception Requests

The CPU handles both reset requests and interrupt requests. A priority decoder is used to evaluate the priority of pending interrupt requests.

5.17.4.2 Interrupt Prioritization

The INT module contains a priority decoder to determine the priority for all interrupt requests pending for the CPU. If more than one interrupt request is pending, the interrupt request with the higher vector address wins the prioritization.

The following conditions must be met for an I bit maskable interrupt request to be processed.

1. The local interrupt enabled bit in the peripheral module must be set.
2. The I bit in the condition code register (CCR) of the CPU must be cleared.
3. There is no SWI, TRAP, or X bit maskable request pending.

NOTE

All non I bit maskable interrupt requests always have higher priority than the I bit maskable interrupt requests. If the X bit in the CCR is cleared, it is possible to interrupt an I bit maskable interrupt by an X bit maskable interrupt. It is possible to nest non maskable interrupt requests, e.g., by nesting SWI or TRAP calls.

Since an interrupt vector is only supplied at the time when the CPU requests it, it is possible that a higher priority interrupt request could override the original interrupt request that caused the CPU to request the vector. In this case, the CPU will receive the highest priority vector and the system will process this interrupt request first, before the original interrupt request is processed.

If the interrupt source is unknown (for example, in the case where an interrupt request becomes inactive after the interrupt has been recognized, but prior to the CPU vector request), the vector address supplied to the CPU will default to that of the spurious interrupt vector.

NOTE

Care must be taken to ensure that all interrupt requests remain active until the system begins execution of the applicable service routine; otherwise, the exception request may not get processed at all or the result may be a spurious interrupt request (vector at address (vector base + 0x0080)).

5.17.4.3 Reset Exception Requests

The INT module supports three system reset exception request types (Refer to the Clock and Reset generator module for details):

1. Pin reset, power-on reset or illegal address reset, low voltage reset (if applicable)
2. Clock monitor reset request
3. COP watchdog reset request

5.17.4.4 Exception Priority

The priority (from highest to lowest) and address of all exception vectors issued by the INT module upon request by the CPU is shown in Table 312.

Table 312. Exception Vector Map and Priority

Vector Address[240]	Source
0xFFFE	Pin reset, power-on reset, illegal address reset, low voltage reset (if applicable)
0xFFFC	Clock monitor reset
0xFFFA	COP watchdog reset
(Vector base + 0x00F8)	Unimplemented opcode trap
(Vector base + 0x00F6)	Software interrupt instruction (SWI) or BDM vector request
(Vector base + 0x00F4)	X bit maskable interrupt request (XIRQ or D2D error interrupt)[241]
(Vector base + 0x00F2)	IRQ or D2D interrupt request[242]
(Vector base + 0x00F0–0x0082)	Device specific I bit maskable interrupt sources (priority determined by the low byte of the vector address, in descending order)
(Vector base + 0x0080)	Spurious interrupt

Notes
240.16-bit vector address based
241.D2D error interrupt on MCUs featuring a D2D initiator module, otherwise XIRQ pin interrupt
242.D2D interrupt on MCUs featuring a D2D initiator module, otherwise IRQ pin interrupt

5.17.5 Initialization/Application Information

5.17.5.1 Initialization

After a system reset, the software should:

1. Initialize the interrupt vector base register, if the interrupt vector table is not located at the default location (0xFF80–0xFFF9).
2. Enable I bit maskable interrupts by clearing the I bit in the CCR.
3. Enable the X bit maskable interrupt by clearing the X bit in the CCR.

5.18.5.1 Chip Bus Control

The S12PMMC controls the address buses and the data buses that interface the bus masters (CPU12, S12SBDM) with the rest of the system (master buses). In addition, the MMC handles all CPU read data bus swapping operations. All internal resources are connected to specific target buses (see Figure 62).

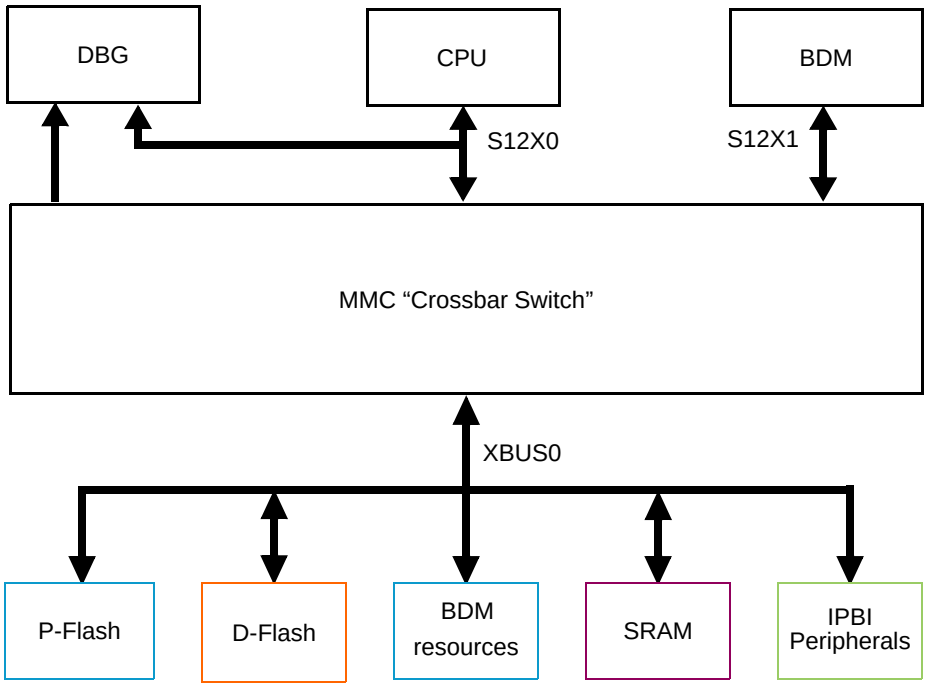


Figure 62. S12I platform

5.18.5.1.1 Master Bus Prioritization Regarding Access Conflicts on Target Buses

The arbitration scheme allows only one master to be connected to a target at any given time. The following rules apply when prioritizing accesses from different masters to the same target bus:

- CPU12 always has priority over BDM.
- BDM has priority over CPU12 when its access is stalled for more than 128 cycles. In the later case the CPU will be stalled after finishing the current operation and the BDM will gain access to the bus.

5.18.5.2 Interrupts

The MMC does not generate any interrupts.

5.18.6 Initialization/Application Information

5.18.6.1 CALL and RTC Instructions

CALL and RTC instructions are uninterruptable CPU instructions that automate page switching in the program page window. The CALL instruction is similar to the JSR instruction, but the subroutine that is called can be located anywhere in the local address space or in any Flash or ROM page visible through the program page window. The CALL instruction calculates and stacks a return address, stacks the current PPAGE value and writes a new instruction-supplied value to the PPAGE register. The PPAGE value controls which of the 256 possible pages is visible through the 16 kbyte program page window in the 64 kbyte local CPU memory map. Execution then begins at the address of the called subroutine.

4. COPOSCSEL: In Normal mode (if PROT=0) until CPMUCOP write once is taken. If COPOSCSEL was cleared by UPOSC=0 (entering Full Stop mode with COPOSCSEL=1 or insufficient OSCCLK quality), then COPOSCSEL can be set again once.

NOTE

After writing CPMUCLKS register, it is strongly recommended to read back CPMUCLKS register to make sure that write of PLLSEL, RTIOSCSEL and COPOSCSEL was successful.

Table 412. CPMUCLKS Descriptions

Field	Description
7 PLLSEL	PLL Select Bit This bit selects the PLLCLK as source of the system clocks (core clock and bus clock). PLLSEL can only be set to 0, if UPOSC=1. UPOSC= 0 sets the PLLSEL bit. Entering Full Stop mode sets the PLLSEL bit. 0 System clocks are derived from OSCCLK if oscillator is up (UPOSC=1, $f_{BUS} = f_{OSC} / 2$. 1 System clocks are derived from PLLCLK, $f_{BUS} = f_{PLL} / 2$.
6 PSTP	Pseudo Stop Bit This bit controls the functionality of the oscillator during Stop mode. 0 Oscillator is disabled in Stop mode (Full Stop mode). 1 Oscillator continues to run in Stop mode (Pseudo Stop mode), option to run RTI and COP. **Note:** Pseudo Stop mode allows for faster STOP recovery and reduces the mechanical stress and aging of the resonator in case of frequent STOP conditions at the expense of a slightly increased power consumption. **Note:** When starting up the external oscillator (either by programming OSCE bit to 1 or on exit from Full Stop mode with OSCE bit is already 1) the software must wait for a minimum time equivalent to the startup time of the external oscillator t_{UPOSC} before entering Pseudo Stop mode.
3 PRE	**RTI Enable During Pseudo Stop Bit** — PRE enables the RTI during Pseudo Stop mode. 0 RTI stops running during Pseudo Stop mode. 1 RTI continues running during Pseudo Stop mode if RTIOSCSEL=1. **Note:** If PRE=0 or RTIOSCSEL=0 then the RTI will go static while Stop mode is active. The RTI counter will not be reset.
2 PCE	**COP Enable During Pseudo Stop Bit** — PCE enables the COP during Pseudo Stop mode. 0 COP stops running during Pseudo Stop mode 1 COP continues running during Pseudo Stop mode if COPOSCSEL=1 **Note:** If PCE=0 or COPOSCSEL=0 then the COP will go static while Stop mode is active. The COP counter will not be reset.
1 RTIOSCSEL	**RTI Clock Select**— RTIOSCSEL selects the clock source to the RTI. Either IRCCLK or OSCCLK. Changing the RTIOSCSEL bit re-starts the RTI timeout period. RTIOSCSEL can only be set to 1, if UPOSC=1. UPOSC= 0 clears the RTIOSCSEL bit. 0 RTI clock source is IRCCLK. 1 RTI clock source is OSCCLK.
0 COPOSCSEL	**COP Clock Select**— COPOSCSEL selects the clock source to the COP. Either IRCCLK or OSCCLK. Changing the COPOSCSEL bit re-starts the COP timeout period. COPOSCSEL can only be set to 1, if UPOSC=1. UPOSC= 0 clears the COPOSCSEL bit. 0 COP clock source is IRCCLK. 1 COP clock source is OSCCLK

5.24.3.2.14 Flash Reserved3 Register (FRSV3)

This Flash register is reserved for factory testing.

Table 499. Flash Reserved3 Register (FRSV3)

Address: 0x010E

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

All bits in the FRSV3 register read 0 and are not writable.

5.24.3.2.15 Flash Reserved4 Register (FRSV4)

This Flash register is reserved for factory testing.

Table 500. Flash Reserved4 Register (FRSV4)

Address: 0x010F

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

All bits in the FRSV4 register read 0 and are not writable.

5.24.3.2.16 Flash Option Register (FOPT)

The FOPT register is the Flash option register.

Table 501. Flash Option Register (FOPT)

Address: 0x0110

	7	6	5	4	3	2	1	0
R	NV[7:0]							
W								
Reset	F	F	F	F	F	F	F	F

= Unimplemented or Reserved

All bits in the FOPT register are readable but are not writable.

During the reset sequence, the FOPT register is loaded from the Flash nonvolatile byte in the Flash configuration field, at global address 0x3_FF0E located in P-Flash memory (see Table 463), as indicated by reset condition F in Figure 501. If a double bit fault is detected while reading the P-Flash phrase containing the Flash nonvolatile byte during the reset sequence, all bits in the FOPT register will be set.

Table 502. FOPT Field Descriptions

Field	Description
7–0 NV[7:0]	**Nonvolatile Bits** — The NV[7:0] bits are available as nonvolatile bits. Refer to the device user guide for proper use of the NV bits.

5.24.4.3.2.1 Define FCCOB Contents

The FCCOB parameter fields must be loaded with all required parameters for the Flash command being executed. Access to the FCCOB parameter fields is controlled via the CCOBIX bits in the FCCOBIX register (see Section 5.24.3.2.3, “Flash CCOB Index Register (FCCOBIX)").

The contents of the FCCOB parameter fields are transferred to the Memory Controller when the user clears the CCIF command completion flag in the FSTAT register (writing 1 clears the CCIF to 0). The CCIF flag will remain clear until the Flash command has completed. Upon completion, the Memory Controller will return CCIF to 1 and the FCCOB register will be used to communicate any results. The flow for a generic command write sequence is shown in Figure 113.

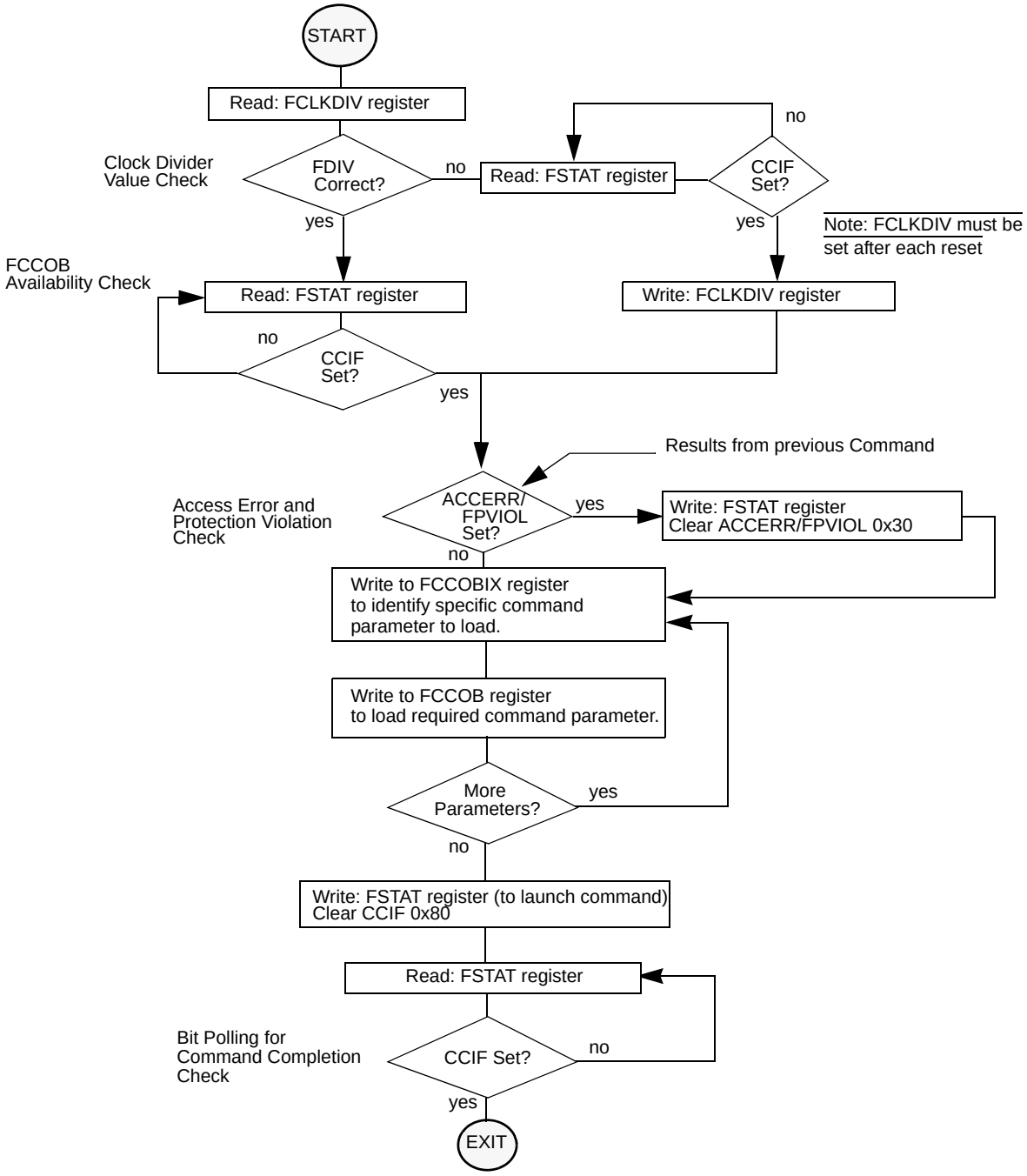


Figure 113. Generic Flash Command Write Sequence Flowchart

Table 565. Module Memory Map

Offset[308]	Name		7	6	5	4	3	2	1	0
0xE7	TRIM_LVT	R	0	0	0	0	0	0	0	LVT
	Trim low voltage threshold	W								
0xE8	TRIM_OSC (hi)	R								
	Trim LP oscillator	W				LPOSC[12:0]				
0xE9	TRIM_OSC (lo)	R								
	Trim LP oscillator	W								
0xEA-0xEF	Reserved	R	0	0	0	0	0	0	0	0
		W								

Notes
308.Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

6.3.2.1 Trim Bandgap 0 (TRIM_BG0 (hi))

Table 566. Trim Bandgap 0 (TRIM_BG0 (hi))

Offset[309] 0xE0 Access: User read/write

	7	6	5	4	3	2	1	0
R	0	0	TCIBG2[2:0]			TCIBG1[2:0]		
W								
Reset	0	0	0	0	0	0	0	0

Notes
309.Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 567. Trim Bandgap 0 (TRIM_BG0 (hi)) - Register Field Descriptions

Field	Description
5-3 TCIBG2[2:0]	The optimal content of this register is determined during final test and stored in the microcontroller IFR. For proper operation of the MM912_637, the content has to be copied to this location. See Section 6.2.1, “IFR - Trimming Content for Analog Die Functionality" for location information.
2-0 TCIBG1[2:0]	

6.3.2.2 Trim Bandgap 0 (TRIM_BG0 (lo))

Table 568. Trim Bandgap 0 (TRIM_BG0 (lo))

Offset[310] 0xE1 Access: User read/write

	7	6	5	4	3	2	1	0
R	0	0	IBG2[2:0]			IBG1[2:0]		
W								
Reset	0	0	0	0	0	0	0	0

Notes
310.Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

6.3.2.9 Trim LP Oscillator (TRIM_OSC (hi), TRIM_OSC (lo))

Table 582. Trim LP Oscillator (TRIM_OSC (hi), TRIM_OSC (lo))

Offset[317] 0xE8 — Access: User read/write

	7	6	5	4	3	2	1	0
R				LPOSC[12:8]				
W								
Reset	0	0	0	0	0	0	0	0
R	LPOSC[7:0]							
W								
Reset	0	0	1	1	1	1	1	1

Notes
317.Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 583. Trim LP Oscillator (TRIM_OSC (hi), TRIM_OSC (lo)) - Register Field Descriptions

Field	Description
12-0 LPOSC[12:0]	The optimal content of this register is determined during final test and stored in the microcontroller IFR. For proper operation of the MM912_637, the content has to be copied to this location. See Section 6.2.1, “IFR - Trimming Content for Analog Die Functionality" for location information.