Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	FR60 RISC
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	I²C
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	49
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f492pmc-ge1

FUJITSU MICROELECTRONICS
DATA SHEET

DS07-16912-1E

32-bit Microcontrollers

CMOS

FR60 MB91490 Series

MB91F492 / FV470

■ DESCRIPTION

The MB91490 series is Fujitsu's general-purpose 32-bit RISC microcontroller, which is designed for embedded control applications that require high-speed processing performance.
This series uses the FR60 CPU, which is compatible with the FR* family of CPUs.

* : FR, the abbreviation of FUJITSU RISC controller, is a line of products of Fujitsu Microelectronics Limited.

■ FEATURES

- FR60 CPU
  - 32-bit RISC, load/store architecture, five-stage pipeline
  - Operating frequency of 80 MHz (PLL clock multiplied)
  - 16-bit fixed-length instructions (basic instructions)
  - Instruction execution speed : one instruction per cycle
  - Memory-to-memory transfer, bit processing, barrel shift instructions, etc. : instructions suitable for embedded applications
  - Function entry and exit instructions, multi load/store instructions of register contents : instructions compatible with C language.
  - Register interlock function to facilitate assembly-language coding
  - Built-in multiplier/instruction-level support
    - Signed 32-bit multiplication : 5 cycles
    - Signed 16-bit multiplication : 3 cycles
  - Interrupts (save PC and PS) : 6 cycles, 16 priority levels
  - Harvard architecture allowing program access and data access to be executed simultaneously
  - Instructions compatible with the FR family

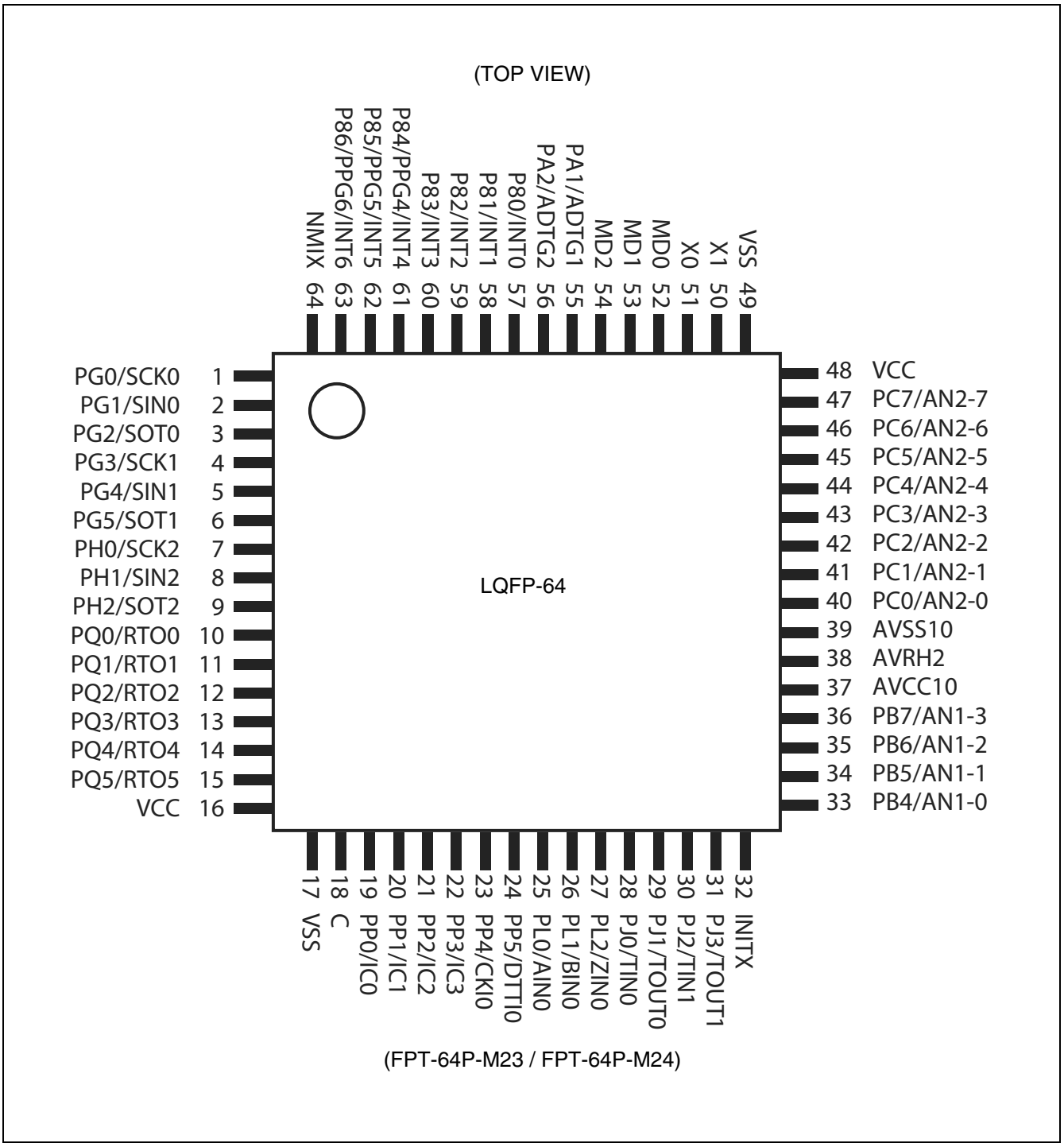
(Continued)

For the information for microcontroller supports, see the following web site.

http://edevice.fujitsu.com/micom/en-support/

2010.2

■ PIN ASSIGNMENT



(FPT-64P-M23 / FPT-64P-M24)

Pin no.	Pin name	I/O circuit type*	Function
4	SCK1 (SCL1)	D	Clock I/O of multi-function serial interface 1 (used in I²C mode, SCL1)
	PG3		General-purpose I/O port
5	SIN1	D	Data input of multi-function serial interface 1 (not used in I²C mode)
	PG4		General-purpose I/O port
6	SOT1 (SDA1)	D	Data output of multi-function serial interface 1 (used in I²C mode, SDA1)
	PG5		General-purpose I/O port
7	SCK2 (SCL2)	D	Clock I/O of multi-function serial interface 2 (used in I²C mode, SCL2)
	PH0		General-purpose I/O port
8	SIN2	D	Data input of multi-function serial interface 2 (not used in I²C mode)
	PH1		General-purpose I/O port
9	SOT2 (SDA2)	D	Data output of multi-function serial interface 2 (used in I²C mode, SDA2)
	PH2		General-purpose I/O port
28	TIN0	D	Base timer 0 input
	PJ0		General-purpose I/O port
29	TOUT0	D	Base timer 0 output
	PJ1		General-purpose I/O port
30	TIN1	D	Base timer 1 input
	PJ2		General-purpose I/O port
31	TOUT1	D	Base timer 1 output
	PJ3		General-purpose I/O port
25	AIN0	D	8/16-bit up count input pin for up/down counter 0
	PL0		General-purpose I/O port
26	BIN0	D	8/16-bit down count input pin for up/down counter 0
	PL1		General-purpose I/O port
27	ZIN0	D	8/16-bit reset input pin for up/down counter 0
	PL2		General-purpose I/O port
19	IC0	D	Trigger input of input capture 0
	PP0		General-purpose I/O port
20	IC1	D	Trigger input of input capture 1
	PP1		General-purpose I/O port

(Continued)

• Order of power turning ON/OFF

Use the following procedure for turning the power on or off. If not using the A/D converter, connect $AV_{CC} = V_{CC}$ and $AV_{SS} = V_{SS}$. Turn on the power supply in the sequence $V_{CC} \rightarrow AV_{CC} \rightarrow$ AVRH2, and turn off the power in the reverse sequence.

• Source oscillation input when turning on the power

When turning the power on, maintain the clock input until the device is released from the oscillation stabilization wait state.

• Cautions for operation during PLL clock mode

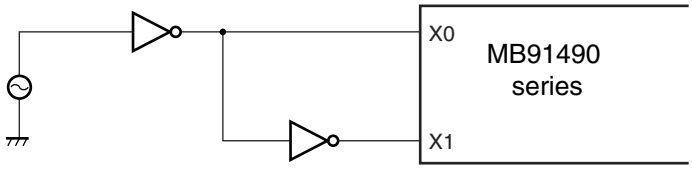
Even if the oscillator comes off or the clock input stops with the PLL clock selected for MB91490 series, MB91490 series may continue to operate at the free-run frequency of the PLL's internal self-oscillating oscillator circuit.
Performance of this operation, however, cannot be guaranteed.

• Using an external clock

When using an external clock, you must always input clock signals with opposite phase from X0 pin to X1 pin simultaneously. However, as the X1 pin halts with an output at the "H" level during stop mode, insert a resistor of approximately 1 kΩ externally to prevent a conflict between the two outputs if using stop mode (oscillation stop mode).

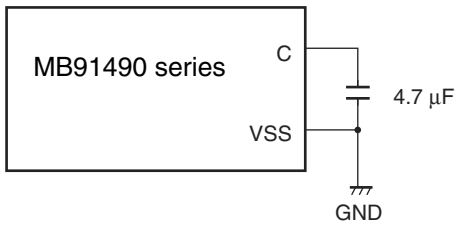
The figure below shows an example of how to use an external clock.

• Example of Using an External Clock



• C pin

As MB91490 series includes an internal regulator, always connect a bypass capacitor of approximately 4.7 µF to the C pin for use by the regulator.

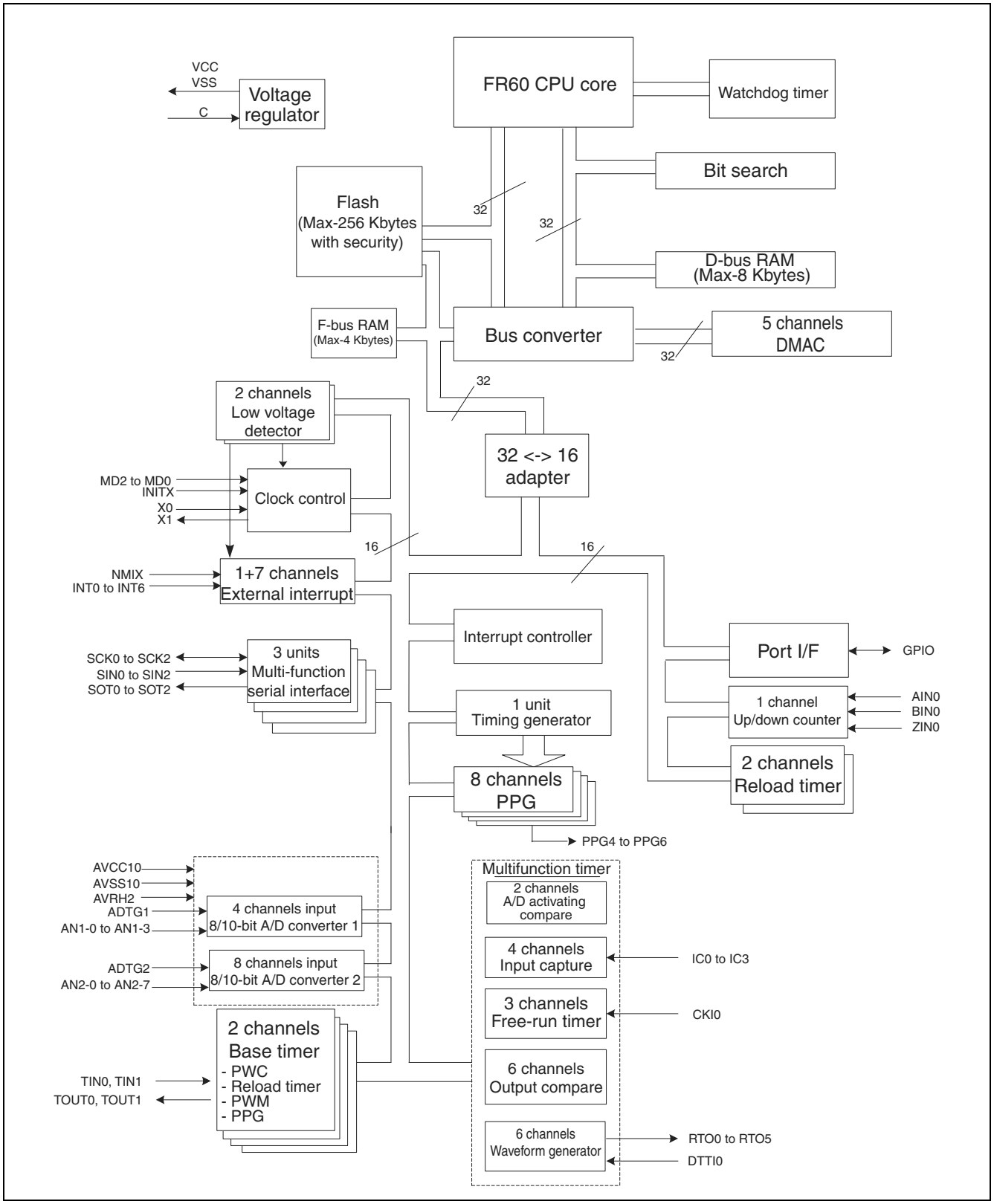


• Software reset on the synchronous mode

Be sure to meet the following two conditions before setting 0 to the SRST bit of STCR (standby control register) when the software reset is used on the synchronous mode.

- Set the interrupt enable flag (I-Flag) to interrupts disabled (I-Flag=0).
- Not used NMI

■ BLOCK DIAGRAM



■ MEMORY SPACE

1. Memory Space

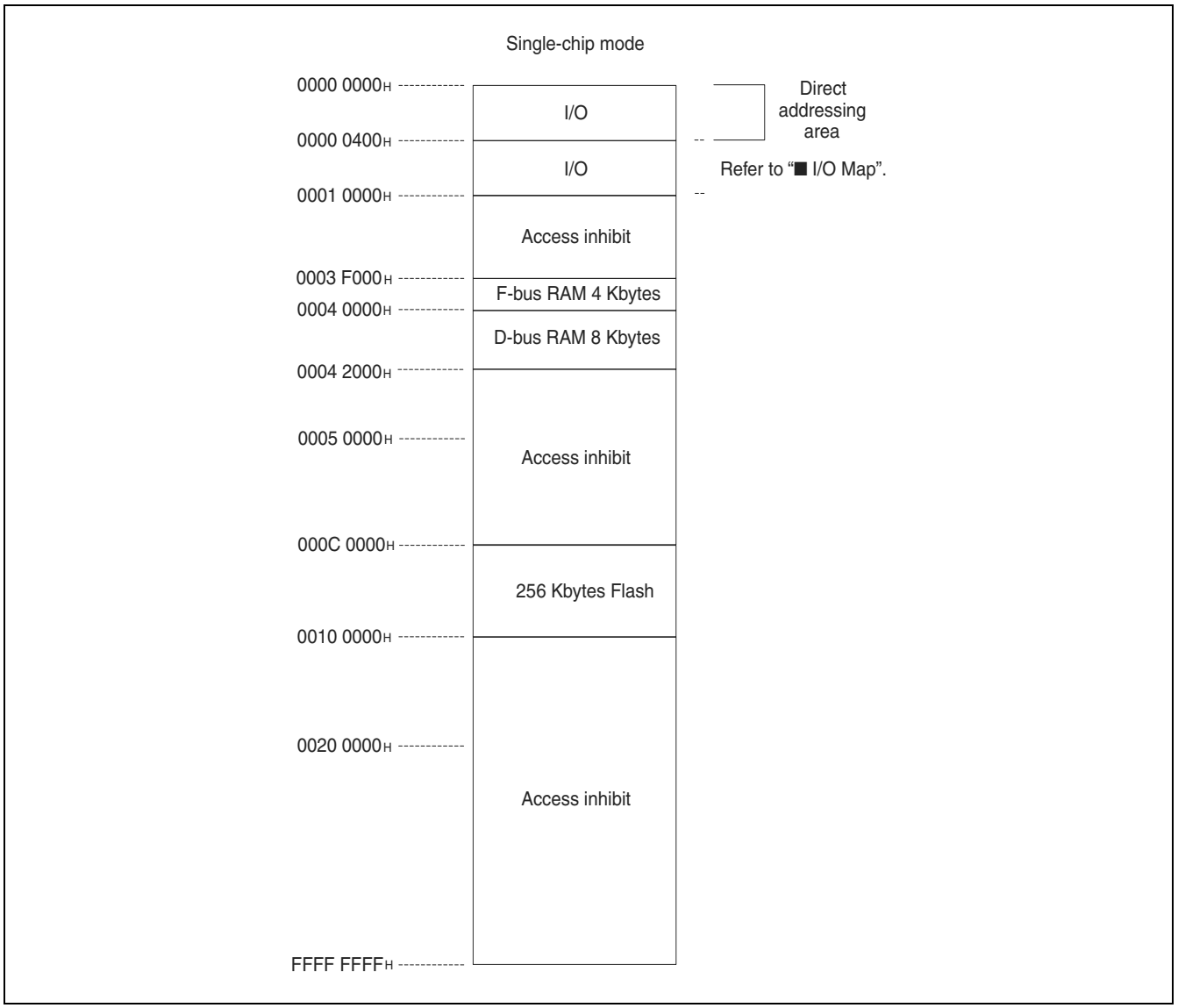
The FR family has 4 Gbytes of logical address space (2^{32} addresses) available to the CPU by linear access.

• Direct Addressing Areas

The following address space areas are used as I/O areas.
These areas are called direct addressing areas, in which the address of an operand can be specified directly by the instruction. The size of directly addressable areas depends on the length of the data being accessed as shown below.

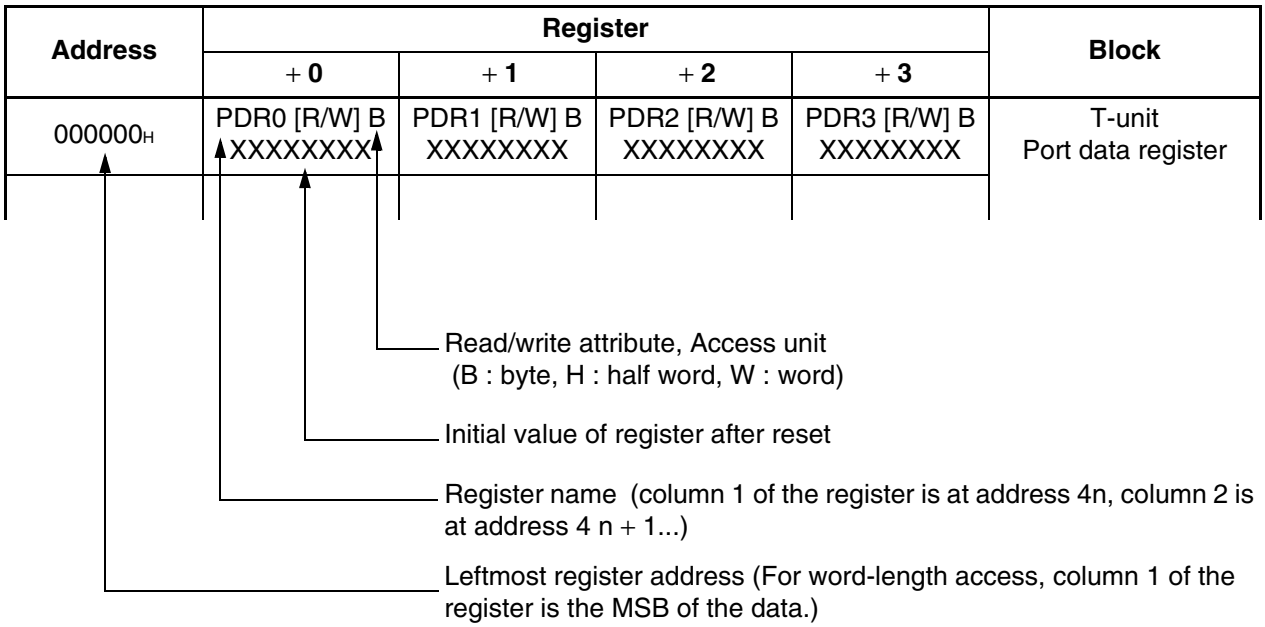
→ byte data access : 000_H to $0FF_H$
→ half word data access : 000_H to $1FF_H$
→ word data access : 000_H to $3FF_H$

2. Memory Map



■ I/O MAP

[How to read the table]



Note : Initial values of register bits are represented as follows :

" 1 " : Initial Value " 1 "

" 0 " : Initial Value " 0 "

" X " : Initial Value " undefined "

" - " : No physical register at this location

Access to addresses where the data access properties have not been documented is prohibited.

Address	Register				Block
	+0	+1	+2	+3	
000060H	SSR0 [R/W, R] B, H, W 00000011	ESCR0 [R/W]/ IBSR0 [R/W, R] B, H, W 00000000	SCR0 [R/W] / IBCR0 [R/W, R] B, H, W 00000000	SMR0 [R/W] B, H, W 000-0000	Multi-function serial interface 0
000064H	BGR01[R/W] B, H, W 00000000	BGR00 [R/W] B, H, W 00000000	RDR0 [R]/ TDR0 [W] H, W -------0 00000000		
000068H	—		ISMK0 [R/W] B, H 01111111	ISBA0 [R/W] B, H 00000000	
00006CH	—				(Reserved)
000070H	SSR1 [R/W, R] B, H, W 00000011	ESCR1 [R/W]/ IBSR1 [R/W, R] B, H, W 00000000	SCR1 [R/W] / IBCR1 [R/W, R] B, H, W 00000000	SMR1 [R/W] B, H, W 000-0000	Multi-function serial interface 1
000074H	BGR11 [R/W] B, H, W 00000000	BGR10 [R/W] B, H, W 00000000	RDR1 [R]/ TDR1 [W] H, W -------0 00000000		
000078H	—		ISMK1 [R/W] B, H 01111111	ISBA1 [R/W] B, H 00000000	
00007CH	—				(Reserved)
000080H	SSR2 [R/W, R] B, H, W 00000011	ESCR2 [R/W]/ IBSR2 [R/W, R] B, H, W 00000000	SCR2 [R/W] / IBCR2 [R/W, R] B, H, W 00000000	SMR2 [R/W] B, H, W 000-0000	Multi-function serial interface 2
000084H	BGR21 [R/W] B, H, W 00000000	BGR20 [R/W] B, H, W 00000000	RDR2 [R]/ TDR2 [W] H, W -------0 00000000		
000088H	—		ISMK2 [R/W] B, H 01111111	ISBA2 [R/W] B, H 00000000	
00008CH	—				(Reserved)

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000520H to 00053CH	—				(Reserved)
000540H	RCR10 [W] B, H, W XXXXXXXX	RCR00 [W] B, H, W XXXXXXXX	UDCR10 [R] B, H, W 00000000	UDCR00 [R] B, H, W 00000000	Up/down counter 0
000544H	CCRH0 [R/W] B, H 00000000	CCRL0 [R/W, R] B, H -0001000	—	CSR0 [R/W, R] B 00000000	
000548H to 00057CH	—				(Reserved)
000580H	BT1TMR [R] B, H, W 00000000 00000000		BT1TMCR [R/W] B, H, W -0000000 00000000		Base timer 1
000584H	—	BT1STC [R/W] B 00000000	—		
000588H	BT1PCSR/BT1PRLL [R/W] H, W XXXXXXXX XXXXXXXX		BT1PDUT/BT1PRLH/BT1DTBF [R/W] H, W XXXXXXXX XXXXXXXX		
00058CH to 000600H	—				(Reserved)
000604H	—		PCR8 [R/W] B -0000000	—	Pull-up resistor control register
000608H	PCRA [R/W] B, H -----00-	PCRB [R/W] B, H 0000----	PCRC [R/W] B 00000000	—	
00060CH	—		PCRG [R/W] B, H --000000	PCRH [R/W] B, H -----000	
000610H	PCRJ [R/W] B ----0000	—	PCRL [R/W] B -----000	—	
000614H	PCRP [R/W] B, H --000000	PCRQ [R/W] B, H --000000	—		
000618H to 000FFCH	—				(Reserved)

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
007030H	WA00 [R/W] W -------- ----XXXX XXXXXXXX XXXXXX--				Wild register control block
007034H	WD00 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
007038H	WA01 [R/W] W -------- ----XXXX XXXXXXXX XXXXXX--				
00703CH	WD01 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
007040H	WA02 [R/W] W -------- ----XXXX XXXXXXXX XXXXXX--				
007044H	WD02 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
007048H	WA03 [R/W] W -------- ----XXXX XXXXXXXX XXXXXX--				
00704CH	WD03 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
007050H	WA04 [R/W] W -------- ----XXXX XXXXXXXX XXXXXX--				
007054H	WD04 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
007058H	WA05 [R/W] W -------- ----XXXX XXXXXXXX XXXXXX--				
00705CH	WD05 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
007060H	WA06 [R/W] W -------- ----XXXX XXXXXXXX XXXXXX--				
007064H	WD06 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
007068H	WA07 [R/W] W -------- ----XXXX XXXXXXXX XXXXXX--				
00706CH	WD07 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
007070H	WA08 [R/W] W -------- ----XXXX XXXXXXXX XXXXXX--				
007074H	WD08 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

(Continued)

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
007078H	WA09 [R/W] W -------- ----XXXX XXXXXXXX XXXXXX--				Wild register control block
00707CH	WD09 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
007080H	WA10 [R/W] W -------- ----XXXX XXXXXXXX XXXXXX--				
007084H	WD10 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
007088H	WA11 [R/W] W -------- ----XXXX XXXXXXXX XXXXXX--				
00708CH	WD11 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
007090H	WA12 [R/W] W -------- ----XXXX XXXXXXXX XXXXXX--				
007094H	WD12 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
007098H	WA13 [R/W] W -------- ----XXXX XXXXXXXX XXXXXX--				
00709CH	WD13 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0070A0H	WA14 [R/W] W -------- ----XXXX XXXXXXXX XXXXXX--				
0070A4H	WD14 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0070A8H	WA15 [R/W] W -------- ----XXXX XXXXXXXX XXXXXX--				
0070ACH	WD15 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0070B0H to 0FFFFCH	—				(Reserved)

* : The lower 16 bits (DTC15 to DTC0) of DMACA0 to DMACA4 cannot be accessed as bytes.

Notes :
- Data is undefined in reserved or (—) area.
- Do not execute read modify write (RMW) instruction on registers having a write-only bit.
- The initial values are varied depending on the product series. Please refer to the hardware manual of MB91490 series for more details.

(Continued)

Interrupt source	Interrupt number		Interrupt level	Offset	TBR default address
	Decimal	Hexa-decimal			
OCU2/OCU3 (match)	61	3D	ICR45	308_H	$000FFF08_H$
OCU4/OCU5 (match)	62	3E	ICR46	304_H	$000FFF04_H$
Interrupt delay source bit	63	3F	ICR47	300_H	$000FFF00_H$
System reserved (Used by REALOS)	64	40	—	$2FC_H$	$000FFEFC_H$
System reserved (Used by REALOS)	65	41	—	$2F8_H$	$000FFEF8_H$
System reserved	66	42	—	$2F4_H$	$000FFEF4_H$
System reserved	67	43	—	$2F0_H$	$000FFEF0_H$
System reserved	68	44	—	$2EC_H$	$000FFEEC_H$
System reserved	69	45	—	$2E8_H$	$000FFEE8_H$
System reserved	70	46	—	$2E4_H$	$000FFEE4_H$
System reserved	71	47	—	$2E0_H$	$000FFEE0_H$
System reserved	72	48	—	$2DC_H$	$000FFEDC_H$
System reserved	73	49	—	$2D8_H$	$000FFED8_H$
System reserved	74	4A	—	$2D4_H$	$000FFED4_H$
System reserved	75	4B	—	$2D0_H$	$000FFED0_H$
System reserved	76	4C	—	$2CC_H$	$000FFECC_H$
System reserved	77	4D	—	$2C8_H$	$000FFEC8_H$
System reserved	78	4E	—	$2C4_H$	$000FFEC4_H$
System reserved	79	4F	—	$2C0_H$	$000FFEC0_H$
Used by INT instruction	80 to 255	50 to FF	—	$2BC_H$ to 000_H	$000FFEBC_H$ to $000FFC00_H$

■ PIN STATUS IN EACH CPU STATE

Terms used as the status of pins mean as follows.

- Input enabled
  Means that the input function can be used.

- Input disabled
  Indicates that the input function cannot be used.

- Input fixed to “0”
  A state of a pin, in which "0" is transmitted to internal circuitry, with the external input shut off by the input gate adjacent to the pin.

- Output Hi-Z
  Means to place a pin in a high impedance state by disabling the pin driving transistor from driving.

- Preserving the previous state
  Means to output the state existing immediately prior to entering this mode.
  That is, to output according to an internal resource with an output when it is operating or to preserve an output when the output is provided, for example, as a port.

- Input enabled when external interrupt function selected and enabled
  Inputs are allowed only when the pin is configured as an external interrupt request input pin and the external interrupt request is enabled.

• List of pin status

Pin name	Function	During initialization		In sleep mode	In stop mode	
		INITX = "L"*1 or when Low voltage detection reset occurs	INITX = "H"*2 or when Low voltage detection reset is released		HIZ = 0	HIZ = 1
NMIX	NMIX	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
P80 to P83	INT0 to INT3	Output Hi-Z/ Input disabled	Output Hi-Z/ Input enabled	Input enabled	Input enabled	Output Hi-Z/ Input "0" fixed
P84	INT4/PPG4					
P85	INT5/PPG5					Input enabled when interrupt function selected and enabled
P86	INT6/PPG6					
PA1, PA2	ADTG1, ADTG2	Output Hi-Z/ Input disabled	Output Hi-Z/ Input enabled	Retention of the immediately prior state	Retention of the immediately prior state	Output Hi-Z/ Input "0" fixed
PB4 to PB7	AN1-0 to AN1-3	Output Hi-Z/ Input disabled	Output Hi-Z/ Input "0" fixed	Retention of the immediately prior state	Retention of the immediately prior state	Output Hi-Z/ Input "0" fixed
PC0 to PC7	AN2-0 to AN2-7					
PG0, PG3	SCK0, SCK1	Output Hi-Z/ Input disabled	Output Hi-Z/ Input enabled	Retention of the immediately prior state	Retention of the immediately prior state	Output Hi-Z/Input "0" fixed
PG1, PG4	SIN0, SIN1					
PG2, PG5	SOT0, SOT1					
PH0	SCK2					
PH1	SIN2					
PH2	SOT2					
PJ0, PJ2	TIN0, TIN1	Output Hi-Z/ Input disabled	Output Hi-Z/ Input enabled	Retention of the immediately prior state	Retention of the immediately prior state	Output Hi-Z/Input "0" fixed
PJ1, PJ3	TOUT0, TOUT1					
PL0	AIN0	Output Hi-Z/ Input disabled	Output Hi-Z/ Input enabled	Retention of the immediately prior state	Retention of the immediately prior state	Output Hi-Z/Input "0" fixed
PL1	BIN0					
PL2	ZIN0					
PP0 to PP3	IC0 to IC3	Output Hi-Z/ Input disabled	Output Hi-Z/ Input enabled	Retention of the immediately prior state	Retention of the immediately prior state	Output Hi-Z/Input "0" fixed
PP4	CKI0					
PP5	DTTI0					
PQ0 to PQ5	RTO0 to RTO5					

*1 : INITX = "L" : Indicates the pin status with INITX remaining at the "L" level.

*2 : INITX = "H" : Indicates the pin status existing immediately after INITX transition from "L" to "H" level.

4. Flash Memory Write/Erase Characteristics

Parameter	Condition	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time (8 Kbytes sectors)	V_{CC} = 5.0 V, T_A = + 25 °C	—	0.5	2.0	s	Not including time for internal writing before deletion.
Word write time	V_{CC} = 5.0 V, T_A = + 25 °C	—	6	100	µs	Not including system-level overhead time.
Chip erase time	V_{CC} = 5.0 V, T_A = + 25 °C	—	1.8	29.5	s	Not including system-level overhead time.
Erase/write cycle	—	10000	—	—	cycle	
Flash memory data hold time	—	10	—	—	year	

(2) PLL Oscillation stabilization time (LOCK UP TIME)

(V_{CC} = 2.7 V to 5.5 V, V_{SS} = AVSS10 = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Symbol	Pin Name	Condition	Value		Unit
				Min	Max	
PLL Oscillation stabilization wait time (LOCK UP TIME)	t_{LOCK}*	—	—	600	—	µs

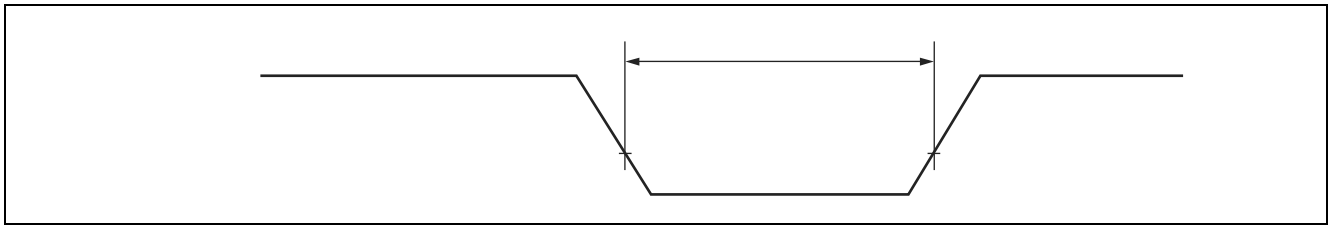
* : The length of time to wait for the PLL oscillations to stabilize.

(3) Reset Input Ratings

(V_{CC} = 2.7 V to 5.5 V, V_{SS} = AVSS10 = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Symbol	Pin Name	Condition	Value		Unit
				Min	Max	
INITX input time (at power-on)	t_{INTL}	INITX	—	$t_{PON} + t_{STBL}$ + Oscillation time of oscillator + $tc \times 2^{13}$	—	ns
INITX input time (at STOP)				Oscillation time of oscillator + $tc \times 10$	—	ns
INITX input time (other than the above)				$tc \times 10$	—	ns

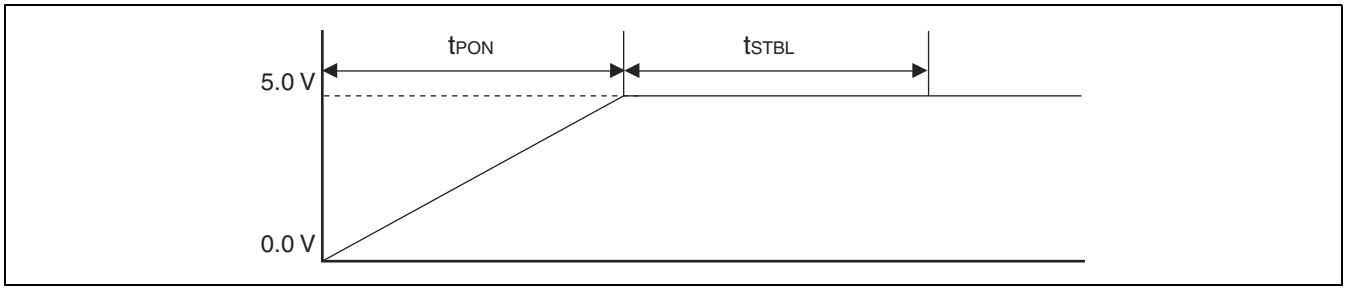
Notes : • For t_C (clock cycle time) , refer to “(1) Clock Timing”.
• For t_{PON} and t_{STBL}, refer to “ (4) Power on Rise Time /Power-on Stabilization Time Ratings”.



(4) Power on Rise Time /Power-on Stabilization Time Ratings

(V_{SS} = AVSS10 = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Symbol	Pin Name	Condition	Value		Unit
				Min	Max	
Power on rise time	t_{PON}	VCC	—	600	—	µs
power-on stabilization time	t_{STBL}			600	—	µs



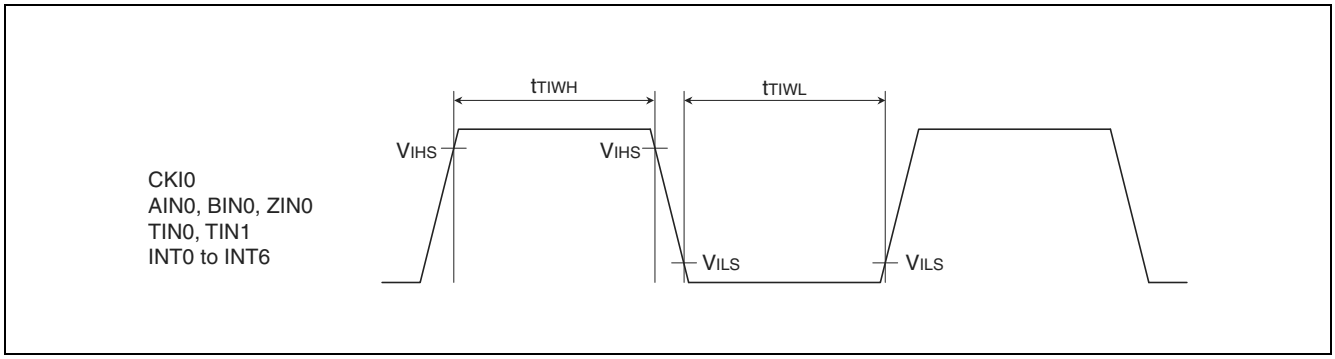
(6) Free-run Timer Clock, Up/Down Counter, Base Timer, and External Interrupt Input Timing

(V_{CC} = 2.7 V to 5.5 V, V_{SS} = AVSS10 = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Symbol	Pin Name	Condition	Value		Unit
				Min	Max	
Free-run timer input clock pulse width	t_{TIWH} t_{TIWL}	CKI0	—	4 × t_{CYCP}	—	ns
Up-down counter input pulse width		AIN0 BIN0 ZIN0		4 × t_{CYCP}	—	ns
Base timer input pulse width		TIN0, TIN1		4 × t_{CYCP}	—	ns
External interrupt input pulse width		INT0 to INT6		4 × t_{CYCP}	—	ns
				1.0*	—	µs

* : In stop mode

Note : t_{CYCP} indicates the peripheral clock cycle time.



b. Slave Mode

(V_{CC} = 2.7 V to 5.5 V, V_{SS} = AVSS10 = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Condition	Standard Mode		Fast Mode*3		Unit	Remarks
				Min	Max	Min	Max		
SCL clock frequency	f_{SCL}	SDAn, SCLn	R=1 kΩ, C=50 pF*4	0	100	0	400	kHz	
"L" width of the SCL clock	t_{LOW}			4.7	—	1.3	—	µs	
"H" width of the SCL clock	t_{HIGH}			4.0	—	0.6	—	µs	
Bus free time between STOP and START conditions	t_{BUS}			4.7	—	1.3	—	µs	
SCL ↓ → SDA output delay time	t_{DLDAT}			—	$5 \times t_{CYCP}$ *1	—	$5 \times t_{CYCP}$ *1	ns	
Setup time for a repeated START condition SCL ↑ → SDA ↓	t_{SUSTA}			4.7	—	0.6	—	µs	
Hold time for a repeated START condition SDA ↓ → SCL ↓	t_{HDSTA}			4.0	—	0.6	—	µs	The first clock pulse is generated after this.
Setup time for STOP condition SCL ↑ → SDA ↑	t_{SUSTO}			4.0	—	0.6	—	µs	
SDA Data input hold time (vs. SCL ↓)	t_{HDDAT}			$2 \times t_{CYCP}$ *1	—	$2 \times t_{CYCP}$ *1	—	µs	
SDA Data input setup time (vs. SCL ↑)	t_{SUDAT}			250	—	100 *2	—	ns	

*1 : t_{CYCP} indicates the peripheral clock cycle time.

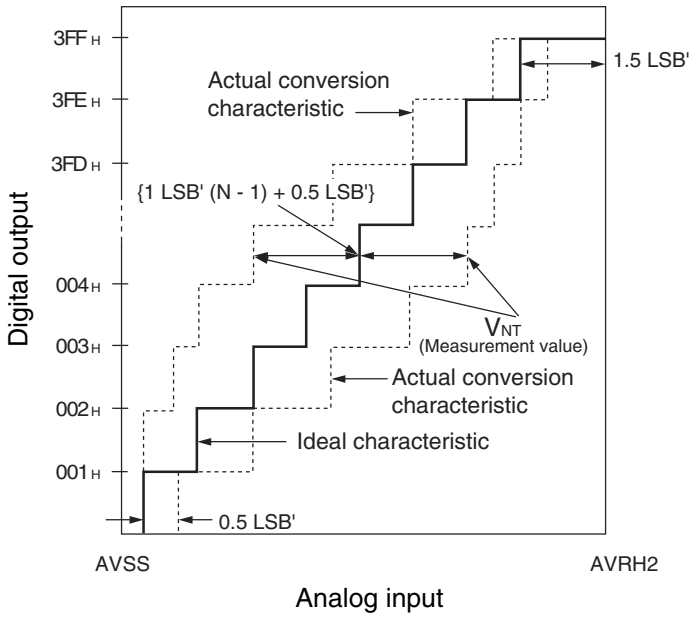
*2 : A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement $t_{SUDAT} \geq 250$ ns must then be met.
If a device does not extend the "L" period of the SCL signal, it is necessary to output the next piece of data to the SDA line 1250 ns (SDA and SCL rising Max time + t_{SUDAT}) before the SCL line is released.

*3 : For use at over 100 kHz, set the peripheral clock to at least 6 MHz.

*4 : R and C are pull-up resistance and load capacitance of the SCL and SDA lines.

(Continued)

Total error



$$1\ \text{LSB'}\ (\text{ideal value}) = \frac{\text{AVRH2} - \text{AVSS}}{1024}\ [\text{V}]$$

$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB'} \times (\text{N} - 1) + 0.5\ \text{LSB'}\}}{1\ \text{LSB'}}$$

N : A/D converter digital output value

V_{NT} : Voltage at which digital output changes from (N + 1) H to NH.

V_{OT}' (ideal value) = AVSS + 0.5 LSB' [V]

V_{FST}' (ideal value) = AVRH2 – 1.5 LSB' [V]

MEMO