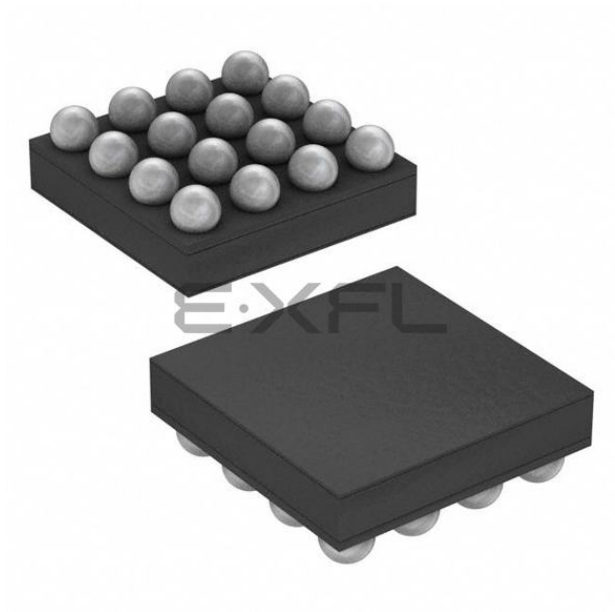
Analog Devices Inc./Maxim Integrated - MAXQ617V-L000+UW Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	MAXQ20S
Core Size	16-Bit
Speed	12MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	10
Program Memory Size	80KB (40K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.67V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-20°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	16-WFBGA, WLBGA
Supplier Device Package	16-WLP
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/maxq617v-l000-uw

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ELECTRICAL CHARACTERISTICS (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested.)

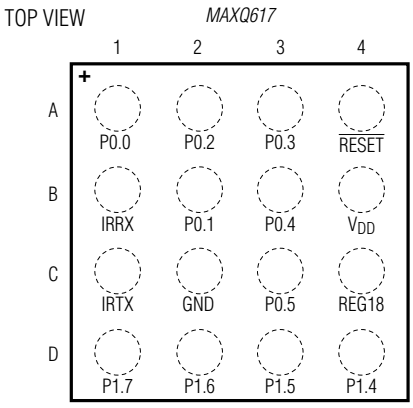
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Stop Mode Resume Time	t_{ON}			375 + ($8192t_{CK}$)		µs
Input Low Voltage for IRRX and All Port Pins	V_{IL}		V_{GND}		0.3 V_{DD}	V
Input High Voltage for IRRX and All Port Pins	V_{IH}		0.7 V_{DD}		V_{DD}	V
Input Hysteresis (Schmitt)	V_{IHYS}	V_{DD} = 3.3V, T_A = +25°C		300		mV
IRRX Input Filter Pulse-Width Reject	t_{IRRX_R}				50	ns
IRRX Input Filter Pulse-Width Accept	t_{IRRX_A}		300			ns
IRTX Sink Current	I_{IRTX}	$V_{IRTX} \geq$ 0.25V	200			mA
Output Low Voltage for All Port Pins	V_{OL}	V_{DD} = 3.6V, I_{OL} = 11mA		0.4	0.5	V
		V_{DD} = 2.35V, I_{OL} = 8mA		0.4	0.5	
		V_{DD} = 1.8V, I_{OL} = 4.5mA		0.4	0.5	
Output High Voltage All Port Pins	V_{OH}	I_{OH} = -2mA	V_{DD} - 0.5		V_{DD}	V
Input/Output Pin Capacitance for All Port Pins	C_{IO}			15		pF
Input Leakage Current for All Pins	I_L	Internal pullup disabled	-100		+100	nA
Input Pullup Resistor for $\overline{RESET}$, IRRX, and All Port Pins	R_{PU}	V_{DD} = 3.0V, V_{OL} = 0.4V	16	28	39	kΩ
		V_{DD} = 1.8V, V_{OL} = 0.4V	18	31	43	kΩ
LEARNING AMPLIFIER						
IRRX Amplifier Input Low Detection	I_{DL}	V_{DD} = 1.8V, I_{RRCVEN} = 1			0.2	µA
IRRX Amplifier Input High Detection	I_{DH}	V_{DD} = 1.8V, I_{RRCVEN} = 1	1.25			µA
CLOCK						
Internal Oscillator Frequency	f_{OSC}			12		MHz
Internal Oscillator Variability	f_{OSC_VAR}	T_A = -20°C to +70°C			±1%	MHz
		T_A = +25°C, V_{DD} = 1.8V			±0.5%	
		T_A = +15°C to +40°C, V_{DD} = 1.8V ±5%		±0.5%		

ELECTRICAL CHARACTERISTICS (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
System Clock Period	t_{CK}			$1/f_{OSC}$		ns
System Clock Frequency	f_{CK}			$1/t_{CK}$		MHz
NANOPOWER RING						
Nanopower Ring Frequency	f_{NANO}	T_A = +25°C	3.0	8.0	20.0	kHz
		T_A = +25°C, V_{DD} = POR voltage	1.7	2.4		
WAKE-UP TIMER						
Wakeup Timer Interval	t_{WAKEUP}		$1/f_{NANO}$		$65,535/f_{NANO}$	s
FLASH MEMORY						
System Clock During Flash Programming/Erase	$f_{FPSYSCLK}$	$f_{FPSYSCLK}$/(FCKDIV[3:0]+1) must equal 1MHz, verify PFI = 0 before calling utility ROM.		f_{OSC}		MHz
Flash Erase Time	t_{ME}	Mass erase		40		ms
	t_{ERASE}	Page erase		40		ms
Flash Programming Time per Word	t_{PROG}	Excluding utility ROM overhead		40		µs
Write/Erase Cycles			20,000			Cycles
Data Retention		T_A = +25°C	100			Years

Ball Configuration



WLP

Ball Description

BALL	NAME	FUNCTION
		POWER BALLS
B4	V_{DD}	Supply Voltage
C2	GND	Ground. Connect directly to the ground plane.
C4	REG18	1.8V Regulator Output. This pin must be connected to ground through a 1.0µF external ceramic-chip capacitor. The capacitor must be placed as close to this pin as possible. No devices other than the capacitor should be connected to this pin.
		RESET BALLS
A4	$\overline{\text{RESET}}$	Digital, Active-Low Reset Input/Output. The device remains in reset as long as this pin is low and begins executing from the utility ROM at address 8000h when this pin returns to a high state. The pin includes pullup current source; if this pin is driven by an external device, it should be driven by an open-drain source capable of sinking in excess of 4mA. This pin can be left unconnected if there is no need to place the device in a reset state using an external signal. This pin is driven low as an output when an internal reset condition occurs.
		IR FUNCTION BALLS
C1	IRTX	IR Transmit Output. This pin defaults to a high-impedance input with the weak pullup disabled during all forms of reset. Software must configure this pin after release from reset to remove the high-impedance input condition.
B1	IRRX	IR Receive Input. This pin defaults to a high-impedance input with the weak pullup disabled during all forms of reset. Software must configure this pin after release from reset to remove the high-impedance input condition and to enable the IR amplifier if desired.

Ball Description (continued)

BALL	NAME	FUNCTION	
GENERAL-PURPOSE I/O AND SPECIAL FUNCTION BALLS			
		Port 0 General-Purpose, Digital I/O Pins. These port pins function as general-purpose I/O pins with their input and output states controlled by the PD0, PO0, and PI0 registers. All port pins default to high-impedance mode after a reset. Software must configure these pins after release from reset to remove the high-impedance condition. All special functions must be enabled from software before they can be used.	
		GPIO PORT PIN	**SPECIAL FUNCTION**
A1	P0.0 RX0 MOSI INT0	P0.0	RX0: USART receive MOSI: SPI master out slave in INT0: External interrupt 0
B2	P0.1 TX0 MISO INT1	P0.1	TX0: USART transmit MISO: SPI master in slave out INT1: External interrupt 1
A2	P0.2 SCL0 SCLK INT2	P0.2	SCL0: I^2C clock SCLK: SPI clock INT2: External interrupt 2
A3	P0.3 SDA0 SSEL INT3	P0.3	SDA0: I^2C data SSEL: SPI slave select INT3: External interrupt 3
B3	P0.4 TBA0 INT4	P0.4	TBA0: Timer B A0 INT4: External interrupt 4
C3	P0.5 TBB0 INT5	P0.5	TBB0: Timer B B0 INT5: External interrupt 5
		Port 1 General-Purpose, Digital I/O Pins. These port pins function as general-purpose I/O pins with their input and output states controlled by the PD1, PO1, and PI1 registers. The JTAG pins default to their JTAG function with weak pullups enabled after a reset. The JTAG function can be disabled using the TAP bit in the SC register.	
		GPIO PORT PIN	**SPECIAL FUNCTION**
D4	P1.4/TCK/SCL1	P1.4	SCL1: I^2C clock, TCK: JTAG test clock
D3	P1.5/TDI/SDA1	P1.5	SDA1: I^2C data, TDI: JTAG data input
D2	P1.6/TMS	P1.6	TMS: JTAG test mode select
D1	P1.7/TDO	P1.7	TDO: JTAG Data Output. TDO functions as the test-data output on reset and defaults to an input with a weak pullup. The output function of the test data is only enabled during the TAP's Shift_IR or Shift_DR states.

Detailed Description

The MAXQ617 provides integrated, low-cost solutions that simplify the design of IR communications equipment such as universal remote controls. Standard features include the highly optimized, single-cycle, MAXQ, 16-bit RISC core; 80KB flash memory; 4KB data RAM; soft stack; 16 general-purpose registers; and three data pointers. The MAXQ core has the industry's best MIPS/mA rating, allowing developers to achieve the same performance as competing microcontrollers at substantially lower clock rates. Lower active-mode current combined with the even lower stop-mode current (0.2µA typ) results in increased battery life. Application-specific peripherals include flexible timers for generating IR carrier frequencies and modulation. A high-current IR drive pin operates with an internal receiver amplifier without external components. It also includes general-purpose I/O pins ideal for keypad matrix input, and a power-fail-detection circuit to notify the application when the supply voltage is nearing the microcontroller's minimum operating voltage.

The internal 12MHz oscillator requires no external components and executes instructions. Operating from DC to 12MHz, almost all instructions execute in a single clock cycle (83.3ns at 12MHz), enabling nearly 12MIPS true-code operation. When active device operation is not required, an ultra-low-power stop mode can be invoked from software, resulting in quiescent current consumption of less than 0.2µA (typ) and 2.0µA (max). The combination of high-performance instructions and ultra-low stop-mode current increases battery life over competing microcontrollers. An integrated POR circuit with brownout support resets the device to a known condition following a power-up cycle or brownout condition. Additionally, a power-fail warning flag is set, and a power-fail interrupt can be generated when the system voltage falls below the power-fail warning voltage, V_{PFW}. The configurable power-fail warning feature allows the application to notify the user that the system supply is low and appropriate action should be taken.

Microprocessor

The device is based on Maxim Integrated's low-power, 16-bit MAXQ20S. The core supports the Harvard memory architecture with separate 16-bit program and data address buses. A fixed 16-bit instruction word is standard, but data can be arranged in 8 or 16 bits. The MAXQ core in the device is implemented as a pipelined processor with performance approaching 1MIPS per MHz. The 16-bit data path is implemented around register modules, and each register module contributes specific functions to the core. The accumulator module consists of sixteen 16-bit registers and is tightly coupled with the arithmetic logic unit (ALU). A configurable soft stack supports program flow.

Execution of instructions is triggered by data transfer between functional register modules or between a functional register module and memory. Because data movement involves only source and destination modules, circuit switching activities are limited to active modules only. For power-conscious applications, this approach localizes power dissipation and minimizes switching noise. The modular architecture also provides a maximum of flexibility and reusability that are important for a microprocessor used in embedded applications.

The MAXQ instruction set is highly orthogonal. All arithmetical and logical operations can use any register in conjunction with the accumulator. Data movement is supported from any register to any other register. Memory is accessed through specific data-pointer registers with autoincrement/decrement support.

Memory

The microcontroller incorporates several memory types:

- 80KB flash memory
- 4KB SRAM data memory
- Dedicated utility ROM
- Soft stack

Stack Memory

The device provides a soft stack that can be used to store program return addresses (for subroutine calls and interrupt handling) and other general-purpose data. This soft stack is located in the SRAM data memory, which means that the SRAM data memory must be shared between the soft stack and general-purpose application data storage. However, the location and size of the soft stack is determined by the user, providing maximum flexibility when allocating resources for a particular application. The stack is used automatically by the processor when the CALL, RET, and RETI instructions are executed and when an interrupt is serviced. An application can also store and retrieve values explicitly using the stack by means of the PUSH, POP, and POPI instructions.

The SP pointer indicates the current top of the stack, which initializes by default to the top of the SRAM data memory. As values are pushed onto the stack, the SP pointer decrements, which means that the stack grows downward towards the bottom (lowest address) of the data memory. Popping values off the stack causes the SP pointer value to increase. Refer to the *User's Guide* for more details.

Utility ROM

The utility ROM is located in program space beginning at address 8000h. This ROM includes the following routines:

- Production test routines (internal memory tests, memory loader, etc.), which are used for internal testing only, and are generally of no use to the end-application developer
- User-callable routines for buffer copying and fast table lookup (more information on these routines can be found in the *User's Guide)*

Following any reset, execution begins in the utility ROM at address 8000h. At this point, unless test mode has been invoked (which requires special programming through the JTAG interface), the utility ROM in the device always automatically jumps to location 0000h, which is the beginning of user application code.

Watchdog Timer

The internal watchdog timer greatly increases system reliability. The timer resets the device if software execution is disturbed. The watchdog timer is a free-running counter designed to be periodically reset by the application software. If software is operating correctly, the counter is periodically reset and never reaches its maximum count. However, if software operation is interrupted, the timer does not reset, triggering a system reset and optionally a watchdog timer interrupt. This protects the system against electrical noise or electrostatic discharge (ESD) upsets that could cause uncontrolled processor operation. The internal watchdog timer is an upgrade to older designs with external watchdog devices, reducing system cost and simultaneously increasing reliability.

The watchdog timer functions as the source of both the watchdog timer timeout and the watchdog timer reset. The timeout period can be programmed in a range of 2^{15} to 2^{24} system clock cycles. An interrupt is generated when the timeout period expires if the interrupt is enabled. All watchdog timer resets follow the programmed interrupt timeouts by 512 system clock cycles. If the watchdog timer is not restarted for another full interval in this time period, a system reset occurs when the reset timeout expires. See Table 1.

IR Carrier Generation and Modulation Timer

The dedicated IR timer/counter module simplifies low-speed infrared (IR) communication. The IR timer implements two pins (IRTX and IRRX) for supporting IR transmit and receive, respectively. The IRTX pin has no corresponding port pin designation, so the standard PD, PO, and PI port control status bits are not present. However, the IRTX pin output can be manipulated high or low using the PWCN.IRTXOUT and PWCN.IRTXOE bits when the IR timer is not enabled (i.e., IREN = 0).

Table 1. Watchdog Interrupt Timeout (Sysclk = 12MHz, CD[1:0] = 00)

WD[1:0]	WATCHDOG CLOCK	WATCHDOG INTERRUPT TIMEOUT	WATCHDOG RESET AFTER WATCHDOG INTERRUPT (µs)
00	Sysclk/2^{15}	2.7ms	42.7
01	Sysclk/2^{18}	21.9ms	42.7
10	Sysclk/2^{21}	174.7ms	42.7
11	Sysclk/2^{24}	1.4s	42.7

The IR timer is composed of a carrier generator and a carrier modulator. The carrier generation module uses the 16-bit IR carrier register (IRCA) to define the high and low time of the carrier through the IR carrier high byte (IRCAH) and IR carrier low byte (IRCAL). The carrier modulator uses the IR data bit (IRDATA) and IR modulator time register (IRMT) to determine whether the carrier or the idle condition is present on IRTX.

The IR timer is enabled when the IR enable bit (IREN) is set to 1. The IR Value register (IRV) defines the beginning value for the carrier modulator. During transmission, the IRV register is initially loaded with the IRMT value and begins down counting towards 0000h, whereas in receive mode it counts upward from the initial IRV register value. During the receive operation, the IRV register can be configured to reload with 0000h when capture occurs on detection of selected edges or can be allowed to continue free-running throughout the receive operation. An overflow occurs when the IR timer value rolls over from 0FFFFh to 0000h. The IR overflow flag (IROV) is set to 1 and an interrupt is generated if enabled (IRIE = 1).

Carrier Generation Module

The IRCAH byte defines the carrier high time in terms of the number of IR input clocks, whereas the IRCAL byte defines the carrier low time.

- IR Input Clock (f_{IRCLK}) = $f_{SYS}/2^{IRDIV[2:0]}$
- Carrier Frequency ($f_{CARRIER}$) = f_{IRCLK}/(IRCAH + IRCAL + 2)
- Carrier High Time = IRCAH + 1
- Carrier Low Time = IRCAL + 1
- Carrier Duty Cycle = (IRCAH + 1)/(IRCAH + IRCAL + 2)

During transmission, the IRCA register is latched for each IRV down-count interval, and is sampled along with the IRTXPOL and IRDATA bits at the beginning of each new IRV down-count interval so that duty-cycle variation and frequency shifting is possible from one interval to the next, which is illustrated in Figure 1.

Figure 2 illustrates the basic carrier generation and its path to the IRTX output pin. The IR transmit polarity bit (IRTXPOL) defines the starting/idle state and the carrier polarity of the IRTX pin when the IR timer is enabled.

IR Transmission

During IR transmission (IRMODE = 1), the carrier generator creates the appropriate carrier waveform, while the carrier modulator performs the modulation. The carrier modulation can be performed as a function of carrier cycles or IRCLK cycles dependent on the setting of the IRCFME bit. When IRCFME = 0, the IRV down counter is clocked by the carrier frequency and thus the modulation is a function of carrier cycles (Figure 3). When IRCFME = 1, the IRV down counter is clocked by IRCLK, allowing carrier modulation timing with IRCLK resolution.

The IRTXPOL bit defines the starting/idle state as well as the carrier polarity for the IRTX pin. If IRTXPOL = 1, the IRTX pin is set to a logic-high when the IR timer module is enabled. If IRTXPOL = 0, the IRTX pin is set to a logic-low when the IR timer is enabled.

A separate register bit, IR data (IRDATA), is used to determine whether the carrier generator output is output to the IRTX pin for the next IRMT carrier cycles. When IRDATA = 1, the carrier waveform (or inversion of this waveform if IRTXPOL = 1) is output on the IRTX pin during the next IRMT cycles. When IRDATA = 0, the idle condition, as defined by IRTXPOL, is output on the IRTX pin during the next IRMT cycles.

The IR timer acts as a down counter in transmit mode. An IR transmission starts when the IREN bit is set to 1 when IRMODE = 1; when the IRMODE bit is set to 1 when IREN = 1; or when IREN and IRMODE are both set to 1 in the same instruction. The IRMT and IRCA registers, along with the IRDATA and IRTXPOL bits, are sampled at the beginning of the transmit process and every time the IR timer value reload its value. When the IRV reaches 0000h value, on the next carrier clock, it does the following:

1) Reloads IRV with IRMT.
2) Samples IRCA, IRDATA, and IRTXPOL.
3) Generates IRTX accordingly.
4) Sets IRIF to 1.
5) Generates an interrupt to the CPU if enabled (IRIE = 1).

To terminate the current transmission, the user can switch to receive mode (IRMODE = 0) or clear IREN to 0.

Carrier Modulation Time = IRMT + 1 carrier cycles

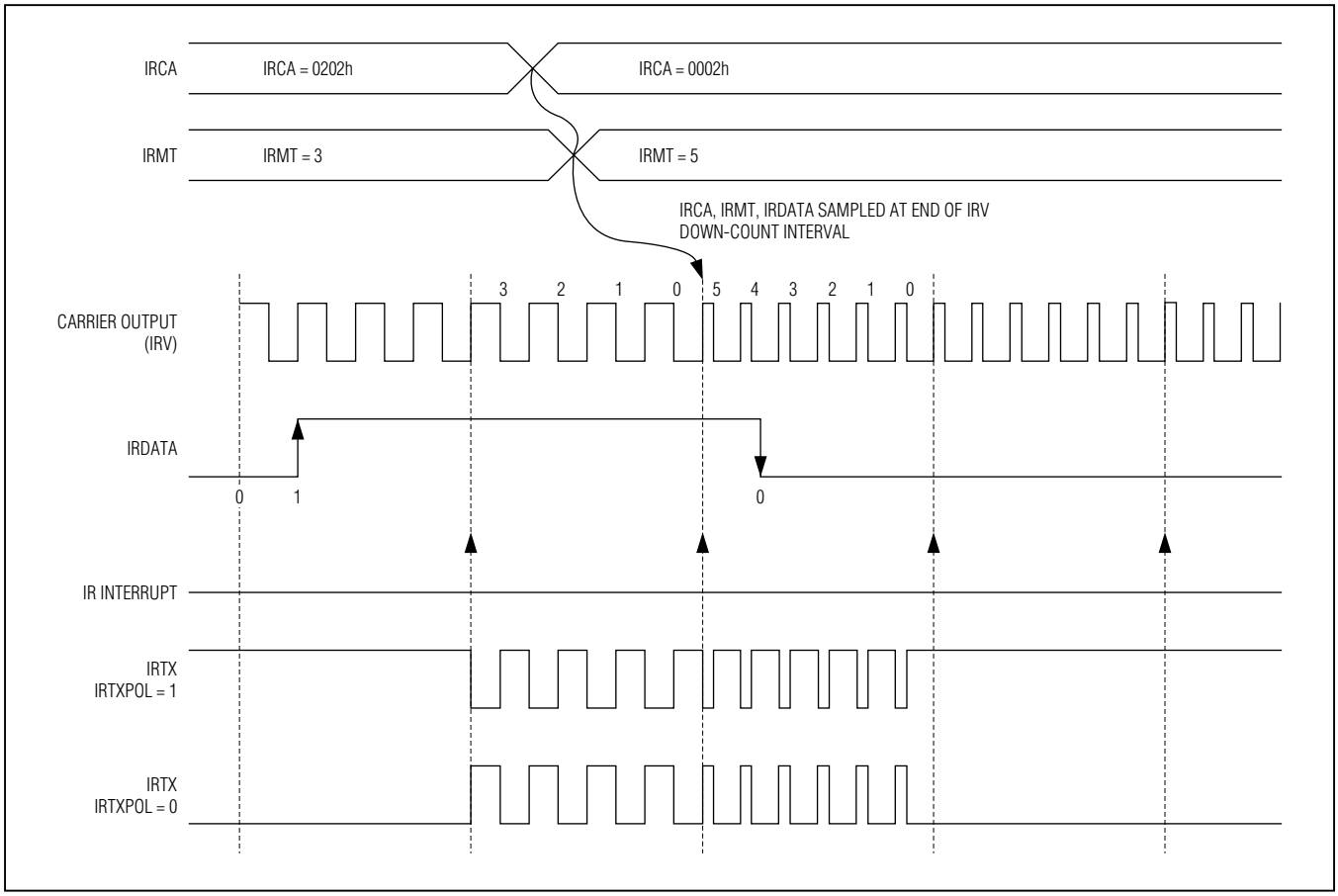


Figure 1. IR Transmit Frequency Shifting Example (IRCFME = 0)

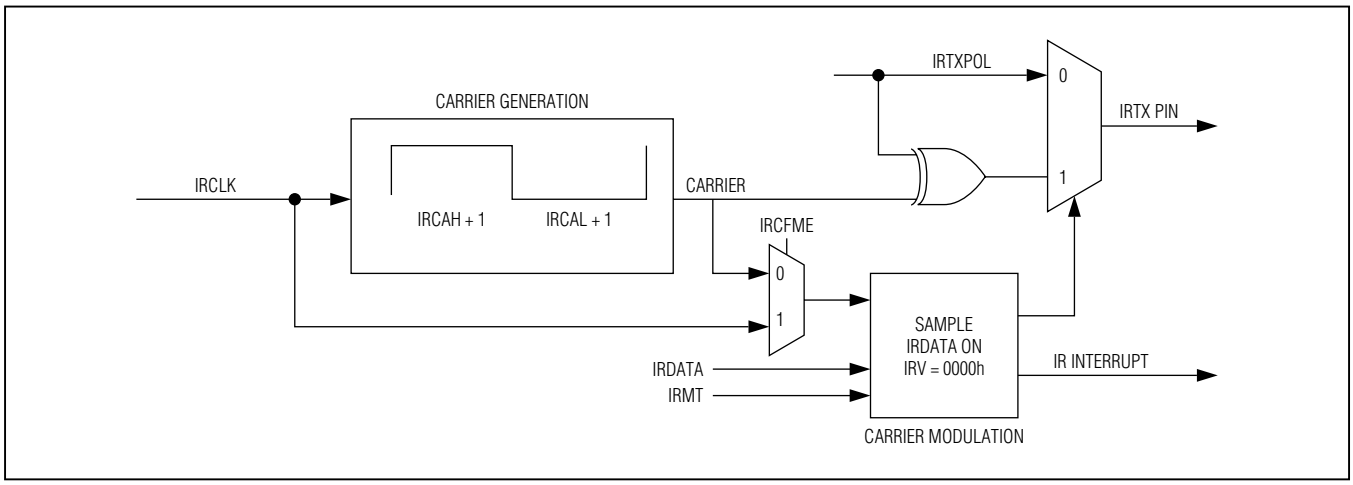


Figure 2. IR Transmit Carrier Generation and Carrier Modulator Control

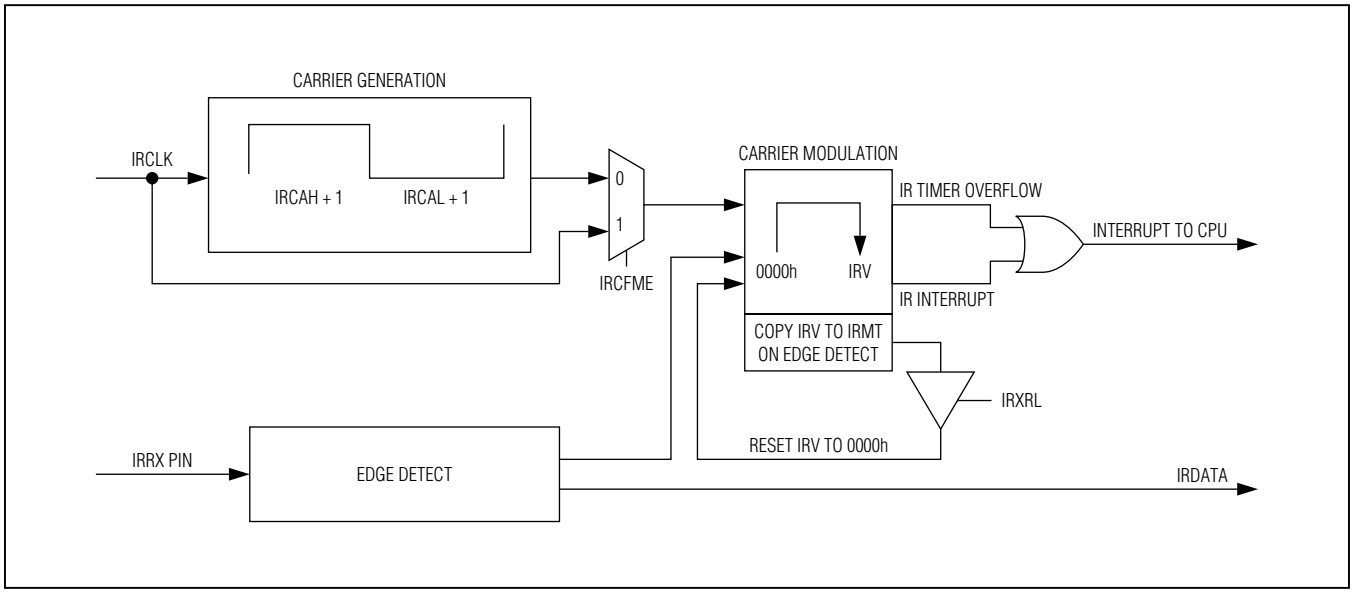


Figure 4. IR Capture

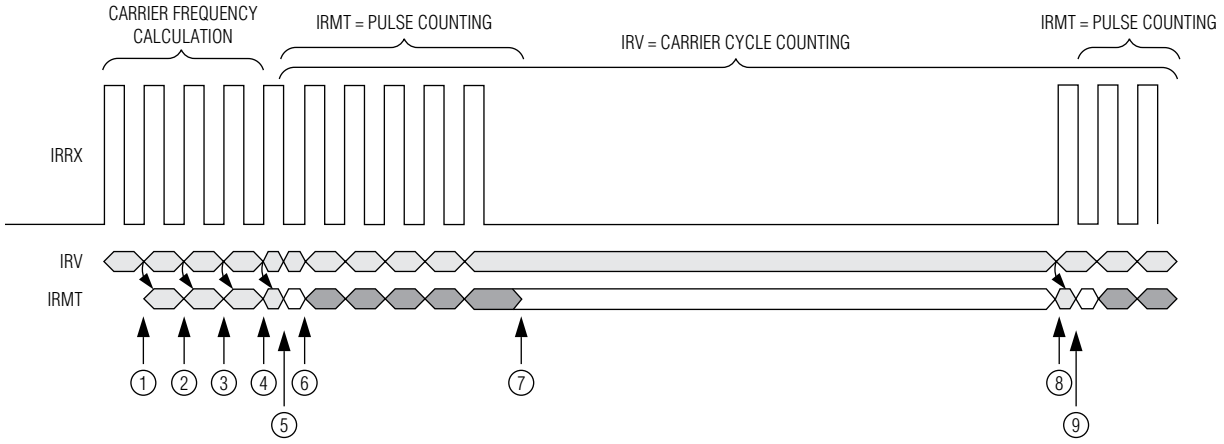
Carrier Burst-Count Mode

A special mode reduces the CPU processing burden when performing IR learning functions. Typically, when operating in an IR learning capacity, some number of carrier cycles are examined for frequency determination. Once the frequency has been determined, the IR receive function can be reduced to counting the number of carrier pulses in the burst and the duration of the combined mark-space time within the burst. To simplify this process, the receive burst-count mode (as enabled by the RXBCNT bit) can be used. When RXBCNT = 0, the standard IR receive capture functionality is in place. When RXBCNT = 1, the IRV capture operation is disabled and the interrupt flag associated with the capture no longer denotes a capture. In the carrier burst-count mode, the IRMT register only counts qualified edges. The IRIF interrupt flag (normally used to signal a capture when RXBCNT = 0) now becomes set if two IRCA cycles elapse without getting a qualified edge. The IRIF interrupt flag thus denotes absence of the carrier and the beginning of a space in the receive signal. When the RXBCNT bit is changed from 0 to 1, the IRMT register is set to 0001h. The IRCFME bit is still used to define whether the IRV register is counting system IRCLK clocks or IRCA-defined carrier cycles. The IRXRL bit defines whether the IRV register is reloaded with 0000h on detection of a qualified edge (per the IRRXSEL[1:0] bits). Figure 5 and the descriptive sequence embedded in the figure illustrate the expected usage of the receive burst-count mode.

16-Bit Timers/Counters

The microcontroller provides two timers/counters that support the following functions:

- 16-bit timer/counter
- 16-bit up/down autoreload
- Counter function of external pulse
- 16-bit timer with capture
- 16-bit timer with compare
- Input/output enhancements for pulse-width modulation
- Set/reset/toggle output state on comparator match
- Prescaler with 2^n divider (for n = 0, 2, 4, 6, 8, 10)



① TO ④ CAPTURE INTERRUPT (IRIF = 1).
IRV ≥ IRMT.
IRV = 0 (IF IRXRL = 1).

⑤ SOFTWARE SETS IRCA = CARRIER FREQUENCY.
SOFTWARE SETS RXBCNT = 1 (WHICH CLEARS IRMT = 0001 IN HARDWARE).
SOFTWARE CLEARS IRCFME = 0 SO THAT IRV COUNTS CARRIER CYCLES. IRV IS RESET TO 0 ON QUALIFIED EDGE DETECTION IF IRXRL = 1.
SOFTWARE ADDS TO IRMT THE NUMBER OF PULSES USED FOR CARRIER MEASUREMENT.
IRCA x 2x COUNTER FOR SPACE CAN BEGIN IMMEDIATELY (QUALIFIED EDGE RESETS).

⑥ QUALIFIED EDGE DETECTED: IRMT++
IRV RESET TO 0 IF IRXRL = 1.

⑦ IRCA x 2 PERIOD ELAPSES: IRIF = 1; CARRIER ABSENCE = SPACE.
BURST MARK = IRMT PULSES.
SOFTWARE CLEARS RXBCNT = 0 SO THAT WE CAPTURE ON THE NEXT QUALIFIED EDGE.

⑧ QUALIFIED EDGE DETECTED: IRIF = 1, CAPTURE IRV IRMT AS THE BURST SPACE (PLUS UP TO ONE CARRIER CYCLE).

⑨ SOFTWARE SET RXBCNT = 1 AS IN (5).
CONTINUE (5) TO (8) UNTIL LEARNING SPACE EXCEEDS SOME DURATION. IRV ROLLOVERS CAN BE USED.

Figure 5. Receive Burst-Count Example

Serial Peripherals

Serial Peripheral Interface (SPI)

The device provides two SPI ports. The SPI is an inter-device bus protocol that provides fast, synchronous, full-duplex communications between devices. The integrated SPI interface acts as either an SPI master or slave device. The master drives the synchronous clock and selects which of several slaves is being addressed. Every SPI peripheral consists of a single shift register and control circuitry so that an addressed serial peripheral interface SPI peripheral is simultaneously transmitting and receiving. The maximum SPI master transfer rate is Sysclk/2. When operating as an SPI slave, the device can support up to Sysclk/4 SPI transfer rate. Data can be transferred as an 8-bit or 16-bit value, MSB first. In addition, the SPI module supports configuration of the active SSEL state through the slave active-select pin.

Four signals are used in SPI communication:

- **SCLK:** The synchronous clock used by all devices. The master drives this clock and the slaves receive the clock. Note that SCLK can be gated and need not be driven between SPI transactions.
- **MOSI:** Master out-slave in. This is the main data line driven by the master to all slaves on the SPI bus. Only the selected slave clocks data from MOSI.

- **MISO:** Master in-slave out. This is the main data line driven by the selected slave to the master. Only the selected slave may drive this circuit. In fact, it is the only circuit in the SPI bus arrangement that a slave is ever permitted to drive.
- **SSEL:** This signal is unique to each slave. When active (generally low), the selected slave must drive MISO.

I²C Bus

The microcontroller provides two internal I²C bus master/slave peripherals for communication with a wide variety of other I²C-enabled devices. The I²C bus is a 2-wire, bidirectional bus using two bus lines—the serial data line (SDA) and the serial clock line (SCL)—and a ground line. Both the SDA and SDL lines must be driven as open-collector/drain outputs. External resistors are required to pull the lines to a logic-high state.

The device supports both the master and slave protocols. In the master mode, the device has ownership of the I²C bus, drives the clock, and generates the START and STOP signals. This allows it to send data to a slave or receive data from a slave as required. In slave mode, the device relies on an externally generated clock to drive SCL and responds to data and commands only when requested by the I²C master device.

USART

The device provides two USART peripherals with operation modes described in Table 2. The USART provides the following features:

- 2-wire interface
- Full-duplex operation for asynchronous data transfers
- Half-duplex operation for synchronous data transfers
- Programmable interrupt when transmit or receive data operation completes
- Independent programmable baud-rate generator
- Optional 9th bit parity support
- Start/stop bit support

General-Purpose I/O

The microcontroller provides port pins for general-purpose I/O that have the following features:

- CMOS output drivers
- Schmitt trigger inputs
- Optional weak pullup to V_{DD} when operating in input mode

While the microcontroller is in a reset state, all port pins become high impedance with both weak pullups and input buffers disabled, unless otherwise noted.

From a software perspective, each port appears as a group of peripheral registers with unique addresses. Special function pins can also be used as general-purpose I/O pins when the special functions are disabled. For a detailed description of the special functions available for each pin, refer to the *User's Guide*.

On-Chip Oscillator

The device provides an internal 12MHz oscillator that requires no external components, thereby reducing system cost, PCB area, and radiated EMI.

Operating Modes

The lowest power mode of operation is stop mode. In this mode, CPU state and memories are preserved, but the CPU is not actively running. Wake-up sources include external I/O interrupts, the power-fail warning interrupt, wake-up timer, or a power-fail reset. Any time the microcontroller is in a state where code does not need to be executed, the user software can put the device into stop mode. The nanopower ring oscillator is an internal ultra-low-power (400nA) 8kHz ring oscillator that can be used to drive a wake-up timer that exits stop mode. The wake-up timer is programmable by software in steps of 125µs up to approximately 8s.

Table 2. USART Mode Details

MODE	TYPE	START BITS	DATA BITS	STOP BITS
Mode 0	Synchronous	N/A	8	N/A
Mode 1	Asynchronous	1	8	1
Mode 2	Asynchronous	1	8 + 1	1
Mode 3	Asynchronous	1	8 + 1	1

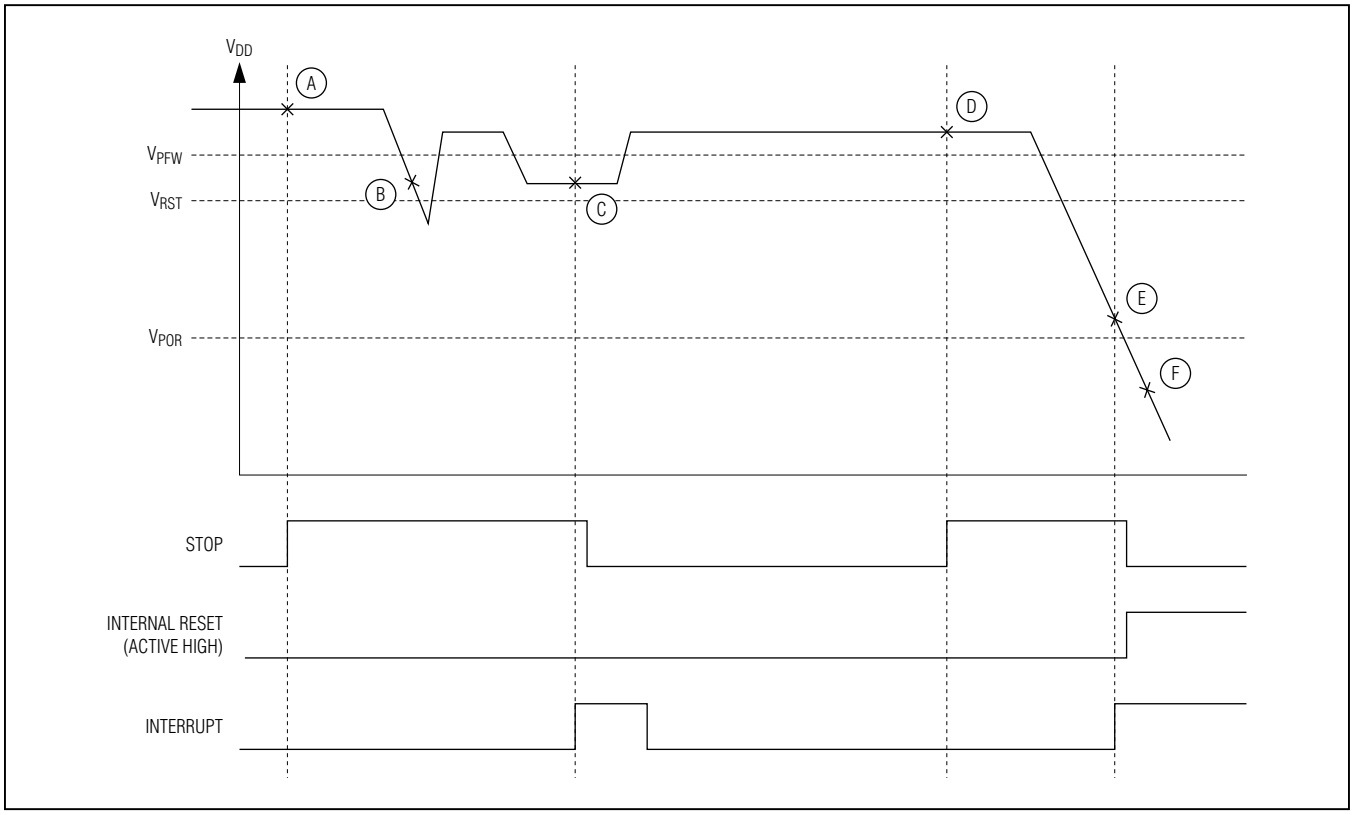


Figure 8. Stop Mode Power-Fail Detection with Power-Fail Monitor Disabled

Table 6. Stop Mode Power-Fail Detection States with Power-Fail Monitor Disabled

STATE	POWER-FAIL	INTERNAL REGULATOR	CRYSTAL OSCILLATOR	SRAM RETENTION	COMMENTS
A	Off	Off	Off	Yes	Application enters stop mode. $V_{DD} > V_{RST}$. CPU in stop mode.
B	Off	Off	Off	Yes	$V_{DD} < V_{PFW}$. Power-fail not detected because power-fail monitor is disabled.
C	On	On	On	Yes	$V_{RST} < V_{DD} < V_{PFW}$. An interrupt occurs that causes the CPU to exit stop mode. Power-fail monitor is turned on, detects a power-fail warning, and sets the power-fail interrupt flag. Turn on regulator and crystal. Crystal warmup time, t_{XTAL_RDY}. On stop mode exit, CPU vectors to the higher priority of power-fail and the interrupt that causes stop mode exit.

Infrared Remote Control System-on-Chip

Additional Documentation

Engineers must have the following documents to fully use this device:

- This data sheet, containing pin descriptions, feature overviews, and electrical specifications.
- The device-appropriate user guide, containing detailed information and programming guidelines for core features and peripherals.
- Errata sheets for specific revisions noting deviations from published specifications.

For information regarding these documents, visit Technical Support at **support.maximintegrated.com/micro**.

Development and Technical Support

Contact technical support for information about highly versatile, affordable development tools, available from Maxim Integrated and third-party vendors.

- Evaluation kits
- Compilers
- Integrated development environments (IDEs)
- USB interface modules for programming and debugging

For technical support, go to **support.maximintegrated.com/micro**.

Ordering Information/Selector Guide

PART	TEMP RANGE	OPERATING VOLTAGE (V)	PROGRAM MEMORY (KB)	DATA MEMORY (KB)	GPIO	PIN-PACKAGE
MAXQ617V-XXXX+T	-20°C to +70°C	1.67 to 3.6	80 Flash	4	10	16 WLP

Note: *The 4-digit suffix "-XXXX" indicates a device preprogrammed at Maxim Integrated with proprietary customer-supplied software. For more information on factory preprogramming of this device, contact Maxim Integrated at* ***support.maximintegrated.com/micro****.*
+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 WLP	W162K2+1	21-0491	Refer to Application Note 1891

Appendix A

I²C SERIAL PERIPHERAL SPECIFICATIONS

(Figure 9 and Figure 10)

PARAMETER	SYMBOL	CONDITIONS	STANDARD MODE		FAST MODE		UNITS
			MIN	MAX	MIN	MAX	
Input Low Voltage	V_{IL_I2C}	Supply voltages that mismatch I²C bus levels must relate input levels to the R_P pullup voltage	-0.5	0.3 x V_{DD}	-0.5	0.3 x V_{DD}	V
Input High Voltage	V_{IH_I2C}	Supply voltages that mismatch I²C bus levels must relate input levels to the R_P pullup voltage	0.7 x V_{DD}		0.7 x V_{DD}	V_{DD} + 0.5V	V
Input Hysteresis (Schmitt)	V_{IHYS_I2C}	V_{DD} > 2V			0.05 x V_{DD}		V
Output Logic-Low (Open Drain or Open Collector)	V_{OL_I2C}	V_{DD} > 2V, 3mA sink current	0	0.4	0	0.4	V
Capacitive Load for Each Bus Line	C_B			400		400	pF
Output Fall Time from V_{IH_MIN} to V_{IL_MAX} with Bus Capacitance from 10pF to 400pF	t_{OF_I2C}	t_{R/F_I2C} exceeds t_{OF_I2C}, which permits RS to be connected as shown in figure		250	20 + 0.1C_B	250	ns
Pulse Width of Spike Filtering That Must Be Suppressed by Input Filter	t_{SP_I2C}				0	50	ns
Input Current on I/O	I_{IN_I2C}	Input voltage from 0.1 x V_{DD} to 0.9 x V_{DD}	-10	+10	-10	+10	µA
I/O Capacitance	C_{IO_I2C}			10		10	pF
I²C Bus Operating Frequency	f_{I2C}		0	100	0	400	kHz
System Frequency	f_{SYS}		0.90		3.60		MHz
I²C Bit Rate	f_{I2C}			f_{SYS}/8		f_{SYS}/8	Hz
Hold Time After (Repeated) START	$t_{HD:STA}$		4.0		0.6		µs
Clock Low Period	t_{LOW_I2C}		4.7		1.3		µs
Clock High Period	t_{HIGH_I2C}		4.0		0.6		µs
Setup Time for Repeated START	$t_{SU:STA}$		4.7		0.6		µs

I²C SERIAL PERIPHERAL SPECIFICATIONS (continued)

(Figure 9 and Figure 10)

PARAMETER	SYMBOL	CONDITIONS	STANDARD MODE		FAST MODE		UNITS
			MIN	MAX	MIN	MAX	
Hold Time for Data	$t_{HD:DAT}$	A device must internally provide a hold time of at least 300ns for $V_{IH\_I2C(MIN)}$ to bridge the undefined region of the falling edge of SCL. The maximum $t_{HD:DAT}$ needs to be met only if the device does not stretch the SCL low period	0	3.45	0	0.9	µs
Setup Time for Data	$t_{SU:DAT}$	A fast-mode I²C bus device can be used in a standard-mode I²C bus system; if such a device does not stretch the low period of the SCL signal, it must output the next data bit to the SDA line $t_{R\_I2C(MAX)} + t_{SU:DAT}$ = 1000 + 250 = 1250ns (according to the standard-mode I²C specification) before the SCL line is released	250		100		ns
SDA/SCL Fall Time	t_{F_I2C}			300	20 + 0.1C_B	300	ns
SDA/SCL Rise Time	t_{R_I2C}			1000	20 + 0.1C_B	300	ns
Setup Time for STOP	$t_{SU:STO}$		4.0		0.6		µs
Bus Free Time Between STOP and START	t_{BUF}		4.7		1.3		µs
Noise Margin at the Low Level for Each Connected Device (Including Hysteresis)	V_{nL_I2C}		0.1 x V_{DD}		0.1 x V_{DD}		V
Noise Margin at the Low Level for Each Connected Device (Including Hysteresis)	V_{nH_I2C}		0.2 x V_{DD}		0.2 x V_{DD}		V

SERIAL PERIPHERAL INTERFACE (SPI) SPECIFICATIONS

(Figure 11 and Figure 12)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SPI Master Operating Frequency	$1/t_{MCK}$				$f_{CK}/2$	MHz
SPI Slave Operating Frequency	$1/t_{SCK}$				$f_{CK}/4$	MHz
SCLK Output Pulse-Width High/ Low	t_{MCH}, t_{MCL}		$t_{MCK}/2$ - 35			ns
MOSI Output Hold Time After SCLK Sample Edge	t_{MOH}		$t_{MCK}/2$ - 35			ns
MOSI Output Valid to Sample Edge	t_{MOV}		$t_{MCK}/2$ - 35			ns
MISO Input Valid to SCLK Sample Edge Rise/Fall Setup	t_{MIS}		35			ns
MISO Input to SCLK Sample Edge Rise/Fall Hold	t_{MIH}		0			ns
SCLK Input Pulse-Width High/Low	t_{SCH}, t_{SCL}			$t_{SCK}/2$		ns
SSEL Active to First Shift Edge	t_{SSE}			50		ns
MOSI Input to SCLK Sample Edge Rise/Fall Setup	t_{SIS}		35			ns
MOSI Input from SCLK Sample Edge Transition Hold	t_{SIH}		35			ns
MISO Output Valid After SCLK Shift Edge Transition	t_{SOV}				70	ns
SCLK Inactive to SSEL Rising	t_{SD}		35			ns

SPI Timing Diagrams

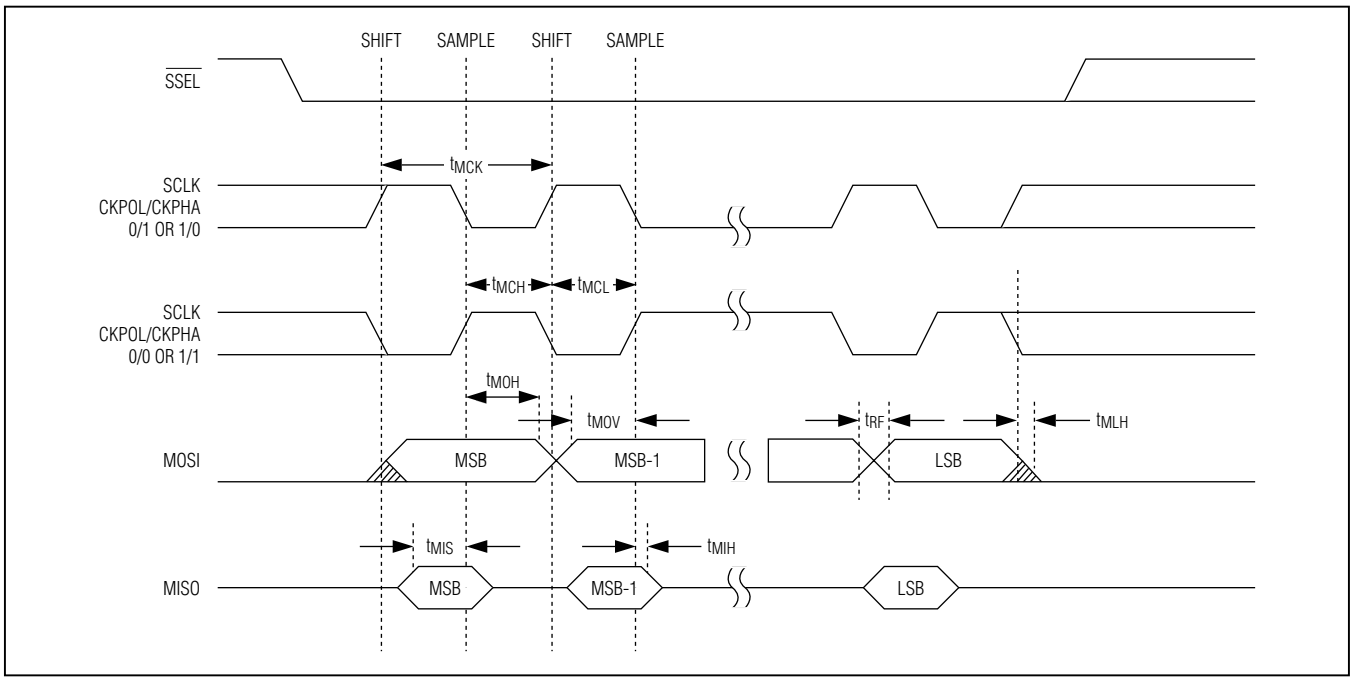


Figure 11. SPI Master Communication Timing

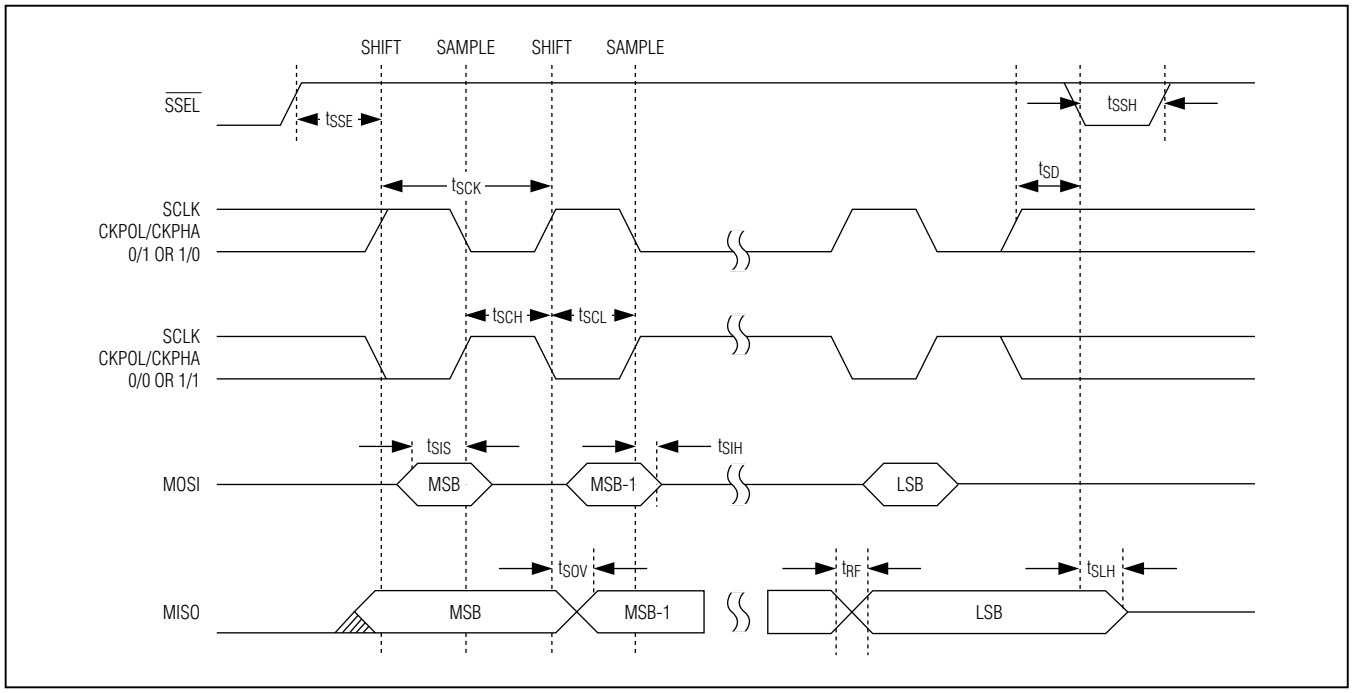


Figure 12. SPI Slave Communication Timing

USART MODE 0 SPECIFICATIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TXD Clock Period	t_{XLXL}	SM2 = 0		$12t_{CLCL}$		ns
		SM2 = 1		$4t_{CLCL}$		ns
TXD Clock High Time	t_{XHXL}	SM2 = 0		$3t_{CLCL}$		ns
		SM2 = 1		$2t_{CLCL}$		ns
RXD Output Data Valid to TXD Clock Rising Edge	t_{QVXH}	SM2 = 0		$10t_{CLCL}$		ns
		SM2 = 1		$3t_{CLCL}$		ns
RXD Output Data Hold from TXD Clock Rising Edge	t_{XHQH}	SM2 = 0		$2t_{CLCL}$		ns
		SM2 = 1		t_{CLCL}		ns
RXD Input Data Valid to TXD Clock Rising Edge	t_{DVXH}	SM2 = 0		t_{CLCL}		ns
		SM2 = 1		t_{CLCL}		ns
RXD Input Data Hold after TXD Clock Rising Edge	t_{XHDH}	SM2 = 0		t_{CLCL}		ns
		SM2 = 1		t_{CLCL}		ns

USART Timing

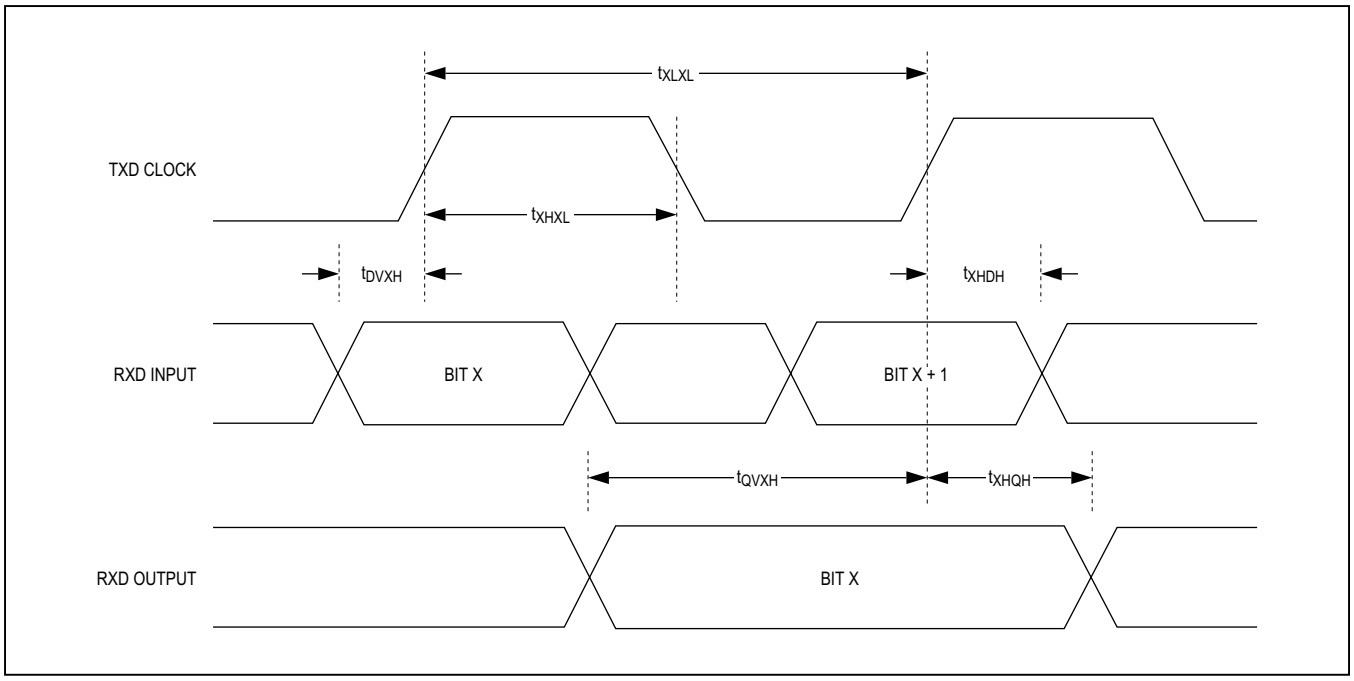


Figure 13. USART Timing Diagram

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/13	Initial release	—