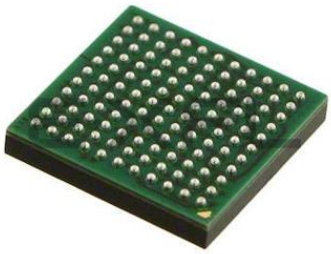


**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 50MHz |
| Connectivity | I²C, IrDA, SPI, UART/USART, USB, USB OTG |
| Peripherals | DMA, I²S, LVD, POR, PWM, WDT |
| Number of I/O | 64 |
| Program Memory Size | 512KB (512K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 64K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.71V ~ 3.6V |
| Data Converters | A/D 20x16b; D/A 1x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 121-LFBGA |
| Supplier Device Package | 121-MAPBGA (8x8) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mk21dn512vmc5 |

# 1 Ordering parts

## 1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to freescale.com and perform a part number search for the following device numbers: PK21 and MK21 .

# 2 Part identification

## 2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

## 2.2 Format

Part numbers for this device have the following format:

Q K## A M FFF R T PP CC N

## 2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

| Field | Description | Values |
|---|---|---|
| Q | Qualification status | • M = Fully qualified, general market flow<br>• P = Prequalification |
| K## | Kinetis family | • K21 |
| A | Key attribute | • D = Cortex-M4 w/ DSP<br>• F = Cortex-M4 w/ DSP and FPU |
| M | Flash memory type | • N = Program flash only<br>• X = Program flash and FlexMemory |

*Table continues on the next page...*

| Field | Description | Values |
|---|---|---|
| Q | Qualification status | • M = Fully qualified, general market flow<br>• P = Prequalification |
| ## | Kinetis family | • 1# = K11/K12<br>• 2# = K21/K22 |
| C | Speed | • G = 50 MHz |
| F | Flash memory configuration | • G = 128 KB + Flex<br>• H = 256 KB + Flex<br>• 9 = 512 KB |
| T | Temperature range (°C) | • V = –40 to 105 |
| PP | Package identifier | • MC = 121 MAPBGA |

This tables lists some examples of small package marking along with the original part numbers:

| Original part number | Alternate part number |
|---|---|
| MK21DX128VMC5 | M21GGVMC |
| MK21DX256VMC5 | M21GHVMC |
| MK21DN512VMC5 | M21G9VMC |

# 3 Terminology and guidelines

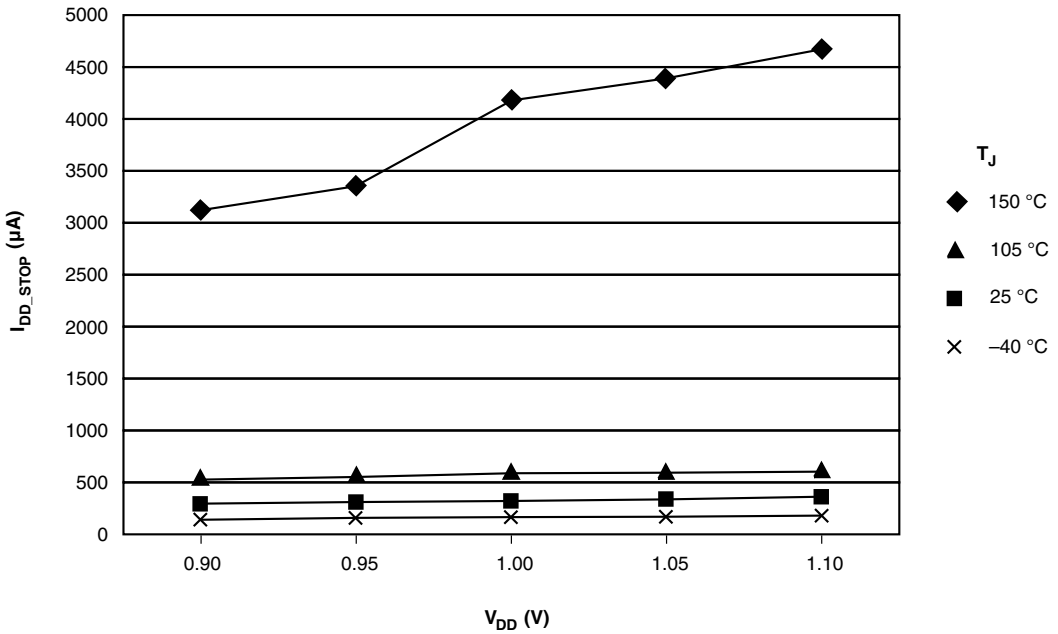
## 3.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

### 3.1.1 Example

This is an example of an operating requirement:

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DD}$ | 1.0 V core supply voltage | 0.9 | 1.1 | V |




## 3.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

| Symbol | Description | Value | Unit |
|---|---|---|---|
| $T_A$ | Ambient temperature | 25 | °C |
| $V_{DD}$ | 3.3 V supply voltage | 3.3 | V |

# 4 Ratings

## 4.1 Thermal handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $T_{STG}$ | Storage temperature | –55 | 150 | °C | 1 |
| $T_{SDR}$ | Solder temperature, lead-free | — | 260 | °C | 2 |

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

## 5.2.4 Power mode transition operating behaviors

All specifications except $t_{POR}$, and VLLSx→RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 50 MHz
- Bus clock = 50 MHz
- Flash clock = 25 MHz
- MCG mode: FEI

**Table 5. Power mode transition operating behaviors**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $t_{POR}$ | After a POR event, amount of time from the point $V_{DD}$ reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip.<br>• 1.71 V/($V_{DD}$ slew rate) ≤ 300 µs<br>• 1.71 V/($V_{DD}$ slew rate) > 300 µs | <br><br>—<br>— | <br><br>300<br>1.7 V / ($V_{DD}$ slew rate) | µs | 1 |
| | • VLLS0 → RUN | — | 135 | µs | |
| | • VLLS1 → RUN | — | 135 | µs | |
| | • VLLS2 → RUN | — | 85 | µs | |
| | • VLLS3 → RUN | — | 85 | µs | |
| | • LLS → RUN | — | 6 | µs | |
| | • VLPS → RUN | — | 5.2 | µs | |
| | • STOP → RUN | — | 5.2 | µs | |

1. Normal boot (FTFL_OPT[LPBOOT]=1)

## 5.2.5 Power consumption operating behaviors

**Table 6. Power consumption operating behaviors**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $I_{DDA}$ | Analog supply current | — | — | See note | mA | 1 |
| $I_{DD\_RUN}$ | Run mode current — all peripheral clocks disabled, code executing from flash<br>• @ 1.8 V<br>• @ 3.0 V | <br>—<br>— | <br>12.98<br>12.93 | <br>14<br>13.8 | <br>mA<br>mA | 2 |

*Table continues on the next page...*

**Table 6. Power consumption operating behaviors (continued)**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $I_{DD\_VLLS1}$ | Very low-leakage stop mode 1 current at 3.0 V<br>• @ –40 to 25°C<br>• @ 50°C<br>• @ 70°C<br>• @ 105°C | — | 1.03<br>1.92<br>4.03<br>17.43 | 1.8<br>7.5<br>15.9<br>28.7 | µA | |
| $I_{DD\_VLLS0}$ | Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit enabled<br>• @ –40 to 25°C<br>• @ 50°C<br>• @ 70°C<br>• @ 105°C | — | 0.543<br>1.36<br>3.39<br>16.52 | 1.1<br>7.58<br>14.3<br>24.1 | µA | |
| $I_{DD\_VLLS0}$ | Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit disabled<br>• @ –40 to 25°C<br>• @ 50°C<br>• @ 70°C<br>• @ 105°C | — | 0.359<br>1.03<br>2.87<br>15.20 | 0.95<br>6.8<br>15.4<br>25.3 | µA | |
| $I_{DD\_VBAT}$ | Average current when CPU is not accessing RTC registers at 3.0 V<br>• @ –40 to 25°C<br>• @ 50°C<br>• @ 70°C<br>• @ 105°C | — | 0.91<br>1.1<br>1.5<br>4.3 | 1.1<br>1.35<br>1.85<br>5.7 | µA | 9 |

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. 50 MHz core and system clock, 25 MHz bus clock, and 25 MHz flash clock. MCG configured for FEI mode. All peripheral clocks disabled.
3. 50 MHz core and system clock, 25 MHz bus clock, and 25 MHz flash clock. MCG configured for FEI mode. All peripheral clocks enabled, and peripherals are in active operation.
4. Max values are measured with CPU executing DSP instructions
5. 25 MHz core and system clock, 25 MHz bus clock, and 12.5 MHz flash clock. MCG configured for FEI mode.
6. 4 MHz core, system, and bus clock and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. Code executing from flash.
7. 4 MHz core, system, and bus clock and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks enabled but peripherals are not in active operation. Code executing from flash.
8. 4 MHz core, system, and bus clock and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled.
9. Includes 32 kHz oscillator current and RTC operation.

### 5.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE mode
- USB regulator disabled
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFL

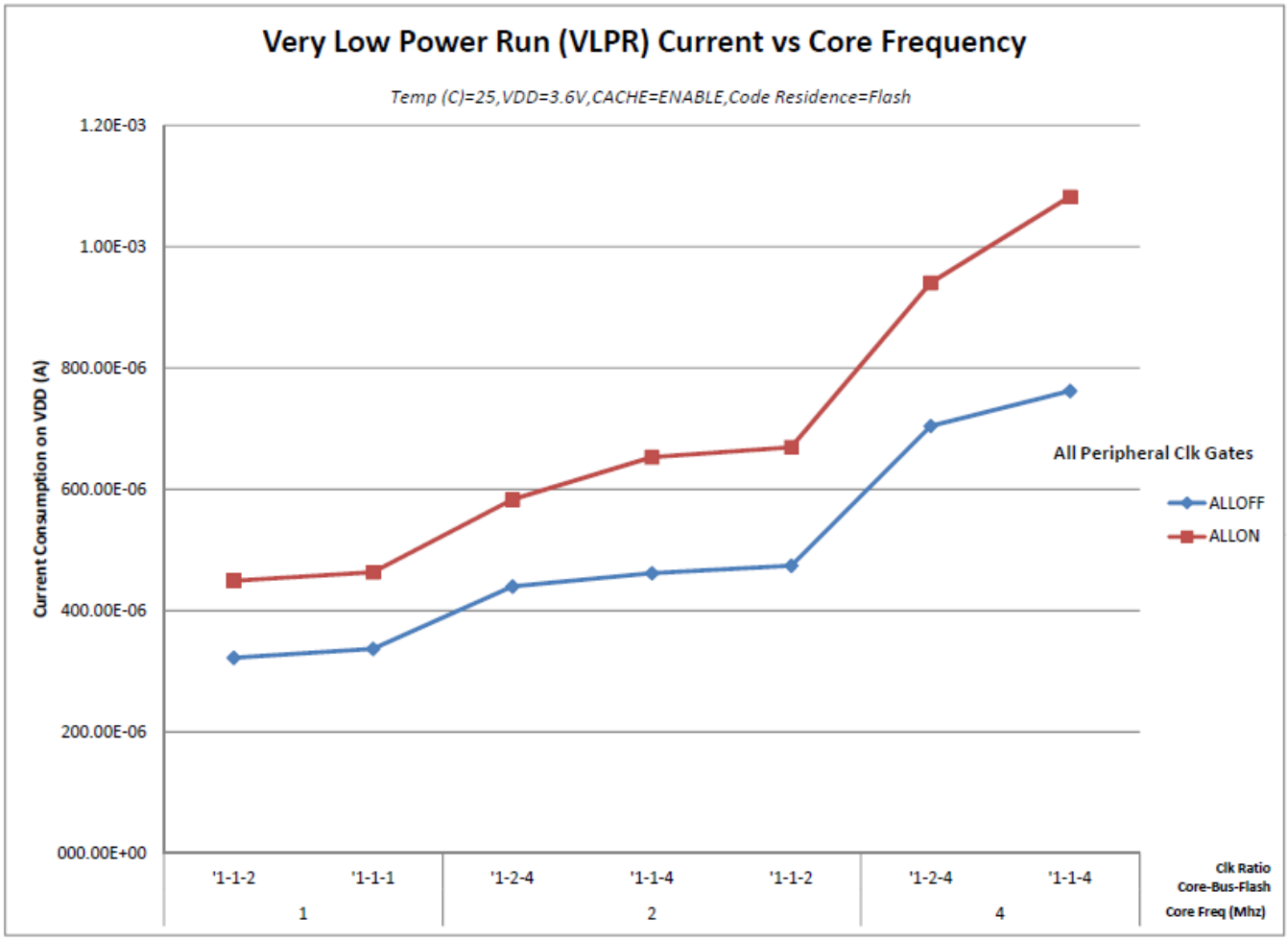



**Figure 3. VLPR mode supply current vs. core frequency**

## 5.2.6 EMC radiated emissions operating behaviors

**Table 7. EMC radiated emissions operating behaviors [1]**

| Symbol | Description | Frequency band (MHz) | Typ. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{RE1}$ | Radiated emissions voltage, band 1 | 0.15–50 | 19 | dBµV | 2, 3 |
| $V_{RE2}$ | Radiated emissions voltage, band 2 | 50–150 | 21 | dBµV | |
| $V_{RE3}$ | Radiated emissions voltage, band 3 | 150–500 | 19 | dBµV | |
| $V_{RE4}$ | Radiated emissions voltage, band 4 | 500–1000 | 11 | dBµV | |
| $V_{RE\_IEC}$ | IEC level | 0.15–1000 | L | — | 3, 4 |

1. This data was collected on a MK20DN128VLH5 64pin LQFP device.
2. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*. Measurements were made while the microcontroller was running basic application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.

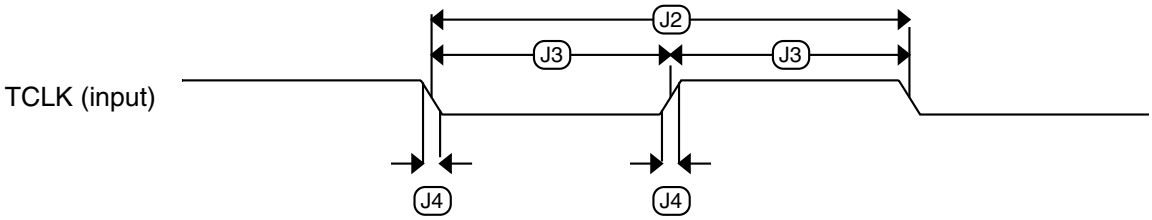



**Figure 4. Test clock input timing**

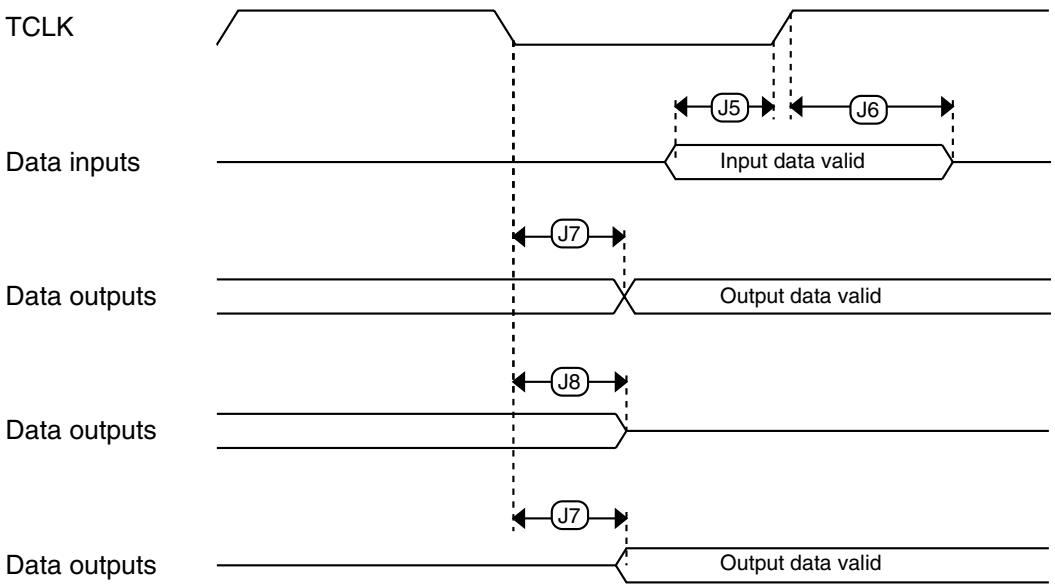



**Figure 5. Boundary scan (JTAG) timing**

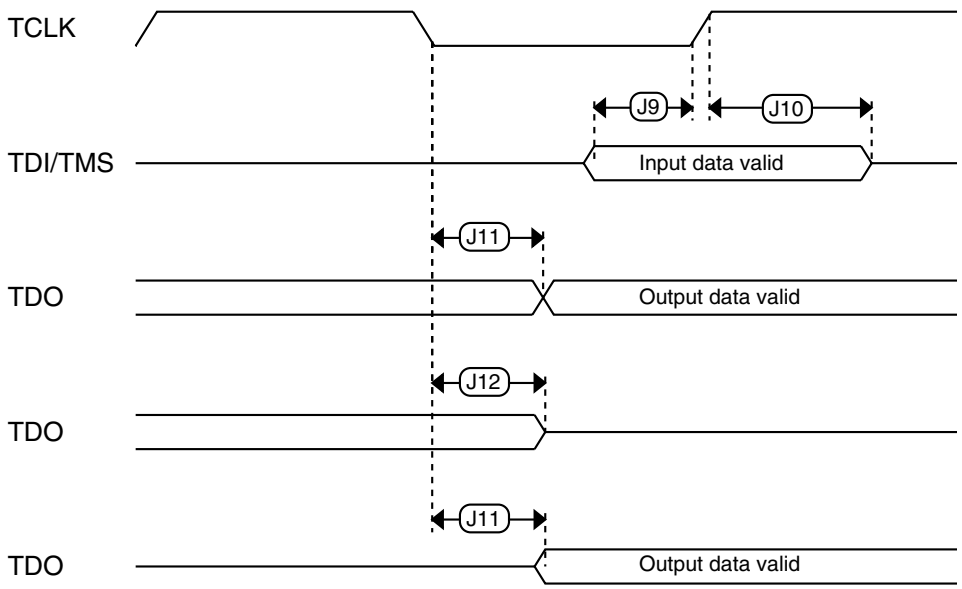



**Figure 6. Test Access Port timing**

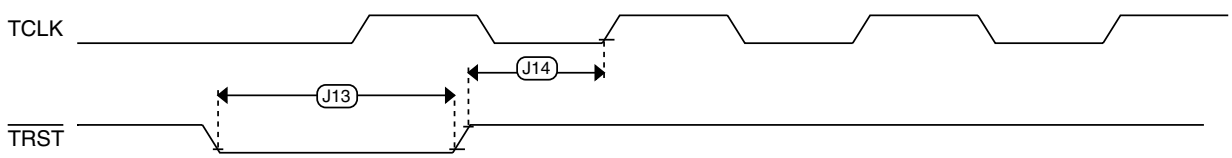



**Figure 7. $\overline{\text{TRST}}$ timing**

## 6.2 System modules

There are no specifications necessary for the device's system modules.

## 6.3 Clock modules

## 6.3.1 MCG specifications

**Table 14. MCG specifications**

| Symbol | Description | | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $f_{ints\_ft}$ | Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C | | — | 32.768 | — | kHz | |
| $f_{ints\_t}$ | Internal reference frequency (slow clock) — user trimmed | | 31.25 | — | 39.0625 | kHz | |
| $\Delta_{fdco\_res\_t}$ | Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM | | — | ± 0.3 | ± 0.6 | $\%f_{dco}$ | 1 |
| $\Delta f_{dco\_res\_t}$ | Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM only | | — | ± 0.2 | ± 0.5 | $\%f_{dco}$ | 1 |
| $\Delta f_{dco\_t}$ | Total deviation of trimmed average DCO output frequency over voltage and temperature | | — | +0.5/-0.7 | ± 2 | $\%f_{dco}$ | 1, 2 |
| $\Delta f_{dco\_t}$ | Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C | | — | ± 0.3 | ±1 | $\%f_{dco}$ | 1, 2 |
| $f_{intf\_ft}$ | Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C | | — | 4 | — | MHz | |
| $f_{intf\_t}$ | Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C | | 3 | — | 5 | MHz | |
| $f_{loc\_low}$ | Loss of external clock minimum frequency — RANGE = 00 | | (3/5) x $f_{ints\_t}$ | — | — | kHz | |
| $f_{loc\_high}$ | Loss of external clock minimum frequency — RANGE = 01, 10, or 11 | | (16/5) x $f_{ints\_t}$ | — | — | kHz | |
| FLL | | | | | | | |
| $f_{fll\_ref}$ | FLL reference frequency range | | 31.25 | — | 39.0625 | kHz | |
| $f_{dco}$ | DCO output frequency range | Low range (DRS=00) 640 × $f_{fll\_ref}$ | 20 | 20.97 | 25 | MHz | 3, 4 |
| | | Mid range (DRS=01) 1280 × $f_{fll\_ref}$ | 40 | 41.94 | 50 | MHz | |
| | | Mid-high range (DRS=10) 1920 × $f_{fll\_ref}$ | 60 | 62.91 | 75 | MHz | |
| | | High range (DRS=11) 2560 × $f_{fll\_ref}$ | 80 | 83.89 | 100 | MHz | |
| $f_{dco\_t\_DMX32}$ | DCO output frequency | Low range (DRS=00) 732 × $f_{fll\_ref}$ | — | 23.99 | — | MHz | 5, 6 |
| | | Mid range (DRS=01) 1464 × $f_{fll\_ref}$ | — | 47.97 | — | MHz | |
| | | Mid-high range (DRS=10) 2197 × $f_{fll\_ref}$ | — | 71.99 | — | MHz | |
| | | High range (DRS=11) 2929 × $f_{fll\_ref}$ | — | 95.98 | — | MHz | |

*Table continues on the next page...*

4. Crystal startup time is defined as the time between oscillator being enabled and OSCINIT bit in the MCG_S register being set.

**NOTE**

The 32 kHz oscillator works in low power mode by default and cannot be moved into high power/gain mode.

## 6.3.3 32 kHz oscillator electrical characteristics

### 6.3.3.1 32 kHz oscillator DC electrical specifications

**Table 17. 32kHz oscillator DC electrical specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{BAT}$ | Supply voltage | 1.71 | — | 3.6 | V |
| $R_F$ | Internal feedback resistor | — | 100 | — | MΩ |
| $C_{para}$ | Parasitical capacitance of EXTAL32 and XTAL32 | — | 5 | 7 | pF |
| $V_{pp}$[1] | Peak-to-peak amplitude of oscillation | — | 0.6 | — | V |

1. When a crystal is being used with the 32 kHz oscillator, the EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

### 6.3.3.2 32 kHz oscillator frequency specifications

**Table 18. 32 kHz oscillator frequency specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $f_{osc\_lo}$ | Oscillator crystal | — | 32.768 | — | kHz | |
| $t_{start}$ | Crystal start-up time | — | 1000 | — | ms | 1 |
| $v_{ec\_extal32}$ | Externally provided input clock amplitude | 700 | — | $V_{BAT}$ | mV | 2, 3 |

1. Proper PC board layout procedures must be followed to achieve specifications.
2. This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The oscillator remains enabled and XTAL32 must be left unconnected.
3. The parameter specified is a peak-to-peak value and $V_{IH}$ and $V_{IL}$ specifications do not apply. The voltage of the applied clock must be within the range of $V_{SS}$ to $V_{BAT}$.

# 6.4 Memories and memory interfaces

## 6.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

### 6.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

**Table 19. NVM program/erase timing specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $t_{hvpgm4}$ | Longword Program high-voltage time | — | 7.5 | 18 | µs | |
| $t_{hversscr}$ | Sector Erase high-voltage time | — | 13 | 113 | ms | 1 |
| $t_{hversblk256k}$ | Erase Block high-voltage time for 256 KB | — | 104 | 904 | ms | 1 |

1. Maximum time based on expectations at cycling end-of-life.

### 6.4.1.2 Flash timing specifications — commands

**Table 20. Flash command timing specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| | Read 1s Block execution time | | | | | |
| $t_{rd1blk64k}$ | • 64 KB data flash | — | — | 0.9 | ms | |
| $t_{rd1blk256k}$ | • 256 KB program flash | — | — | 1.7 | ms | |
| $t_{rd1sec2k}$ | Read 1s Section execution time (flash sector) | — | — | 60 | µs | 1 |
| $t_{pgmchk}$ | Program Check execution time | — | — | 45 | µs | 1 |
| $t_{rdrsrc}$ | Read Resource execution time | — | — | 30 | µs | 1 |
| $t_{pgm4}$ | Program Longword execution time | — | 65 | 145 | µs | |
| | Erase Flash Block execution time | | | | | 2 |
| $t_{ersblk64k}$ | • 64 KB data flash | — | 58 | 580 | ms | |
| $t_{ersblk256k}$ | • 256 KB program flash | — | 122 | 985 | ms | |
| $t_{ersscr}$ | Erase Flash Sector execution time | — | 14 | 114 | ms | 2 |
| | Program Section execution time | | | | | |
| $t_{pgmsec512}$ | • 512 bytes flash | — | 2.4 | — | ms | |
| $t_{pgmsec1k}$ | • 1 KB flash | — | 4.7 | — | ms | |
| $t_{pgmsec2k}$ | • 2 KB flash | — | 9.3 | — | ms | |
| $t_{rd1all}$ | Read 1s All Blocks execution time | — | — | 1.8 | ms | |
| $t_{rdonce}$ | Read Once execution time | — | — | 25 | µs | 1 |
| $t_{pgmonce}$ | Program Once execution time | — | 65 | — | µs | |
| $t_{ersall}$ | Erase All Blocks execution time | — | 250 | 2000 | ms | 2 |
| $t_{vfykey}$ | Verify Backdoor Access Key execution time | — | — | 30 | µs | 1 |

*Table continues on the next page...*

## Table 20. Flash command timing specifications (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| | Swap Control execution time | | | | | |
| $t_{swapx01}$ | • control code 0x01 | — | 200 | — | µs | |
| $t_{swapx02}$ | • control code 0x02 | — | 70 | 150 | µs | |
| $t_{swapx04}$ | • control code 0x04 | — | 70 | 150 | µs | |
| $t_{swapx08}$ | • control code 0x08 | — | — | 30 | µs | |
| | Program Partition for EEPROM execution time | | | | | |
| $t_{pgmpart64k}$ | • 64 KB FlexNVM | — | 138 | — | ms | |
| | Set FlexRAM Function execution time: | | | | | |
| $t_{setramff}$ | • Control Code 0xFF | — | 70 | — | µs | |
| $t_{setram32k}$ | • 32 KB EEPROM backup | — | 0.8 | 1.2 | ms | |
| $t_{setram64k}$ | • 64 KB EEPROM backup | — | 1.3 | 1.9 | ms | |
| | Byte-write to FlexRAM for EEPROM operation | | | | | |
| $t_{eewr8bers}$ | Byte-write to erased FlexRAM location execution time | — | 175 | 260 | µs | 3 |
| | Byte-write to FlexRAM execution time: | | | | | |
| $t_{eewr8b32k}$ | • 32 KB EEPROM backup | — | 385 | 1800 | µs | |
| $t_{eewr8b64k}$ | • 64 KB EEPROM backup | | 475 | 2000 | µs | |
| | Word-write to FlexRAM for EEPROM operation | | | | | |
| $t_{eewr16bers}$ | Word-write to erased FlexRAM location execution time | — | 175 | 260 | µs | |
| | Word-write to FlexRAM execution time: | | | | | |
| $t_{eewr16b32k}$ | • 32 KB EEPROM backup | — | 385 | 1800 | µs | |
| $t_{eewr16b64k}$ | • 64 KB EEPROM backup | — | 475 | 2000 | µs | |
| | Longword-write to FlexRAM for EEPROM operation | | | | | |
| $t_{eewr32bers}$ | Longword-write to erased FlexRAM location execution time | — | 360 | 540 | µs | |
| | Longword-write to FlexRAM execution time: | | | | | |
| $t_{eewr32b32k}$ | • 32 KB EEPROM backup | — | 630 | 2050 | µs | |
| $t_{eewr32b64k}$ | • 64 KB EEPROM backup | — | 810 | 2250 | µs | |

1. Assumes 25 MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.
3. For byte-writes to an erased FlexRAM location, the aligned word containing the byte must be erased.

### 6.4.1.3 Flash high voltage current behaviors

**Table 21. Flash high voltage current behaviors**

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $I_{DD\_PGM}$ | Average current adder during high voltage flash programming operation | — | 2.5 | 6.0 | mA |
| $I_{DD\_ERS}$ | Average current adder during high voltage flash erase operation | — | 1.5 | 4.0 | mA |

### 6.4.1.4 Reliability specifications

**Table 22. NVM reliability specifications**

| Symbol | Description | Min. | Typ.[1] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| | Program Flash | | | | | |
| $t_{nvmretp10k}$ | Data retention after up to 10 K cycles | 5 | 50 | — | years | |
| $t_{nvmretp1k}$ | Data retention after up to 1 K cycles | 20 | 100 | — | years | |
| $n_{nvmcycp}$ | Cycling endurance | 10 K | 50 K | — | cycles | 2 |
| | Data Flash | | | | | |
| $t_{nvmretd10k}$ | Data retention after up to 10 K cycles | 5 | 50 | — | years | |
| $t_{nvmretd1k}$ | Data retention after up to 1 K cycles | 20 | 100 | — | years | |
| $n_{nvmcycd}$ | Cycling endurance | 10 K | 50 K | — | cycles | 2 |
| | FlexRAM as EEPROM | | | | | |
| $t_{nvmretee100}$ | Data retention up to 100% of write endurance | 5 | 50 | — | years | |
| $t_{nvmretee10}$ | Data retention up to 10% of write endurance | 20 | 100 | — | years | |
| | Write endurance | | | | | 3 |
| $n_{nvmwree16}$ | • EEPROM backup to FlexRAM ratio = 16 | 35 K | 175 K | — | writes | |
| $n_{nvmwree128}$ | • EEPROM backup to FlexRAM ratio = 128 | 315 K | 1.6 M | — | writes | |
| $n_{nvmwree512}$ | • EEPROM backup to FlexRAM ratio = 512 | 1.27 M | 6.4 M | — | writes | |
| $n_{nvmwree4k}$ | • EEPROM backup to FlexRAM ratio = 4096 | 10 M | 50 M | — | writes | |

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at -40 °C ≤ $T_j$ ≤ °C.
3. Write endurance represents the number of writes to each FlexRAM location at -40 °C ≤Tj ≤ °C influenced by the cycling endurance of the FlexNVM (same value as data flash) and the allocated EEPROM backup per subsystem. Minimum and typical values assume all byte-writes to FlexRAM.

### 6.5.1 DryIce Tamper Electrical Specifications

Information about security-related modules is not included in this document and is available only after a nondisclosure agreement (NDA) has been signed. To request an NDA, please contact your local Freescale sales representative.

## 6.6 Analog

### 6.6.1 ADC electrical specifications

The 16-bit accuracy specifications listed in Table 24 and Table 25 are achievable on the differential pins ADCx_DP0, ADCx_DM0.

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

#### 6.6.1.1 16-bit ADC operating conditions

**Table 24. 16-bit ADC operating conditions**

| Symbol | Description | Conditions | Min. | Typ.[1] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $V_{DDA}$ | Supply voltage | Absolute | 1.71 | — | 3.6 | V | |
| $\Delta V_{DDA}$ | Supply voltage | Delta to $V_{DD}$ ($V_{DD} - V_{DDA}$) | -100 | 0 | +100 | mV | 2 |
| $\Delta V_{SSA}$ | Ground voltage | Delta to $V_{SS}$ ($V_{SS} - V_{SSA}$) | -100 | 0 | +100 | mV | 2 |
| $V_{REFH}$ | ADC reference voltage high | | 1.13 | $V_{DDA}$ | $V_{DDA}$ | V | |
| $V_{REFL}$ | ADC reference voltage low | | $V_{SSA}$ | $V_{SSA}$ | $V_{SSA}$ | V | |
| $V_{ADIN}$ | Input voltage | • 16-bit differential mode<br>• All other modes | VREFL<br>VREFL | —<br>— | 31/32 * VREFH<br>VREFH | V | |
| $C_{ADIN}$ | Input capacitance | • 16-bit mode<br>• 8-bit / 10-bit / 12-bit modes | —<br>— | 8<br>4 | 10<br>5 | pF | |
| $R_{ADIN}$ | Input resistance | | — | 2 | 5 | kΩ | |
| $R_{AS}$ | Analog source resistance | 13-bit / 12-bit modes<br>$f_{ADCK}$ < 4 MHz | — | — | 5 | kΩ | 3 |
| $f_{ADCK}$ | ADC conversion clock frequency | ≤ 13-bit mode | 1.0 | — | 18.0 | MHz | 4 |
| $f_{ADCK}$ | ADC conversion clock frequency | 16-bit mode | 2.0 | — | 12.0 | MHz | 4 |

*Table continues on the next page...*

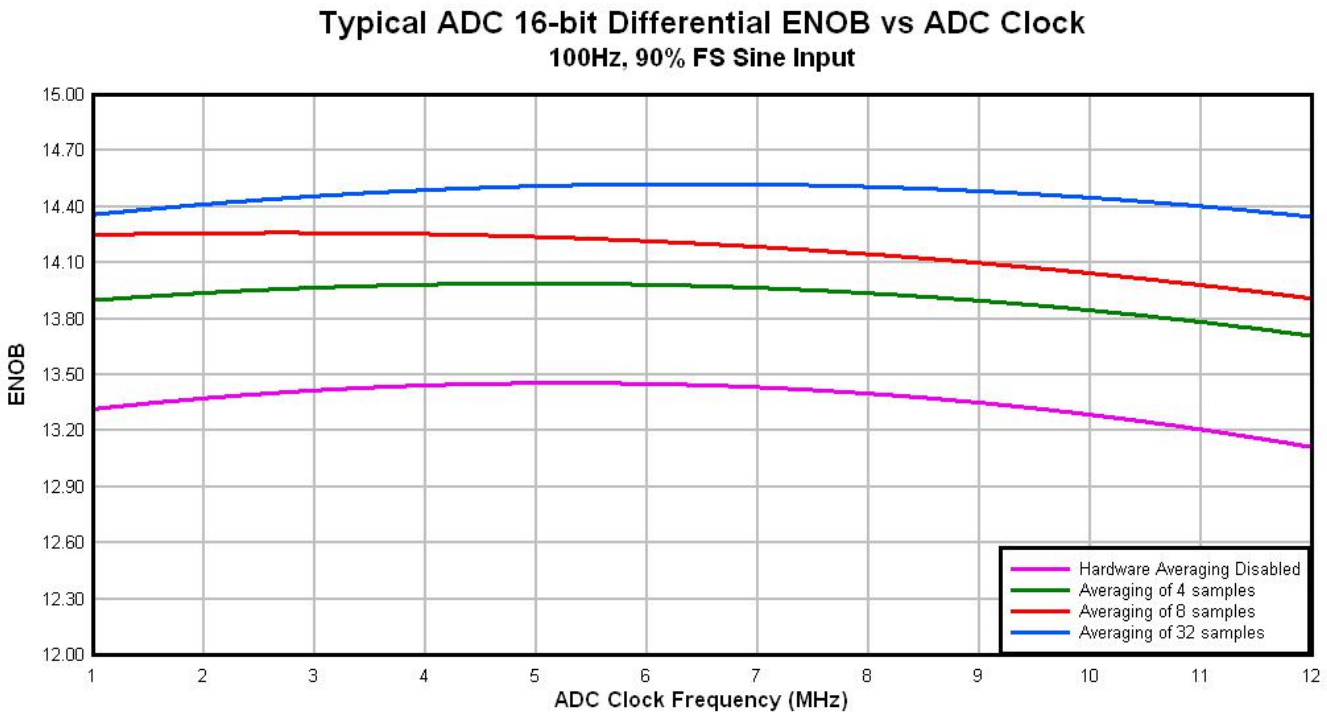



**Figure 10. Typical ENOB vs. ADC_CLK for 16-bit differential mode**

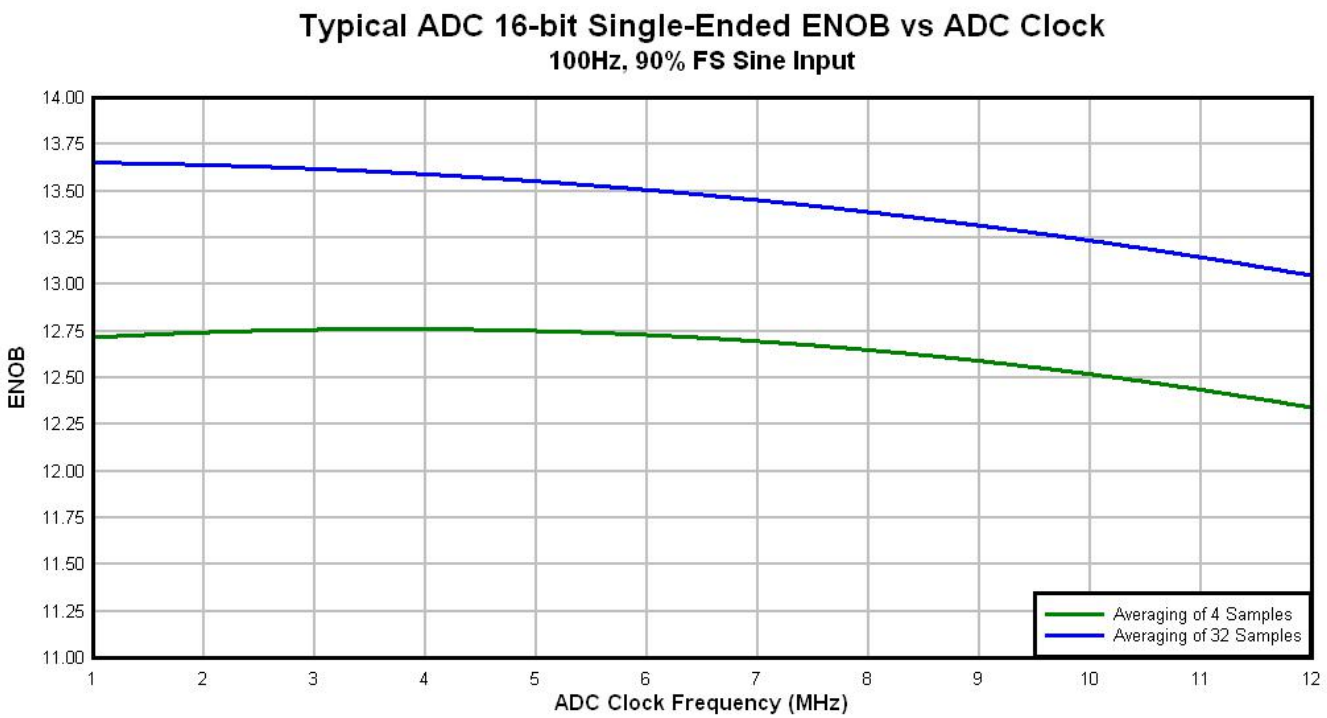



**Figure 11. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode**

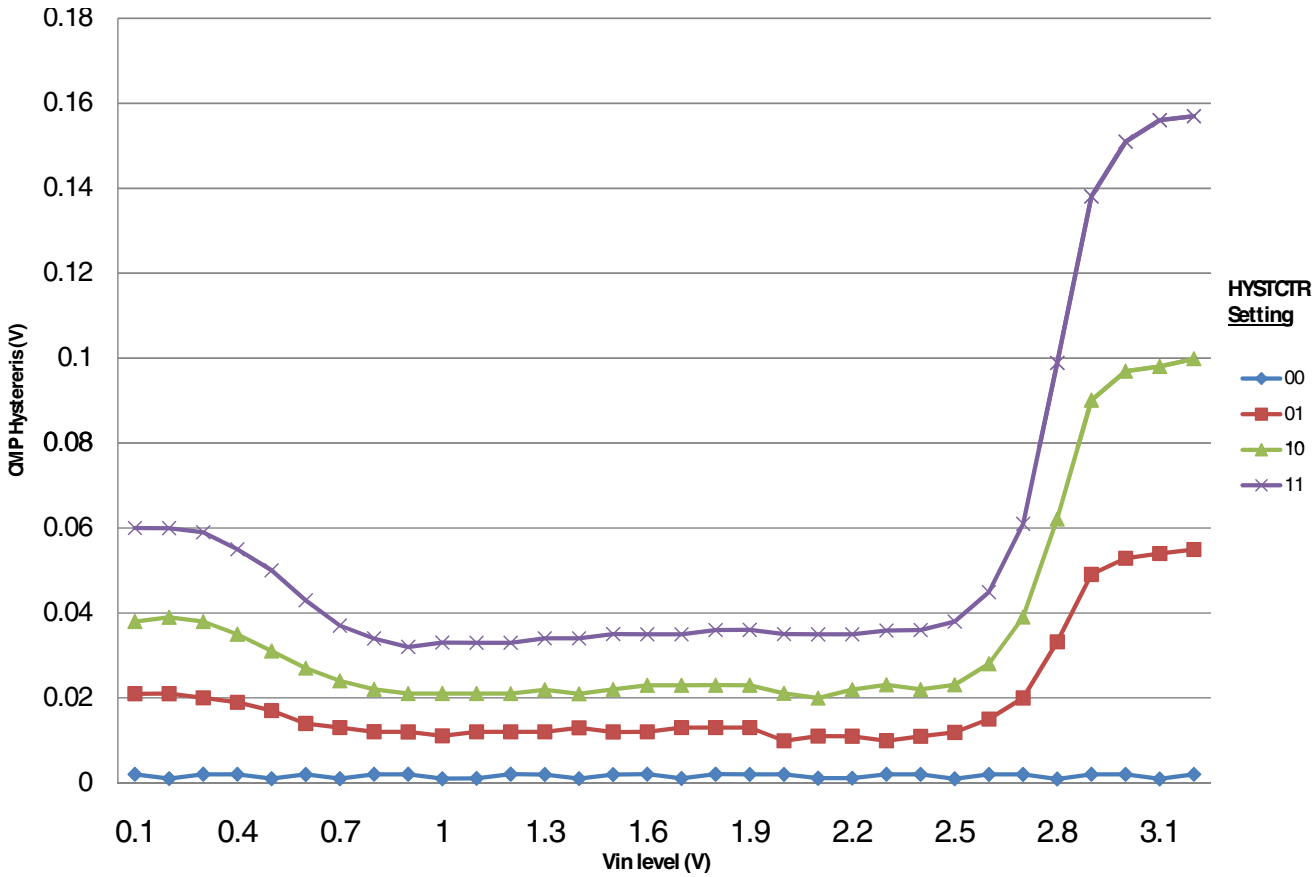



**Figure 13. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)**

## 6.6.3 12-bit DAC electrical characteristics

### 6.6.3.1 12-bit DAC operating requirements

**Table 27. 12-bit DAC operating requirements**

| Symbol | Desciption | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{DDA}$ | Supply voltage | 1.71 | 3.6 | V | |
| $V_{DACR}$ | Reference voltage | 1.13 | 3.6 | V | 1 |
| $T_A$ | Temperature | Operating temperature range of the device | | °C | |
| $C_L$ | Output load capacitance | — | 100 | pF | 2 |
| $I_L$ | Output load current | — | 1 | mA | |

1. The DAC reference can be selected to be $V_{DDA}$ or the voltage output of the VREF module (VREF_OUT)
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC

## Table 33. Master mode DSPI timing (full voltage range) (continued)

| Num | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| DS4 | DSPI_SCK to DSPI_PCS*n* invalid delay | ($t_{BUS}$ x 2) – 4 | — | ns | 3 |
| DS5 | DSPI_SCK to DSPI_SOUT valid | — | 10 | ns | |
| DS6 | DSPI_SCK to DSPI_SOUT invalid | -4.5 | — | ns | |
| DS7 | DSPI_SIN to DSPI_SCK input setup | 20.5 | — | ns | |
| DS8 | DSPI_SCK to DSPI_SIN input hold | 0 | — | ns | |

1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
2. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
3. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

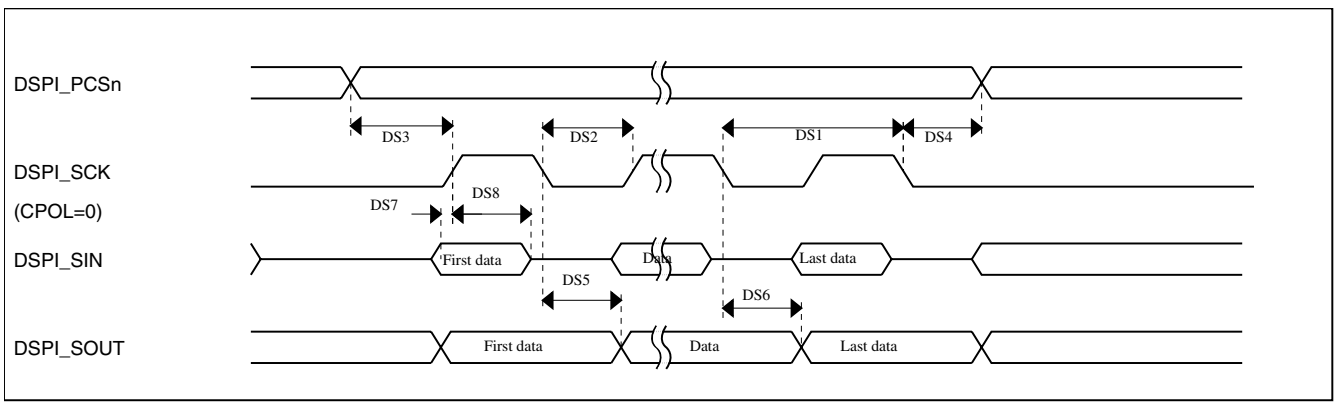



**Figure 18. DSPI classic SPI timing — master mode**

## Table 34. Slave mode DSPI timing (full voltage range)

| Num | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| | Operating voltage | 1.71 | 3.6 | V |
| | Frequency of operation | — | 6.25 | MHz |
| DS9 | DSPI_SCK input cycle time | 8 x $t_{BUS}$ | — | ns |
| DS10 | DSPI_SCK input high/low time | ($t_{SCK}$/2) - 4 | ($t_{SCK/2)}$ + 4 | ns |
| DS11 | DSPI_SCK to DSPI_SOUT valid | — | 20 | ns |
| DS12 | DSPI_SCK to DSPI_SOUT invalid | 0 | — | ns |
| DS13 | DSPI_SIN to DSPI_SCK input setup | 2 | — | ns |
| DS14 | DSPI_SCK to DSPI_SIN input hold | 7 | — | ns |
| DS15 | $\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven | — | 19 | ns |
| DS16 | $\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven | — | 19 | ns |

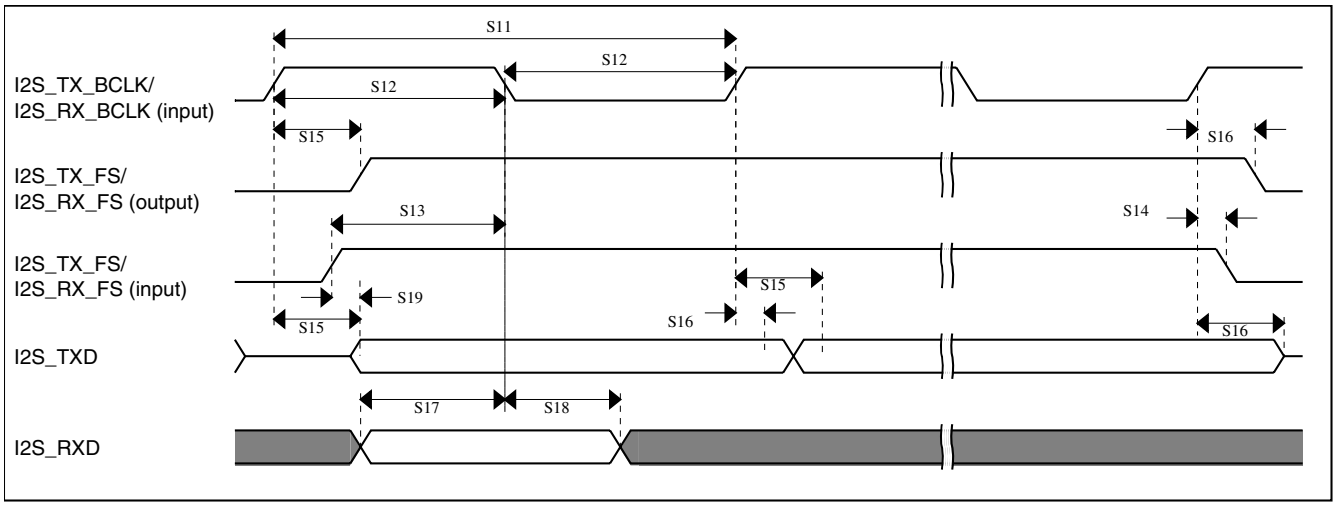



**Figure 21. I2S/SAI timing — slave modes**

## 6.8.9 VLPR, VLPW, and VLPS mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in VLPR, VLPW, and VLPS modes.

**Table 37. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range)**

| Num. | Characteristic | Min. | Max. | Unit |
|---|---|---|---|---|
| | Operating voltage | 1.71 | 3.6 | V |
| S1 | I2S_MCLK cycle time | 62.5 | — | ns |
| S2 | I2S_MCLK pulse width high/low | 45% | 55% | MCLK period |
| S3 | I2S_TX_BCLK/I2S_RX_BCLK cycle time (output) | 250 | — | ns |
| S4 | I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low | 45% | 55% | BCLK period |
| S5 | I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid | — | 45 | ns |
| S6 | I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid | 0 | — | ns |
| S7 | I2S_TX_BCLK to I2S_TXD valid | — | 45 | ns |
| S8 | I2S_TX_BCLK to I2S_TXD invalid | 0 | — | ns |
| S9 | I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK | 75 | — | ns |
| S10 | I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK | 0 | — | ns |

| 121 MAP BGA | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | EzPort |
|---|---|---|---|---|---|---|---|---|---|---|
| C2 | NC | NC | | | | | | | | |
| C1 | NC | NC | | | | | | | | |
| D2 | NC | NC | | | | | | | | |
| D1 | NC | NC | | | | | | | | |
| E1 | NC | NC | | | | | | | | |

## 8.2 K21 Pinouts

The below figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.

## Table 39. Revision History (continued)

| Rev. No. | Date | Substantial Changes |
|---|---|---|
| 2 | 7/2012 | • Updated section "Power consumption operating behaviors".<br>• Updated section "Flash timing specifications — program and erase".<br>• Updated section "Flash timing specifications — commands".<br>• Removed the 32K ratio from "Write endurance" in section "Reliability specifications".<br>• Updated IDDstby maximum value in section "VREG electrical specifications".<br>• Added the charts in section "Diagram: Typical IDD_RUN operating behavior". |
| 3 | 8/2012 | • Updated section "Power consumption operating behaviors".<br>• Updated section "EMC radiated emissions operating behaviors".<br>• Updated section "MCG specifications".<br>• Added applicable notes in section "Signal Multiplexing and Pin Assignments". |
| 4 | 8/2013 | • Updated section "Power consumption operating behaviors"<br>• Updated section "MCG specifications"<br>• Updated section "16-bit ADC operating conditions"<br>• Added section "Small package marking" |