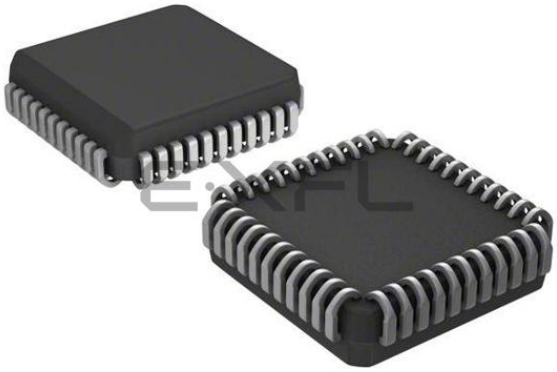


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	80C51
Core Size	8-Bit
Speed	60MHz
Connectivity	SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	34
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.6x16.6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at89c51rd2-slrum

1. Description

AT89C51RD2/ED2 is high performance CMOS Flash version of the 80C51 CMOS single chip 8-bit microcontroller. It contains a 64-Kbyte Flash memory block for code and for data.

The 64-Kbytes Flash memory can be programmed either in parallel mode or in serial mode with the ISP capability or with software. The programming voltage is internally generated from the standard V_{CC} pin.

The AT89C51RD2/ED2 retains all of the features of the Atmel 80C52 with 256 bytes of internal RAM, a 9-source 4-level interrupt controller and three timer/counters. The AT89C51ED2 provides 2048 bytes of EEPROM for nonvolatile data storage.

In addition, the AT89C51RD2/ED2 has a Programmable Counter Array, an XRAM of 1792 bytes, a Hardware Watchdog Timer, SPI interface, Keyboard, a more versatile serial channel that facilitates multiprocessor communication (EUART) and a speed improvement mechanism (X2 Mode).

The fully static design of the AT89C51RD2/ED2 allows to reduce system power consumption by bringing the clock frequency down to any value, including DC, without loss of data.

The AT89C51RD2/ED2 has 2 software-selectable modes of reduced activity and an 8-bit clock prescaler for further reduction in power consumption. In the Idle mode the CPU is frozen while the peripherals and the interrupt system are still operating. In the Power-down mode the RAM is saved and all other functions are inoperative.

The added features of the AT89C51RD2/ED2 make it more powerful for applications that need pulse width modulation, high speed I/O and counting capabilities such as alarms, motor control, corded phones, and smart card readers.

Table 1-1. Memory Size and I/O Pins

Package	Flash (Bytes)	XRAM (Bytes)	Total RAM (Bytes)	I/O
PLCC44/VQFP44	64K	1792	2048	34
PLCC68/VQFP64	64K	1792	2048	50

8. Dual Data Pointer Register (DPTR)

The additional data pointer can be used to speed up code execution and reduce code size.

The dual DPTR structure is a way by which the chip will specify the address of an external data memory location. There are two 16-bit DPTR registers that address the external memory, and a single bit called DPS = AUXR1.0 (see Table 8-1) that allows the program code to switch between them (Refer to Figure 8-1).

Figure 8-1. Use of Dual Pointer

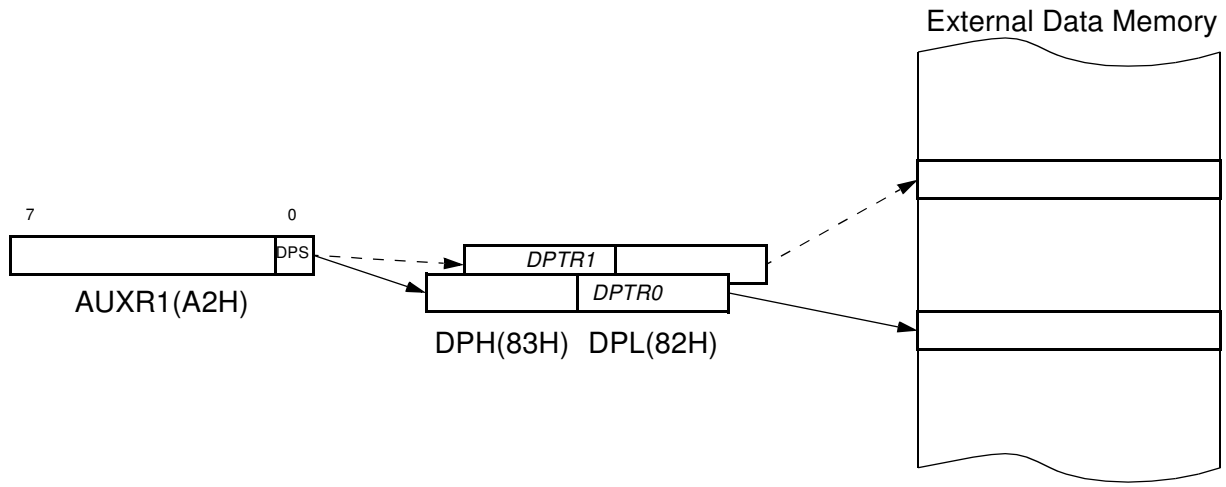


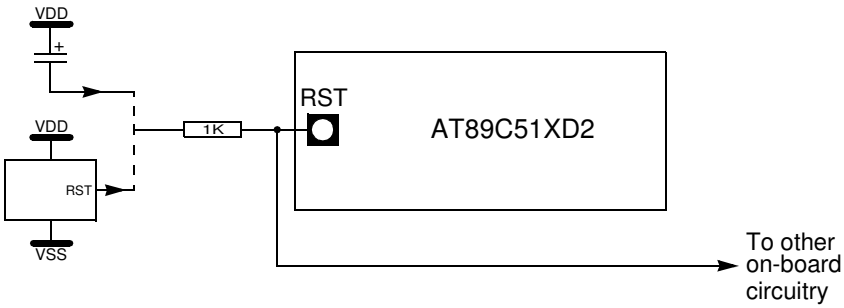
Table 8-1. AUXR1 Register

AUXR1- Auxiliary Register 1(0A2h)

7	6	5	4	3	2	1	0
-	-	ENBOOT	-	GF3	0	-	DPS

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	ENBOOT	**Enable Boot Flash** Cleared to disable boot ROM. Set to map the boot ROM between F800h - 0FFFFh.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	GF3	This bit is a general-purpose user flag.(1)
2	0	Always cleared
1	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
0	DPS	**Data Pointer Selection** Cleared to select DPTR0. Set to select DPTR1.

Figure 10-3. Recommended Reset Output Schematic



11. Power Monitor

The POR/PFD function monitors the internal power-supply of the CPU core memories and the peripherals, and if needed, suspends their activity when the internal power supply falls below a safety threshold. This is achieved by applying an internal reset to them.

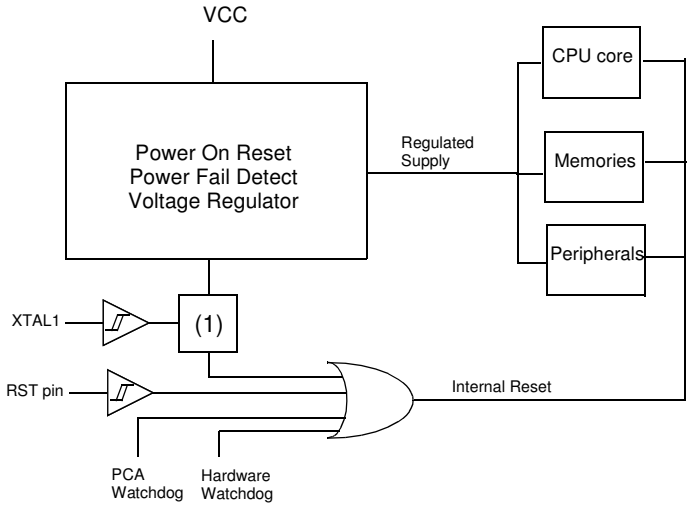
By generating the Reset the Power Monitor insures a correct start up when AT89C51RD2/ED2 is powered up.

11.1 Description

In order to startup and maintain the microcontroller in correct operating mode, V_{CC} has to be stabilized in the V_{CC} operating range and the oscillator has to be stabilized with a nominal amplitude compatible with logic level VIH/VIL.

These parameters are controlled during the three phases: power-up, normal operation and power going down. See Figure 11-1.

Figure 11-1. Power Monitor Block Diagram



Note: 1. Once XTAL1 High and low levels reach above and below VIH/VIL. a 1024 clock period delay will extend the reset coming from the Power Fail Detect. If the power falls below the Power Fail Detect threshold level, the Reset will be applied immediately.

The Voltage regulator generates a regulated internal supply for the CPU core the memories and the peripherals. Spikes on the external Vcc are smoothed by the voltage regulator.

The Power fail detect monitor the supply generated by the voltage regulator and generate a reset if this supply falls below a safety threshold as illustrated in the Figure 11-2 below.

Table 13-1. CMOD Register

CMOD - PCA Counter Mode Register (D9h)

7	6	5	4	3	2	1	0
CIDL	**WDTE**	**-**	**-**	**-**	**CPS1**	**CPS0**	**ECF**

Bit Number	Bit Mnemonic	Description
7	CIDL	**Counter Idle Control** Cleared to program the PCA Counter to continue functioning during idle Mode. Set to program PCA to be gated off during idle.
6	WDTE	**Watchdog Timer Enable** Cleared to disable Watchdog Timer function on PCA Module 4. Set to enable Watchdog Timer function on PCA Module 4.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	CPS1	**PCA Count Pulse Select** CPS1 CPS0 Selected PCA input 0 0 Internal clock $F_{CLK\ PERIPH}/6$ 0 1 Internal clock $F_{CLK\ PERIPH}/2$ 1 0 Timer 0 Overflow 1 1 External clock at ECI/P1.2 pin (max rate = $F_{CLK\ PERIPH}/4$)
1	CPS0	
0	ECF	**PCA Enable Counter Overflow Interrupt** Cleared to disable CF bit in CCON to inhibit an interrupt. Set to enable CF bit in CCON to generate an interrupt.

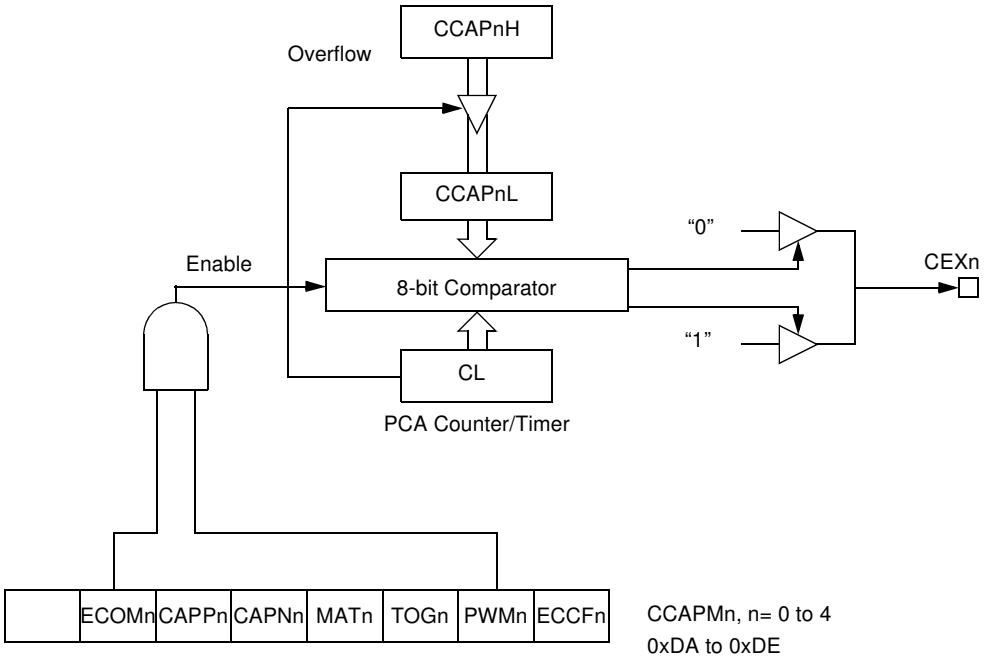
Reset Value = 00XX X000b

Not bit addressable

The CCON register contains the run control bit for the PCA and the flags for the PCA timer (CF) and each module (Refer to Table 13-2).

- Bit CR (CCON.6) must be set by software to run the PCA. The PCA is shut off by clearing this bit.
- Bit CF: The CF bit (CCON.7) is set when the PCA counter overflows and an interrupt will be generated if the ECF bit in the CMOD register is set. The CF bit can only be cleared by software.
- Bits 0 through 4 are the flags for the modules (bit 0 for module 0, bit 1 for module 1, etc.) and are set by hardware when either a match or a capture occurs. These flags also can only be cleared by software.

Figure 13-6. PCA PWM Mode



13.5 PCA Watchdog Timer

An on-board watchdog timer is available with the PCA to improve the reliability of the system without increasing chip count. Watchdog timers are useful for systems that are susceptible to noise, power glitches, or electrostatic discharge. Module 4 is the only PCA module that can be programmed as a watchdog. However, this module can still be used for other modes if the watchdog is not needed. Figure 13-4 shows a diagram of how the watchdog works. The user pre-loads a 16-bit value in the compare registers. Just like the other compare modes, this 16-bit value is compared to the PCA timer value. If a match is allowed to occur, an internal reset will be generated. This will not cause the RST pin to be driven high.

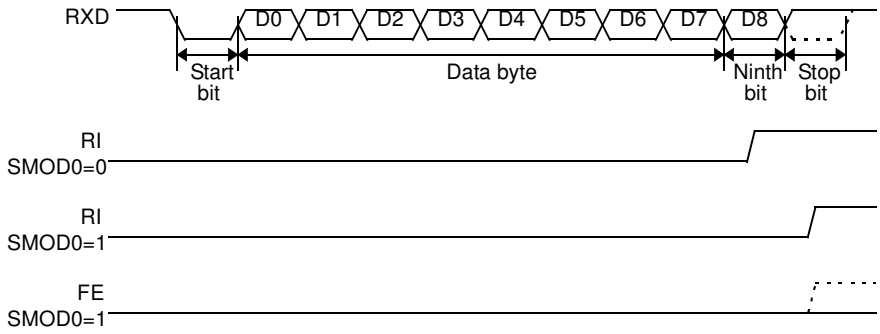
In order to hold off the reset, the user has three options:

1. Periodically change the compare value so it will never match the PCA timer.
2. Periodically change the PCA timer value so it will never match the compare values.
3. Disable the watchdog by clearing the WDTE bit before a match occurs and then re-enable it.

The first two options are more reliable because the watchdog timer is never disabled as in option #3. If the program counter ever goes astray, a match will eventually occur and cause an internal reset. The second option is also not recommended if other PCA modules are being used. Remember, the PCA timer is the time base for all modules; changing the time base for other modules would not be a good idea. Thus, in most applications the first solution is the best option.

This watchdog timer won't generate a reset out on the reset pin.

Figure 14-3. UART Timings in Modes 2 and 3



14.2 Automatic Address Recognition

The automatic address recognition feature is enabled when the multiprocessor communication feature is enabled (SM2 bit in SCON register is set).

Implemented in hardware, automatic address recognition enhances the multiprocessor communication feature by allowing the serial port to examine the address of each incoming command frame. Only when the serial port recognizes its own address, the receiver sets RI bit in SCON register to generate an interrupt. This ensures that the CPU is not interrupted by command frames addressed to other devices.

If desired, the user may enable the automatic address recognition feature in mode 1.In this configuration, the stop bit takes the place of the ninth data bit. Bit RI is set only when the received command frame address matches the device's address and is terminated by a valid stop bit.

To support automatic address recognition, a device is identified by a given address and a broadcast address.

Note: The multiprocessor communication and automatic address recognition features cannot be enabled in mode 0 (i. e. setting SM2 bit in SCON register in mode 0 has no effect).

14.2.1 Given Address

Each device has an individual address that is specified in SADDR register; the SADEN register is a mask byte that contains don't-care bits (defined by zeros) to form the device's given address. The don't-care bits provide the flexibility to address one or more slaves at a time. The following example illustrates how a given address is formed.

To address a device by its individual address, the SADEN mask byte must be `1111 1111b`.

For example:

```
SADDR0101 0110b
SADEN1111 1100b
Given0101 01XXb
```

The following is an example of how to use given addresses to address different slaves:

```
Slave A:SADDR1111 0001b
   SADEN1111 1010b
   Given1111 0X0Xb


Slave B:SADDR1111 0011b
   SADEN1111 1001b
   Given1111 0XX1b
```

Table 17-3. IENO Register

IEN0 - Interrupt Enable Register (A8h)

7	6	5	4	3	2	1	0
EA	**EC**	**ET2**	**ES**	**ET1**	**EX1**	**ET0**	**EX0**

Bit Number	Bit Mnemonic	Description
7	EA	**Enable All interrupt bit** Cleared to disable all interrupts. Set to enable all interrupts.
6	EC	**PCA interrupt enable bit** Cleared to disable. Set to enable.
5	ET2	**Timer 2 overflow interrupt Enable bit** Cleared to disable timer 2 overflow interrupt. Set to enable timer 2 overflow interrupt.
4	ES	**Serial port Enable bit** Cleared to disable serial port interrupt. Set to enable serial port interrupt.
3	ET1	**Timer 1 overflow interrupt Enable bit** Cleared to disable timer 1 overflow interrupt. Set to enable timer 1 overflow interrupt.
2	EX1	**External interrupt 1 Enable bit** Cleared to disable external interrupt 1. Set to enable external interrupt 1.
1	ET0	**Timer 0 overflow interrupt Enable bit** Cleared to disable timer 0 overflow interrupt. Set to enable timer 0 overflow interrupt.
0	EX0	**External interrupt 0 Enable bit** Cleared to disable external interrupt 0. Set to enable external interrupt 0.

Reset Value = 0000 0000b

Bit addressable

20. ONCE® Mode (ON- Chip Emulation)

The ONCE mode facilitates testing and debugging of systems using AT89C51RD2/ED2 without removing the circuit from the board. The ONCE mode is invoked by driving certain pins of the AT89C51RD2/ED2; the following sequence must be exercised:

- Pull ALE low while the device is in reset (RST high) and $\overline{\text{PSEN}}$ is high.
- Hold ALE low as RST is deactivated.

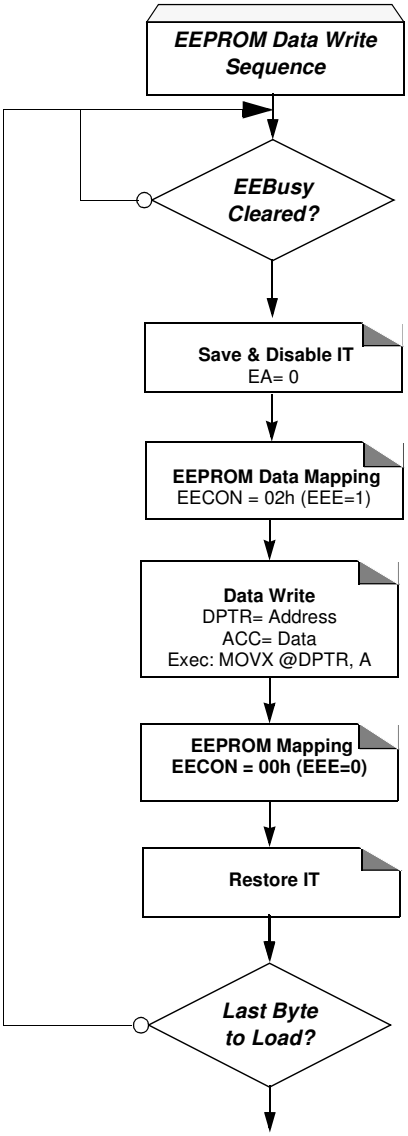
While the AT89C51RD2/ED2 is in ONCE mode, an emulator or test CPU can be used to drive the circuit. Table 20-1 shows the status of the port pins during ONCE mode.

Normal operation is restored when normal reset is applied.

Table 20-1. External Pin Status During ONCE Mode

ALE	PSEN	Port 0	Port 1	Port 2	Port 3	Port I2	XTALA1/2	XTALB1/2
Weak pull-up	Weak pull-up	Float	Weak pull-up	Weak pull-up	Weak pull-up	Float	Active	Active

Figure 23-1. Recommended EEPROM Data Write Sequence



23.2 Read Data

The following procedure is used to read the data stored in the EEPROM memory:

- Check EEBUSY flag
- If the user application interrupts routines use XRAM memory space: Save and disable interrupts.
- Load DPTR with the address to read
- Set bit EEE of EECON register
- Execute a MOVX A, @DPTR
- Clear bit EEE of EECON register
- Restore interrupts.

24. Flash/EEPROM Memory

The Flash memory increases EEPROM and ROM functionality with in-circuit electrical erasure and programming. It contains 64K bytes of program memory organized respectively in 512 pages of 128 bytes. This memory is both parallel and serial In-System Programmable (ISP). ISP allows devices to alter their own program memory in the actual end product under software control. A default serial loader (bootloader) program allows ISP of the Flash.

The programming **does not require** external dedicated programming voltage. The necessary high programming voltage is generated on-chip using the standard V_{CC} pins of the microcontroller.

24.1 Features

- Flash EEPROM Internal Program Memory
- Boot vector allows user provided Flash loader code to reside anywhere in the Flash memory space. This configuration provides flexibility to the user.
- Default loader in Boot ROM allows programming via the serial port without the need of a user provided loader.
- Up to 64K bytes external program memory if the internal program memory is disabled (EA = 0).
- Programming and erasing voltage with standard power supply
- Read/Programming/Erase:
  - Byte-wise read without wait state
  - Byte or page erase and programming (10 ms)
- Typical programming time (64K bytes) is 22s with on chip serial bootloader
- Parallel programming with 87C51 compatible hardware interface to programmer
- Programmable security for the code in the Flash
- 100K write cycles
- 10 years data retention

24.2 Flash Programming and Erasure

The 64-K byte Flash is programmed by bytes or by pages of 128 bytes. It is not necessary to erase a byte or a page before programming. The programming of a byte or a page includes a self erase before programming.

There are three methods of programming the Flash memory:

1. The on-chip ISP bootloader may be invoked which will use low level routines to program the pages. The interface used for serial downloading of Flash is the UART.
2. The Flash may be programmed or erased in the end-user application by calling low-level routines through a common entry point in the Boot ROM.
3. The Flash may be programmed using the parallel method by using a conventional EPROM programmer. The parallel programming method used by these devices is similar to that used by EPROM 87C51 but it is not identical and the commercially available programmers need to have support for the AT89C51RD2/ED2. The bootloader and the Application Programming Interface (API) routines are located in the BOOT ROM.

Mnemonic	Definition	Default value	Description
BSB	Boot Status Byte	0FFh	
SSB	Software Security Byte	FFh	
	Copy of the Manufacturer Code	58h	Atmel
	Copy of the Device ID #1: Family Code	D7h	C51 X2, Electrically Erasable
	Copy of the Device ID #2: Memories Size and Type	ECh	AT89C51RD2/ED2 64KB
	Copy of the Device ID #3: Name and Revision	EFh	AT89C51RD2/ED2 64KB, Revision 0

After programming the part by ISP, the BSB must be cleared (00h) in order to allow the application to boot at 0000h.

The content of the Software Security Byte (SSB) is described in Table 24-4 and Table 24-5.

To assure code protection from a parallel access, the HSB must also be at the required level.

Table 24-4. Software Security Byte

7	6	5	4	3	2	1	0
-	-	-	-	-	-	LB1	LB0

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** Do not clear this bit.
6	-	**Reserved** Do not clear this bit.
5	-	**Reserved** Do not clear this bit.
4	-	**Reserved** Do not clear this bit.
3	-	**Reserved** Do not clear this bit.
2	-	**Reserved** Do not clear this bit.
1-0	LB1-0	User Memory Lock Bits See Table 24-5

The two lock bits provide different levels of protection for the on-chip code and data, when programmed as shown in Table 24-5.

Table 24-5. User Memory Lock Bits of the SSB

Program Lock Bits			
Security Level	**LB0**	**LB1**	**Protection Description**
1	1	1	No program lock features enabled.
2	0	1	ISP programming of the Flash is disabled.
3	X	0	Same as 2, also verify through ISP programming interface is disabled.

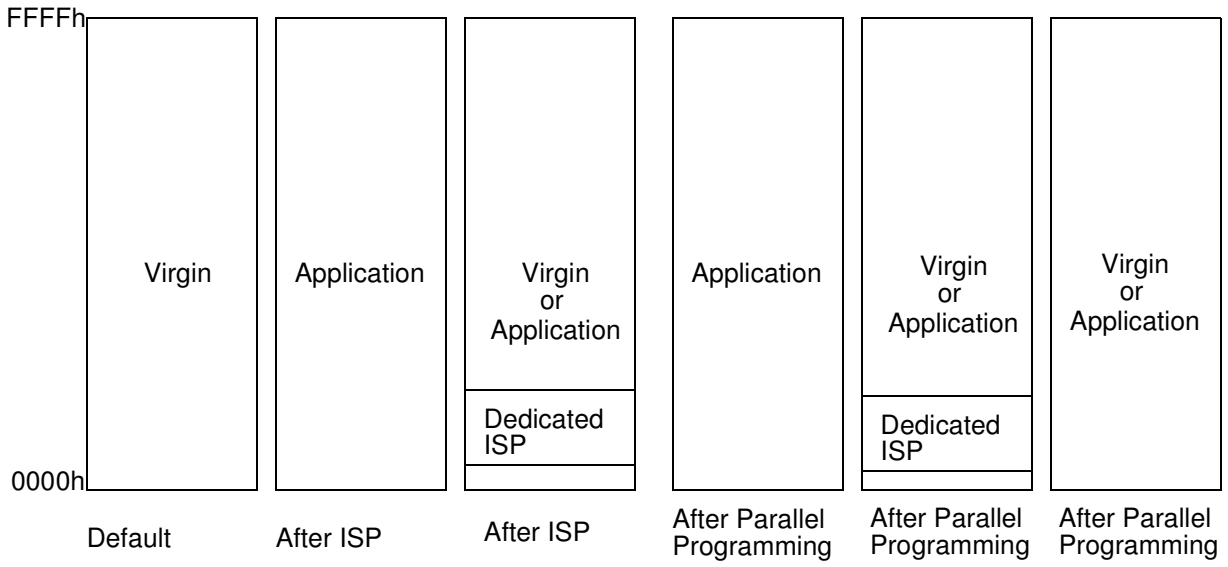
Note: X: Do not care
WARNING: Security level 2 and 3 should only be programmed after Flash verification.

24.4 Flash Memory Status

AT89C51RD2/ED2 parts are delivered in standard with the ISP ROM bootloader.

After ISP or parallel programming, the possible contents of the Flash memory are summarized in Figure 24-1:

Figure 24-1. Flash Memory Possible Contents



24.5 Memory Organization

When the $\overline{EA}$ pin is high, the processor fetches instructions from internal program Flash. If the $\overline{EA}$ pin is tied low, all program memory fetches are from external memory.

24.6 Bootloader Architecture

24.6.1 Introduction

The bootloader manages communication according to a specifically defined protocol to provide the whole access and service on Flash memory. Furthermore, all accesses and routines can be called from the user application.

- SBV = FCh
- SSB = FFh

The Full Chip Erase does not affect the bootloader.

24.8.3 Checksum Error

When a checksum error is detected, send ‘X’ followed with CR&LF.

24.9 Flow Description

24.9.1 Overview

An initialization step must be performed after each Reset. After microcontroller reset, the bootloader waits for an autobaud sequence (see section ‘Autobaud Performances’).

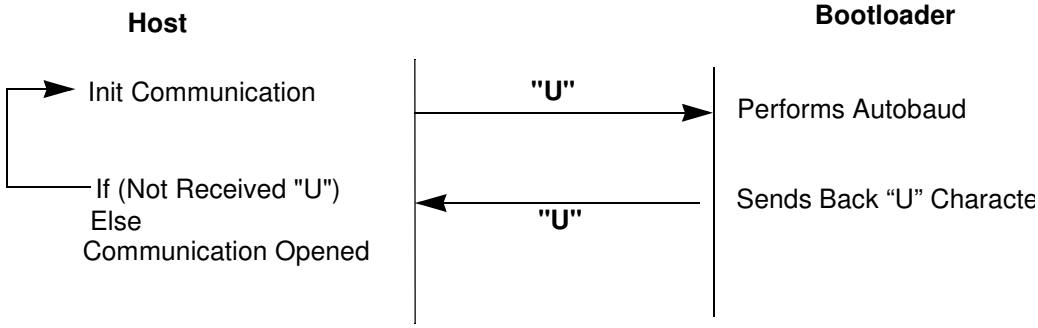
When the communication is initialized, the protocol depends on the record type requested by the host.

FLIP, a software utility to implement ISP programming with a PC, is available from the Atmel web site.

24.9.2 Communication Initialization

The host initializes the communication by sending a ’U’ character to help the bootloader to compute the baudrate (autobaud).

Figure 24-7. Initialization



24.9.3 Autobaud Performances

The ISP feature allows a wide range of baud rates in the user application. It is also adaptable to a wide range of oscillator frequencies. This is accomplished by measuring the bit-time of a single bit in a received character. This information is then used to program the baud rate in terms of timer counts based on the oscillator frequency. The ISP feature requires that an initial character (an uppercase U) be sent to the AT89C51RD2/ED2 to establish the baud rate. Table show the autobaud capability.

Table 24-8. Autobaud Performances

Frequency (MHz) / Baudrate (kHz)	1.8432	2	2.4576	3	3.6864	4	5	6	7.3728
2400	OK	OK	OK	OK	OK	OK	OK	OK	OK

24.9.5 Write/Program Commands Description

This flow is common to the following frames:

- Flash/EEPROM Programming Data Frame
- EOF or Atmel Frame (only Programming Atmel Frame)
- Config Byte Programming Data Frame
- Baud Rate Frame

Figure 24-9. Write/Program Flow

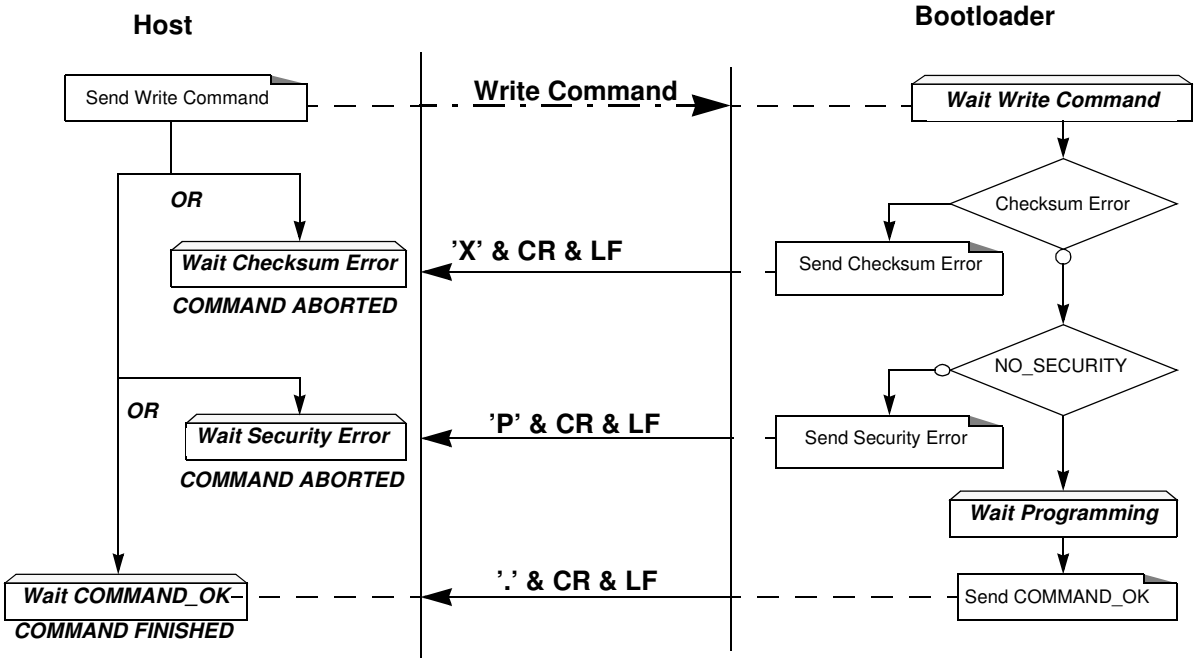
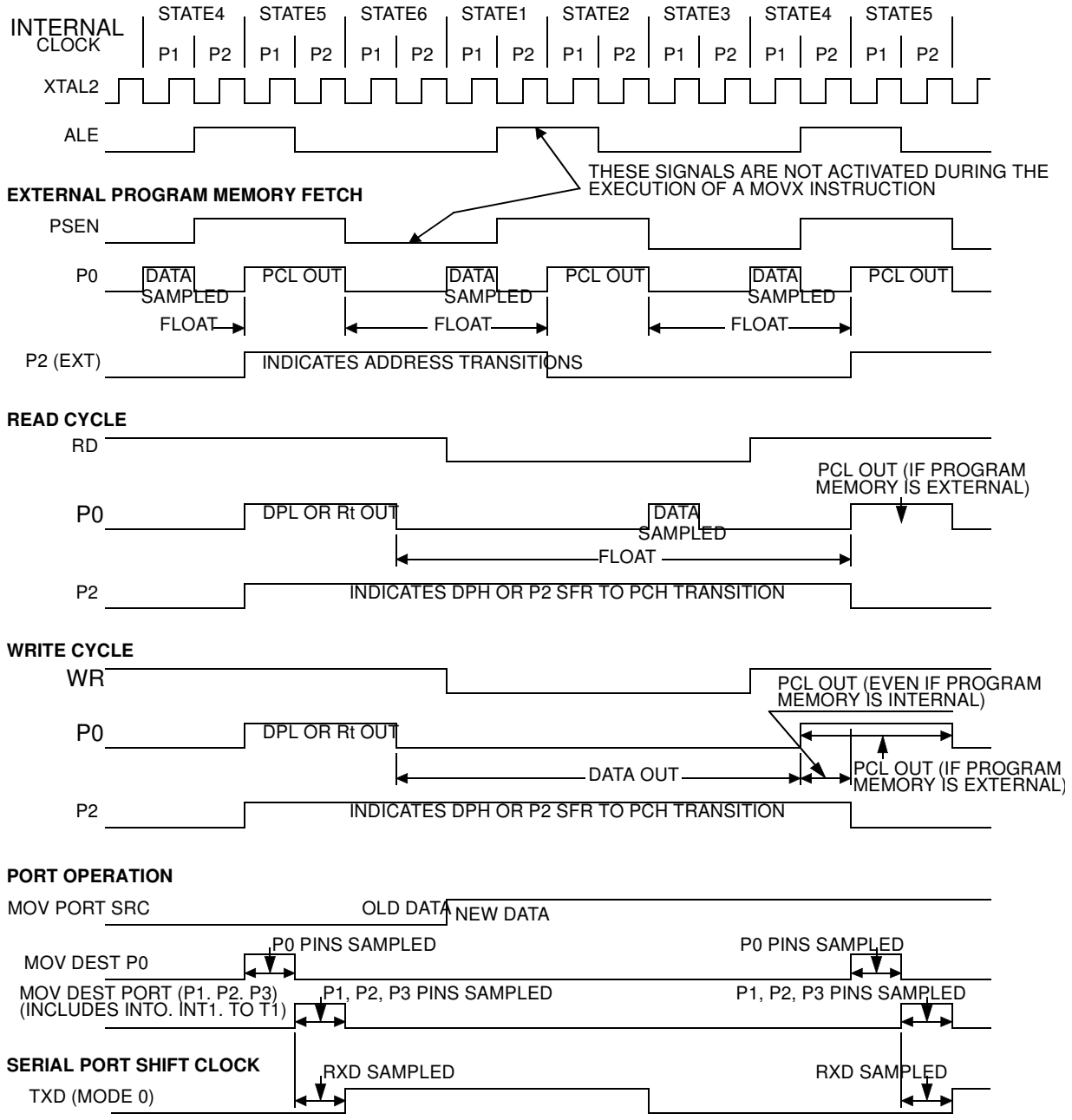


Figure 25-5. Internal Clock Signals



This diagram indicates when signals are clocked internally. The time it takes the signals to propagate to the pins, however, ranges from 25 to 125 ns. This propagation delay is dependent on variables such as temperature and pin loading. Propagation also varies from output to output and component. Typically though (T_A = 25°C fully loaded) $\overline{RD}$ and $\overline{WR}$ propagation delays are approximately 50 ns. The other signals are typically 85 ns. Propagation delays are incorporated in the AC specifications.

STANDARD NOTES FOR PQFP/ VQFP / TQFP / DQFP

1/ CONTROLLING DIMENSIONS : INCHES

2/ ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y 14.5M - 1982.

3/ "D1 AND E1" DIMENSIONS DO NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 mm (0.010 INCH). THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE BODY SIZE BY AS MUCH AS 0.15 mm.

4/ DATUM PLANE "H" LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.

5/ DATUM "A" AND "D" TO BE DETERMINED AT DATUM PLANE H.

6/ DIMENSION " f " DOES NOT INCLUDE DAMBAR PROTUSION ALLOWABLE DAMBAR PROTUSION SHALL BE 0.08mm/.003" TOTAL IN EXCESS OF THE " f " DIMENSION AT MAXIMUM MATERIAL CONDITION . DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

Headquarters

Atmel Corporation
2325 Orchard Parkway
San Jose, CA 95131
USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

International

Atmel Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Atmel Europe
Le Krebs
8, Rue Jean-Pierre Timbaud
BP 309
78054 Saint-Quentin-en-
Yvelines Cedex
France
Tel: (33) 1-30-60-70-00
Fax: (33) 1-30-60-71-11

Atmel Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Product Contact

Web Site
www.atmel.com

Technical Support
Enter Product Line E-mail

Sales Contact
www.atmel.com/contacts

Literature Requests
www.atmel.com/literature

4235K–8051–05/08