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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800
Core Size	16-Bit
Speed	80MHz
Connectivity	CANbus, EBI/EMI, SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	16
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/dsp56f803bu80e

Table 1. 56F803 Ordering Information

Part	Supply Voltage	Package Type	Pin Count	Ambient Frequency (MHz)	Order Number
56F803	3.0–3.6 V	Low Profile Plastic Quad Flat Pack (LQFP)	100	80	DSP56F803BU80E[1]

1 This package is RoHS compliant

Document Revision History

Version History	Description of Change
Rev. 16	Added revision history. Added this text to footnote 2 in **Table 3-8**: “However, the high pulse width does not have to be any particular percent of the low pulse width.”

- Four General Purpose Quad Timers: Timer A (sharing pins with Quad Dec0), Timers B &C without external pins and Timer D with two pins
- CAN 2.0 B module with 2-pin ports for transmit and receive
- Serial Communication Interface (SCI) with two pins (or two additional GPIO lines)
- Serial Peripheral Interface (SPI) with configurable 4-pin port (or four additional GPIO lines)
- Computer Operating Properly (COP) Watchdog timer
- Two dedicated external interrupt pins
- Sixteen multiplexed General Purpose I/O (GPIO) pins
- External reset input pin for hardware reset
- JTAG/On-Chip Emulation (OnCE™) for unobtrusive, processor speed-independent debugging
- Software-programmable, Phase Locked Loop-based frequency synthesizer for the controller core clock

1.1.4 Energy Information

- Fabricated in high-density CMOS with 5V-tolerant, TTL-compatible digital inputs
- Uses a single 3.3V power supply
- On-chip regulators for digital and analog circuitry to lower cost and reduce noise
- Wait and Stop modes available

1.2 56F803 Description

The 56F803 is a member of the 56800 core-based family of processors. It combines, on a single chip, the processing power of a DSP and the functionality of a microcontroller with a flexible set of peripherals to create an extremely cost-effective solution. Because of its low cost, configuration flexibility, and compact program code, the 56F803 is well-suited for many applications. The 56F803 includes many peripherals that are especially useful for applications such as motion control, smart appliances, steppers, encoders, tachometers, limit switches, power supply and control, automotive control, engine management, noise suppression, remote utility metering, and industrial control for power, lighting, and automation.

The 56800 core is based on a Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The MCU-style programming model and optimized instruction set allow straightforward generation of efficient, compact device and control code. The instruction set is also highly efficient for C compilers to enable rapid development of optimized control applications.

The 56F803 supports program execution from either internal or external memories. Two data operands can be accessed from the on-chip Data RAM per instruction cycle. The 56F803 also provides two external dedicated interrupt lines, and up to 16 General Purpose Input/Output (GPIO) lines, depending on peripheral configuration.

The 56F803 controller includes 31.5K words (16-bit) of Program Flash and 4K words of Data Flash (each programmable through the JTAG port) with 512 words of Program RAM and 2K words of Data RAM. It also supports program execution from external memory.

A total of 2K words of Boot Flash is incorporated for easy customer-inclusion of field-programmable

Part 2 Signal/Connection Descriptions

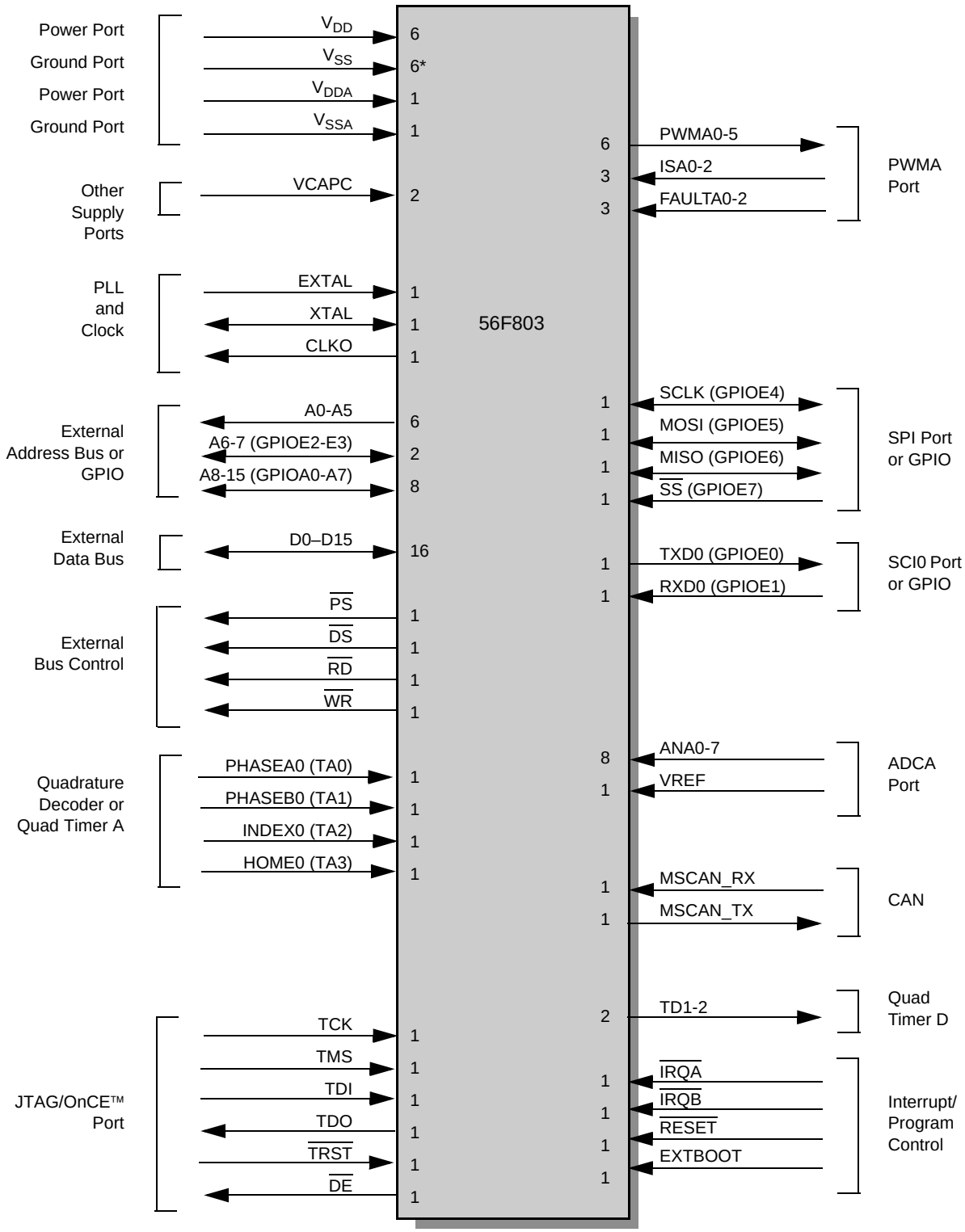
2.1 Introduction

The input and output signals of the 56F803 are organized into functional groups, as shown in **Table 2-1** and as illustrated in **Figure 2-1**. In **Table 2-2** through **Table 2-17**, each table row describes the signal or signals present on a pin.

Table 2-1 Functional Group Pin Allocations

Functional Group	Number of Pins	Detailed Description
Power (V_{DD} or V_{DDA})	7	**Table 2-2**
Ground (V_{SS} or V_{SSA})	7	**Table 2-3**
Supply Capacitors	2	**Table 2-4**
PLL and Clock	3	**Table 2-5**
Address Bus[1]	16	**Table 2-6**
Data Bus	16	**Table 2-7**
Bus Control	4	**Table 2-8**
Interrupt and Program Control	4	**Table 2-9**
Pulse Width Modulator (PWM) Port	12	**Table 2-10**
Serial Peripheral Interface (SPI) Port[1]	4	**Table 2-11**
Quadrature Decoder Port[2]	4	**Table 2-12**
Serial Communications Interface (SCI) Port[1]	2	**Table 2-13**
CAN Port	2	**Table 2-14**
Analog to Digital Converter (ADC) Port	9	**Table 2-15**
Quad Timer Module Port	2	**Table 2-16**
JTAG/On-Chip Emulation (OnCE)	6	**Table 2-17**

1. Alternately, GPIO pins
2. Alternately, Quad Timer pins



*includes TCS pin which is reserved for factory use and is tied to VSS

Figure 2-1 56F803 Signals Identified by Functional Group[1]

1. Alternate pin functionality is shown in parenthesis.

2.3 Clock and Phase Locked Loop Signals

Table 2-5 PLL and Clock

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**EXTAL**	Input	Input	**External Crystal Oscillator Input**—This input should be connected to an 8MHz external crystal or ceramic resonator. For more information, please refer to **Section 3.5**.
1	**XTAL**	Input/ Output	Chip-driven	**Crystal Oscillator Output**—This output should be connected to an 8MHz external crystal or ceramic resonator. For more information, please refer to **Section 3.5**. This pin can also be connected to an external clock source. For more information, please refer to **Section 3.5.3**.
1	**CLKO**	Output	Chip-driven	**Clock Output**—This pin outputs a buffered clock signal. By programming the CLKOSEL[4:0] bits in the CLKO Select Register (CLKOSR), the user can select between outputting a version of the signal applied to XTAL and a version of the device's master clock at the output of the PLL. The clock frequency on this pin can also be disabled by programming the CLKOSEL[4:0] bits in CLKOSR.

2.4 Address, Data, and Bus Control Signals

Table 2-6 Address Bus Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
6	**A0–A5**	Output	Tri-stated	**Address Bus**—A0–A5 specify the address for external Program or Data memory accesses.
2	**A6–A7** **GPIOE2–GPIOE3**	Output Input/Output	Tri-stated Input	**Address Bus**—A6–A7 specify the address for external Program or Data memory accesses. **Port E GPIO**—These two pins are General Purpose I/O (GPIO) pins that can be individually programmed as input or output pins. After reset, the default state is Address Bus.
8	**A8–A15** **GPIOA0–GPIOA7**	Output Input/Output	Tri-stated Input	**Address Bus**—A8–A15 specify the address for external Program or Data memory accesses. **Port A GPIO**—These eight pins are General Purpose I/O (GPIO) pins that can be individually programmed as input or output pins. After reset, the default state is Address Bus.

Table 2-9 Interrupt and Program Control Signals (Continued)

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**RESET**	Input (Schmitt)	Input	**Reset**—This input is a direct hardware reset on the processor. When RESET is asserted low, the controller is initialized and placed in the Reset state. A Schmitt trigger input is used for noise immunity. When the RESET pin is deasserted, the initial chip operating mode is latched from the EXTBOOT pin. The internal reset signal will be deasserted synchronous with the internal clocks, after a fixed number of internal clocks. To ensure a complete hardware reset, RESET and TRST should be asserted together. The only exception occurs in a debugging environment when a hardware device reset is required and it is necessary not to reset the OnCE/JTAG module. In this case, assert RESET, but do not assert TRST.
1	**EXTBOOT**	Input (Schmitt)	Input	**External Boot**—This input is tied to V_{DD} to force device to boot from off-chip memory. Otherwise, it is tied to V_{SS}.

2.6 Pulse Width Modulator (PWM) Signals

Table 2-10 Pulse Width Modulator (PWMA) Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
6	**PWMA0–5**	Output	Tri-stated	**PWMA0–5**— These are six PWMA output pins.
3	**ISA0–2**	Input (Schmitt)	Input	**ISA0–2**— These three input current status pins are used for top/bottom pulse width correction in complementary channel operation for PWMA.
3	**FAULTA0–2**	Input (Schmitt)	Input	**FAULTA0–2**— These three fault input pins are used for disabling selected PWMA outputs in cases where fault conditions originate off-chip.

Absolute maximum ratings given in **Table 3-1** are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond these ratings may affect device reliability or cause permanent damage to the device.

The 56F803 DC/AC electrical specifications are preliminary and are from design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications will be published after complete characterization and device qualifications have been completed.

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Table 3-1 Absolute Maximum Ratings

Characteristic	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	V_{SS} – 0.3	V_{SS} + 4.0	V
All other input voltages, excluding Analog inputs	V_{IN}	V_{SS} – 0.3	V_{SS} + 5.5V	V
Voltage difference V_{DD} to V_{DDA}	ΔV_{DD}	- 0.3	0.3	V
Voltage difference V_{SS} to V_{SSA}	ΔV_{SS}	- 0.3	0.3	V
Analog inputs ANA0-7 and VREF	V_{IN}	V_{SSA}– 0.3	V_{DDA}+ 0.3	V
Analog inputs EXTAL and XTAL	V_{IN}	V_{SSA}– 0.3	V_{SSA}+ 3.0	V
Current drain per pin excluding V_{DD}, V_{SS}, PWM outputs, TCS, V_{PP}, V_{DDA}, V_{SSA}	I	—	10	mA

Table 3-2 Recommended Operating Conditions

Characteristic	Symbol	Min	Typ	Max	Unit
Supply voltage, digital	V_{DD}	3.0	3.3	3.6	V
Supply Voltage, analog	V_{DDA}	3.0	3.3	3.6	V
Voltage difference V_{DD} to V_{DDA}	ΔV_{DD}	-0.1	-	0.1	V

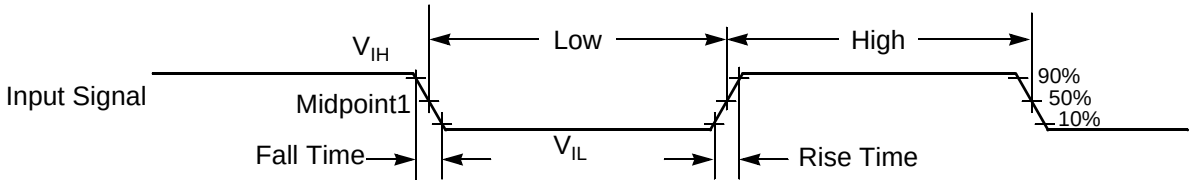
4. Thermal Characterization Parameter, Psi-JT (Ψ_{JT}), is the “resistance” from junction to reference point thermocouple on top center of case as defined in JESD51-2. Ψ_{JT} is a useful value to use to estimate junction temperature in steady state customer environments.
5. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
6. See Section 5.1 from more details on thermal design considerations.
7. TJ = Junction Temperature
   TA = Ambient Temperature

3.2 DC Electrical Characteristic

Table 3-4 DC Electrical Characteristics

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to $+85°C$, $C_L \leq 50$pF, $f_{op} = 80$MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Input high voltage (XTAL/EXTAL)	V_{IHC}	2.25	—	2.75	V
Input low voltage (XTAL/EXTAL)	V_{ILC}	0	—	0.5	V
Input high voltage (Schmitt trigger inputs)[1]	V_{IHS}	2.2	—	5.5	V
Input low voltage (Schmitt trigger inputs)[1]	V_{ILS}	-0.3	—	0.8	V
Input high voltage (all other digital inputs)	V_{IH}	2.0	—	5.5	V
Input low voltage (all other digital inputs)	V_{IL}	-0.3	—	0.8	V
Input current high (pullup/pulldown resistors disabled, $V_{IN}=V_{DD}$)	I_{IH}	-1	—	1	µA
Input current low (pullup/pulldown resistors disabled, $V_{IN}=V_{SS}$)	I_{IL}	-1	—	1	µA
Input current high (with pullup resistor, $V_{IN}=V_{DD}$)	I_{IHPU}	-1	—	1	µA
Input current low (with pullup resistor, $V_{IN}=V_{SS}$)	I_{ILPU}	-210	—	-50	µA
Input current high (with pulldown resistor, $V_{IN}=V_{DD}$)	I_{IHPD}	20	—	180	µA
Input current low (with pulldown resistor, $V_{IN}=V_{SS}$)	I_{ILPD}	-1	—	1	µA
Nominal pullup or pulldown resistor value	R_{PU}, R_{PD}		30		KΩ
Output tri-state current low	I_{OZL}	-10	—	10	µA
Output tri-state current high	I_{OZH}	-10	—	10	µA



Note: The midpoint is $V_{IL} + (V_{IH} - V_{IL})/2$.

Figure 3-2 Input Signal Measurement References

Figure 3-3 shows the definitions of the following signal states:

- Active state, when a bus or signal is driven, and enters a low impedance state
- Tri-stated, when a bus or signal is placed in a high impedance state
- Data Valid state, when a signal level has reached V_{OL} or V_{OH}
- Data Invalid state, when a signal level is in transition between V_{OL} and V_{OH}

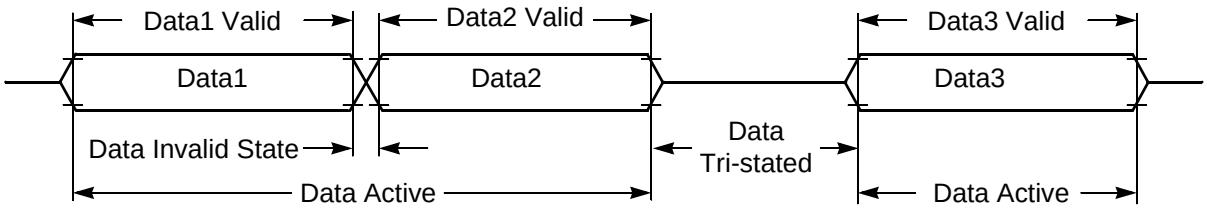


Figure 3-3 Signal States

3.4 Flash Memory Characteristics

Table 3-5 Flash Memory Truth Table

Mode	XE[1]	YE[2]	SE[3]	OE[4]	PROG[5]	ERASE[6]	MAS1[7]	NVSTR[8]
Standby	L	L	L	L	L	L	L	L
Read	H	H	H	H	L	L	L	L
Word Program	H	H	L	L	H	L	L	H
Page Erase	H	L	L	L	L	H	L	H
Mass Erase	H	L	L	L	L	H	H	H

1. X address enable, all rows are disabled when XE = 0
2. Y address enable, YMUX is disabled when YE = 0
3. Sense amplifier enable
4. Output enable, tri-state Flash data out bus when OE = 0

3.5.2 Ceramic Resonator

It is also possible to drive the internal oscillator with a ceramic resonator, assuming the overall system design can tolerate the reduced signal integrity. In **Figure 3-8**, a typical ceramic resonator circuit is shown. Refer to supplier's recommendations when selecting a ceramic resonator and associated components. The resonator and components should be mounted as close as possible to the EXTAL and XTAL pins. The internal 56F80x oscillator circuitry is designed to have no external load capacitors present. As shown in **Figure 3-7** no external load capacitors should be used.

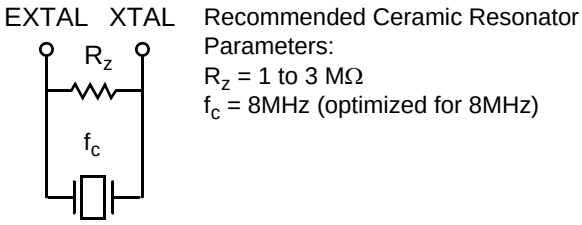


Figure 3-8 Connecting a Ceramic Resonator

Note: Freescale recommends only two terminal ceramic resonators vs. three terminal resonators (which contain an internal bypass capacitor to ground).

3.5.3 External Clock Source

The recommended method of connecting an external clock is given in **Figure 3-9**. The external clock source is connected to XTAL and the EXTAL pin is grounded.

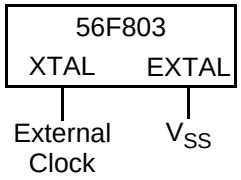


Figure 3-9 Connecting an External Clock Signal

1. Timing is both wait state and frequency dependent. In the formulas listed, WS = the number of wait states and T = Clock Period. For 80MHz operation, T = 12.5ns.

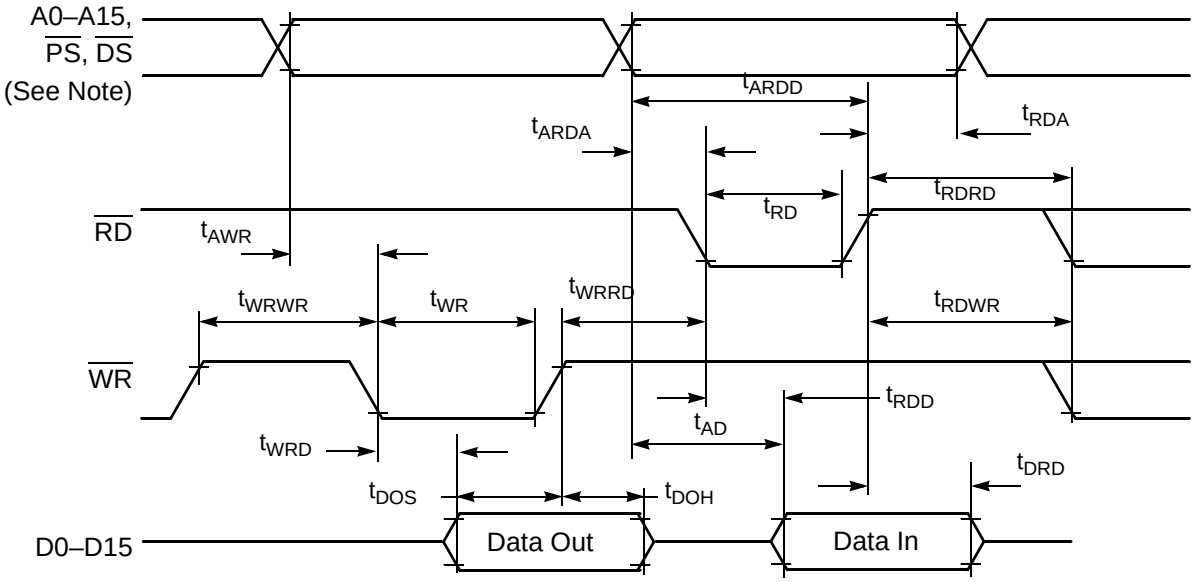
2. Parameters listed are guaranteed by design.

To calculate the required access time for an external memory for any frequency < 80Mhz, use this formula:

Top = Clock period @ desired operating frequency

WS = Number of wait states

Memory Access Time = (Top*WS) + (Top- 11.5)



Note: During read-modify-write instructions and internal instructions, the address lines do not change state.

Figure 3-11 External Bus Asynchronous Timing

3.7 Reset, Stop, Wait, Mode Select, and Interrupt Timing

Table 3-11 Reset, Stop, Wait, Mode Select, and Interrupt Timing [1, 5]

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$V, $T_A = –40°$ to $+85°$C, $C_L \leq 50$pF

Characteristic	Symbol	Min	Max	Unit	See Figure
$\overline{\text{RESET}}$ Assertion to Address, Data and Control Signals High Impedance	t_{RAZ}	—	21	ns	Figure 3-12
Minimum $\overline{\text{RESET}}$ Assertion Duration[2] OMR Bit 6 = 0 OMR Bit 6 = 1	t_{RA}	 275,000T 128T	 — —	 ns ns	Figure 3-12
$\overline{\text{RESET}}$ De-assertion to First External Address Output	t_{RDA}	33T	34T	ns	Figure 3-12

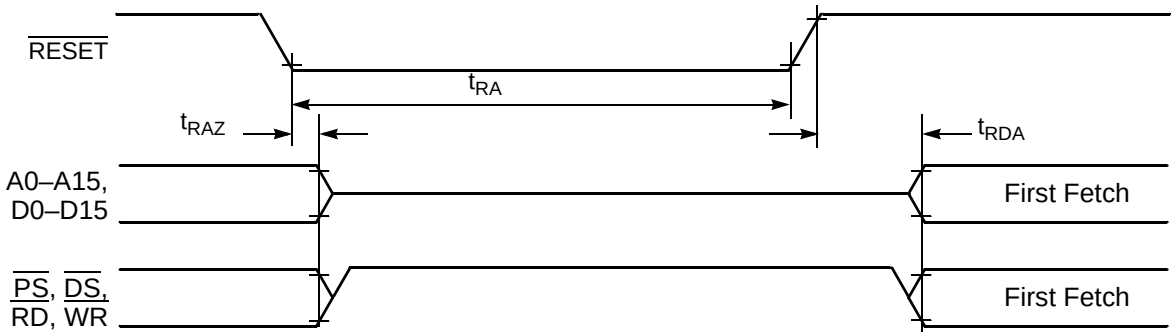


Figure 3-12 Asynchronous Reset Timing

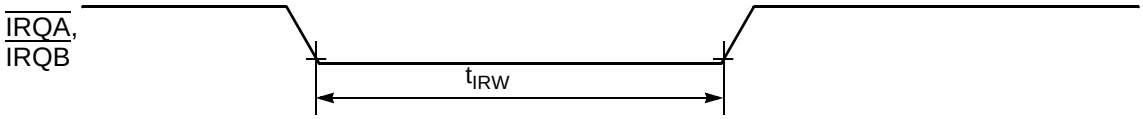


Figure 3-13 External Interrupt Timing (Negative-Edge-Sensitive)

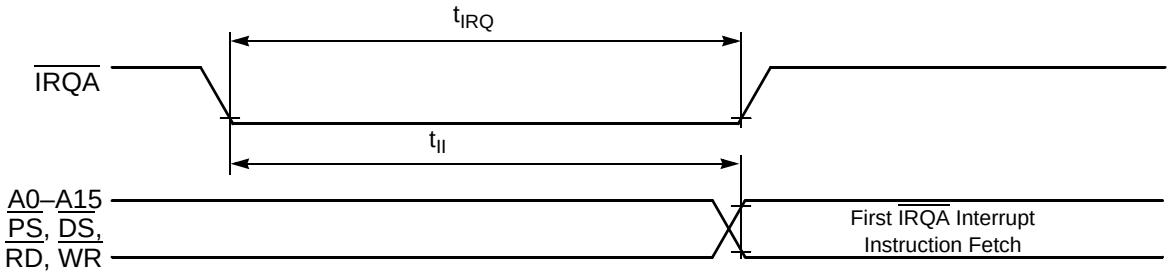


Figure 3-17 Recovery from Stop State Using IRQA Interrupt Service

3.8 Serial Peripheral Interface (SPI) Timing

Table 3-12 SPI Timing[1]

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$V, $T_A = –40°$ to $+85°$C, $C_L \leq 50$pF, $f_{OP} = 80$MHz

Characteristic	Symbol	Min	Max	Unit	See Figure
Cycle time Master Slave	t_C	 50 25	 — —	 ns ns	Figures **3-18**, , **3-20**, **3-21**
Enable lead time Master Slave	t_{ELD}	 — 25	 — —	 ns ns	Figure **3-21**
Enable lag time Master Slave	t_{ELG}	 — 100	 — —	 ns ns	Figure **3-21**
Clock (SCLK) high time Master Slave	t_{CH}	 17.6 12.5	 — —	ns ns	Figures **3-18**, , **3-20**, **3-21**
Clock (SCLK) low time Master Slave	t_{CL}	 24.1 25	 — —	 ns ns	Figures **3-18**, , **3-20**, **3-21**
Data set-up time required for inputs Master Slave	t_{DS}	 20 0	 — —	 ns ns	Figures **3-18**, , **3-20**, **3-21**
Data hold time required for inputs Master Slave	t_{DH}	 0 2	 — —	 ns ns	Figures **3-18**, , **3-20**, **3-21**
Access time (time to data active from high-impedance state) Slave	t_A	4.8	15	ns	Figure **3-21**
Disable time (hold time to high-impedance state) Slave	t_D	3.7	15.2	ns	Figure **3-21**

Table 3-12 SPI Timing[1]

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$V, $T_A = –40°$ to $+85°$C, $C_L \leq 50$pF, $f_{OP} = 80$MHz

Characteristic	Symbol	Min	Max	Unit	See Figure
Data Valid for outputs Master Slave (after enable edge)	t_{DV}	 — —	 4.5 20.4	 ns ns	Figures **3-18**, , **3-20**, **3-21**
Data invalid Master Slave	t_{DI}	 0 0	 — —	 ns ns	Figures **3-18**, , **3-20**, **3-21**
Rise time Master Slave	t_R	 — —	 11.5 10.0	 ns ns	Figures **3-18**, , **3-20**, **3-21**
Fall time Master Slave	t_F	 — —	 9.7 9.0	 ns ns	Figures **3-18**, , **3-20**, **3-21**

1. Parameters listed are guaranteed by design.

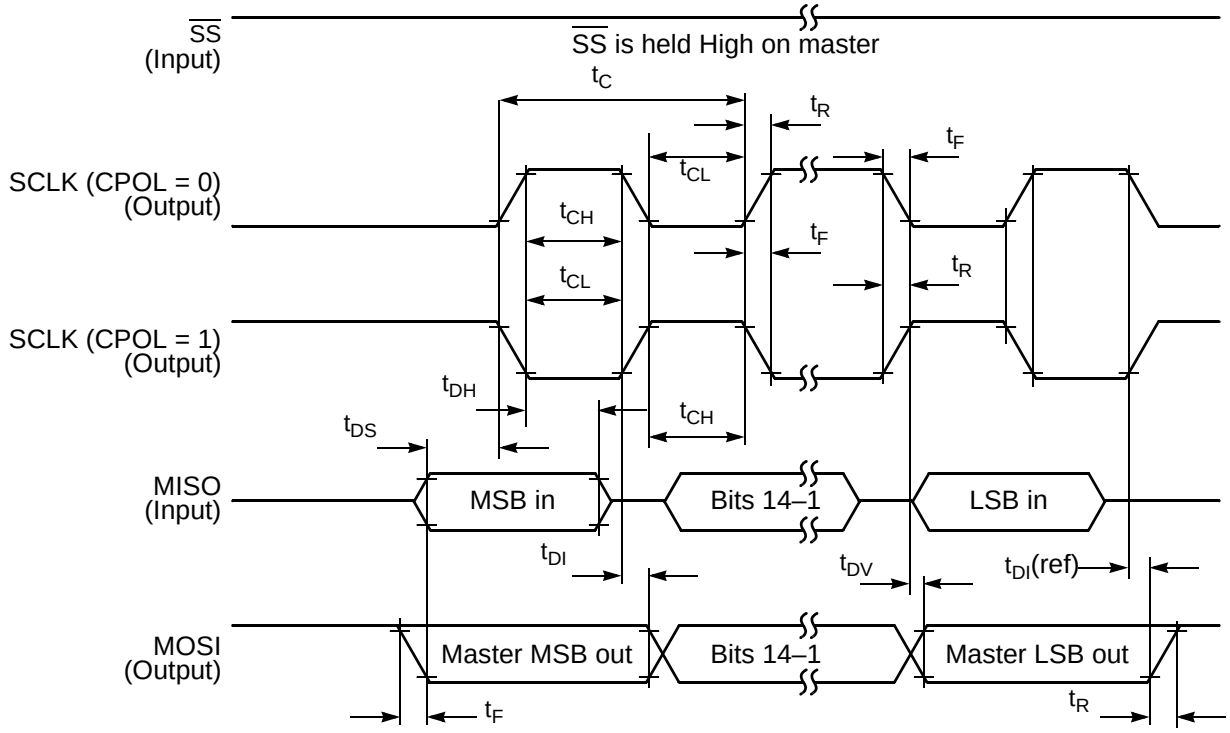


Figure 3-18 SPI Master Timing (CPHA = 0)

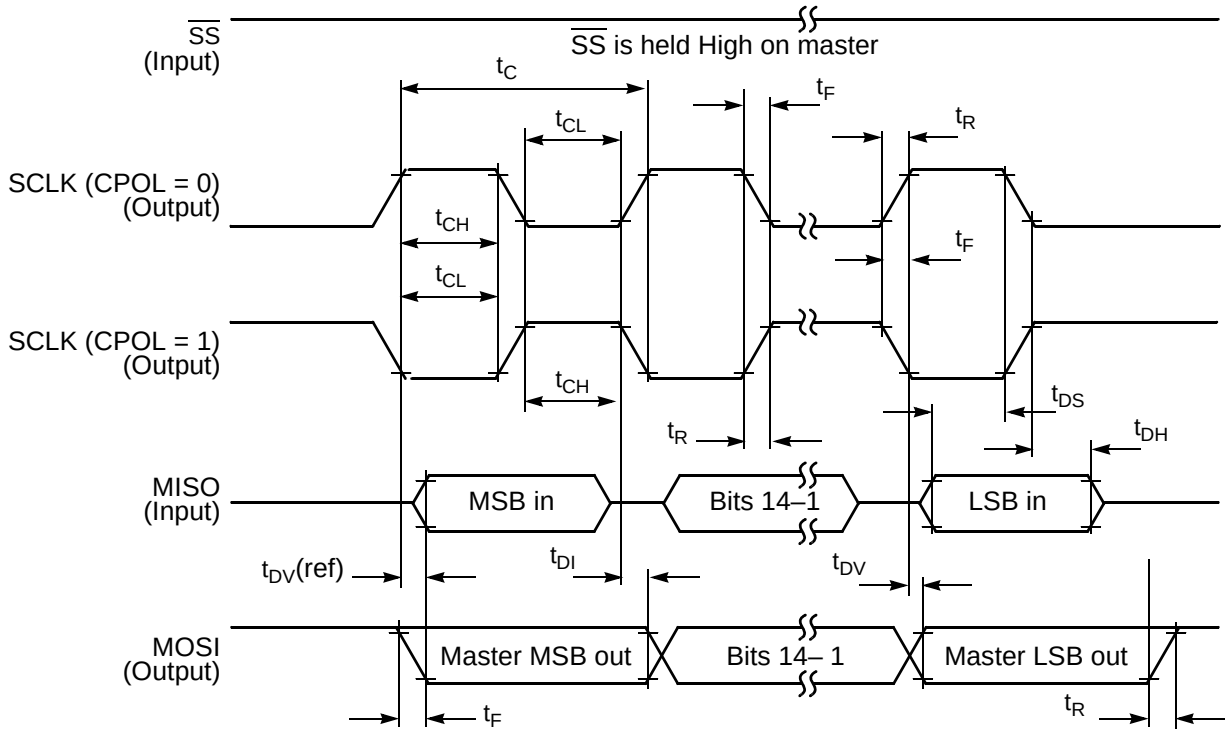


Figure 3-19 SPI Master Timing (CPHA = 1)

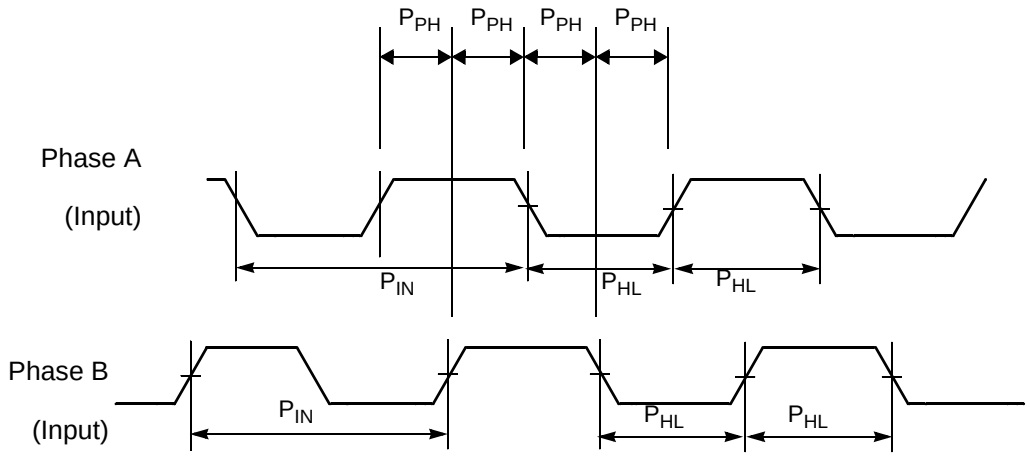


Figure 3-23 Quadrature Decoder Timing

3.11 Serial Communication Interface (SCI) Timing

Table 3-15 SCI Timing[4]

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to $+85°C$, $C_L \leq 50$pF, $f_{OP} = 80$MHz

Characteristic	Symbol	Min	Max	Unit
Baud Rate[1]	BR	—	$(f_{MAX}*2.5)/(80)$	Mbps
RXD[2] Pulse Width	RXD_{PW}	0.965/BR	1.04/BR	ns
TXD[3] Pulse Width	TXD_{PW}	0.965/BR	1.04/BR	ns

1. f_{MAX} is the frequency of operation of the system clock in MHz.
2. The RXD pin in SCI0 is named RXD0 and the RXD pin in SCI1 is named RXD1.
3. The TXD pin in SCI0 is named TXD0 and the TXD pin in SCI1 is named TXD1.
4. Parameters listed are guaranteed by design.

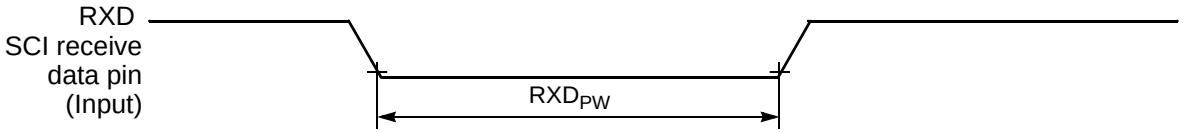


Figure 3-24 RXD Pulse Width

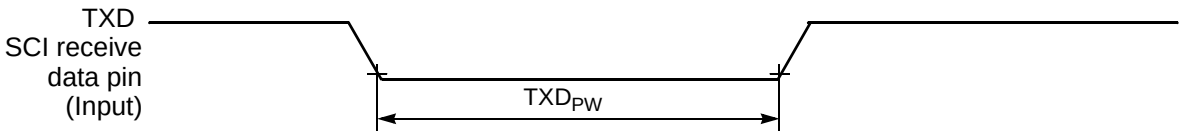


Figure 3-25 TXD Pulse Width

3.12 Analog-to-Digital Converter (ADC) Characteristics

Table 3-16 ADC Characteristics

Characteristic	Symbol	Min	Typ	Max	Unit
ADC input voltages	V_{ADCIN}	0[1]	—	V_{REF}[2]	V
Resolution	R_{ES}	12	—	12	Bits
Integral Non-Linearity[3]	INL	—	+/- 2.5	+/- 4	LSB[4]
Differential Non-Linearity	DNL	—	+/- 0.9	+/- 1	LSB[4]
Monotonicity	GUARANTEED				
ADC internal clock[5]	f_{ADIC}	0.5	—	5	MHz
Conversion range	R_{AD}	V_{SSA}	—	V_{DDA}	V
Power-up time	t_{ADPU}	—	16	—	t_{AIC} cycles[6]
Conversion time	t_{ADC}	—	6	—	t_{AIC} cycles[6]
Sample time	t_{ADS}	—	1	—	t_{AIC} cycles[6]
Input capacitance	C_{ADI}	—	5	—	pF[6]
Gain Error (transfer gain)[5]	E_{GAIN}	0.95	1.00	1.10	—
Offset Voltage[5]	V_{OFFSET}	-80	-15	+20	mV
Total Harmonic Distortion[5]	THD	60	64	—	dB
Signal-to-Noise plus Distortion[5]	SINAD	55	60	—	dB
Effective Number of Bits[5]	ENOB	9	10	—	bit
Spurious Free Dynamic Range[5]	SFDR	65	70	—	dB
Bandwidth	BW	—	100	—	KHz

3.14 JTAG Timing

Table 3-18 JTAG Timing[1, 3]

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to $+85°C$, $C_L \leq 50$pF, $f_{OP} = 80$MHz

Characteristic	Symbol	Min	Max	Unit
TCK frequency of operation[2]	f_{OP}	DC	10	MHz
TCK cycle time	t_{CY}	100	—	ns
TCK clock pulse width	t_{PW}	50	—	ns
TMS, TDI data set-up time	t_{DS}	0.4	—	ns
TMS, TDI data hold time	t_{DH}	1.2	—	ns
TCK low to TDO data valid	t_{DV}	—	26.6	ns
TCK low to TDO tri-state	t_{TS}	—	23.5	ns
$\overline{\text{TRST}}$ assertion time	t_{TRST}	50	—	ns
$\overline{\text{DE}}$ assertion time	t_{DE}	4T	—	ns

1. Timing is both wait state and frequency dependent. For the values listed, T = clock cycle. For 80MHz operation, T = 12.5ns.
2. TCK frequency of operation must be less than 1/8 the processor rate.
3. Parameters listed are guaranteed by design.

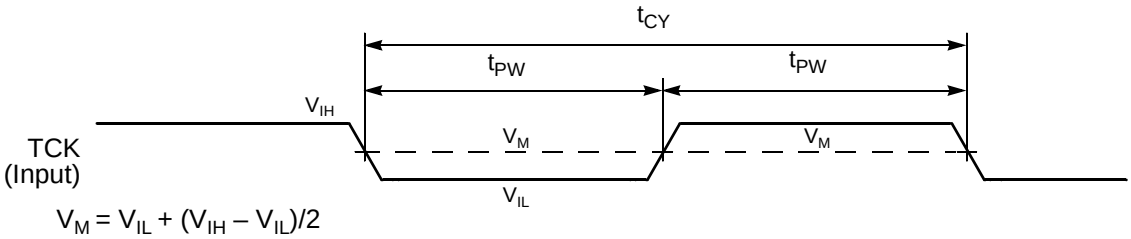


Figure 3-28 Test Clock Input Timing Diagram

Table 4-1 56F803 Pin Identification By Pin Number

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
1	D10	26	A14	51	AN2	76	TXD0
2	D11	27	A15	52	AN3	77	RXD0
3	D12	28	V_{SS}	53	AN4	78	EXTBOOT
4	D13	29	WR	54	AN5	79	$\overline{\text{RESET}}$
5	D14	30	RD	55	AN6	80	$\overline{\text{DE}}$
6	D15	31	$\overline{\text{IRQA}}$	56	AN7	81	CLKO
7	A0	32	$\overline{\text{IRQB}}$	57	XTAL	82	TD1
8	V_{DD}	33	TCS	58	EXTAL	83	TD2
9	V_{SS}	34	TCK	59	V_{SSA}	84	SS
10	A1	35	TMS	60	V_{DDA}	85	MISO
11	A2	36	TDI	61	V_{DD}	86	MOSI
12	A3	37	TDO	62	V_{DD}	87	SCLK
13	A4	38	TRST	63	V_{SS}	88	VCAPC
14	A5	39	VCAPC	64	PHASEA0	89	D0
15	A6	40	ISA0	65	PHASEB0	90	D1
16	A7	41	ISA1	66	V_{DD}	91	D2
17	A8	42	ISA2	67	V_{SS}	92	V_{DD}
18	A9	43	FAULTA0	68	INDEX0	93	V_{SS}
19	A10	44	MSCAN_TX	69	HOME0	94	D3
20	A11	45	FAULTA1	70	PWMA0	95	D4
21	A12	46	MSCAN_RX	71	PWMA1	96	D5
22	A13	47	FAULTA2	72	PWMA2	97	D6
23	V_{DD}	48	VREF	73	PWMA3	98	D7
24	$\overline{\text{PS}}$	49	AN0	74	PWMA4	99	D8
25	$\overline{\text{DS}}$	50	AN1	75	PWMA5	100	D9