Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

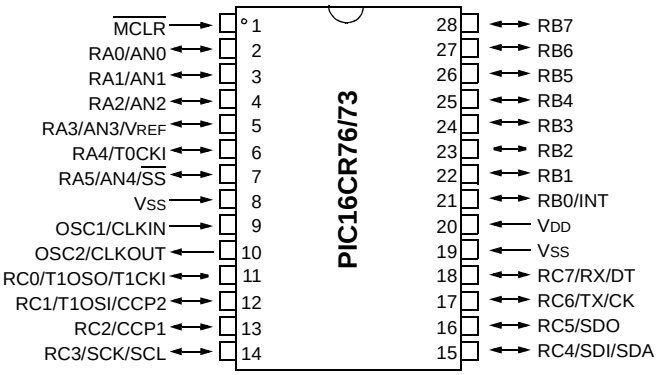
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

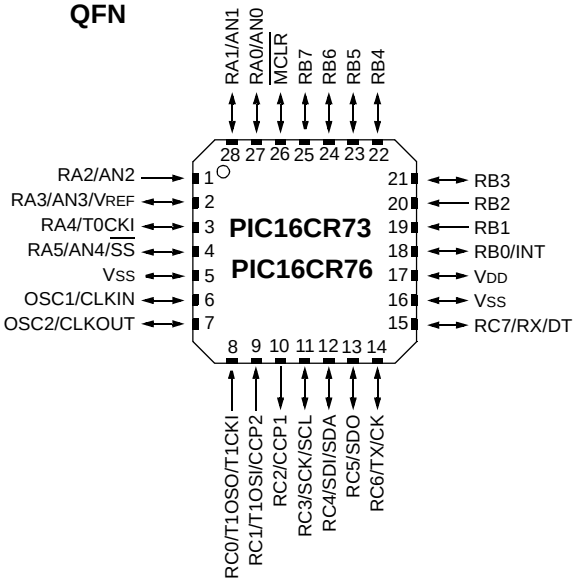
Details	
Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	22
Program Memory Size	7KB (4K x 14)
Program Memory Type	ROM
EEPROM Size	-
RAM Size	192 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 5x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16cr73-i-ss

Pin Diagrams

PDIP, SOIC, SSOP



QFN



PDIP

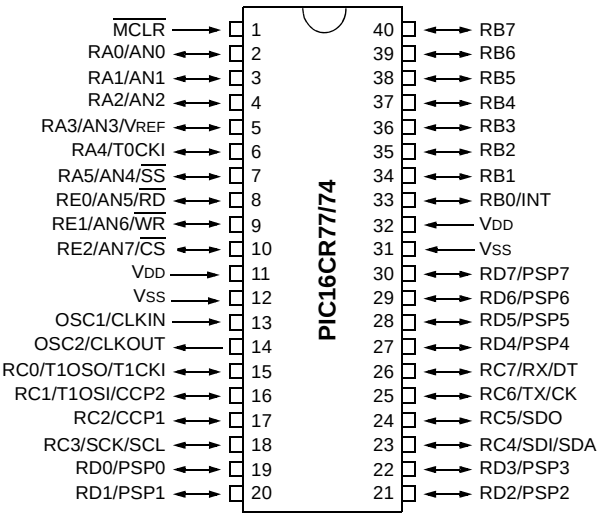


TABLE 1-2: PIC16CR73 AND PIC16CR76 PINOUT DESCRIPTION

Pin Name	PDIP SSOP SOIC Pin#	MLF Pin#	I/O/P Type	Buffer Type	Description
OSC1/CLKIN	9	6		ST/CMOS(3)	Oscillator crystal or external clock input.
OSC1			I		Oscillator crystal input or external clock source input. ST buffer when configured in RC mode. Otherwise CMOS.
CLKIN			I		External clock source input. Always associated with pin function OSC1 (see OSC1/CLKIN, OSC2/CLKOUT pins).
OSC2/CLKOUT	10	7		—	Oscillator crystal or clock output.
OSC2			O		Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
CLKOUT			O		In RC mode, OSC2 pin outputs CLKOUT, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
$\overline{MCLR}$	1	26	I	ST	Master Clear (Reset) input. This pin is an active low Reset to the device.
					PORTA is a bidirectional I/O port.
RA0/AN0	2	27		TTL	
RA0			I/O		Digital I/O.
AN0			I		Analog input 0.
RA1/AN1	3	28		TTL	
RA1			I/O		Digital I/O.
AN1			I		Analog input 1.
RA2/AN2	4	1		TTL	
RA2			I/O		Digital I/O.
AN2			I		Analog input 2.
RA3/AN3/VREF	5	2		TTL	
RA3			I/O		Digital I/O.
AN3			I		Analog input 3.
VREF			I		A/D reference voltage input.
RA4/T0CKI	6	3		ST	
RA4			I/O		Digital I/O – Open drain when configured as output.
T0CKI			I		Timer0 external clock input.
RA5/AN4/$\overline{SS}$	7	4		TTL	
RA5			I/O		Digital I/O.
AN4			I		Analog input 4.
$\overline{SS}$			I		SPI slave select input.
					PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.
RB0/INT	21	18		TTL/ST(1)	
RB0			I/O		Digital I/O.
INT			I		External interrupt.
RB1	22	19	I/O	TTL	Digital I/O.
RB2	23	20	I/O	TTL	Digital I/O.
RB3	24	21	I/O	TTL	Digital I/O.
RB4	25	22	I/O	TTL	Digital I/O.
RB5	26	23	I/O	TTL	Digital I/O.
RB6	27	24	I/O	TTL	Digital I/O.
RB7	28	25	I/O	TTL	Digital I/O.

Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.
2: This buffer is a Schmitt Trigger input when used in Serial Verify mode.
3: This buffer is a Schmitt Trigger input when configured in RC Oscillator mode and a CMOS input otherwise.

TABLE 1-3: PIC16CR74 AND PIC16CR77 PINOUT DESCRIPTION

Pin Name	PDIP Pin#	PLCC Pin#	QFP Pin#	I/O/P Type	Buffer Type	Description
OSC1/CLKIN	13	14	30		ST/CMOS(4)	Oscillator crystal or external clock input.
OSC1				I		Oscillator crystal input or external clock source input. ST buffer when configured in RC mode. Otherwise CMOS.
CLKIN				I		External clock source input. Always associated with pin function OSC1 (see OSC1/CLKIN, OSC2/CLKOUT pins).
OSC2/CLKOUT	14	15	31		—	Oscillator crystal or clock output.
OSC2				O		Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
CLKOUT				O		In RC mode, OSC2 pin outputs CLKOUT, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
$\overline{MCLR}$	1	2	18	I	ST	Master Clear (Reset) input. This pin is an active low Reset to the device.
						PORTA is a bidirectional I/O port.
RA0/AN0	2	3	19		TTL	
RA0				I/O		Digital I/O.
AN0				I		Analog input 0.
RA1/AN1	3	4	20		TTL	
RA1				I/O		Digital I/O.
AN1				I		Analog input 1.
RA2/AN2	4	5	21		TTL	
RA2				I/O		Digital I/O.
AN2				I		Analog input 2.
RA3/AN3/VREF	5	6	22		TTL	
RA3				I/O		Digital I/O.
AN3				I		Analog input 3.
VREF				I		A/D reference voltage input.
RA4/T0CKI	6	7	23		ST	
RA4				I/O		Digital I/O – Open drain when configured as output.
T0CKI				I		Timer0 external clock input.
RA5/AN4/$\overline{SS}$	7	8	24		TTL	
RA5				I/O		Digital I/O.
AN4				I		Analog input 4.
$\overline{SS}$				I		SPI slave select input.

Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as an external interrupt.

2: This buffer is a Schmitt Trigger input when used in Serial Verify mode.

3: This buffer is a Schmitt Trigger input when configured as general purpose I/O and a TTL input when used in the Parallel Slave Port mode (for interfacing to a microprocessor bus).

4: This buffer is a Schmitt Trigger input when configured in RC Oscillator mode and a CMOS input otherwise.

TABLE 1-3: PIC16CR74 AND PIC16CR77 PINOUT DESCRIPTION (CONTINUED)

Pin Name	PDIP Pin#	PLCC Pin#	QFP Pin#	I/O/P Type	Buffer Type	Description
						PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.
RB0/INT	33	36	8		TTL/ST(1)	
RB0				I/O		Digital I/O.
INT				I		External interrupt.
RB1	34	37	9	I/O	TTL	Digital I/O.
RB2	35	38	10	I/O	TTL	Digital I/O.
RB3	36	39	11	I/O	TTL	Digital I/O.
RB4	37	41	14	I/O	TTL	Digital I/O.
RB5	38	42	15	I/O	TTL	Digital I/O.
RB6	39	43	16	I/O	TTL	Digital I/O.
RB7	40	44	17	I/O	TTL	Digital I/O.
						PORTC is a bidirectional I/O port.
RC0/T1OSO/ T1CKI	15	16	32		ST	
				I/O		Digital I/O.
RC0				O		Timer1 oscillator output.
T1OSO				I		Timer1 external clock input.
T1CKI						
RC1/T1OSI/CCP2	16	18	35		ST	
RC1				I/O		Digital I/O.
T1OSI				I		Timer1 oscillator input.
CCP2				I/O		Capture2 input, Compare2 output, PWM2 output.
RC2/CCP1	17	19	36		ST	
RC2				I/O		Digital I/O.
CCP1				I/O		Capture1 input/Compare1 output/PWM1 output.
RC3/SCK/SCL	18	20	37		ST	
RC3				I/O		Digital I/O.
SCK				I/O		Synchronous serial clock input/output for SPI mode.
SCL				I/O		Synchronous serial clock input/output for I^2C™ mode.
RC4/SDI/SDA	23	25	42		ST	
RC4				I/O		Digital I/O.
SDI				I		SPI data in.
SDA				I/O		I^2C™ data I/O.
RC5/SDO	24	26	43		ST	
RC5				I/O		Digital I/O.
SDO				O		SPI data out.
RC6/TX/CK	25	27	44		ST	
RC6				I/O		Digital I/O.
TX				O		USART asynchronous transmit.
CK				I/O		USART 1 synchronous clock.
RC7/RX/DT	26	29	1		ST	
RC7				I/O		Digital I/O.
RX				I		USART asynchronous receive.
DT				I/O		USART synchronous data.

Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

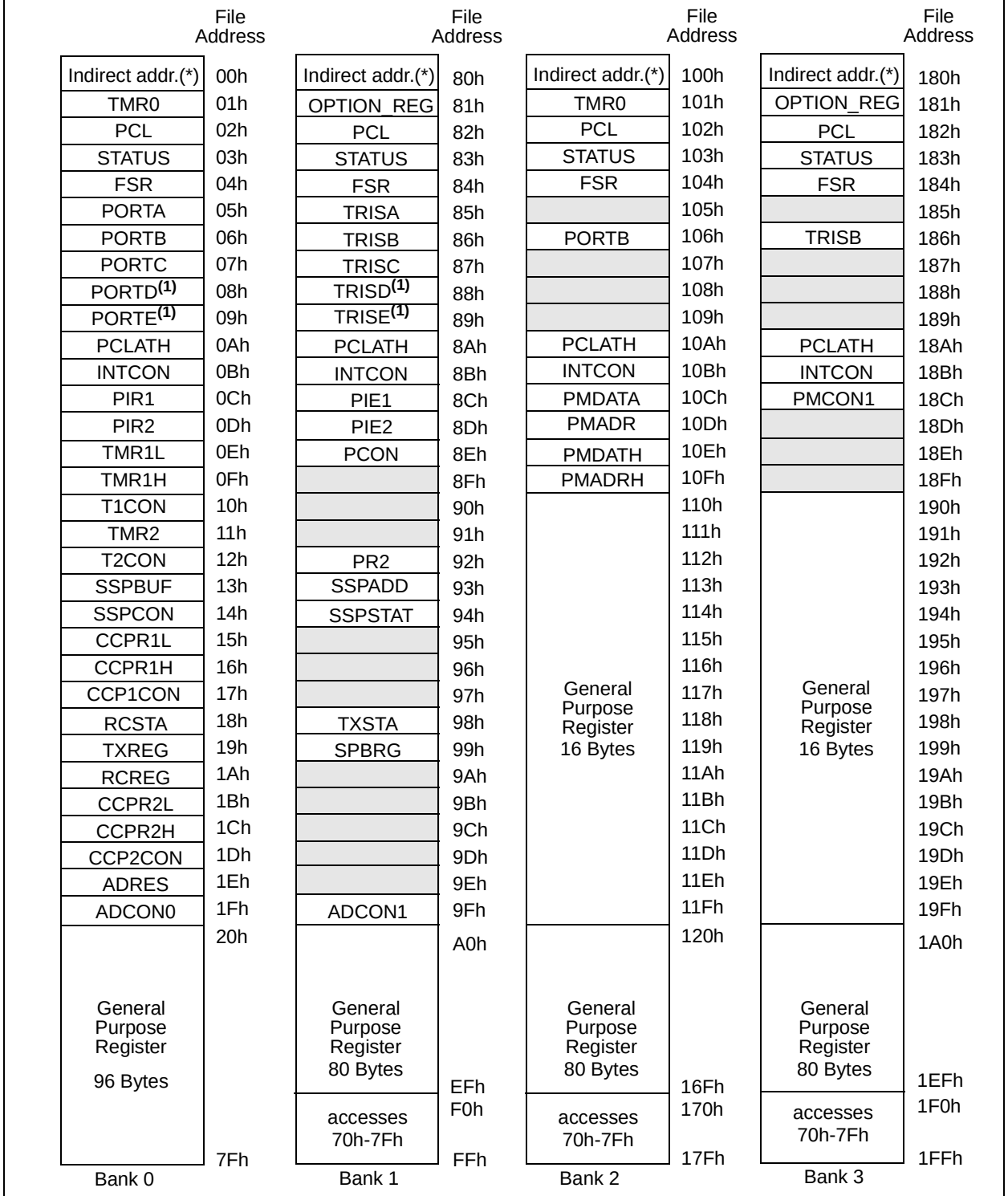
Note 1: This buffer is a Schmitt Trigger input when configured as an external interrupt.

2: This buffer is a Schmitt Trigger input when used in Serial Verify mode.

3: This buffer is a Schmitt Trigger input when configured as general purpose I/O and a TTL input when used in the Parallel Slave Port mode (for interfacing to a microprocessor bus).

4: This buffer is a Schmitt Trigger input when configured in RC Oscillator mode and a CMOS input otherwise.

FIGURE 2-2: PIC16CR77/76 REGISTER FILE MAP



Unimplemented data memory locations, read as '0'.

* Not a physical register.

Note 1: These registers are not implemented on 28-pin devices.

TABLE 2-1: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Details on page
Bank 2											
100h(4)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	27, 96
101h	TMR0	Timer0 Module Register								xxxx xxxx	45, 96
102h(4)	PCL	Program Counter (PC) Least Significant Byte								0000 0000	26, 96
103h(4)	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	19, 96
104h(4)	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	27, 96
105h	—	Unimplemented								—	—
106h	PORTB	PORTB Data Latch when written: PORTB pins when read								xxxx xxxx	34, 96
107h	—	Unimplemented								—	—
108h	—	Unimplemented								—	—
109h	—	Unimplemented								—	—
10Ah(1,4)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	26, 96
10Bh(4)	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000 000x	21, 96
10Ch	PMDATA	Data Register Low Byte								xxxx xxxx	29, 97
10Dh	PMADR	Address Register Low Byte								xxxx xxxx	29, 97
10Eh	PMDATH	—	—	Data Register High Byte						xxxx xxxx	29, 97
10Fh	PMADRH	—	—	—	Address Register High Byte					xxxx xxxx	29, 97
Bank 3											
180h(4)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	27, 96
181h	OPTION_REG	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	20, 44, 96
182h(4)	PCL	Program Counter (PC) Least Significant Byte								0000 0000	26, 96
183h(4)	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	19, 96
184h(4)	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	27, 96
185h	—	Unimplemented								—	—
186h	TRISB	PORTB Data Direction Register								1111 1111	34, 96
187h	—	Unimplemented								—	—
188h	—	Unimplemented								—	—
189h	—	Unimplemented								—	—
18Ah(1,4)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	26, 96
18Bh(4)	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000 000x	21, 96
18Ch	PMCON1	— (6)	—	—	—	—	—	—	RD	1--- ---0	29, 97
18Dh	—	Unimplemented								—	
18Eh	—	Reserved maintain clear								0000 0000	
18Fh	—	Reserved maintain clear								0000 0000	

Legend: x = unknown, u = unchanged, q = value depends on condition, – = unimplemented, read as '0', r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8>, whose contents are transferred to the upper byte of the program counter during branches (CALL or GOTO).

2: Other (non Power-up) Resets include external Reset through $\overline{MCLR}$ and Watchdog Timer Reset.

3: Bits PSPIE and PSPIF are reserved on the 28-pin devices; always maintain these bits clear.

4: These registers can be addressed from any bank.

5: PORTD, PORTE, TRISD and TRISE are not physically implemented on the 28-pin devices, read as '0'.

6: This bit always reads as a '1'.

NOTES:

3.3 Reading the ROM Program Memory

A program memory location may be read by writing two bytes of the address to the PMADR and PMADRH registers and then setting control bit RD (PMCON1<0>). Once the read control bit is set, the microcontroller will use the next two instruction cycles to read the data. The data is available in the PMDATA and PMDATH registers after the second NOP instruction. Therefore, it can be read as two bytes in the following instructions. The PMDATA and PMDATH registers will hold this value until the next read operation.

3.4 Operation During Code-Protect

ROM program memory has its own code-protect mechanism. External Read operations by programmers are disabled if this mechanism is enabled.

The microcontroller can read and execute instructions out of the internal ROM program memory, regardless of the state of the code-protect Configuration bits.

EXAMPLE 3-1: ROM PROGRAM READ

```
            BSF     STATUS, RP1     ;
            BCF     STATUS, RP0     ; Bank 2
            MOVF    ADDRH, W        ;
            MOVWF   PMADRH          ; MSByte of Program Address to read
            MOVF    ADDRL, W        ;
            MOVWF   PMADR           ; LSByte of Program Address to read
            BSF     STATUS, RP0     ; Bank 3 Required

Required    BSF     PMCON1, RD      ; ROM Read Sequence
Sequence    NOP                     ; memory is read in the next two cycles after BSF PMCON1,RD
            NOP                     ;

            BCF     STATUS, RP0     ; Bank 2
            MOVF    PMDATA, W       ; W = LSByte of Program PMDATA
            MOVF    PMDATH, W       ; W = MSByte of Program PMDATA
```

TABLE 3-1: REGISTERS ASSOCIATED WITH PROGRAM ROM

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
10Dh	PMADR	Address Register Low Byte								xxxx xxxx	uuuu uuuu
10Fh	PMADRH	—	—	—	Address Register High Byte					xxxx xxxx	uuuu uuuu
10Ch	PMDATA	Data Register Low Byte								xxxx xxxx	uuuu uuuu
10Eh	PMDATH	—	—	Data Register High Byte						xxxx xxxx	uuuu uuuu
18Ch	PMCON1	—(1)	—	—	—	—	—	—	RD	1--- ---0	1--- ---0

Legend: x = unknown, u = unchanged, r = reserved, – = unimplemented read as '0'. Shaded cells are not used during ROM access.

Note 1: This bit always reads as a '1'.

NOTES:

9.0 SYNCHRONOUS SERIAL PORT (SSP) MODULE

9.1 SSP Module Overview

The Synchronous Serial Port (SSP) module is a serial interface useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be Serial EEPROMs, shift registers, display drivers, A/D converters, etc. The SSP module can operate in one of two modes:

- Serial Peripheral Interface (SPI)
- Inter-Integrated Circuit (I^2C)

An overview of I^2C operations and additional information on the SSP module can be found in the "*PIC® Mid-Range MCU Family Reference Manual*" (DS33023).

Refer to Application Note AN578, "*Use of the SSP Module in the I^2C™ Multi-Master Environment*" (DS00578).

9.2 SPI Mode

This section contains register definitions and operational characteristics of the SPI module. Additional information on the SPI module can be found in the "*PIC® Mid-Range MCU Family Reference Manual*" (DS33023).

SPI mode allows 8 bits of data to be synchronously transmitted and received simultaneously. To accomplish communication, typically three pins are used:

- Serial Data Out (SDO) RC5/SDO
- Serial Data In (SDI) RC4/SDI/SDA
- Serial Clock (SCK) RC3/SCK/SCL

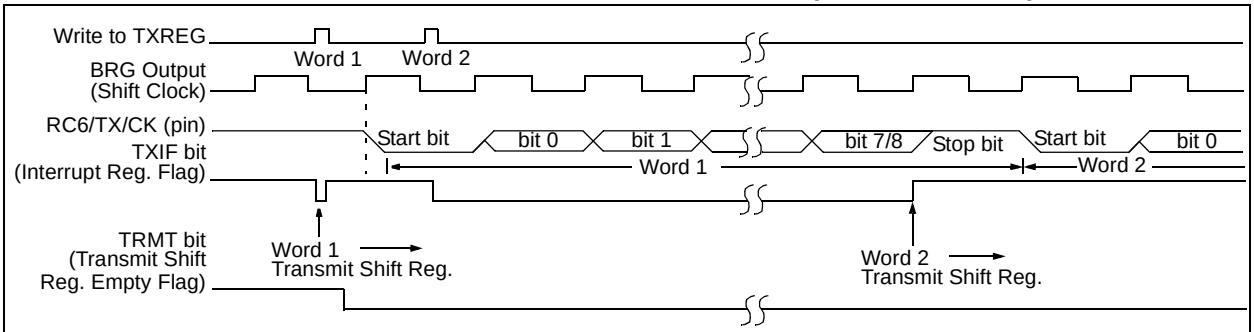
Additionally, a fourth pin may be used when in a Slave mode of operation:

- Slave Select ($\overline{SS}$) RA5/$\overline{SS}$/AN4

When initializing the SPI, several options need to be specified. This is done by programming the appropriate control bits in the SSPCON register (SSPCON<5:0>) and SSPSTAT<7:6>. These control bits allow the following to be specified:

- Master mode (SCK is the clock output)
- Slave mode (SCK is the clock input)
- Clock Polarity (Idle state of SCK)
- Clock edge (output data on rising/falling edge of SCK)
- Clock Rate (Master mode only)
- Slave Select mode (Slave mode only)

FIGURE 10-3: ASYNCHRONOUS MASTER TRANSMISSION (BACK-TO-BACK)



Note: This timing diagram shows two consecutive transmissions.

TABLE 10-5: REGISTERS ASSOCIATED WITH ASYNCHRONOUS TRANSMISSION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
0Bh, 8Bh, 10Bh,18Bh	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF(1)	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
18h	RCSTA	SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D	0000 -00x	0000 -00x
19h	TXREG	USART Transmit Data Register								0000 0000	0000 0000
8Ch	PIE1	PSPIE(1)	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
99h	SPBRG	Baud Rate Generator Register								0000 0000	0000 0000

Legend: x = unknown, – = unimplemented locations read as '0'. Shaded cells are not used for asynchronous transmission.

Note 1: Bits PSPIE and PSPIF are reserved on the PIC16CR73/76; always maintain these bits clear.

10.2.2 USART ASYNCHRONOUS RECEIVER

The receiver block diagram is shown in Figure 10-4. The data is received on the RC7/RX/DT pin and drives the data recovery block. The data recovery block is actually a high-speed shifter operating at x16 times the baud rate, whereas the main receive serial shifter operates at the bit rate, or at FOSC.

Once Asynchronous mode is selected, reception is enabled by setting bit CREN (RCSTA<4>).

The heart of the receiver is the Receive (serial) Shift Register (RSR). After sampling the Stop bit, the received data in the RSR is transferred to the RCREG register (if it is empty). If the transfer is complete, flag bit RCIF (PIR1<5>) is set. The actual interrupt can be enabled/disabled by setting/clearing enable bit RCIE (PIE1<5>). Flag bit RCIF is a read-only bit which is cleared by the hardware. It is cleared when the RCREG register has been read and is empty. The RCREG is a double buffered register (i.e., it is a two-deep FIFO). It is possible for two bytes of data to be received and transferred to the RCREG FIFO and a third byte to begin shifting to the RSR register. On the detection of the Stop bit of the third byte, if the RCREG register is still full, the overrun error bit OERR (RCSTA<1>) will be set. The word in the RSR will be lost. The RCREG register can be read twice to retrieve the two bytes in the FIFO. Overrun bit OERR has to be cleared in software. This is done by resetting the receive logic (CREN is cleared and then set). If bit OERR is set, transfers from the RSR register to the RCREG register are inhibited and no further data will be received, therefore, it is essential to clear error bit OERR if it is set. Framing error bit FERR (RCSTA<2>) is set if a Stop bit is detected as clear. Bit FERR and the 9th receive bit are buffered the same way as the receive data. Reading the RCREG will load bits RX9D and FERR with new values, therefore, it is essential for the user to read the RCSTA register before reading RCREG register, in order not to lose the old FERR and RX9D information.

REGISTER 11-2: ADCON1: (ADDRESS 1Fh)

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	PCFG2	PCFG1	PCFG0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-3 **Unimplemented**: Read as '0'

bit 2-0 **PCFG2:PCFG0**: A/D Port Configuration Control bits

PCFG2:PCFG0	RA0	RA1	RA2	RA5	RA3	RE0(1)	RE1(1)	RE2(1)	VREF
000	A	A	A	A	A	A	A	A	VDD
001	A	A	A	A	VREF	A	A	A	RA3
010	A	A	A	A	A	D	D	D	VDD
011	A	A	A	A	VREF	D	D	D	RA3
100	A	A	D	D	A	D	D	D	VDD
101	A	A	D	D	VREF	D	D	D	RA3
11x	D	D	D	D	D	D	D	D	VDD

A = Analog input
D = Digital I/O

Note 1: RE0, RE1 and RE2 are implemented on the PIC16CR74/77 only.

15.1 DC Characteristics: PIC16CR73/74/76/77 (Industrial, Extended) (Continued)

PIC16CR73/74/76/77 (Industrial, Extended)			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	IDD	**Supply Current (Notes 2, 5)**					
D010		PIC16CR7X	—	0.5	2	mA	XT, RC osc configuration FOSC = 4 MHz, VDD = 3.0V **(Note 4)**
D010A			—	20	48	µA	LP osc configuration FOSC = 32 kHz, VDD = 3.0V, WDT disabled
D010		PIC16CR7X	—	1.1	4	mA	XT, RC osc configuration FOSC = 4 MHz, VDD = 5.5V **(Note 4)**
D013			—	6.3	15	mA	HS osc configuration FOSC = 20 MHz, VDD = 5.5V
D015*	ΔIBOR	**Brown-out Reset Current (Note 6)**	—	30	200	µA	BOR enabled, VDD = 5.0V
D020	IPD	**Power-down Current (Notes 3, 5)**					
		PIC16CR7X	—	2.0	30	µA	VDD = 3.0V, WDT enabled, -40°C to +85°C
D021			—	0.1	5	µA	VDD = 3.0V, WDT disabled, -40°C to +85°C
D020		PIC16CR7X	—	5	42	µA	VDD = 4.0V, WDT enabled, -40°C to +85°C
D021			—	0.1	19	µA	VDD = 4.0V, WDT disabled, -40°C to +85°C
D021A			—	10.5	57	µA	VDD = 4.0V, WDT enabled, -40°C to +125°C
			—	1.5	42	µA	VDD = 4.0V, WDT disabled, -40°C to +125°C
D023*	ΔIBOR	**Brown-out Reset Current (Note 6)**	—	30	200	µA	BOR enabled, VDD = 5.0V

Legend: Shading of rows is to assist in readability of of the table.

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD
MCLR = VDD; WDT enabled/disabled as specified.

3: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impendance state and tied to VDD and VSS.

4: For RC osc configuration, current through REXT is not included. The current through the resistor can be estimated by the formula Ir = VDD/2REXT (mA) with REXT in kOhm.

5: Timer1 oscillator (when enabled) adds approximately 20 µA to the specification. This value is from characterization and is for design guidance only. This is not tested.

6: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

7: When BOR is enabled, the device will operate correctly until the VBOR voltage trip point is reached.

FIGURE 15-3: EXTERNAL CLOCK TIMING

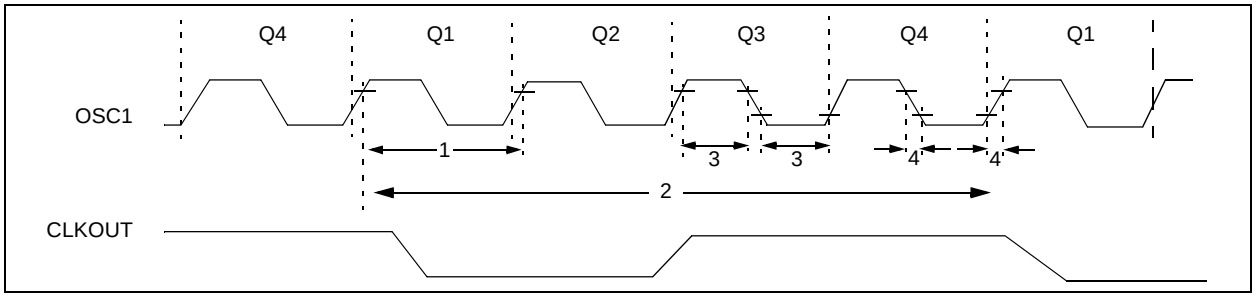


TABLE 15-1: EXTERNAL CLOCK TIMING REQUIREMENTS

Parameter No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
	FOSC	**External CLKIN Frequency (Note 1)**	DC	—	1	MHz	XT osc mode
			DC	—	20	MHz	HS osc mode
			DC	—	32	kHz	LP osc mode
		Oscillator Frequency (Note 1)	DC	—	4	MHz	RC osc mode
			0.1	—	4	MHz	XT osc mode
			4	—	20	MHz	HS osc mode
			5	—	200	kHz	LP osc mode
1	TOSC	**External CLKIN Period (Note 1)**	1000	—	—	ns	XT osc mode
			50	—	—	ns	HS osc mode
			5	—	—	ms	LP osc mode
		Oscillator Period (Note 1)	250	—	—	ns	RC osc mode
			250	—	10,000	ns	XT osc mode
			50	—	250	ns	HS osc mode
			5	—	—	ms	LP osc mode
2	TCY	**Instruction Cycle Time (Note 1)**	200	TCY	DC	ns	TCY = 4/FOSC
3	TosL, TosH	**External Clock in (OSC1) High or Low Time**	500	—	—	ns	XT oscillator
			2.5	—	—	ms	LP oscillator
			15	—	—	ns	HS oscillator
4	TosR, TosF	**External Clock in (OSC1) Rise or Fall Time**	—	—	25	ns	XT oscillator
			—	—	50	ns	LP oscillator
			—	—	15	ns	HS oscillator

† Data in “Typ” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions, with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at “min.” values with an external clock applied to the OSC1/CLKIN pin. When an external clock input is used, the “max.” cycle time limit is “DC” (no clock) for all devices.

FIGURE 16-17: TYPICAL, MINIMUM AND MAXIMUM VOL vs. IOL (VDD = 5V, -40°C TO 125°C)

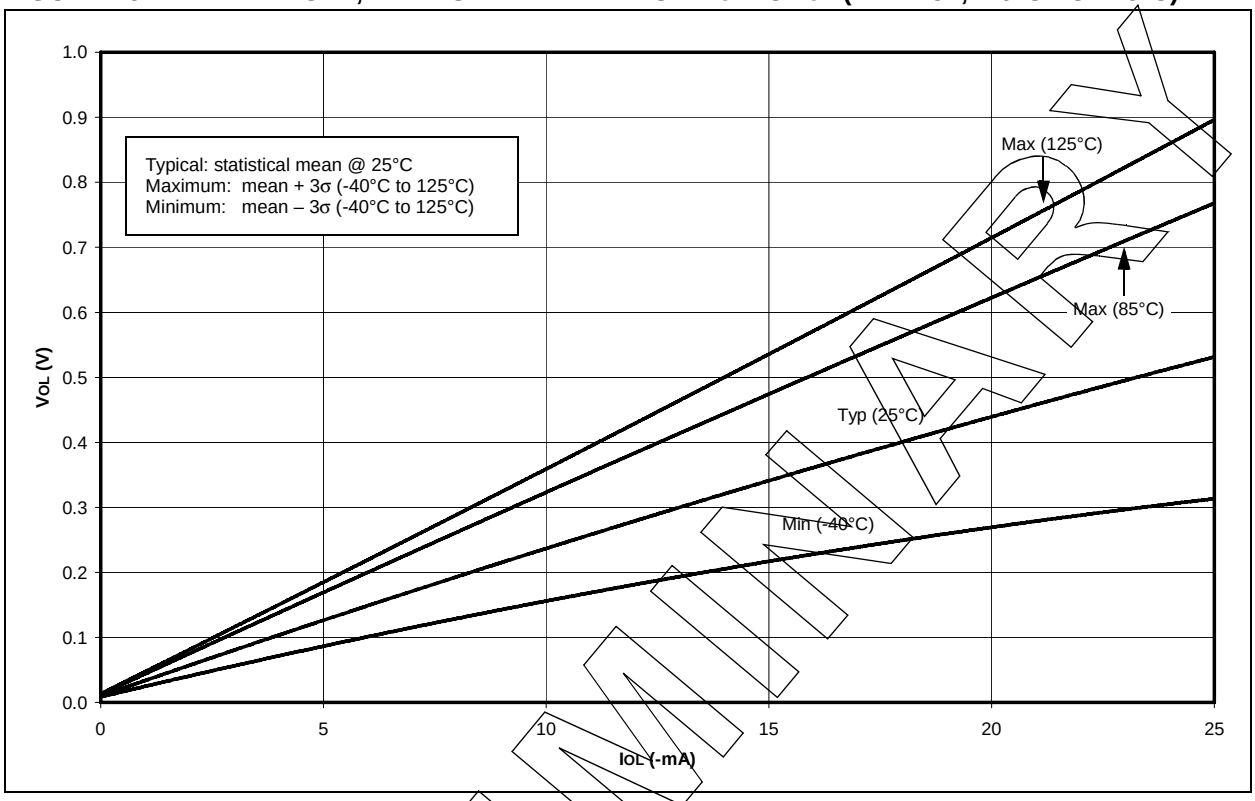


FIGURE 16-18: TYPICAL, MINIMUM AND MAXIMUM VOL vs. IOL (VDD = 3V, -40°C TO 125°C)

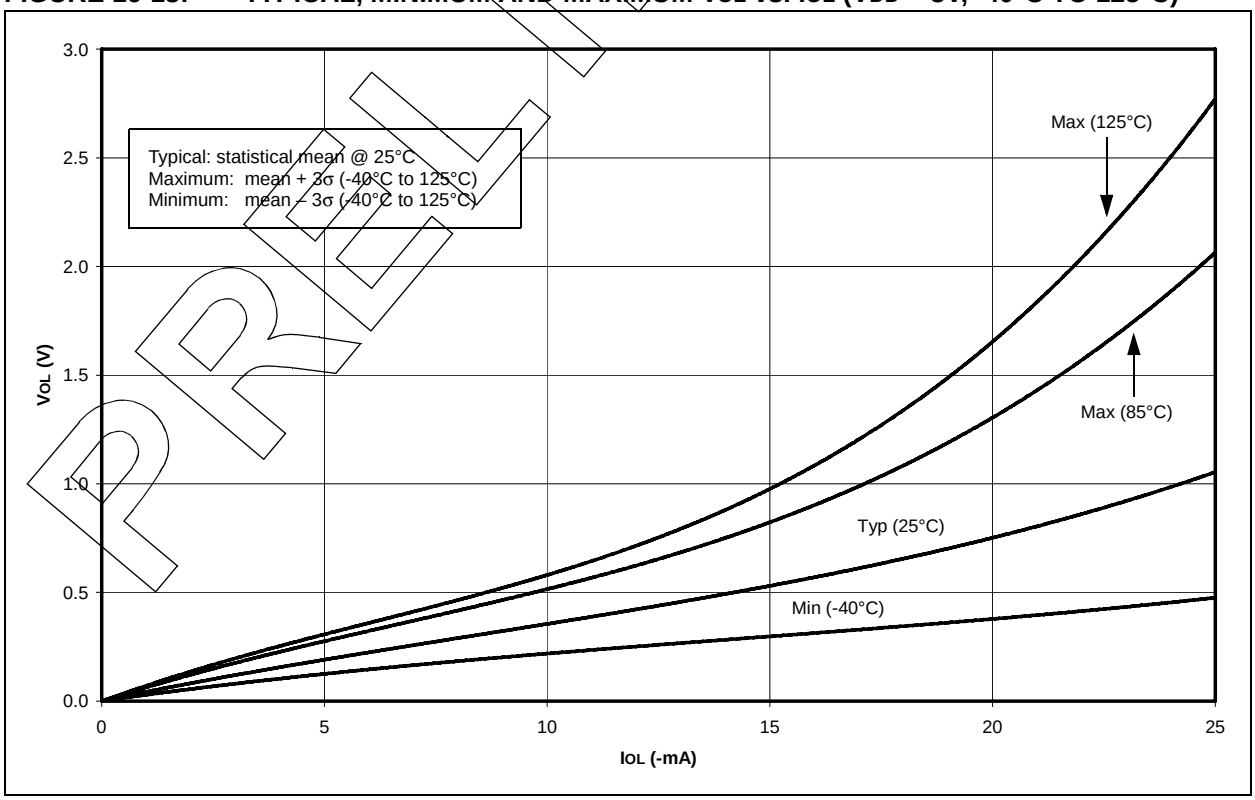


FIGURE 16-19: MINIMUM AND MAXIMUM VIN vs. VDD, (TTL INPUT, -40°C TO 125°C)

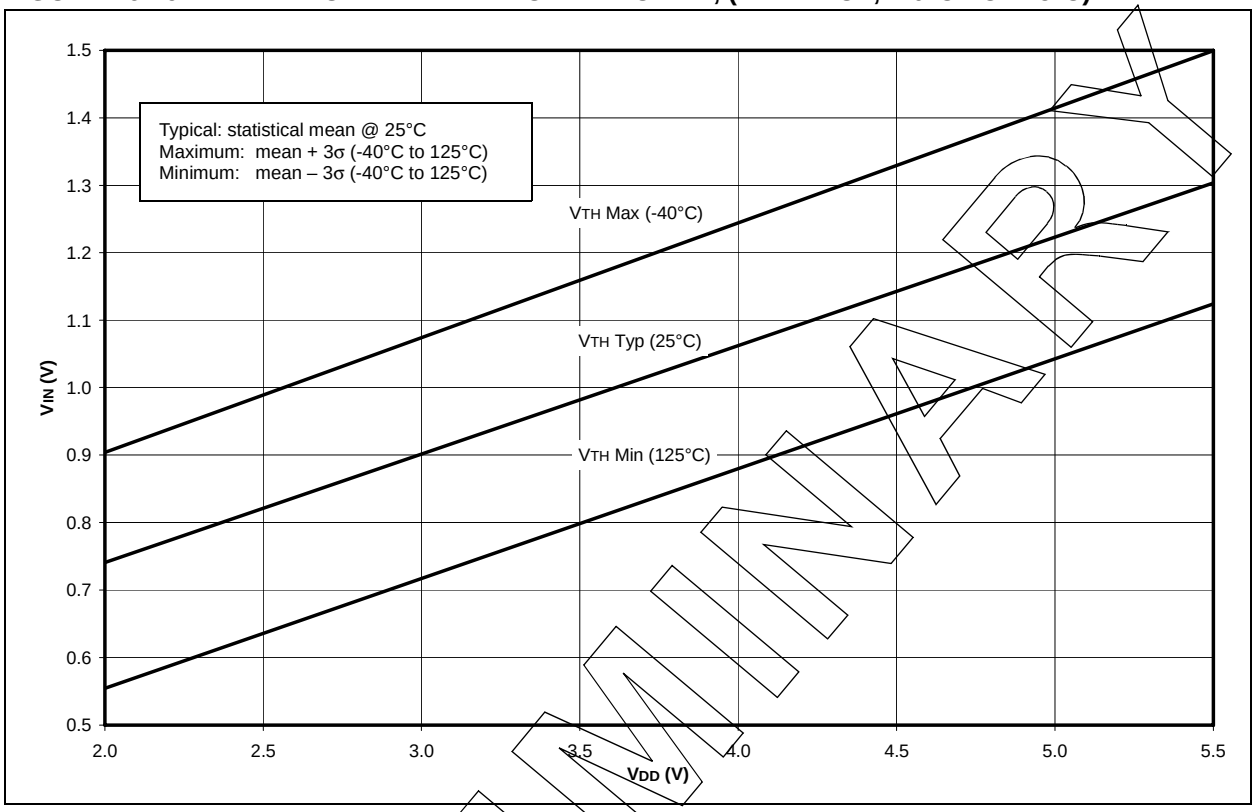
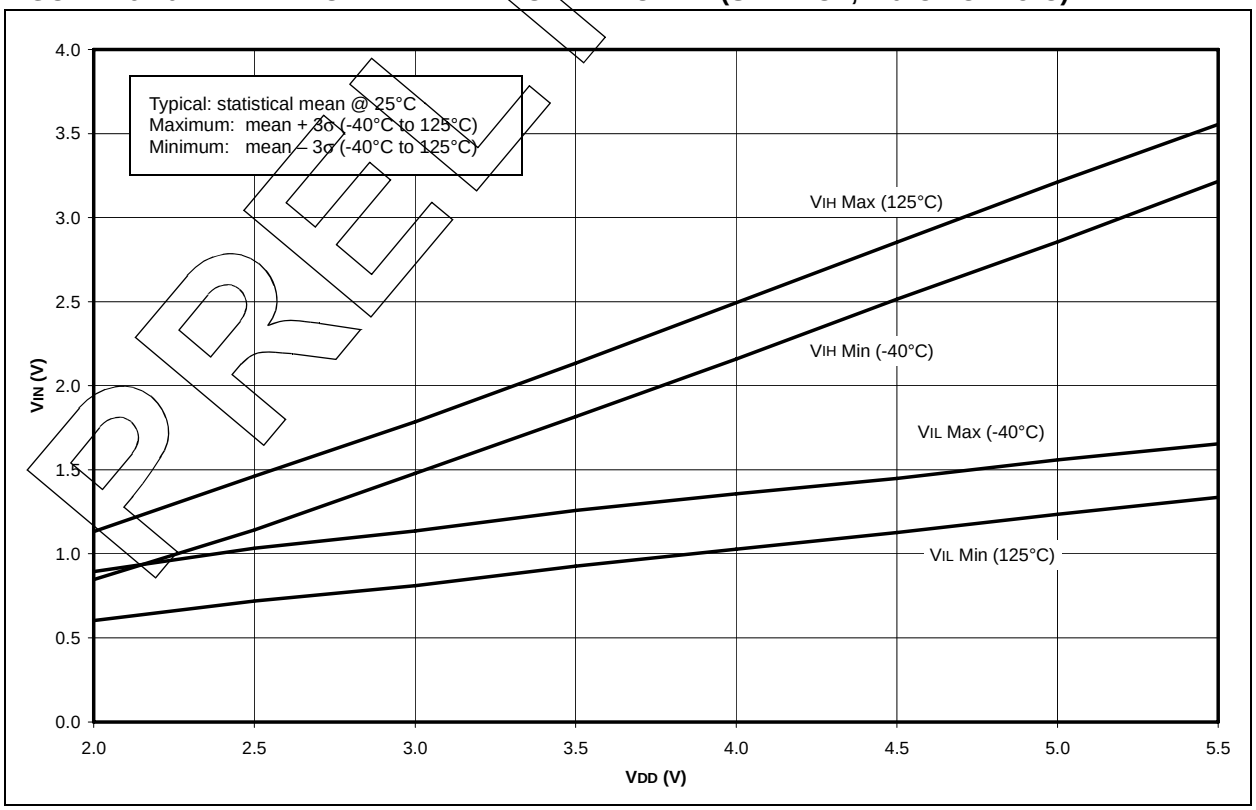
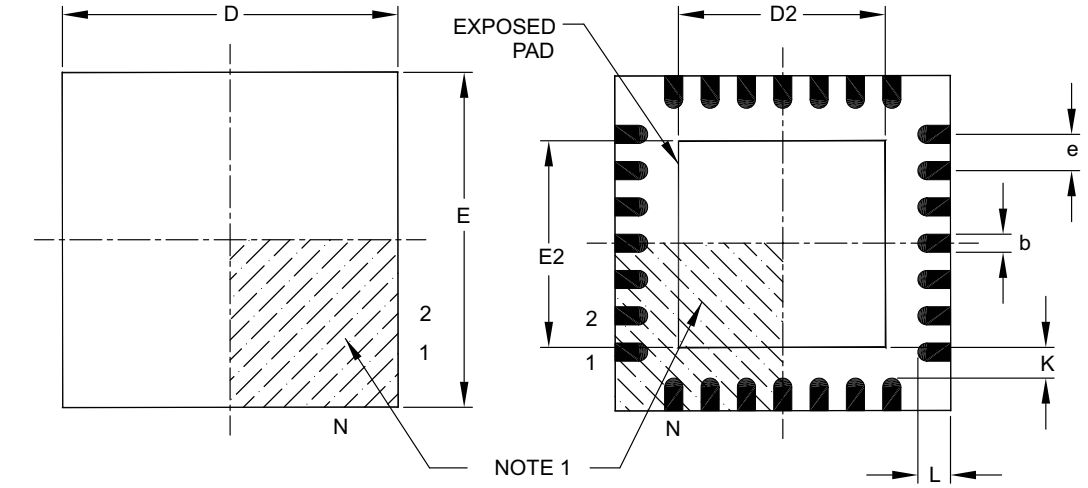


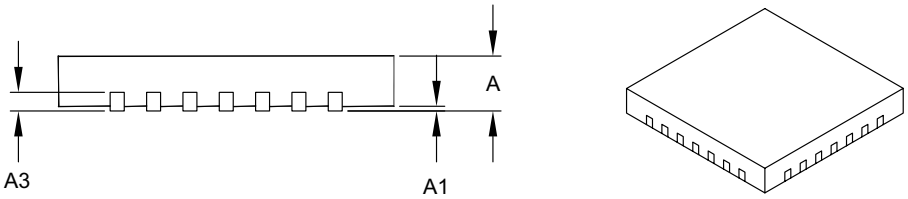
FIGURE 16-20: MINIMUM AND MAXIMUM VIN vs. VDD (ST INPUT, -40°C TO 125°C)



28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		6.00 BSC	
Exposed Pad Width	E2	3.65	3.70	4.20
Overall Length	D		6.00 BSC	
Exposed Pad Length	D2	3.65	3.70	4.20
Contact Width	b	0.23	0.30	0.35
Contact Length	L	0.50	0.55	0.70
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-105B

T

THE MICROCHIP WEB SITE

Microchip provides online support via our WWW site at www.microchip.com. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

CUSTOMER CHANGE NOTIFICATION SERVICE

Microchip's customer notification service helps keep customers current on Microchip products. Subscribers will receive e-mail notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, access the Microchip web site at www.microchip.com, click on Customer Change Notification and follow the registration instructions.

CUSTOMER SUPPORT

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support
- Development Systems Information Line

Customers should contact their distributor, representative or field application engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the web site at: http://support.microchip.com

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX	XXX
Device	Temperature Range	Package	Pattern

Device: PIC16CR73
PIC16CR74
PIC16CR76
PIC16CR77

Temperature Range:
I = -40°C to +85°C (Industrial)
E = -40°C to+125°C (Extended)

Package:
PT = TQFP (Thin Quad Flatpack)
L = PLCC
SO = SOIC
SP = Skinny Plastic DIP
P = PDIP

Pattern: QTP, SQTP, Code or Special Requirements (blank otherwise)

Examples:

Note1: F = Standard Voltage Range
LF = Wide Voltage Range
2: T = in tape and reel PLCC, and TQFP packages only.