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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	66MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (2), 10/100Mbps (2)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 100°C (TA)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc880czp66

- Provides enhanced ATM functionality found on the MPC862 and MPC866 families and includes the following:
  - Improved operation, administration and maintenance (OAM) support
  - OAM performance monitoring (PM) support
  - Multiple APC priority levels available to support a range of traffic pace requirements
  - Port-to-port switching capability without the need for RAM-based microcode
  - Simultaneous MII (100BaseT) and UTOPIA (half- or full -duplex) capability
  - Optional statistical cell counters per PHY
  - UTOPIA L2-compliant interface with added FIFO buffering to reduce the total cell transmission time and multi-PHY support. (The earlier UTOPIA L1 specification is also supported.)
  - Parameter RAM for both SPI and I^2C can be relocated without RAM-based microcode
  - Supports full-duplex UTOPIA master (ATM side) and slave (PHY side) operations using a split bus
  - AAL2/VBR functionality is ROM-resident
- Up to 32-bit data bus (dynamic bus sizing for 8, 16, and 32 bits)
- Thirty-two address lines
- Memory controller (eight banks)
  - Contains complete dynamic RAM (DRAM) controller
  - Each bank can be a chip select or $\overline{\text{RAS}}$ to support a DRAM bank
  - Up to 30 wait states programmable per memory bank
  - Glueless interface to DRAM, SIMMS, SRAM, EPROMs, Flash EPROMs, and other memory devices
  - DRAM controller programmable to support most size and speed memory interfaces
  - Four $\overline{\text{CAS}}$ lines, four $\overline{\text{WE}}$ lines, and one $\overline{\text{OE}}$ line
  - Boot chip-select available at reset (options for 8-, 16-, or 32-bit memory)
  - Variable block sizes (32 Kbytes–256 Mbytes)
  - Selectable write protection
  - On-chip bus arbitration logic
- General-purpose timers
  - Four 16-bit timers or two 32-bit timers
  - Gate mode can enable/disable counting.
  - Interrupt can be masked on reference match and event capture
- Two fast Ethernet controllers (FEC)—Two 10/100 Mbps Ethernet/IEEE Std. 802.3™ CDMA/CS that interface through MII and/or RMII interfaces
- System integration unit (SIU)
  - Bus monitor
  - Software watchdog

- Periodic interrupt timer (PIT)
- Clock synthesizer
- Decrementer and time base
- Reset controller
- IEEE Std 1149.1™ test access port (JTAG)

- Security engine is optimized to handle all the algorithms associated with IPsec, SSL/TLS, SRTP, IEEE Std 802.11i™, and iSCSI processing. Available on the MPC885, the security engine contains a crypto-channel, a controller, and a set of crypto hardware accelerators (CHAs). The CHAs are:
  - Data encryption standard execution unit (DEU)
    - DES, 3DES
    - Two key (K1, K2, K1) or three key (K1, K2, K3)
    - ECB and CBC modes for both DES and 3DES
  - Advanced encryption standard unit (AESU)
    - Implements the Rijndael symmetric key cipher
    - ECB, CBC, and counter modes
    - 128-, 192-, and 256- bit key lengths
  - Message digest execution unit (MDEU)
    - SHA with 160- or 256-bit message digest
    - MD5 with 128-bit message digest
    - HMAC with either algorithm
  - Crypto-channel supporting multi-command descriptor chains
  - Integrated controller managing internal resources and bus mastering
  - Buffer size of 256 bytes for the DEU, AESU, and MDEU, with flow control for large data sizes
- Interrupts
  - Six external interrupt request (IRQ) lines
  - 12 port pins with interrupt capability
  - 23 internal interrupt sources
  - Programmable priority between SCCs
  - Programmable highest priority request
- Communications processor module (CPM)
  - RISC controller
  - Communication-specific commands (for example, GRACEFUL STOP TRANSMIT, ENTER HUNT MODE, and RESTART TRANSMIT)
  - Supports continuous mode transmission and reception on all serial channels
  - 8-Kbytes of dual-port RAM
  - Several serial DMA (SDMA) channels to support the CPM
  - Three parallel I/O registers with open-drain capability

  - Flexible data buffers with multiple buffers per frame
  - Automatic retransmission upon transmit error
- The USB host controller has the following features:
  - Supports control, bulk, interrupt, and isochronous data transfers
  - CRC16 generation and checking
  - NRZI encoding/decoding with bit stuffing
  - Supports both 12- and 1.5-Mbps data rates (automatic generation of preamble token and data rate configuration). Note that low-speed operation requires an external hub.
  - Flexible data buffers with multiple buffers per frame
  - Supports local loop back mode for diagnostics (12 Mbps only)

- Serial peripheral interface (SPI)
  - Supports master and slave modes
  - Supports multiple-master operation on the same bus
- Inter-integrated circuit (I^2C) port
  - Supports master and slave modes
  - Supports a multiple-master environment
- Time-slot assigner (TSA)
  - Allows SCCs and SMCs to run in multiplexed and/or non-multiplexed operation
  - Supports T1, CEPT, PCM highway, ISDN basic rate, ISDN primary rate, user defined
  - 1- or 8-bit resolution
  - Allows independent transmit and receive routing, frame synchronization, and clocking
  - Allows dynamic changes
  - Can be internally connected to four serial channels (two SCCs and two SMCs)
- Parallel interface port (PIP)
  - Centronics interface support
  - Supports fast connection between compatible ports on MPC885/MPC880 and other MPC8xx devices
- PCMCIA interface
  - Master (socket) interface, release 2.1-compliant
  - Supports two independent PCMCIA sockets
  - 8 memory or I/O windows supported
- Debug interface
  - Eight comparators: four operate on instruction address, two operate on data address, and two operate on data
  - Supports conditions: = ≠ < >
  - Each watchpoint can generate a break point internally.
- Normal high and normal low power modes to conserve power

- 1.8-V core and 3.3-V I/O operation
- The MPC885/MPC880 comes in a 357-pin ball grid array (PBGA) package

The MPC885 block diagram is shown in Figure 1.

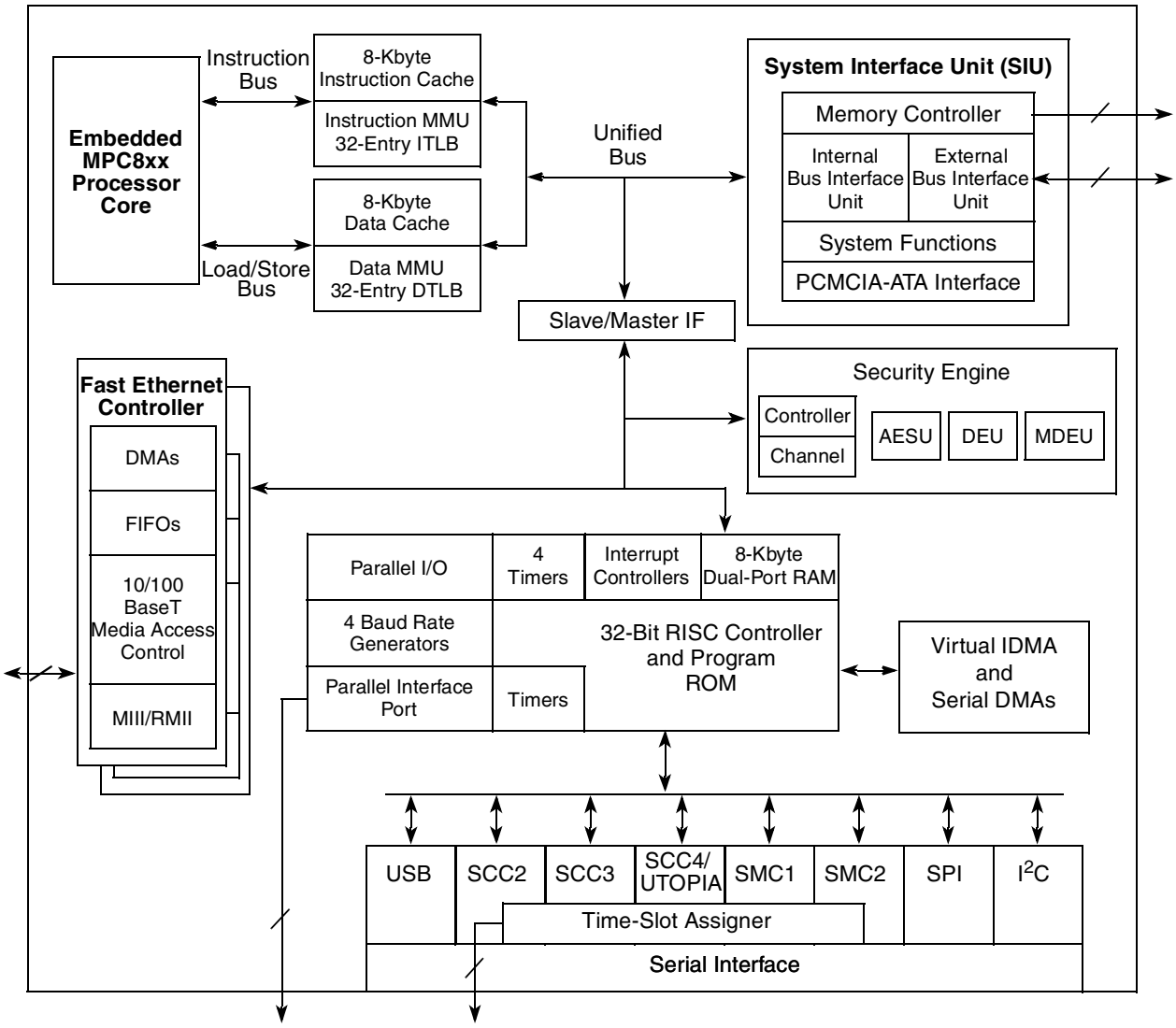

Figure 1. MPC885 Block Diagram

7.6 References

Semiconductor Equipment and Materials International(415) 964-5111
805 East Middlefield Rd
Mountain View, CA 94043

MIL-SPEC and EIA/JESD (JEDEC) specifications800-854-7179 or
(Available from Global Engineering Documents)303-397-7956

JEDEC Specifications http://www.jedec.org

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
2. 2. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

8 Power Supply and Power Sequencing

This section provides design considerations for the MPC885/MPC880 power supply. The MPC885/MPC880 has a core voltage (V_{DDL}) and PLL voltage (V_{DDSYN}), which both operate at a lower voltage than the I/O voltage V_{DDH}. The I/O section of the MPC885/MPC880 is supplied with 3.3 V across V_{DDH} and V_{SS} (GND).

The signals PA[0:15], PB[14:31], PC[4:15], PD[3:15], TDI, TDO, TCK, TRST_B, TMS, MII_TXEN, and MII_MDIO are 5 V tolerant. All inputs cannot be more than 2.5 V greater than V_{DDH}. In addition, 5-V tolerant pins cannot exceed 5.5 V and remaining input pins cannot exceed 3.465 V. This restriction applies to power up/down and normal operation.

One consequence of multiple power supplies is that when power is initially applied the voltage rails ramp up at different rates. The rates depend on the nature of the power supply, the type of load on each power supply, and the manner in which different voltages are derived. The following restrictions apply:

- V_{DDL} must not exceed V_{DDH} during power up and power down.
- V_{DDL} must not exceed 1.9 V, and V_{DDH} must not exceed 3.465 V.

These cautions are necessary for the long-term reliability of the part. If they are violated, the electrostatic discharge (ESD) protection diodes are forward-biased, and excessive current can flow through these diodes. If the system power supply design does not control the voltage sequencing, the circuit shown Figure 5 can be added to meet these requirements. The MUR420 Schottky diodes control the maximum potential difference between the external bus and core power supplies on power up, and the 1N5820 diodes regulate the maximum potential difference on power down.

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B16b	$\overline{BB}$, $\overline{BG}$, $\overline{BR}$, valid to CLKOUT (setup time)[2] (4MIN = 0.00 × B1 + 0.00)	4.00	—	4.00	—	4.00	—	4.00	—	ns
B17	CLKOUT to $\overline{TA}$, $\overline{TEA}$, $\overline{BI}$, $\overline{BB}$, $\overline{BG}$, $\overline{BR}$ valid (hold time) (MIN = 0.00 × B1 + 1.00[3])	1.00	—	1.00	—	2.00	—	2.00	—	ns
B17a	CLKOUT to $\overline{KR}$, $\overline{RETRY}$, $\overline{CR}$ valid (hold time) (MIN = 0.00 × B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B18	D(0:31) valid to CLKOUT rising edge (setup time)[4] (MIN = 0.00 × B1 + 6.00)	6.00	—	6.00	—	6.00	—	6.00	—	ns
B19	CLKOUT rising edge to D(0:31) valid (hold time)[4] (MIN = 0.00 × B1 + 1.00[5])	1.00	—	1.00	—	2.00	—	2.00	—	ns
B20	D(0:31) valid to CLKOUT falling edge (setup time)[6] (MIN = 0.00 × B1 + 4.00)	4.00	—	4.00	—	4.00	—	4.00	—	ns
B21	CLKOUT falling edge to D(0:31) valid (hold time)[6] (MIN = 0.00 × B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B22	CLKOUT rising edge to $\overline{CS}$ asserted GPCM ACS = 00 (MAX = 0.25 × B1 + 6.3)	7.60	13.80	6.30	12.50	3.80	10.00	3.13	9.43	ns
B22a	CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = [0 or 1] (MAX = 0.00 × B1 + 8.00)	—	8.00	—	8.00	—	8.00	—	8.00	ns
B22b	CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = [0 or 1], EBDF = 0 (MAX = 0.25 × B1 + 6.3)	7.60	13.80	6.30	12.50	3.80	10.00	3.13	9.43	ns
B22c	CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = [0 or 1], EBDF = 1 (MAX = 0.375 × B1 + 6.6)	10.90	18.00	10.90	16.00	5.20	12.30	4.69	10.93	ns
B23	CLKOUT rising edge to $\overline{CS}$ negated GPCM read access, GPCM write access ACS = 00 and CSNT = 0 (MAX = 0.00 × B1 + 8.00)	2.00	8.00	2.00	8.00	2.00	8.00	2.00	8.00	ns
B24	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 0 (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	1.80	—	1.13	—	ns
B24a	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 11 TRLX = 0 (MIN = 0.50 × B1 – 2.00)	13.20	—	10.50	—	5.60	—	4.25	—	ns
B25	CLKOUT rising edge to $\overline{OE}$, $\overline{WE}$(0:3) asserted (MAX = 0.00 × B1 + 9.00)	—	9.00	—	9.00	—	9.00	—	9.00	ns
B26	CLKOUT rising edge to $\overline{OE}$ negated (MAX = 0.00 X B1 + 9.00)	2.00	9.00	2.00	9.00	2.00	9.00	2.00	9.00	ns
B27	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 1 (MIN = 1.25 × B1 – 2.00)	35.90	—	29.30	—	16.90	—	13.60	—	ns

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B29h	$\overline{WE}$(0:3) negated to D(0:31) High-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 1 (MIN = 0.375 × B1 – 3.30)	38.40	—	31.10	—	17.50	—	13.85	—	ns
B29i	$\overline{CS}$ negated to D(0:31) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1 (MIN = 0.375 × B1 – 3.30)	38.40	—	31.10	—	17.50	—	13.85	—	ns
B30	$\overline{CS}$, $\overline{WE}$(0:3) negated to A(0:31), BADDR(28:30) Invalid GPCM read/write access[8] (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	1.80	—	1.13	—	ns
B30a	$\overline{WE}$(0:3) negated to A(0:31), BADDR(28:30) Invalid GPCM, write access, TRLX = 0, CSNT = 1, $\overline{CS}$ negated to A(0:31) invalid GPCM write access TRLX = 0, CSNT =1 ACS = 10, or ACS == 11, EBDF = 0 (MIN = 0.50 × B1 – 2.00)	13.20	—	10.50	—	5.60	—	4.25	—	ns
B30b	$\overline{WE}$(0:3) negated to A(0:31) invalid GPCM BADDR(28:30) invalid GPCM write access, TRLX = 1, CSNT = 1. $\overline{CS}$ negated to A(0:31) invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10, or ACS == 11 EBDF = 0 (MIN = 1.50 × B1 – 2.00)	43.50	—	35.50	—	20.70	—	16.75	—	ns
B30c	$\overline{WE}$(0:3) negated to A(0:31), BADDR(28:30) invalid GPCM write access, TRLX = 0, CSNT = 1. $\overline{CS}$ negated to A(0:31) invalid GPCM write access, TRLX = 0, CSNT = 1 ACS = 10, ACS == 11, EBDF = 1 (MIN = 0.375 × B1 – 3.00)	8.40	—	6.40	—	2.70	—	1.70	—	ns
B30d	$\overline{WE}$(0:3) negated to A(0:31), BADDR(28:30) invalid GPCM write access TRLX = 1, CSNT =1, $\overline{CS}$ negated to A(0:31) invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10 or 11, EBDF = 1	38.67	—	31.38	—	17.83	—	14.19	—	ns
B31	CLKOUT falling edge to $\overline{CS}$ valid, as requested by control bit CST4 in the corresponding word in the UPM (MAX = 0.00 × B1 + 6.00)	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B31a	CLKOUT falling edge to $\overline{CS}$ valid, as requested by control bit CST1 in the corresponding word in the UPM (MAX = 0.25 × B1 + 6.80)	7.60	14.30	6.30	13.00	3.80	10.50	3.13	10.00	ns
B31b	CLKOUT rising edge to $\overline{CS}$ valid, as requested by control bit CST2 in the corresponding word in the UPM (MAX = 0.00 × B1 + 8.00)	1.50	8.00	1.50	8.00	1.50	8.00	1.50	8.00	ns
B31c	CLKOUT rising edge to $\overline{CS}$ valid, as requested by control bit CST3 in the corresponding word in the UPM (MAX = 0.25 × B1 + 6.30)	7.60	13.80	6.30	12.50	3.80	10.00	3.13	9.40	ns
B31d	CLKOUT falling edge to $\overline{CS}$ valid, as requested by control bit CST1 in the corresponding word in the UPM EBDF = 1 (MAX = 0.375 × B1 + 6.6)	13.30	18.00	11.30	16.00	7.60	12.30	4.69	11.30	ns

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B36	A(0:31), BADDR(28:30), and D(0:31) to $\overline{\text{GPL}}$ valid, as requested by control bit GxT4 in the corresponding word in the UPM (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	1.80	—	1.13	—	ns
B37	UPWAIT valid to CLKOUT falling edge[9] (MIN = 0.00 × B1 + 6.00)	6.00	—	6.00	—	6.00	—	6.00	—	ns
B38	CLKOUT falling edge to UPWAIT valid [9] (MIN = 0.00 × B1 + 1.00)	1.00	—	1.00	—	1.00	—	1.00	—	ns
B39	$\overline{\text{AS}}$ valid to CLKOUT rising edge[10] (MIN = 0.00 × B1 + 7.00)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B40	A(0:31), TSIZ(0:1), RD/$\overline{\text{WR}}$, $\overline{\text{BURST}}$, valid to CLKOUT rising edge (MIN = 0.00 × B1 + 7.00)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B41	$\overline{\text{TS}}$ valid to CLKOUT rising edge (setup time) (MIN = 0.00 × B1 + 7.00)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B42	CLKOUT rising edge to $\overline{\text{TS}}$ valid (hold time) (MIN = 0.00 × B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B43	$\overline{\text{AS}}$ negation to memory controller signals negation (MAX = TBD)	—	TBD	—	TBD	—	TBD	—	TBD	ns

1 For part speeds above 50 MHz, use 9.80 ns for B11a.

2 The timing required for $\overline{\text{BR}}$ input is relevant when the MPC885/MPC880 is selected to work with the internal bus arbiter. The timing for $\overline{\text{BG}}$ input is relevant when the MPC885/MPC880 is selected to work with the external bus arbiter.

3 For part speeds above 50 MHz, use 2 ns for B17.

4 The D(0:31) input timings B18 and B19 refer to the rising edge of the CLKOUT in which the $\overline{\text{TA}}$ input signal is asserted.

5 For part speeds above 50 MHz, use 2 ns for B19.

6 The D(0:31) input timings B20 and B21 refer to the falling edge of the CLKOUT. This timing is valid only for read accesses controlled by chip-selects under control of the user-programmable machine (UPM) in the memory controller, for data beats where DLT3 = 1 in the RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

7 This formula applies to bus operation up to 50 MHz.

8 The timing B30 refers to $\overline{\text{CS}}$ when ACS = 00 and to $\overline{\text{CS}}$ and $\overline{\text{WE}}$(0:3) when CSNT = 0.

9 The signal UPWAIT is considered asynchronous to the CLKOUT and synchronized internally. The timings specified in B37 and B38 are specified to enable the freeze of the UPM output signals as described in Figure 21.

10 The $\overline{\text{AS}}$ signal is considered asynchronous to the CLKOUT. The timing B39 is specified in order to allow the behavior specified in Figure 24.

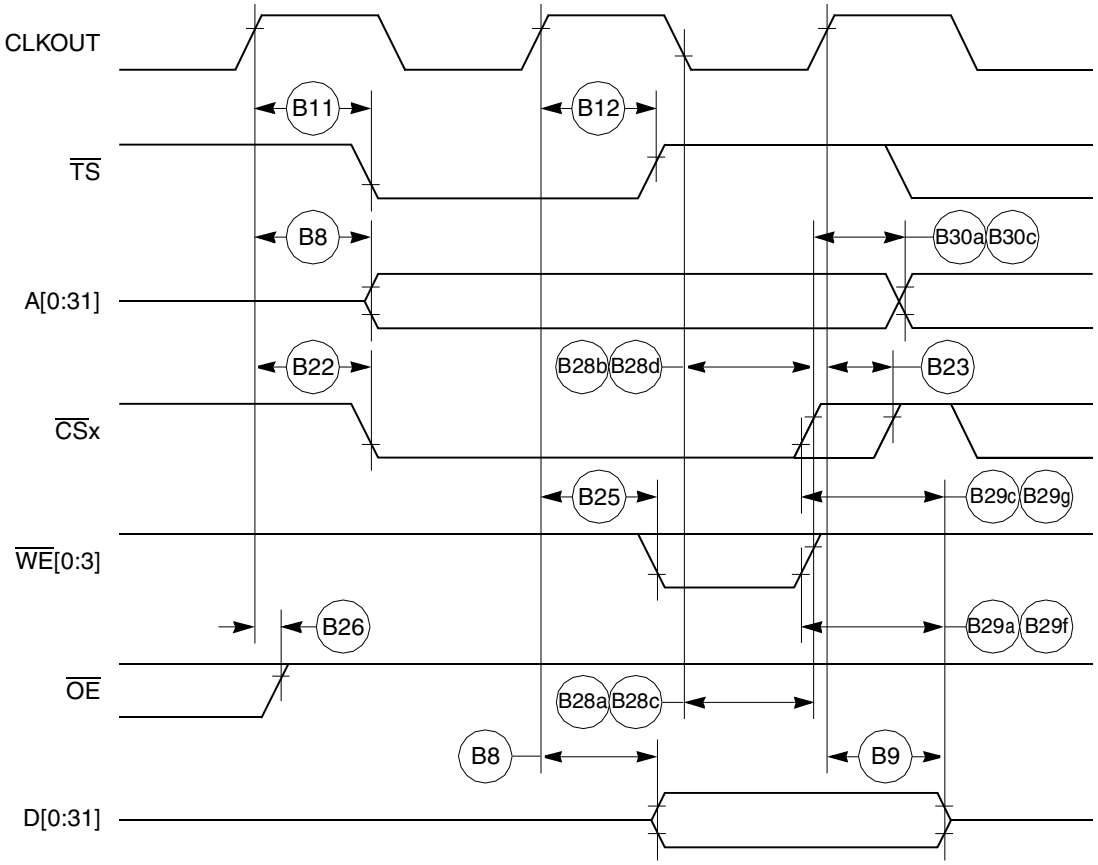

Figure 18. External Bus Write Timing (GPCM Controlled—TRLX = 0, CSNT = 1)

Table 12 shows the PCMCIA port timing for the MPC885/MPC880.

Table 12. PCMCIA Port Timing

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
P57	CLKOUT to OPx valid (MAX = 0.00 × B1 + 19.00)	—	19.00	—	19.00	—	19.00	—	19.00	ns
P58	$\overline{\text{HRESET}}$ negated to OPx drive[1] (MIN = 0.75 × B1 + 3.00)	25.70	—	21.70	—	14.40	—	12.40	—	ns
P59	IP_Xx valid to CLKOUT rising edge (MIN = 0.00 × B1 + 5.00)	5.00	—	5.00	—	5.00	—	5.00	—	ns
P60	CLKOUT rising edge to IP_Xx invalid (MIN = 0.00 × B1 + 1.00)	1.00	—	1.00	—	1.00	—	1.00	—	ns

1 OP2 and OP3 only.

Figure 31 provides the PCMCIA output port timing for the MPC885/MPC880.

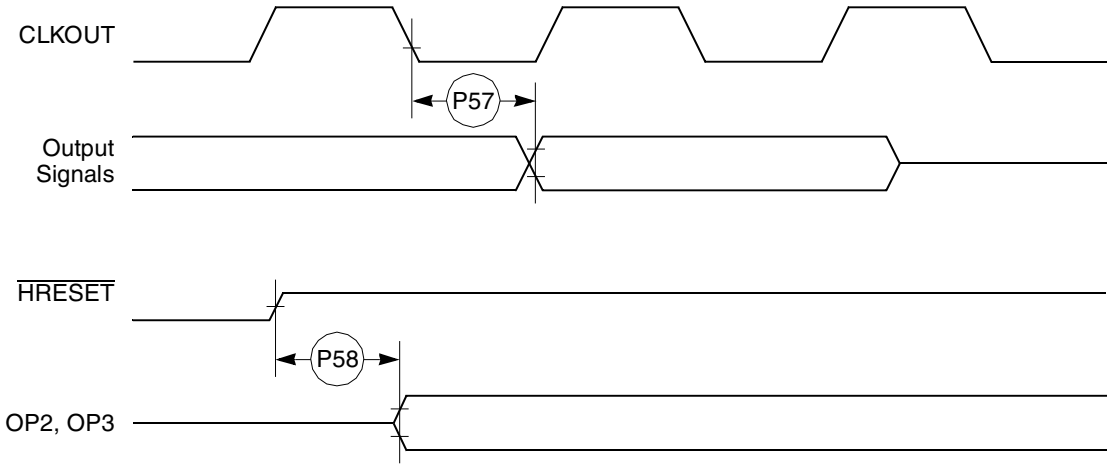

Figure 31. PCMCIA Output Port Timing

Figure 32 provides the PCMCIA input port timing for the MPC885/MPC880.

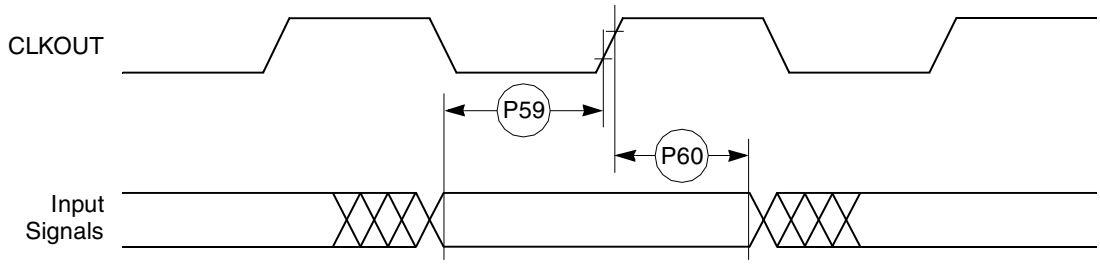

Figure 32. PCMCIA Input Port Timing

Table 21. SI Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
76	L1RXD valid to L1CLK edge (L1RXD setup time)	17.00	—	ns
77	L1CLK edge to L1RXD invalid (L1RXD hold time)	13.00	—	ns
78	L1CLK edge to L1ST(1–4) valid[4]	10.00	45.00	ns
78A	L1SYNC valid to L1ST(1–4) valid	10.00	45.00	ns
79	L1CLK edge to L1ST(1–4) invalid	10.00	45.00	ns
80	L1CLK edge to L1TXD valid	10.00	55.00	ns
80A	L1TSYNC valid to L1TXD valid[4]	10.00	55.00	ns
81	L1CLK edge to L1TXD high impedance	0.00	42.00	ns
82	L1RCLK, L1TCLK frequency (DSC =1)	—	16.00 or SYNCCLK/2	MHz
83	L1RCLK, L1TCLK width low (DSC =1)	P + 10	—	ns
83a	L1RCLK, L1TCLK width high (DSC = 1)[3]	P + 10	—	ns
84	L1CLK edge to L1CLKO valid (DSC = 1)	—	30.00	ns
85	$\overline{\text{L1RQ}}$ valid before falling edge of L1TSYNC[4]	1.00	—	L1TCLK
86	L1GR setup time[2]	42.00	—	ns
87	L1GR hold time	42.00	—	ns
88	L1CLK edge to L1SYNC valid (FSD = 00) CNT = 0000, BYT = 0, DSC = 0)	—	0.00	ns

1 The ratio SyncCLK/L1RCLK must be greater than 2.5/1.
2 These specs are valid for IDL mode only.
3 Where P = 1/CLKOUT. Thus for a 25-MHz CLKO1 rate, P = 40 ns.
4 These strobes and TxD on the first bit of the frame become valid after L1CLK edge or L1SYNC, whichever comes later.

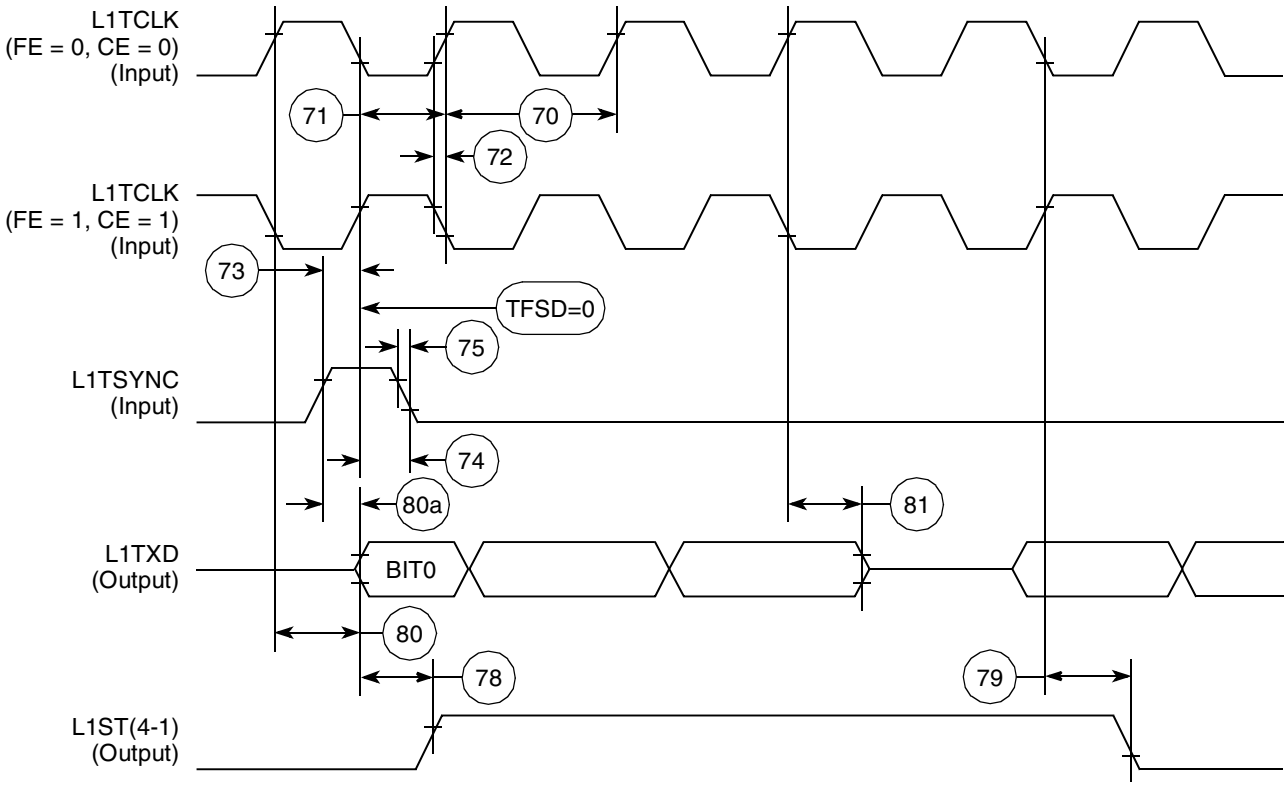

Figure 56. SI Transmit Timing Diagram (DSC = 0)

Figure 59 through Figure 61 show the NMSI timings.

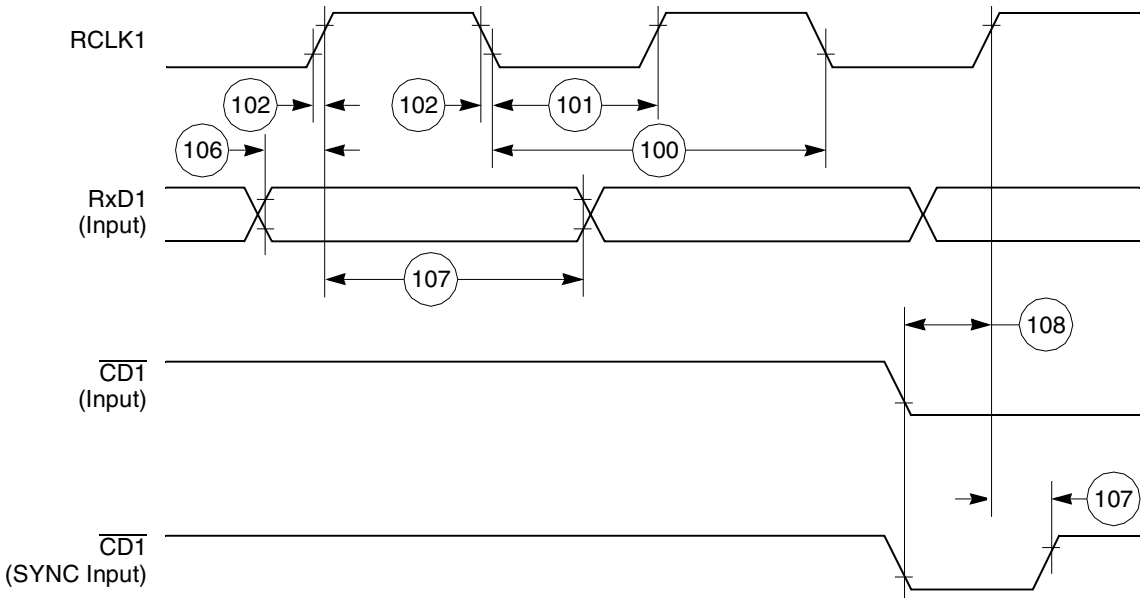

Figure 59. SCC NMSI Receive Timing Diagram

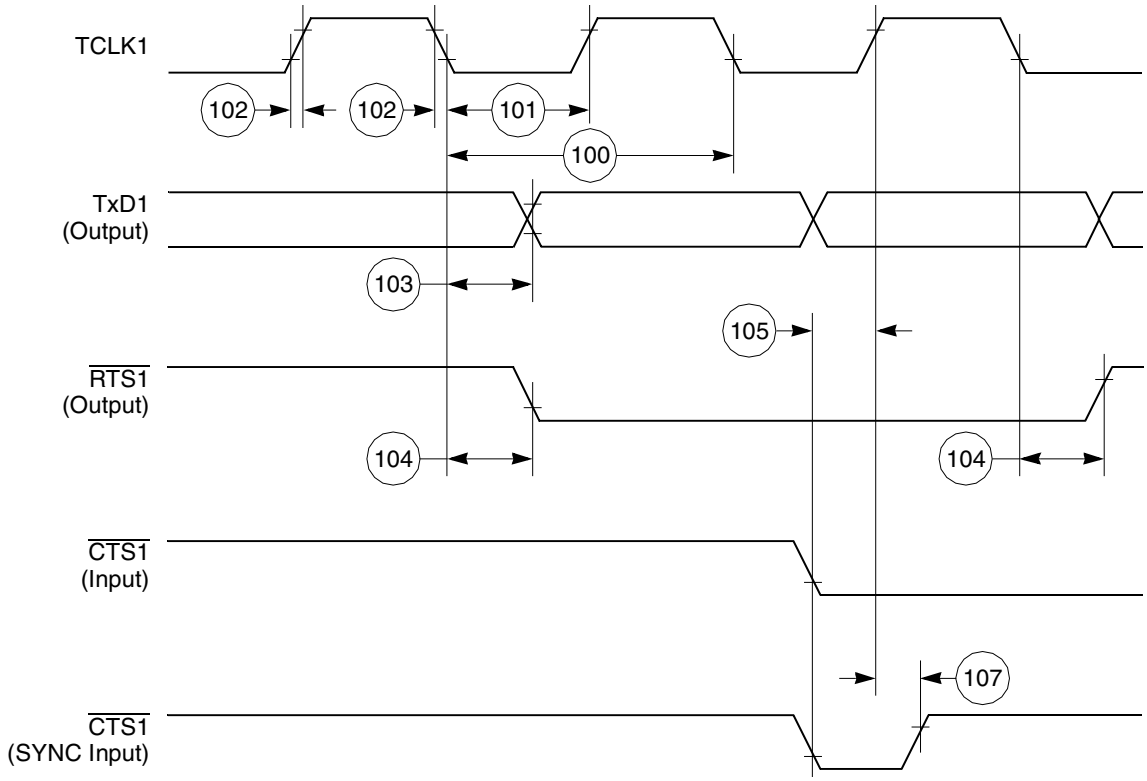

Figure 60. SCC NMSI Transmit Timing Diagram

12.11 SPI Slave AC Electrical Specifications

Table 27 provides the SPI slave timings as shown in Figure 68 and Figure 69.

Table 27. SPI Slave Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
170	Slave cycle time	2	—	t_{cyc}
171	Slave enable lead time	15	—	ns
172	Slave enable lag time	15	—	ns
173	Slave clock (SPICLK) high or low time	1	—	t_{cyc}
174	Slave sequential transfer delay (does not require deselect)	1	—	t_{cyc}
175	Slave data setup time (inputs)	20	—	ns
176	Slave data hold time (inputs)	20	—	ns
177	Slave access time	—	50	ns

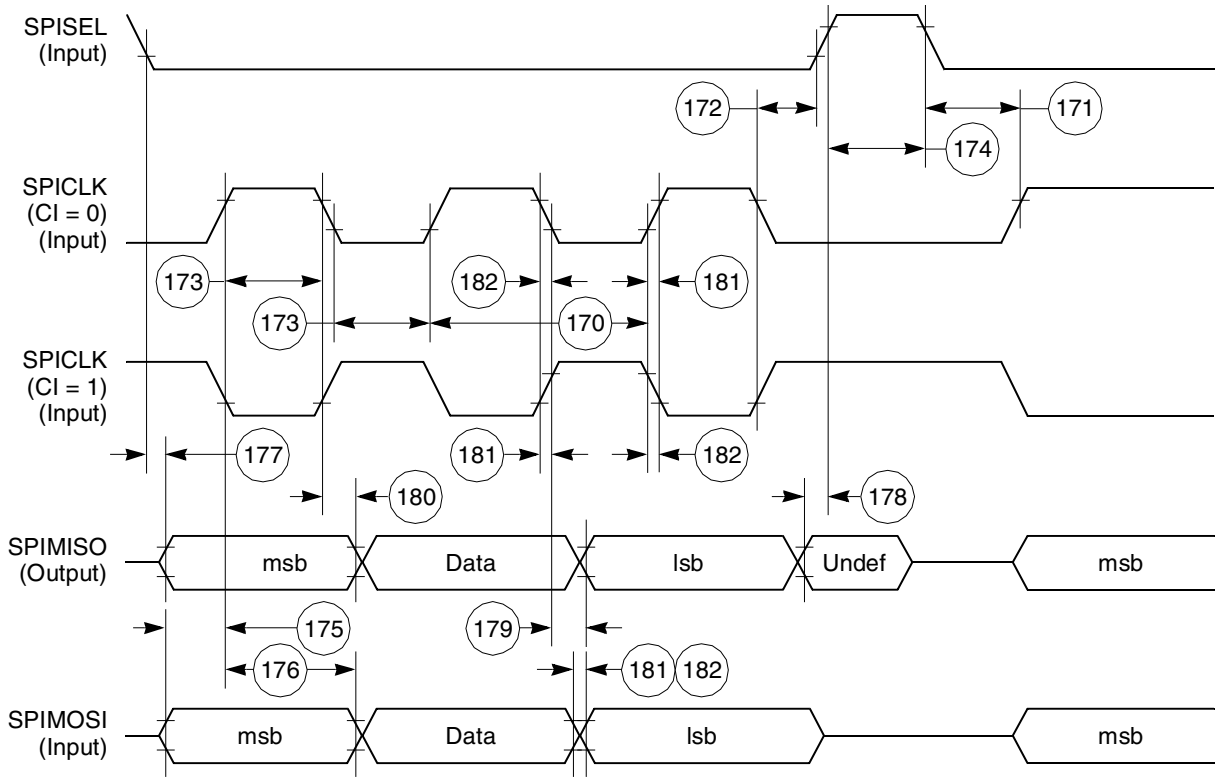

Figure 68. SPI Slave (CP = 0) Timing Diagram

16.1 Pin Assignments

Figure 77 shows the top-view pinout of the PBGA package. For additional information, see the *MPC885 PowerQUICC™ Family Reference Manual*.

NOTE: This is the top view of the device.

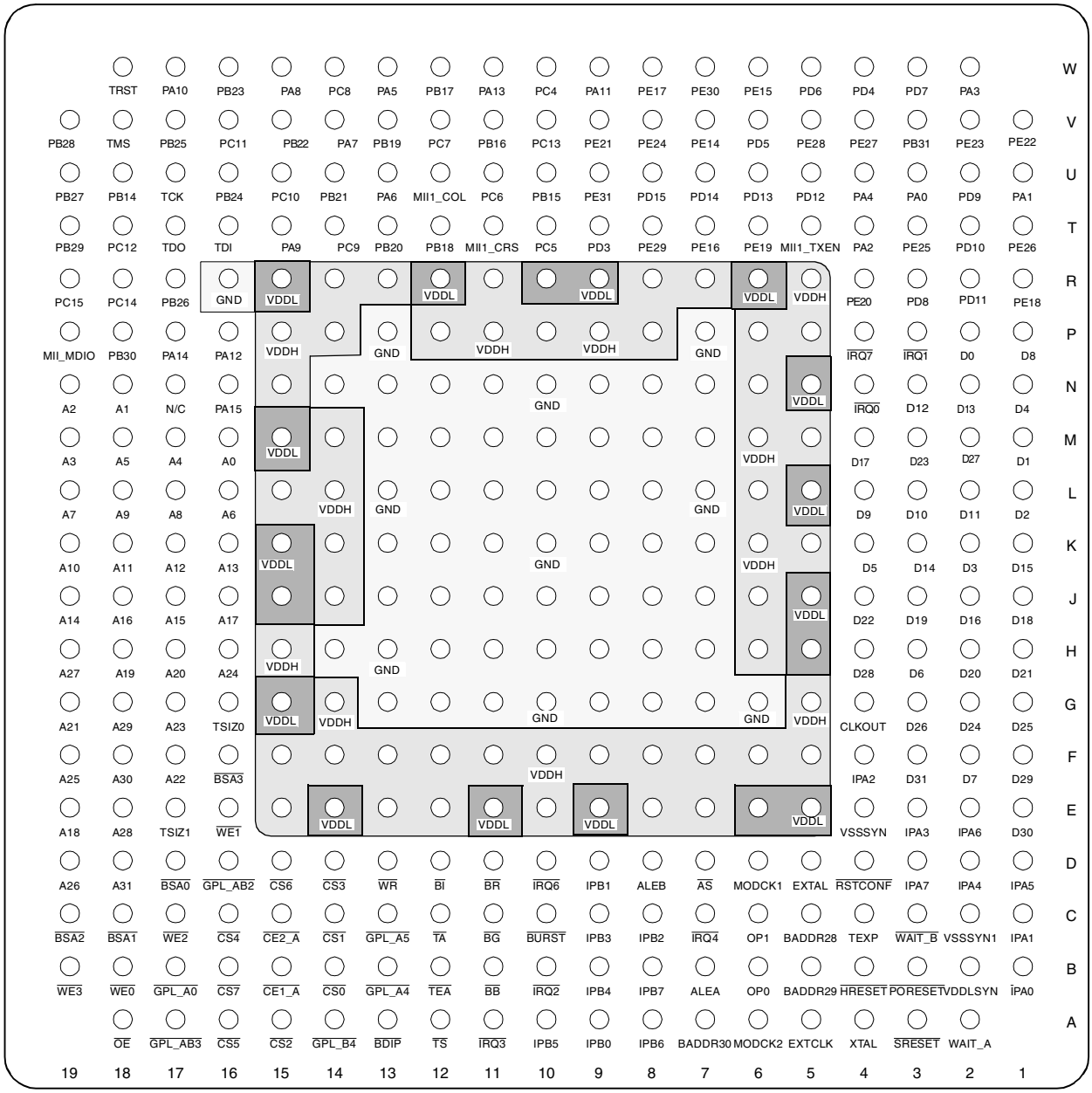

Figure 77. Pinout of the PBGA Package

Table 39. Pin Assignments (continued)

Name	Pin Number	Type
WE0, BS_B0, IORD	B18	Output
WE1, BS_B1, IOWR	E16	Output
WE2, BS_B2, PCOE	C17	Output
WE3, BS_B3, PCWE	B19	Output
BS_A[0:3]	D17, C18, C19, F16	Output
GPL_A0, GPL_B0	B17	Output
OE, GPL_A1, GPL_B1	A18	Output
GPL_A[2:3], GPL_B[2:3], CS[2:3]	D16, A17	Output
UPWAITA, GPL_A4	B13	Bidirectional
UPWAITB, GPL_B4	A14	Bidirectional
GPL_A5	C13	Output
PORESET	B3	Input
RSTCONF	D4	Input
HRESET	B4	Open-drain
SRESET	A3	Open-drain
XTAL	A4	Analog output
EXTAL	D5	Analog input (3.3 V only)
CLKOUT	G4	Output
EXTCLK	A5	Input (3.3 V only)
TEXP	C4	Output
ALE_A	B7	Output
CE1_A	B15	Output
CE2_A	C15	Output
WAIT_A, SOC_Split[1]	A2	Input
WAIT_B	C3	Input
IP_A0, UTPB_Split0[1]	B1	Input
IP_A1, UTPB_Split1[1]	C1	Input
IP_A2, IOIS16_A, UTPB_Split2[1]	F4	Input
IP_A3, UTPB_Split3[1]	E3	Input
IP_A4, UTPB_Split4[1]	D2	Input
IP_A5, UTPB_Split5[1]	D1	Input
IP_A6, UTPB_Split6[1]	E2	Input
IP_A7, UTPB_Split7[1]	D3	Input

Table 39. Pin Assignments (continued)

Name	Pin Number	Type
PA4, $\overline{\text{CTS4}}$, MII1-TXD1, RMII1-TXD1	U4	Bidirectional
PA3, MII1-RXER, RMII1-RXER, BRGO3	W2	Bidirectional
PA2, MII1-RXDV, RMII1-CRS_DV, TXD4	T4	Bidirectional
PA1, MII1-RXD0, RMII1-RXD0, BRGO4	U1	Bidirectional
PA0, MII1-RXD1, RMII1-RXD1, $\overline{\text{TOUT4}}$	U3	Bidirectional
PB31, $\overline{\text{SPISEL}}$, MII1-TXCLK, RMII1-REFCLK	V3	Bidirectional (Optional: open-drain)
PB30, SPICLK	P18	Bidirectional (Optional: open-drain)
PB29, SPIMOSI	T19	Bidirectional (Optional: open-drain)
PB28, SPIMISO, BRGO4	V19	Bidirectional (Optional: open-drain)
PB27, I2CSDA, BRGO1	U19	Bidirectional (Optional: open-drain)
PB26, I2CSCL, BRGO2	R17	Bidirectional (Optional: open-drain)
PB25, RXADDR3[1], TXADDR3, SMTXD1	V17	Bidirectional (Optional: open-drain)
PB24, TXADDR3[1], RXADDR3, SMRXD1	U16	Bidirectional (Optional: open-drain)
PB23, TXADDR2[1], RXADDR2, $\overline{\text{SDACK1}}$, $\overline{\text{SMSYN1}}$	W16	Bidirectional (Optional: open-drain)
PB22, TXADDR4[1], RXADDR4, $\overline{\text{SDACK2}}$, $\overline{\text{SMSYN2}}$	V15	Bidirectional (Optional: open-drain)
PB21, SMTXD2, TXADDR1[1], BRG01, RXADDR1, PHSEL[1]	U14	Bidirectional (Optional: open-drain)
PB20, SMRXD2, L1CLKOA, TXADDR0[1], RXADDR0, PHSEL[0]	T13	Bidirectional (Optional: open-drain)
PB19, MII1-RXD3, $\overline{\text{RTS4}}$	V13	Bidirectional (Optional: open-drain)
PB18, RXADDR4[1], TXADDR4, $\overline{\text{RTS2}}$, L1ST2	T12	Bidirectional (Optional: open-drain)

Table 39. Pin Assignments (continued)

Name	Pin Number	Type
PE14, RXD3, MII2-TXD0, RMII2-TXD0	V7	Bidirectional
TMS	V18	Input
TDI, DSDI	T16	Input
TCK, DSCK	U17	Input
$\overline{\text{TRST}}$	W18	Input
TDO, DSDO	T17	Output
MII1_CRS	T11	Input
MII_MDIO	P19	Bidirectional
MII1_TXEN, RMII1_TXEN	T5	Output
MII1_COL	U12	Input
V_{SSSYN1}	C2	PLL analog V_{DD} and GND
V_{SSSYN}	E4	Power
V_{DDLSYN}	B2	Power
GND	G6, G7, G8, G9, G10, G11, G12, G13, H7, H8, H9, H10, H11, H12, H13, H14, J7, J8, J9, J10, J11, J12, J13, K7, K8, K9, K10, K11, K12, K13, L7, L8, L9, L10, L11, L12, L13, M7, M8, M9, M10, M11, M12, M13, N7, N8, N9, N10, N11, N12, N13, N14, P7, P13, R16	Power
V_{DDL}	E5, E6, E9, E11, E14, G15, H5, J5, J15, K15, L5, M15, N5, R6, R9, R10, R12, R15	Power
V_{DDH}	E7, E8, E10, E12, E13, E15, F5, F6, F7, F8, F9, F10, F11, F12, F13, F14, F15, G5, G14, H6, H15, J6, J14, K5, K6, K14, L6, L14, L15, M5, M6, M14, N6, N15, P5, P6, P8, P9, P10, P11, P12, P14, P15, R5, R7, R8, R11, R13, R14	Power
N/C	N17	No connect

[1] ESAR mode only.

17 Document Revision History

Table 40 lists significant changes between revisions of this hardware specification.

Table 40. Document Revision History

Revision Number	Date	Changes
7	07/2010	In Table 9, "Bus Operation Timings," changed the following: • Updated TRLX condition value for B22a/b/c to "TRLX = [0 or 1]" • Removed TRLX condition for B23 • Updated condition and equation for B30 to "Invalid GPCM read/write access (MIN = 0.25 × B1 – 2.00)" • Updated note 8 to "The timing B30 refers to $\overline{CS}$ when ACS = 00 and to $\overline{CS}$ and $\overline{WE}$(0:3) when CSNT = 0."
6	05/2010	Added minimum load for CLKOUT in Section 10, "Bus Signal Timing."
5	03/2009	Updated formatting of Table 12 , "PCMCIA Port Timing," Table 13, "Debug Port Timing," Table 14, "Reset Timing," and Table 15, "JTAG Timing."
4	08/2007	• On page 1, updated first paragraph and added a second paragraph. • After Table 2, inserted a new figure showing the undershoot/overshoot voltage (Figure 3) and renumbered the rest of the figures. • In Table 9, for reset timings B29f and B29g added footnote indicating that the formula only applies to bus operation up to 50 MHz. • In Figure 6, changed all reference voltage measurement points from 0.2 and 0.8 V to 50% level. • In Table 18, changed num 46 description to read, "$\overline{TA}$ assertion to rising edge ..." • In Figure 49, changed $\overline{TA}$ to reflect the rising edge of the clock.
3.0	7/22/2004	• Added sentence to Spec B1A about EXTCLK and CLKOUT being in Alignment for Integer Values • Added a footnote to Spec 41 specifying that EDM = 1 • Added RMII1_EN under M1II_EN in Table 36 Pin Assignments • Added a tablefootnote to Table 6 DC Electrical Specifications about meeting the VIL Max of the I2C Standard • Put the new part numbers in the Ordering Information Section
2.0	12/2003	• Changed the maximum operating frequency to 133 MHz. • Put in the orderable part numbers that are orderable. • Put the timing in the 80 MHz column. • Rounded the timings to hundredths in the 80 MHz column. • Put the pin numbers in footnotes by the maximum currents in Table 6. • Changed 22 and 41 in the Timing. • Put in the Thermal numbers.
1.0	9/2003	• Added the DSP information in the Features list • Fixed table formatting. • Nontechnical edits. • Released to the external web.
0.9	8/2003	Changed the USB description to full-/low-speed compatible.
0.8	8/2003	Added the Reference to USB 2.0 to the Features list and removed 1.1 from USB on the block diagrams.
0.7	7/2003	Added the RxClav and TxClav signals to PC15.
0.6	6/2003	Changed the pin descriptions per the June 22 spec.
0.5	5/2003	Changed some more typos, put in the phsel and phreq pins. Corrected the USB timing.

Table 40. Document Revision History (continued)

Revision Number	Date	Changes
0.4	5/2003	Changed the pin descriptions for PD8 and PD9.
0.3	05/2003	Corrected the signals that had overlines on them.
0.2	05/2003	Made the changes to the RMII Timing, Made sure all the V_{DDL}, V_{DDH}, and GND show up on the pinout diagram. Changed the SPI Master Timing Specs. 162 and 164.
0.1	04/2003	Added pinout and pinout assignments table. Added the USB timing to Section 14. Added the Reduced MII to Section 15. Removed the Data Parity. Made some changes to the Features list.
0	02/2003	Initial revision.