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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	133MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (2), 10/100Mbps (2)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc880vr133

Table 3. Operating Temperatures

Rating	Symbol	Value	Unit
Temperature[1] (standard)	$T_{A(min)}$	0	°C
	$T_{J(max)}$	95	°C
Temperature (extended)	$T_{A(min)}$	–40	°C
	$T_{J(max)}$	100	°C

1 Minimum temperatures are guaranteed as ambient temperature, T_A. Maximum temperatures are guaranteed as junction temperature, T_J.

This device contains circuitry protecting against damage due to high-static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{DD}).

4 Thermal Characteristics

Table 4 shows the thermal characteristics for the MPC885/MPC880.

Table 4. MPC885/MPC880 Thermal Resistance Data

Rating	Environment		Symbol	Value	Unit
Junction-to-ambient[1]	Natural convection	Single-layer board (1s)	$R_{\theta JA}$[2]	37	°C/W
		Four-layer board (2s2p)	$R_{\theta JMA}$[3]	25	
	Airflow (200 ft/min)	Single-layer board (1s)	$R_{\theta JMA}$[3]	30	
		Four-layer board (2s2p)	$R_{\theta JMA}$[3]	22	
Junction-to-board[4]	—	—	$R_{\theta JB}$	17	
Junction-to-case [5]	—	—	$R_{\theta JC}$	10	
Junction-to-package top[6]	Natural convection	—	Ψ_{JT}	2	
	Airflow (200 ft/min)	—	Ψ_{JT}	2	

1 Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.

2 Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature. For exposed pad packages where the pad would be expected to be soldered, junction-to-case thermal resistance is a simulated value from the junction to the exposed pad without contact resistance.

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B32	CLKOUT falling edge to $\overline{BS}$ valid, as requested by control bit BST4 in the corresponding word in the UPM (MAX = 0.00 × B1 + 6.00)	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B32a	CLKOUT falling edge to $\overline{BS}$ valid, as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 0 (MAX = 0.25 × B1 + 6.80)	7.60	14.30	6.30	13.00	3.80	10.50	3.13	10.00	ns
B32b	CLKOUT rising edge to $\overline{BS}$ valid, as requested by control bit BST2 in the corresponding word in the UPM (MAX = 0.00 × B1 + 8.00)	1.50	8.00	1.50	8.00	1.50	8.00	1.50	8.00	ns
B32c	CLKOUT rising edge to $\overline{BS}$ valid, as requested by control bit BST3 in the corresponding word in the UPM (MAX = 0.25 × B1 + 6.80)	7.60	14.30	6.30	13.00	3.80	10.50	3.13	10.00	ns
B32d	CLKOUT falling edge to $\overline{BS}$ valid, as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 1 (MAX = 0.375 × B1 + 6.60)	13.30	18.00	11.30	16.00	7.60	12.30	4.49	11.30	ns
B33	CLKOUT falling edge to $\overline{GPL}$ valid, as requested by control bit GxT4 in the corresponding word in the UPM (MAX = 0.00 × B1 + 6.00)	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B33a	CLKOUT rising edge to $\overline{GPL}$ valid, as requested by control bit GxT3 in the corresponding word in the UPM (MAX = 0.25 × B1 + 6.80)	7.60	14.30	6.30	13.00	3.80	10.50	3.13	10.00	ns
B34	A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid, as requested by control bit CST4 in the corresponding word in the UPM (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	1.80	—	1.13	—	ns
B34a	A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid, as requested by control bit CST1 in the corresponding word in the UPM (MIN = 0.50 × B1 – 2.00)	13.20	—	10.50	—	5.60	—	4.25	—	ns
B34b	A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid, as requested by CST2 in the corresponding word in UPM (MIN = 0.75 × B1 – 2.00)	20.70	—	16.70	—	9.40	—	6.80	—	ns
B35	A(0:31), BADDR(28:30) to $\overline{CS}$ valid, as requested by control bit BST4 in the corresponding word in the UPM (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	1.80	—	1.13	—	ns
B35a	A(0:31), BADDR(28:30), and D(0:31) to $\overline{BS}$ valid, as requested by BST1 in the corresponding word in the UPM (MIN = 0.50 × B1 – 2.00)	13.20	—	10.50	—	5.60	—	4.25	—	ns
B35b	A(0:31), BADDR(28:30), and D(0:31) to $\overline{BS}$ valid, as requested by control bit BST2 in the corresponding word in the UPM (MIN = 0.75 × B1 – 2.00)	20.70	—	16.70	—	9.40	—	7.40	—	ns

Figure 8 provides the timing for the synchronous output signals.

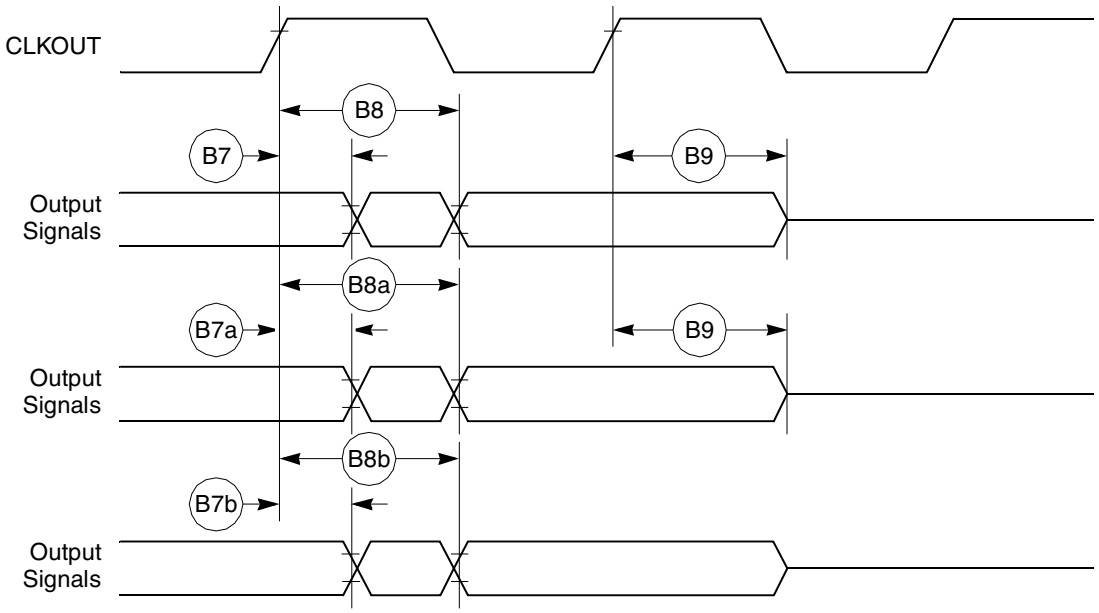

Figure 8. Synchronous Output Signals Timing

Figure 9 provides the timing for the synchronous active pull-up and open-drain output signals.

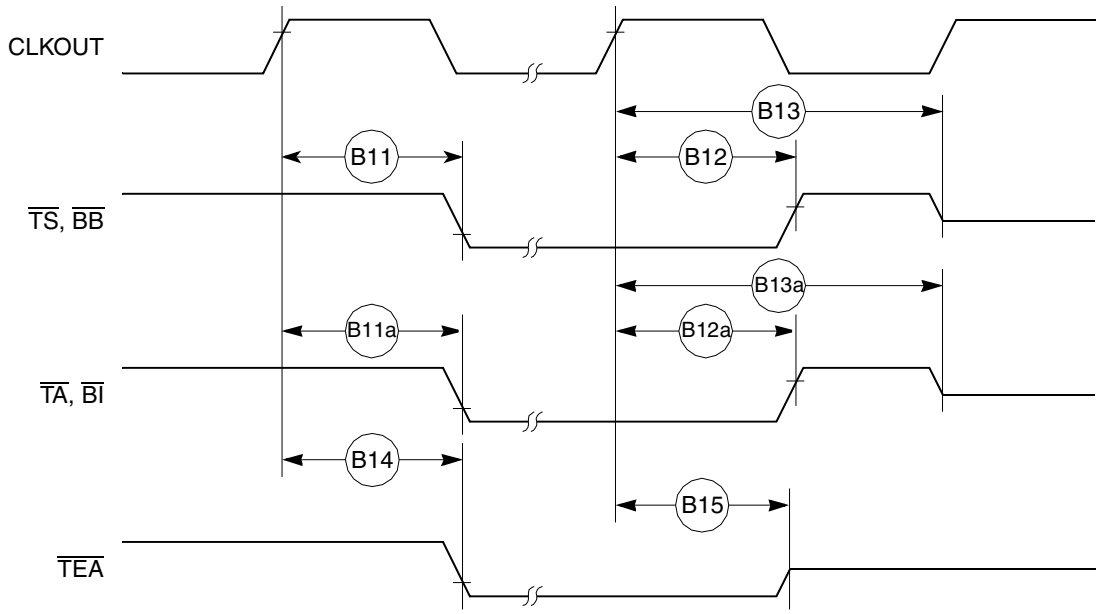

Figure 9. Synchronous Active Pull-Up Resistor and Open-Drain Outputs Signals Timing

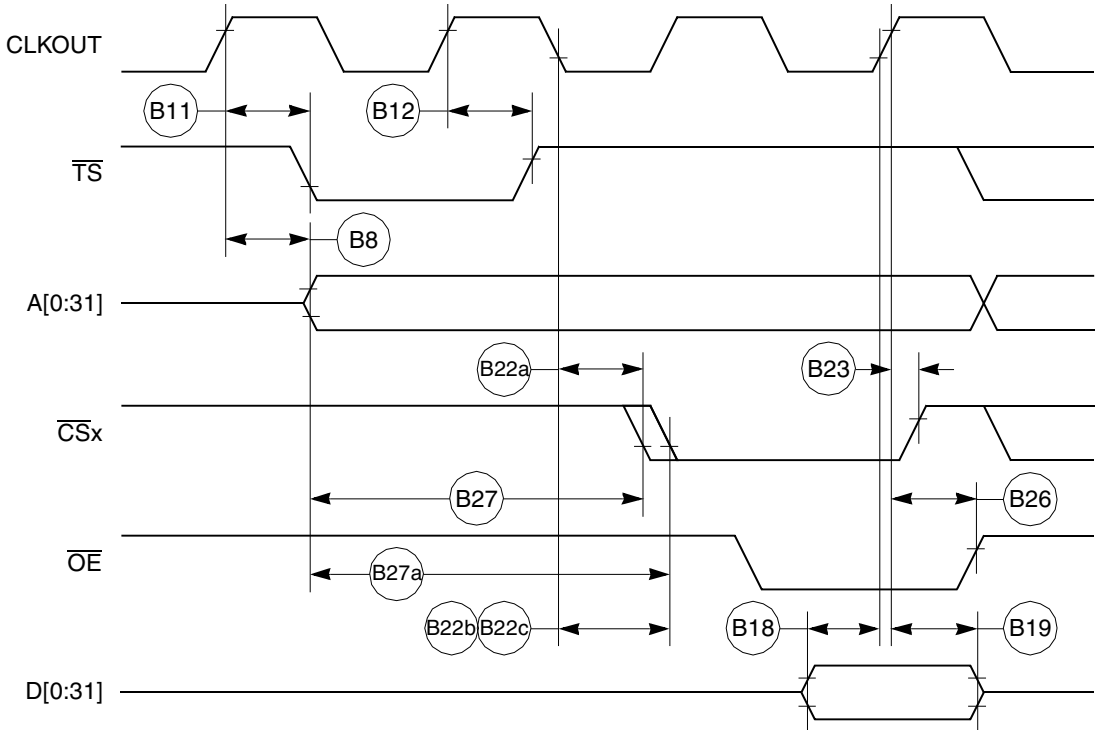

Figure 16. External Bus Read Timing (GPCM Controlled—TRLX = 1, ACS = 10, ACS = 11)

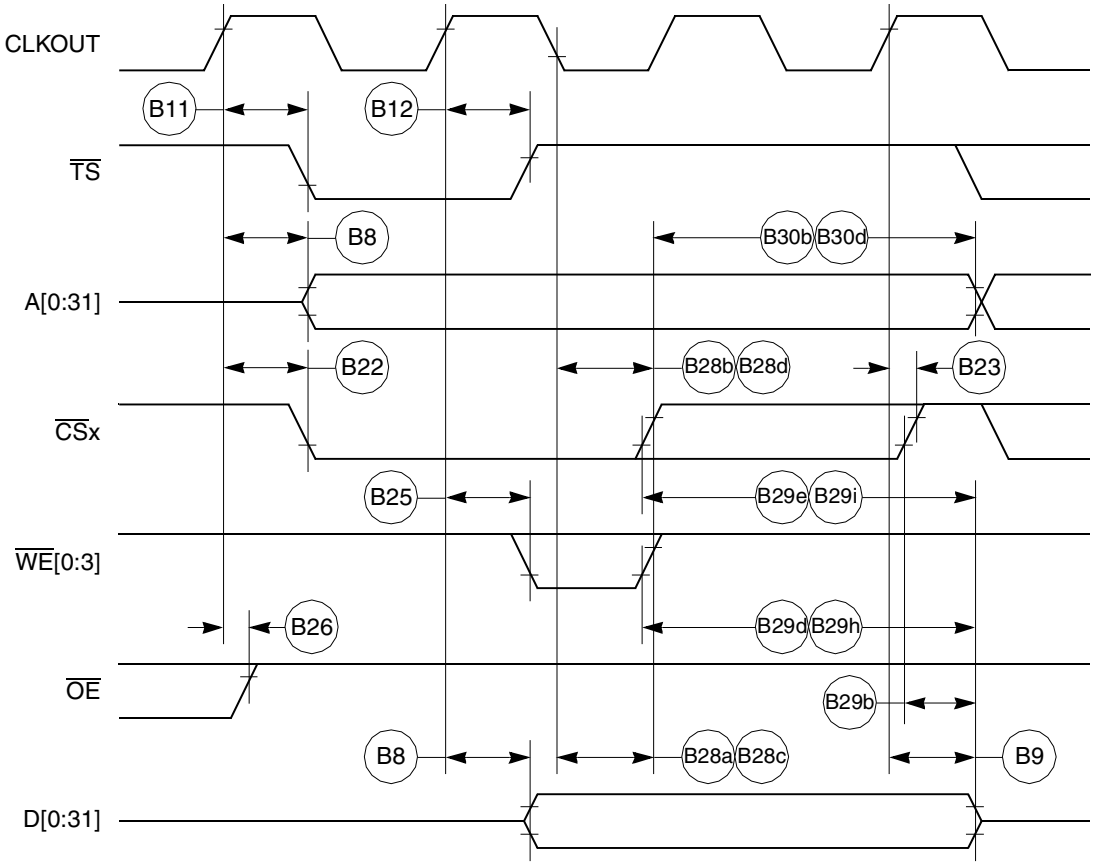

Figure 19. External Bus Write Timing (GPCM Controlled—TRLX = 1, CSNT = 1)

Figure 20 provides the timing for the external bus controlled by the UPM.

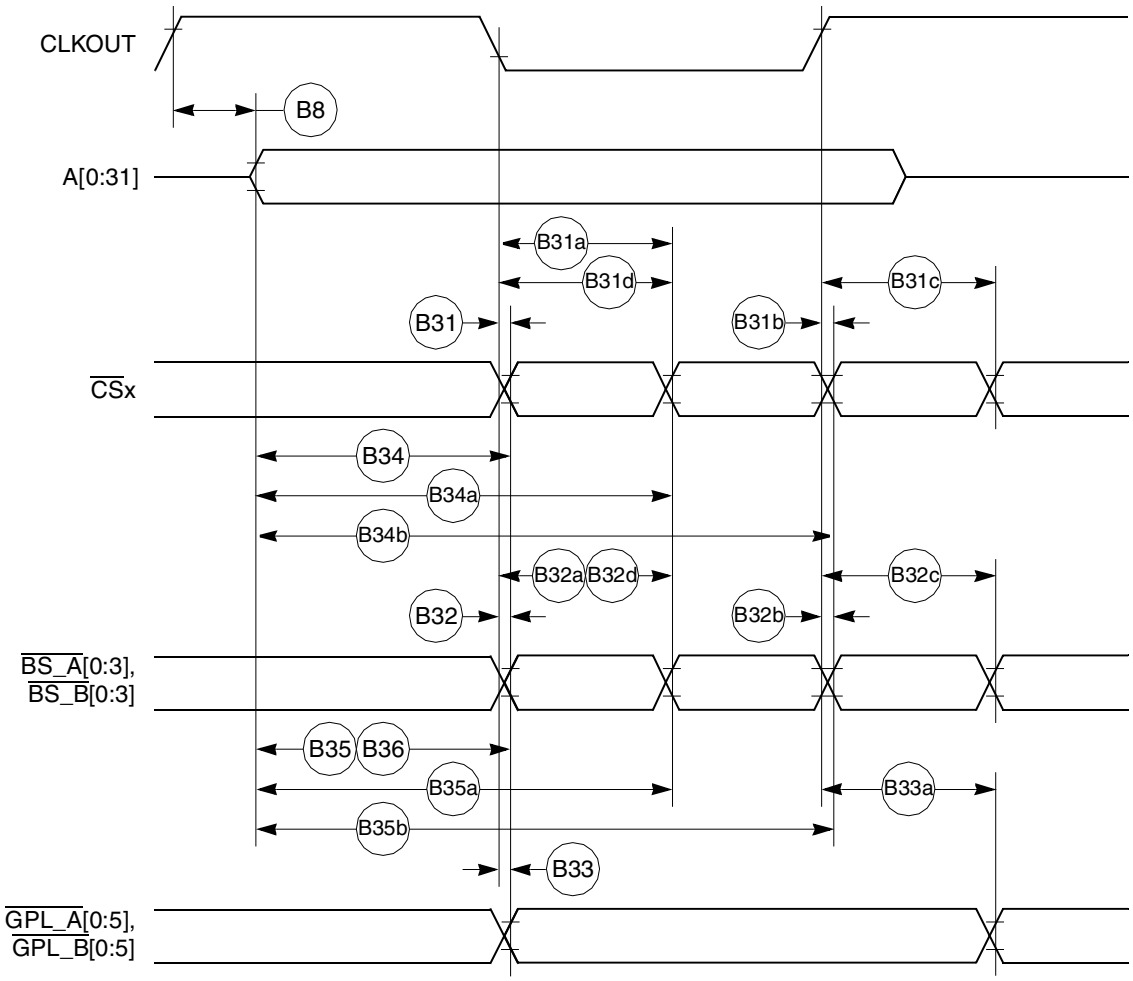

Figure 20. External Bus Timing (UPM-Controlled Signals)

Figure 21 provides the timing for the asynchronous asserted UPWAIT signal controlled by the UPM.

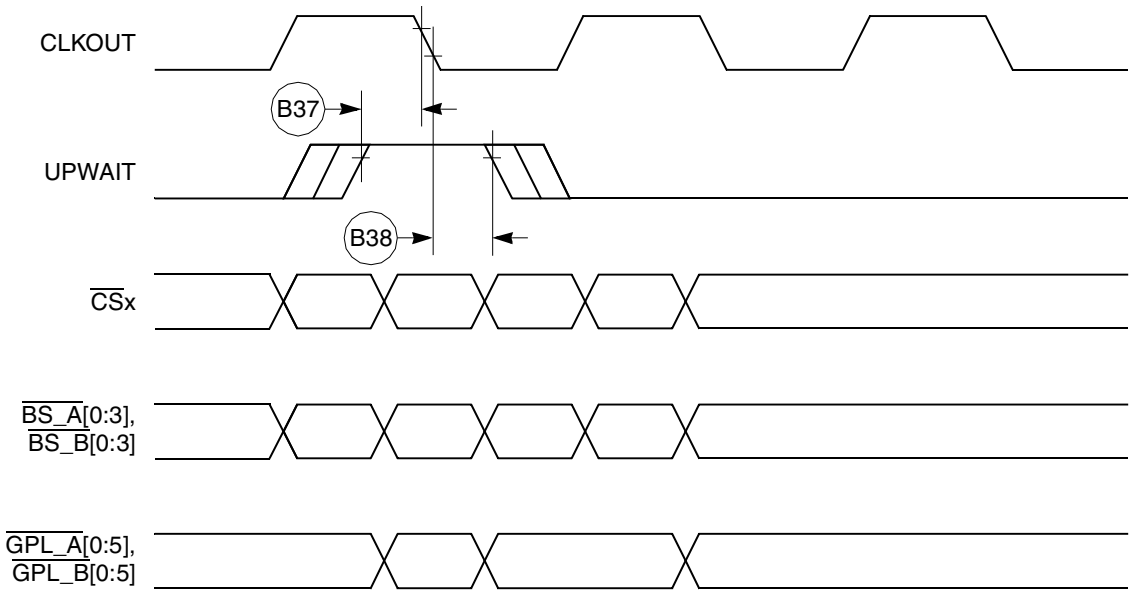

Figure 21. Asynchronous UPWAIT Asserted Detection in UPM-Handled Cycles Timing

Figure 22 provides the timing for the asynchronous negated UPWAIT signal controlled by the UPM.

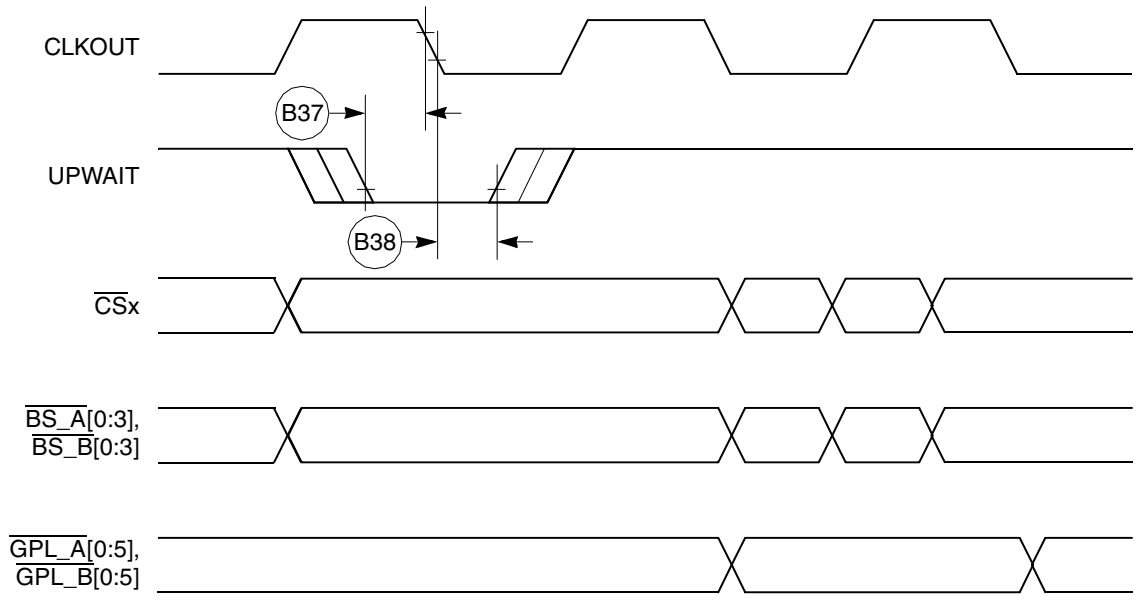

Figure 22. Asynchronous UPWAIT Negated Detection in UPM-Handled Cycles Timing

Figure 28 provides the PCMCIA access cycle timing for the external bus read.

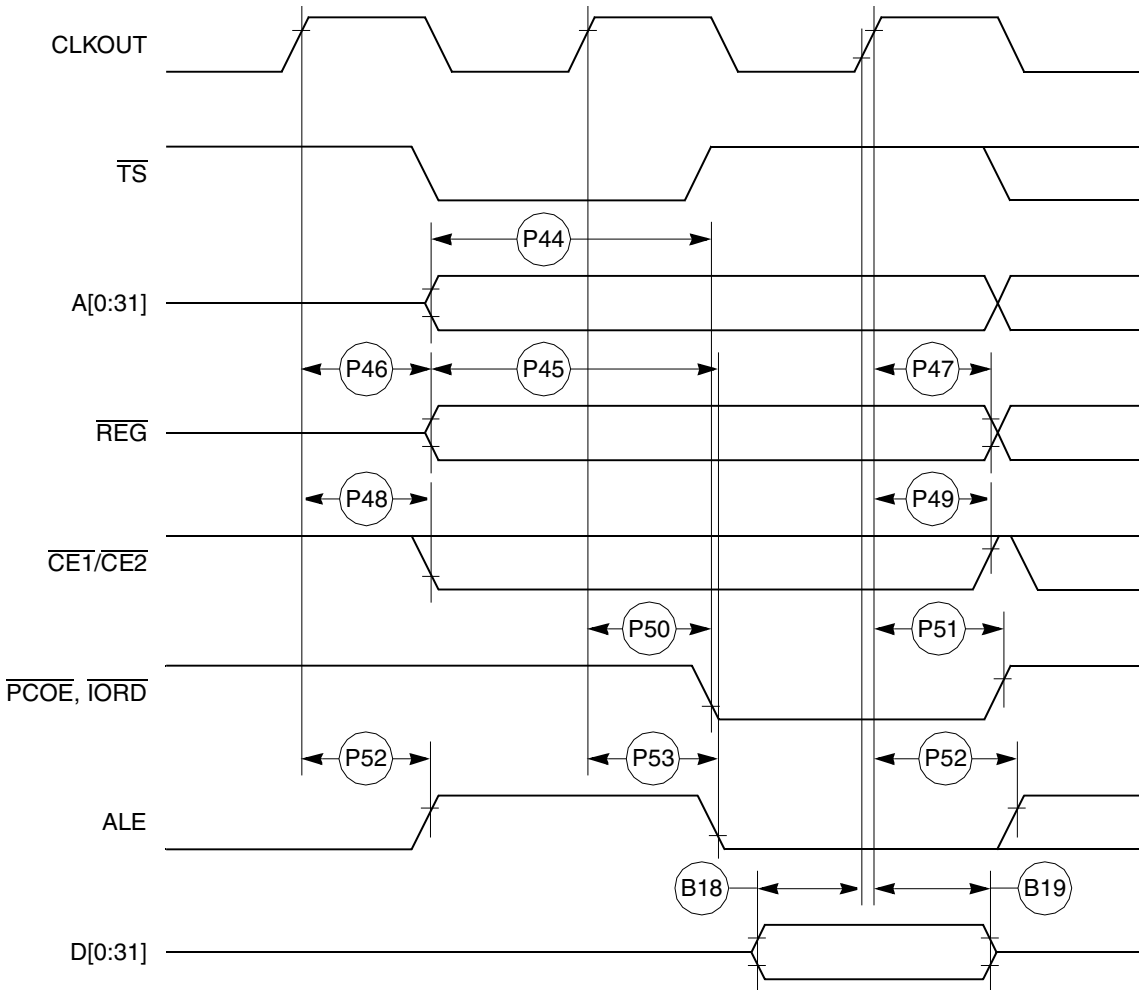

Figure 28. PCMCIA Access Cycles Timing External Bus Read

Figure 29 provides the PCMCIA access cycle timing for the external bus write.

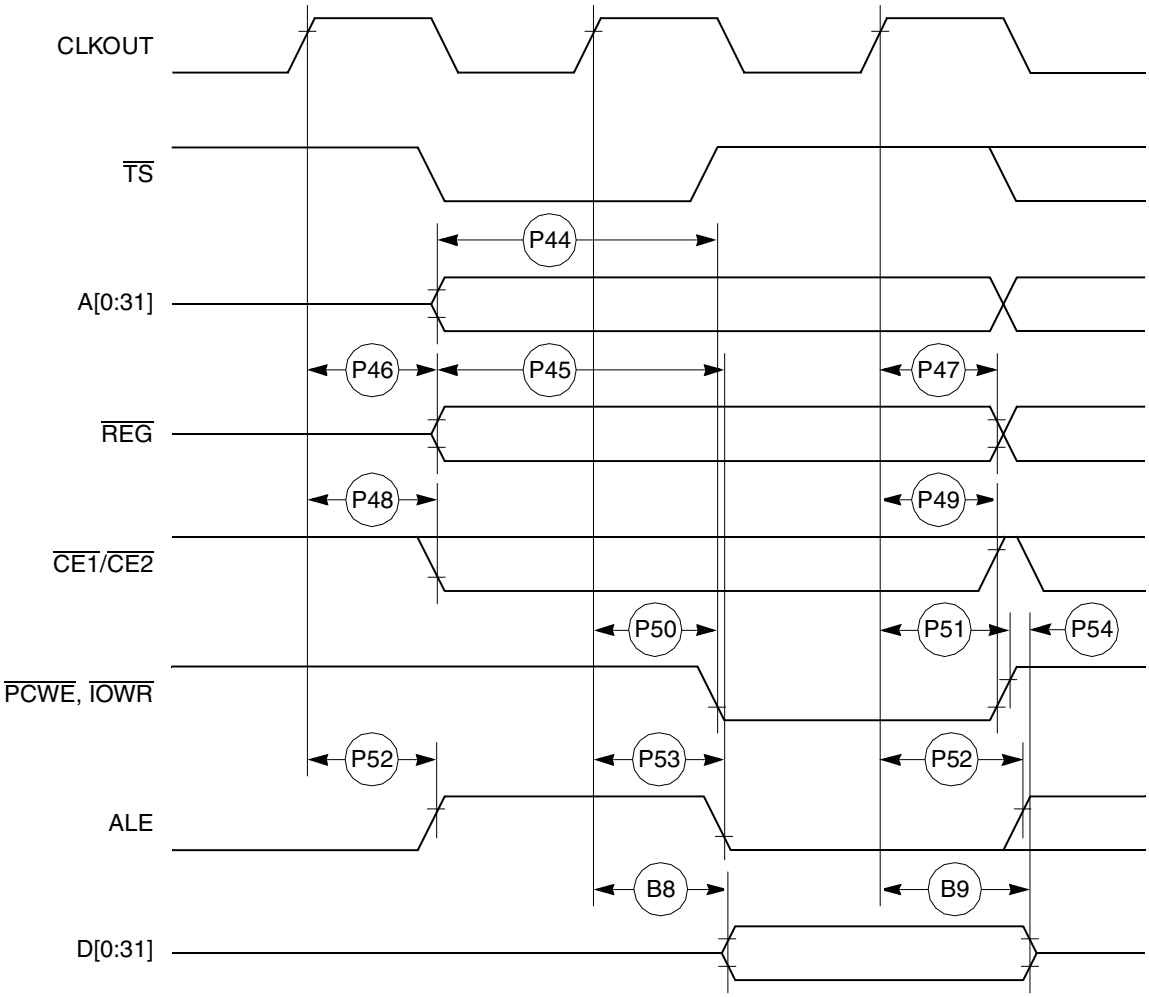

Figure 29. PCMCIA Access Cycles Timing External Bus Write

Figure 30 provides the PCMCIA WAIT signals detection timing.

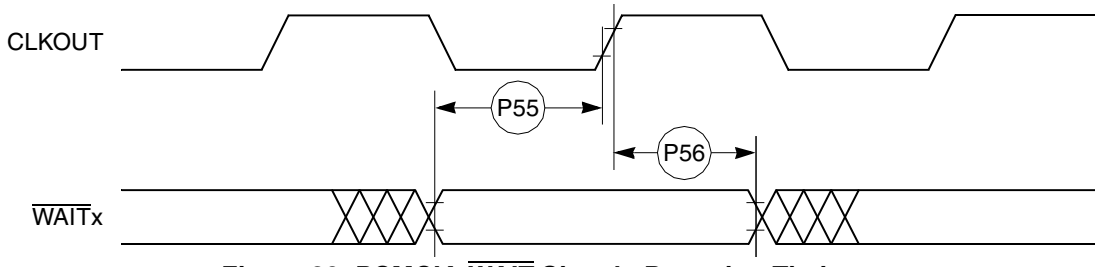

Figure 30. PCMCIA WAIT Signals Detection Timing

Figure 35 shows the reset timing for the data bus configuration.

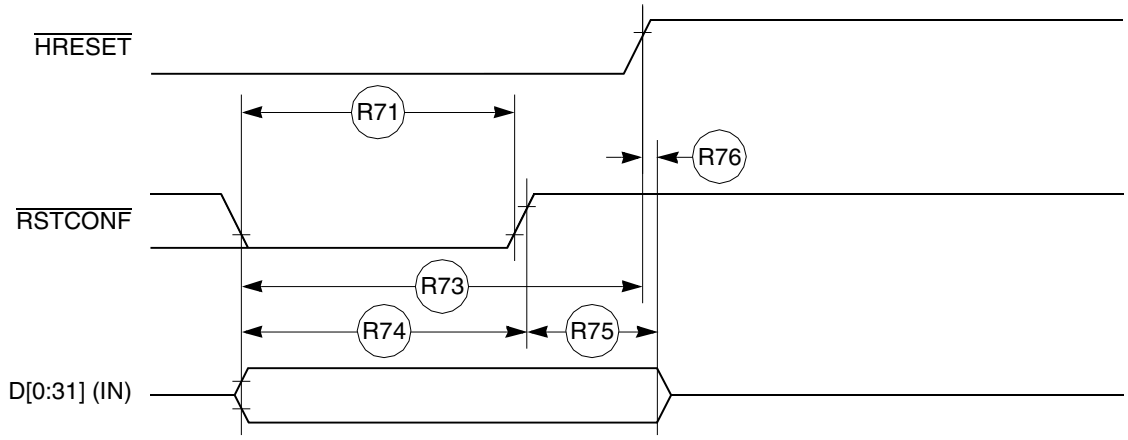

Figure 35. Reset Timing—Configuration from Data Bus

Figure 36 provides the reset timing for the data bus weak drive during configuration.

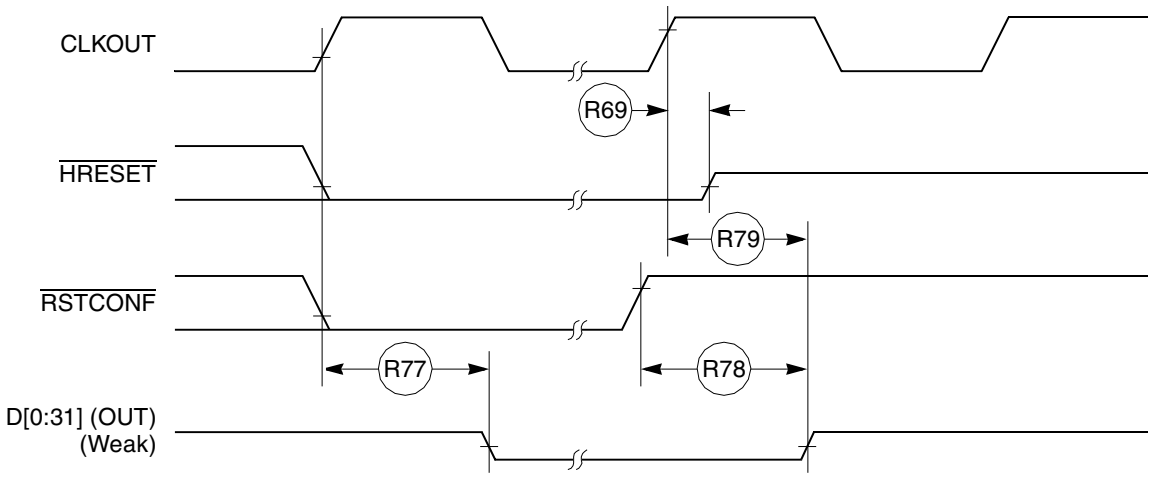

Figure 36. Reset Timing—Data Bus Weak Drive During Configuration

Figure 37 provides the reset timing for the debug port configuration.

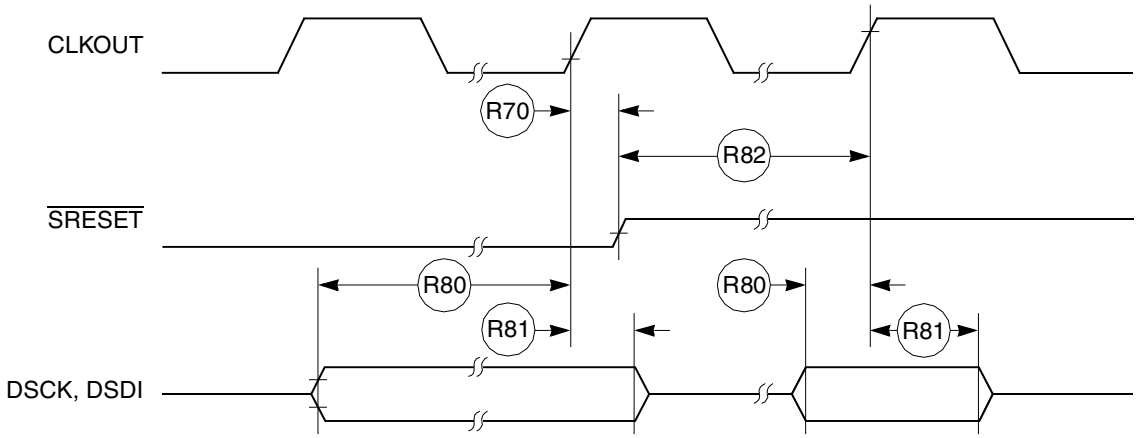

Figure 37. Reset Timing—Debug Port Configuration

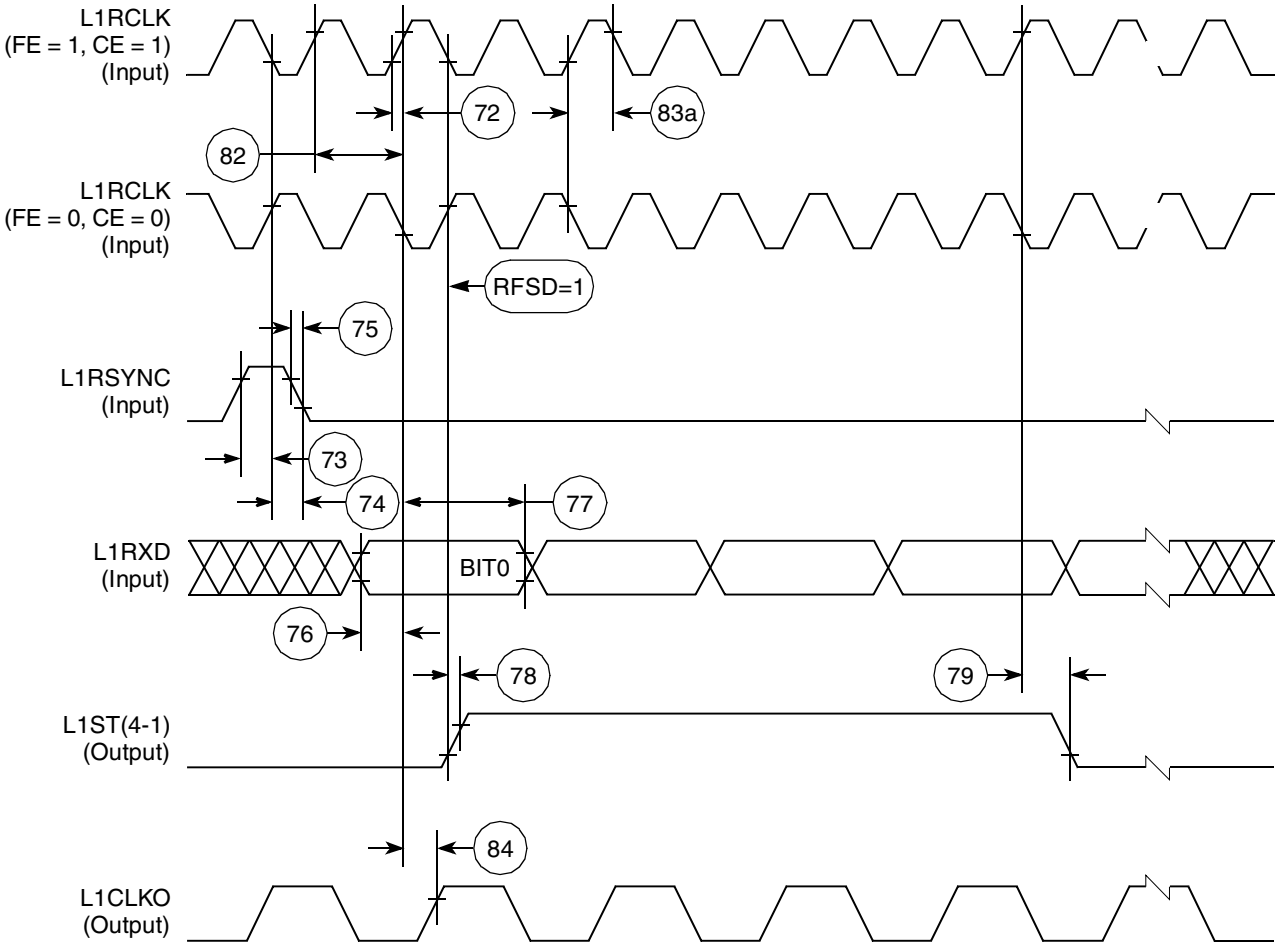

Figure 55. SI Receive Timing with Double-Speed Clocking (DSC = 1)

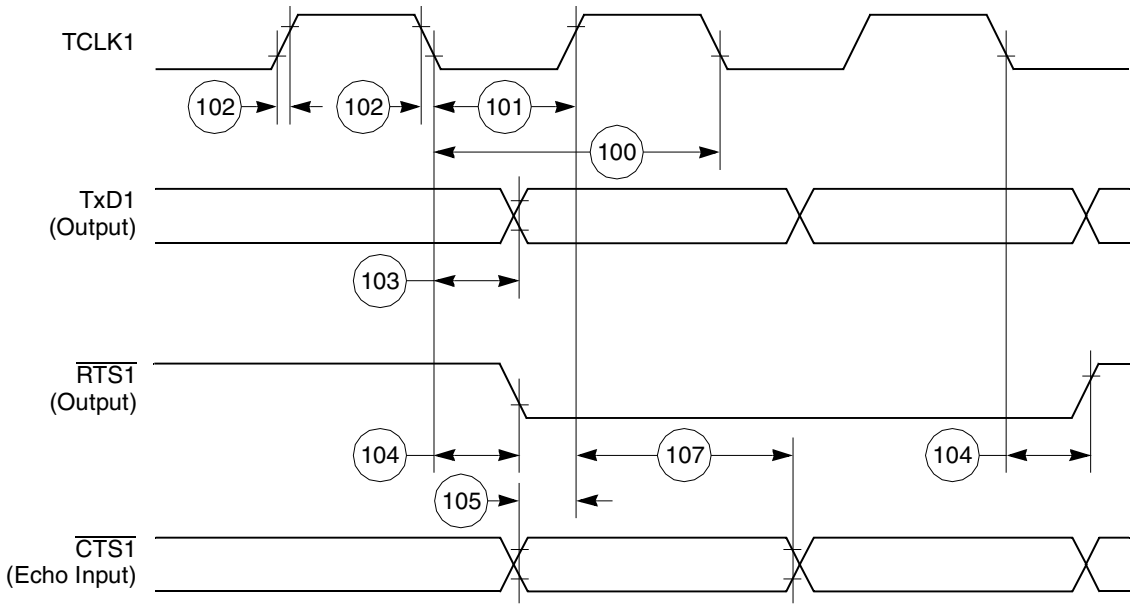

Figure 61. HDLC Bus Timing Diagram

12.8 Ethernet Electrical Specifications

Table 24 provides the Ethernet timings as shown in Figure 62 through Figure 64.

Table 24. Ethernet Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
120	CLSN width high	40	—	ns
121	RCLK1 rise/fall time	—	15	ns
122	RCLK1 width low	40	—	ns
123	RCLK1 clock period[1]	80	120	ns
124	RXD1 setup time	20	—	ns
125	RXD1 hold time	5	—	ns
126	RENA active delay (from RCLK1 rising edge of the last data bit)	10	—	ns
127	RENA width low	100	—	ns
128	TCLK1 rise/fall time	—	15	ns
129	TCLK1 width low	40	—	ns
130	TCLK1 clock period[1]	99	101	ns
131	TXD1 active delay (from TCLK1 rising edge)	—	50	ns
132	TXD1 inactive delay (from TCLK1 rising edge)	6.5	50	ns
133	TENA active delay (from TCLK1 rising edge)	10	50	ns

Table 24. Ethernet Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
134	TENA inactive delay (from TCLK1 rising edge)	10	50	ns
138	CLKO1 low to $\overline{\text{SDACK}}$ asserted[2]	—	20	ns
139	CLKO1 low to $\overline{\text{SDACK}}$ negated [2]	—	20	ns

[1] The ratios SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater than or equal to 2/1.
[2] $\overline{\text{SDACK}}$ is asserted whenever the SDMA writes the incoming frame DA into memory.

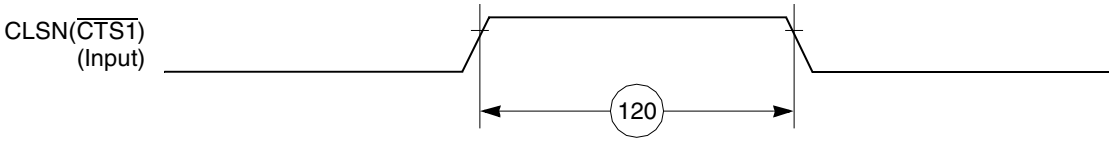

Figure 62. Ethernet Collision Timing Diagram

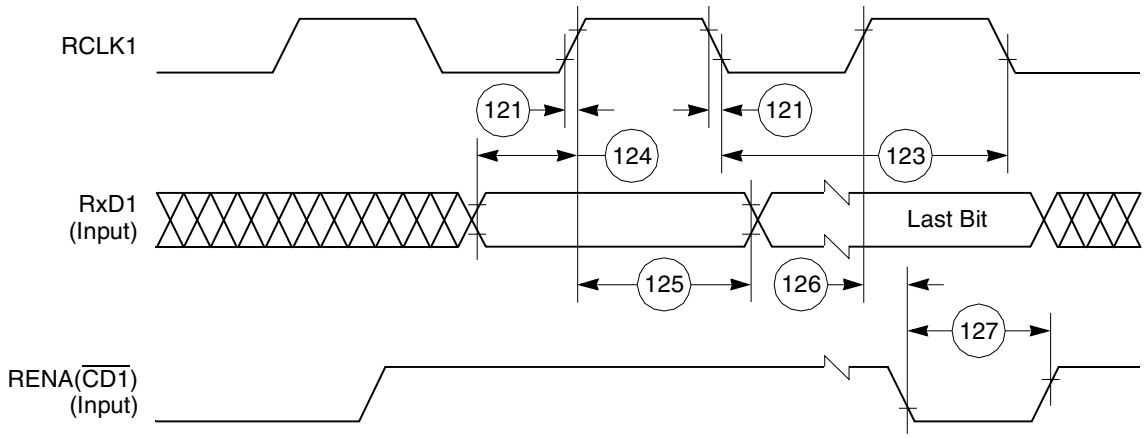

Figure 63. Ethernet Receive Timing Diagram

Table 28. I²C Timing (SCL < 100 kHz) (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
210	SDL/SCL fall time	—	300	ns
211	Stop condition setup time	4.7	—	µs

1 SCL frequency is given by SCL = BRGCLK_frequency/((BRG register + 3) × pre_scaler × 2).
The ratio SyncClk/(BRGCLK/pre_scaler) must be greater or equal to 4/1.

Table 29 provides the I²C (SCL > 100 kHz) timings.

Table 29. I²C Timing (SCL > 100 kHz)

Num	Characteristic	Expression	All Frequencies		Unit
			Min	Max	
200	SCL clock frequency (slave)	fSCL	0	BRGCLK/48	Hz
200	SCL clock frequency (master)[1]	fSCL	BRGCLK/16512	BRGCLK/48	Hz
202	Bus free time between transmissions	—	1/(2.2 × fSCL)	—	s
203	Low period of SCL	—	1/(2.2 × fSCL)	—	s
204	High period of SCL	—	1/(2.2 × fSCL)	—	s
205	Start condition setup time	—	1/(2.2 × fSCL)	—	s
206	Start condition hold time	—	1/(2.2 × fSCL)	—	s
207	Data hold time	—	0	—	s
208	Data setup time	—	1/(40 × fSCL)	—	s
209	SDL/SCL rise time	—	—	1/(10 × fSCL)	s
210	SDL/SCL fall time	—	—	1/(33 × fSCL)	s
211	Stop condition setup time	—	1/2(2.2 × fSCL)	—	s

1 SCL frequency is given by SCL = BrgClk_frequency/((BRG register + 3) × pre_scaler × 2).
The ratio SyncClk/(Brg_Clk/pre_scaler) must be greater or equal to 4/1.

Figure 70 shows the I²C bus timing.

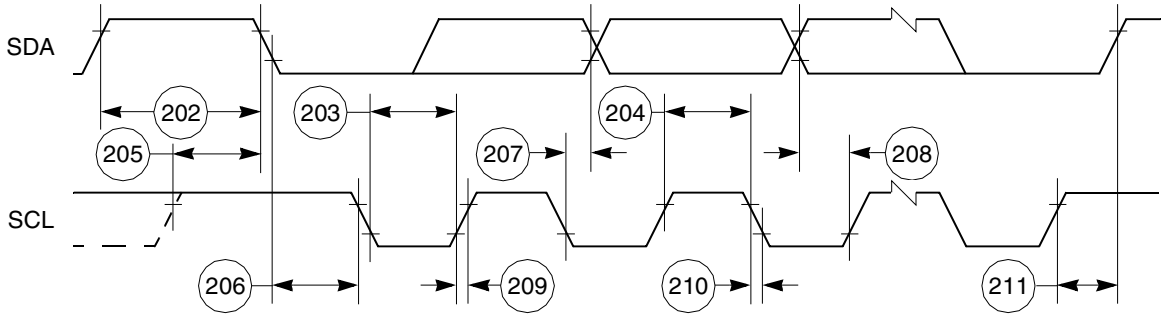

Figure 70. I²C Bus Timing Diagram

Figure 71 shows signal timings during UTOPIA receive operations.

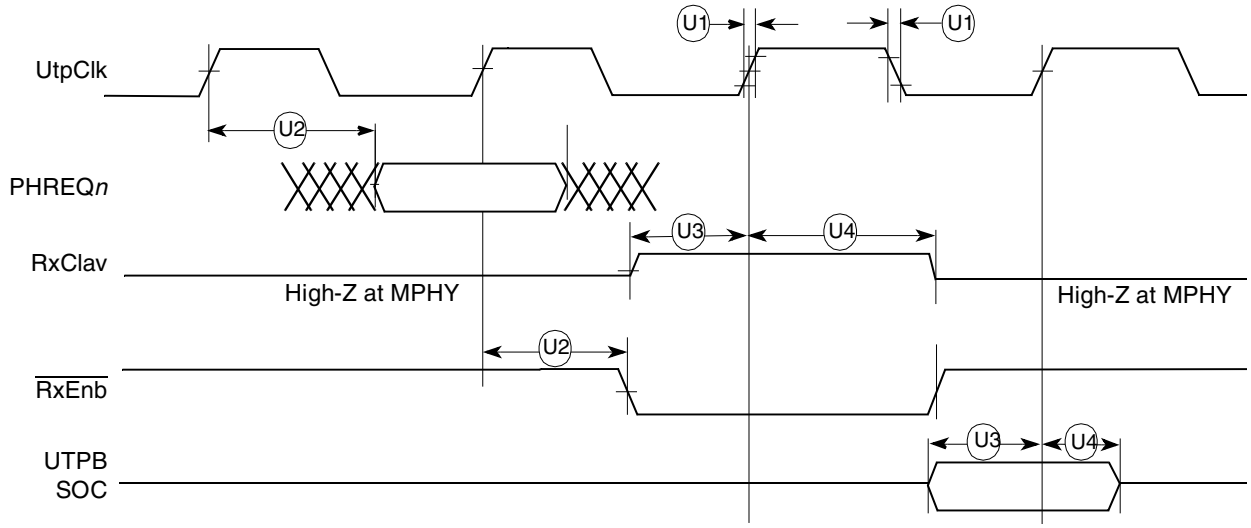

Figure 71. UTOPIA Receive Timing

Figure 72 shows signal timings during UTOPIA transmit operations.

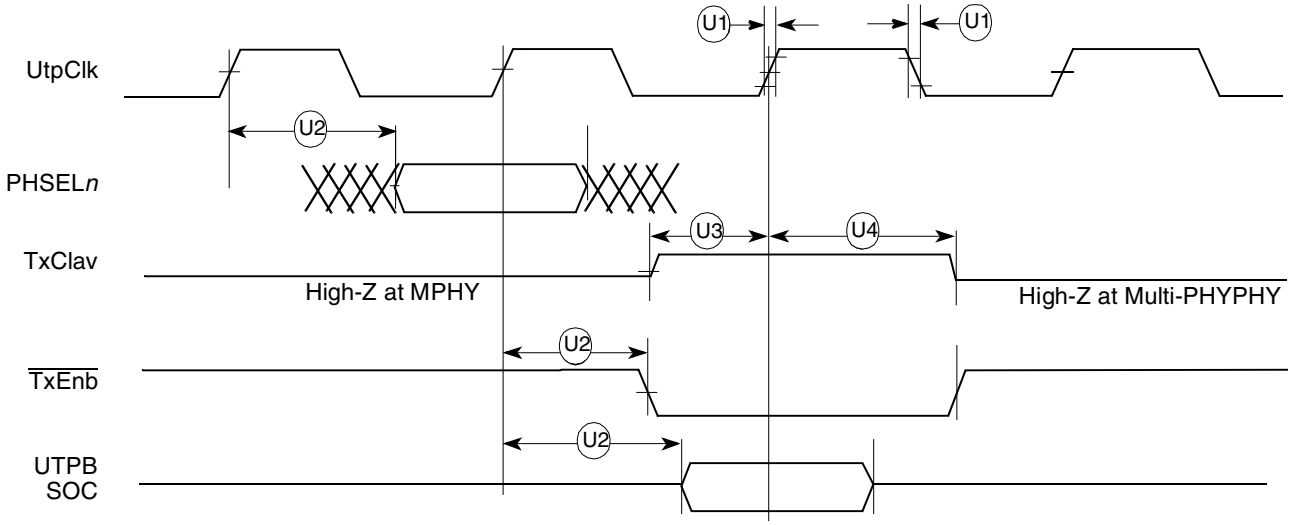

Figure 72. UTOPIA Transmit Timing

14 USB Electrical Characteristics

This section provides the AC timings for the USB interface.

14.1 USB Interface AC Timing Specifications

The USB Port uses the transmit clock on SCC1. Table 33 lists the USB interface timings.

Table 33. USB Interface AC Timing Specifications

Name	Characteristic	All Frequencies		Unit
		Min	Max	
US1	USBCLK frequency of operation[1] Low speed Full speed	 6 48		 MHz MHz
US4	USBCLK duty cycle (measured at 1.5 V)	45	55	%

[1] USBCLK accuracy should be ±500 ppm or better. USBCLK may be stopped to conserve power.

15 FEC Electrical Characteristics

This section provides the AC electrical specifications for the fast Ethernet controller (FEC). Note that the timing specifications for the MII signals are independent of system clock frequency (part speed designation). Also, MII signals use TTL signal levels compatible with devices operating at either 5.0 or 3.3 V.

15.1 MII and Reduced MII Receive Signal Timing

The receiver functions correctly up to a MII_RX_CLK maximum frequency of 25 MHz + 1%. The reduced MII (RMII) receiver functions correctly up to a RMII_REFCLK maximum frequency of 50 MHz + 1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_RX_CLK frequency – 1%.

Table 34 provides information on the MII and RMII receive signal timing.

Table 34. MII Receive Signal Timing

Num	Characteristic	Min	Max	Unit
M1	MII_RXD[3:0], MII_RX_DV, MII_RX_ERR to MII_RX_CLK setup	5	—	ns
M2	MII_RX_CLK to MII_RXD[3:0], MII_RX_DV, MII_RX_ER hold	5	—	ns
M3	MII_RX_CLK pulse width high	35%	65%	MII_RX_CLK period
M4	MII_RX_CLK pulse width low	35%	65%	MII_RX_CLK period
M1_RMII	RMII_RXD[1:0], RMII_CRS_DV, RMII_RX_ERR to RMII_REFCLK setup	4	—	ns
M2_RMII	RMII_REFCLK to RMII_RXD[1:0], RMII_CRS_DV, RMII_RX_ERR hold	2	—	ns

Table 37. MII Serial Management Channel Timing (continued)

Num	Characteristic	Min	Max	Unit
M14	MII_MDC pulse width high	40%	60%	MII_MDC period
M15	MII_MDC pulse width low	40%	60%	MII_MDC period

Figure 76 shows the MII serial management channel timing diagram.

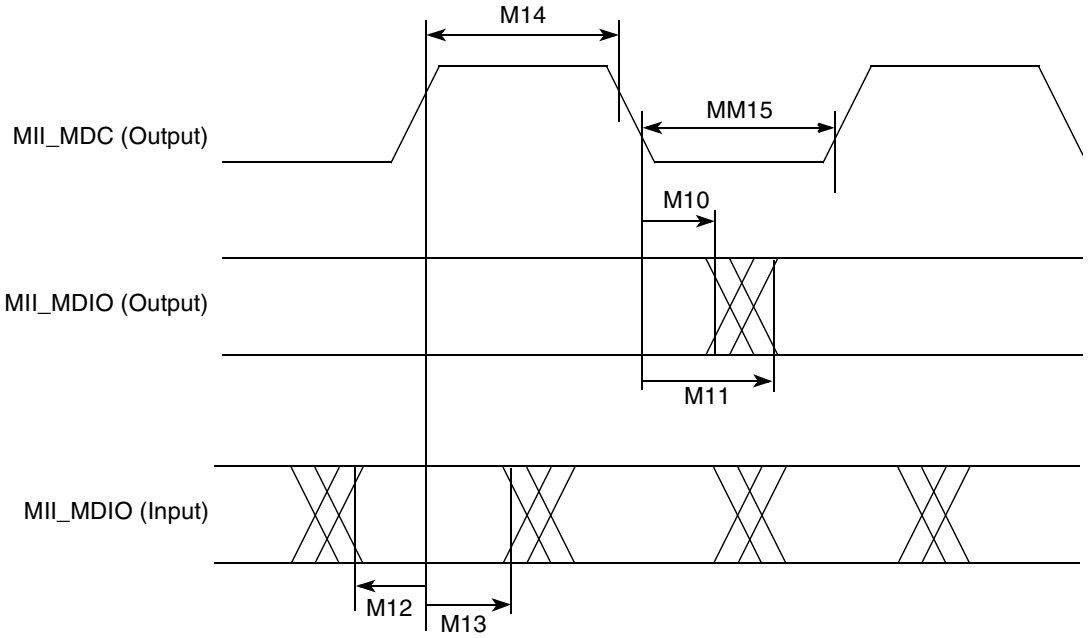

Figure 76. MII Serial Management Channel Timing Diagram

Table 39. Pin Assignments (continued)

Name	Pin Number	Type
PB17, L1ST3, BRGO2, RXADDR1[1], TXADDR1, PHREQ[1]	W12	Bidirectional (Optional: open-drain)
PB16, $\overline{\text{L1RQa}}$, L1ST4, $\overline{\text{RTS4}}$, RXADDR0[1], TXADDR0, PHREQ[0]	V11	Bidirectional (Optional: open-drain)
PB15, TXCLAV, BRG03, RXCLAV	U10	Bidirectional
PB14RXADDR2[1], TXADDR2	U18	Bidirectional
PC15, $\overline{\text{DREQ0}}$, $\overline{\text{RTS3}}$, L1ST1, TXCLAV, RXCLAV	R19	Bidirectional
PC14, $\overline{\text{DREQ1}}$, $\overline{\text{RTS2}}$, L1ST2	R18	Bidirectional
PC13, MII1-TXD3, $\overline{\text{SDACK1}}$	V10	Bidirectional
PC12, MII1-TXD2, $\overline{\text{TOUT1}}$	T18	Bidirectional
PC11, USBRXP	V16	Bidirectional
PC10, USBRXN, $\overline{\text{TGATE1}}$	U15	Bidirectional
PC9, $\overline{\text{CTS2}}$	T14	Bidirectional
PC8, $\overline{\text{CD2}}$, $\overline{\text{TGATE2}}$	W14	Bidirectional
PC7, $\overline{\text{CTS4}}$, L1TSYNCB, USBTXP	V12	Bidirectional
PC6, $\overline{\text{CD4}}$, L1RSYNCB, USBTXN	U11	Bidirectional
PC5, $\overline{\text{CTS3}}$, L1TSYNCA, SDACK2	T10	Bidirectional
PC4, $\overline{\text{CD3}}$, L1RSYNCA	W10	Bidirectional
PD15, L1TSYNCA, UTPB0	U8	Bidirectional
PD14, L1RSYNCA, UTPB1	U7	Bidirectional
PD13, L1TSYNCB, UTPB2	U6	Bidirectional
PD12, L1RSYNCB, UTPB3	U5	Bidirectional
PD11, RXD3, $\overline{\text{RXENB}}$	R2	Bidirectional
PD10, TXD3, $\overline{\text{TXENB}}$	T2	Bidirectional
PD9, TXD4, UTPCLK	U2	Bidirectional
PD8, RXD4, MII-MDC, RMII-MDC	R3	Bidirectional
PD7, $\overline{\text{RTS3}}$, UTPB4	W3	Bidirectional
PD6, $\overline{\text{RTS4}}$, UTPB5	W5	Bidirectional

Table 39. Pin Assignments (continued)

Name	Pin Number	Type
PE14, RXD3, MII2-TXD0, RMII2-TXD0	V7	Bidirectional
TMS	V18	Input
TDI, DSDI	T16	Input
TCK, DSCK	U17	Input
$\overline{\text{TRST}}$	W18	Input
TDO, DSDO	T17	Output
MII1_CRS	T11	Input
MII_MDIO	P19	Bidirectional
MII1_TXEN, RMII1_TXEN	T5	Output
MII1_COL	U12	Input
V_{SSSYN1}	C2	PLL analog V_{DD} and GND
V_{SSSYN}	E4	Power
V_{DDLSYN}	B2	Power
GND	G6, G7, G8, G9, G10, G11, G12, G13, H7, H8, H9, H10, H11, H12, H13, H14, J7, J8, J9, J10, J11, J12, J13, K7, K8, K9, K10, K11, K12, K13, L7, L8, L9, L10, L11, L12, L13, M7, M8, M9, M10, M11, M12, M13, N7, N8, N9, N10, N11, N12, N13, N14, P7, P13, R16	Power
V_{DDL}	E5, E6, E9, E11, E14, G15, H5, J5, J15, K15, L5, M15, N5, R6, R9, R10, R12, R15	Power
V_{DDH}	E7, E8, E10, E12, E13, E15, F5, F6, F7, F8, F9, F10, F11, F12, F13, F14, F15, G5, G14, H6, H15, J6, J14, K5, K6, K14, L6, L14, L15, M5, M6, M14, N6, N15, P5, P6, P8, P9, P10, P11, P12, P14, P15, R5, R7, R8, R11, R13, R14	Power
N/C	N17	No connect

[1] ESAR mode only.

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