Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	66MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (2), 10/100Mbps (2)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc880vr66

- On-chip 16 × 16 multiply accumulate controller (MAC)
  - One operation per clock (two-clock latency, one-clock blockage)
  - MAC operates concurrently with other instructions
  - FIR loop—Four clocks per four multiplies
- Four baud rate generators
  - Independent (can be connected to any SCC or SMC)
  - Allow changes during operation
  - Autobaud support option
- Up to three serial communication controllers (SCCs) supporting the following protocols:
  - Serial ATM capability on SCCs
  - Optional UTOPIA port on SCC4
  - Ethernet/IEEE Std 802.3™ optional on the SCC(s) supporting full 10-Mbps operation
  - HDLC/SDLC
  - HDLC bus (implements an HDLC-based local area network (LAN))
  - Asynchronous HDLC to support point-to-point protocol (PPP)
  - AppleTalk
  - Universal asynchronous receiver transmitter (UART)
  - Synchronous UART
  - Serial infrared (IrDA)
  - Binary synchronous communication (BISYNC)
  - Totally transparent (bit streams)
  - Totally transparent (frame based with optional cyclic redundancy check (CRC))
- Up to two serial management channels (SMCs) supporting the following protocols:
  - UART (low-speed operation)
  - Transparent
  - General circuit interface (GCI) controller
  - Provide management for BRI devices as GCI controller in time-division multiplexed (TDM) channels
- Universal serial bus (USB)—Supports operation as a USB function endpoint, a USB host controller, or both for testing purposes (loop-back diagnostics)
  - USB 2.0 full-/low-speed compatible
  - The USB function mode has the following features:
    - Four independent endpoints support control, bulk, interrupt, and isochronous data transfers.
    - CRC16 generation and checking
    - CRC5 checking
    - NRZI encoding/decoding with bit stuffing
    - 12- or 1.5-Mbps data rate

5 Power Dissipation

Table 5 provides information on power dissipation. The modes are 1:1, where CPU and bus speeds are equal, and 2:1, where CPU frequency is twice bus speed.

Table 5. Power Dissipation (P_D)

Die Revision	Bus Mode	CPU Frequency	Typical[1]	Maximum[2]	Unit
0	1:1	66 MHz	310	390	mW
		80 MHz	350	430	mW
	2:1	133 MHz	430	495	mW

1 Typical power dissipation at V_{DDL} = V_{DDSYN} = 1.8 V, and V_{DDH} is at 3.3 V.
2 Maximum power dissipation at V_{DDL} = V_{DDSYN} = 1.9 V, and V_{DDH} is at 3.5 V.

NOTE

The values in Table 5 represent V_{DDL}-based power dissipation and do not include I/O power dissipation over V_{DDH}. I/O power dissipation varies widely by application due to buffer current, depending on external circuitry.

The V_{DDSYN} power dissipation is negligible.

6 DC Characteristics

Table 6 provides the DC electrical characteristics for the MPC885/MPC880.

Table 6. DC Electrical Specifications

Characteristic	Symbol	Min	Max	Unit
Operating voltage	V_{DDL} (core)	1.7	1.9	V
	V_{DDH} (I/O)	3.135	3.465	V
	V_{DDSYN}[1]	1.7	1.9	V
	Difference between V_{DDL} and V_{DDSYN}	—	100	mV
Input high voltage (all inputs except EXTAL and EXTCLK)[2]	V_{IH}	2.0	3.465	V
Input low voltage[3]	V_{IL}	GND	0.8	V
EXTAL, EXTCLK input high voltage	V_{IHC}	0.7*(V_{DDH})	V_{DDH}	V
Input leakage current, Vin = 5.5 V (except TMS, $\overline{\text{TRST}}$, DSCK and DSDI pins) for 5-V tolerant pins [2]	I_{in}	—	100	µA
Input leakage current, V_{in} = V_{DDH} (except TMS, $\overline{\text{TRST}}$, DSCK, and DSDI)	I_{In}	—	10	µA
Input leakage current, V_{in} = 0 V (except TMS, $\overline{\text{TRST}}$, DSCK and DSDI pins)	I_{In}	—	10	µA
Input capacitance[4]	C_{in}	—	20	pF

If the board temperature is known, an estimate of the junction temperature in the environment can be made using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

$R_{\theta JB}$ = junction-to-board thermal resistance (ºC/W)

T_B = board temperature (ºC)

P_D = power dissipation in package

If the board temperature is known and the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. For this method to work, the board and board mounting must be similar to the test board used to determine the junction-to-board thermal resistance, namely a 2s2p (board with a power and a ground plane) and vias attaching the thermal balls to the ground plane.

7.4 Estimation Using Simulation

When the board temperature is not known, a thermal simulation of the application is needed. The simple two resistor model can be used with the thermal simulation of the application [2], or a more accurate and complex model of the package can be used in the thermal simulation.

7.5 Experimental Determination

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

Ψ_{JT} = thermal characterization parameter

T_T = thermocouple temperature on top of package

P_D = power dissipation in package

The thermal characterization parameter is measured per the JESD51-2 specification published by JEDEC using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by the cooling effects of the thermocouple wire.

7.6 References

Semiconductor Equipment and Materials International(415) 964-5111
805 East Middlefield Rd
Mountain View, CA 94043

MIL-SPEC and EIA/JESD (JEDEC) specifications800-854-7179 or
(Available from Global Engineering Documents)303-397-7956

JEDEC Specifications http://www.jedec.org

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
2. 2. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

8 Power Supply and Power Sequencing

This section provides design considerations for the MPC885/MPC880 power supply. The MPC885/MPC880 has a core voltage (V_{DDL}) and PLL voltage (V_{DDSYN}), which both operate at a lower voltage than the I/O voltage V_{DDH}. The I/O section of the MPC885/MPC880 is supplied with 3.3 V across V_{DDH} and V_{SS} (GND).

The signals PA[0:15], PB[14:31], PC[4:15], PD[3:15], TDI, TDO, TCK, TRST_B, TMS, MII_TXEN, and MII_MDIO are 5 V tolerant. All inputs cannot be more than 2.5 V greater than V_{DDH}. In addition, 5-V tolerant pins cannot exceed 5.5 V and remaining input pins cannot exceed 3.465 V. This restriction applies to power up/down and normal operation.

One consequence of multiple power supplies is that when power is initially applied the voltage rails ramp up at different rates. The rates depend on the nature of the power supply, the type of load on each power supply, and the manner in which different voltages are derived. The following restrictions apply:

- V_{DDL} must not exceed V_{DDH} during power up and power down.
- V_{DDL} must not exceed 1.9 V, and V_{DDH} must not exceed 3.465 V.

These cautions are necessary for the long-term reliability of the part. If they are violated, the electrostatic discharge (ESD) protection diodes are forward-biased, and excessive current can flow through these diodes. If the system power supply design does not control the voltage sequencing, the circuit shown Figure 5 can be added to meet these requirements. The MUR420 Schottky diodes control the maximum potential difference between the external bus and core power supplies on power up, and the 1N5820 diodes regulate the maximum potential difference on power down.

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B36	A(0:31), BADDR(28:30), and D(0:31) to $\overline{\text{GPL}}$ valid, as requested by control bit GxT4 in the corresponding word in the UPM (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	1.80	—	1.13	—	ns
B37	UPWAIT valid to CLKOUT falling edge[9] (MIN = 0.00 × B1 + 6.00)	6.00	—	6.00	—	6.00	—	6.00	—	ns
B38	CLKOUT falling edge to UPWAIT valid [9] (MIN = 0.00 × B1 + 1.00)	1.00	—	1.00	—	1.00	—	1.00	—	ns
B39	$\overline{\text{AS}}$ valid to CLKOUT rising edge[10] (MIN = 0.00 × B1 + 7.00)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B40	A(0:31), TSIZ(0:1), RD/$\overline{\text{WR}}$, $\overline{\text{BURST}}$, valid to CLKOUT rising edge (MIN = 0.00 × B1 + 7.00)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B41	$\overline{\text{TS}}$ valid to CLKOUT rising edge (setup time) (MIN = 0.00 × B1 + 7.00)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B42	CLKOUT rising edge to $\overline{\text{TS}}$ valid (hold time) (MIN = 0.00 × B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B43	$\overline{\text{AS}}$ negation to memory controller signals negation (MAX = TBD)	—	TBD	—	TBD	—	TBD	—	TBD	ns

1 For part speeds above 50 MHz, use 9.80 ns for B11a.

2 The timing required for $\overline{\text{BR}}$ input is relevant when the MPC885/MPC880 is selected to work with the internal bus arbiter. The timing for $\overline{\text{BG}}$ input is relevant when the MPC885/MPC880 is selected to work with the external bus arbiter.

3 For part speeds above 50 MHz, use 2 ns for B17.

4 The D(0:31) input timings B18 and B19 refer to the rising edge of the CLKOUT in which the $\overline{\text{TA}}$ input signal is asserted.

5 For part speeds above 50 MHz, use 2 ns for B19.

6 The D(0:31) input timings B20 and B21 refer to the falling edge of the CLKOUT. This timing is valid only for read accesses controlled by chip-selects under control of the user-programmable machine (UPM) in the memory controller, for data beats where DLT3 = 1 in the RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

7 This formula applies to bus operation up to 50 MHz.

8 The timing B30 refers to $\overline{\text{CS}}$ when ACS = 00 and to $\overline{\text{CS}}$ and $\overline{\text{WE}}$(0:3) when CSNT = 0.

9 The signal UPWAIT is considered asynchronous to the CLKOUT and synchronized internally. The timings specified in B37 and B38 are specified to enable the freeze of the UPM output signals as described in Figure 21.

10 The $\overline{\text{AS}}$ signal is considered asynchronous to the CLKOUT. The timing B39 is specified in order to allow the behavior specified in Figure 24.

Figure 21 provides the timing for the asynchronous asserted UPWAIT signal controlled by the UPM.

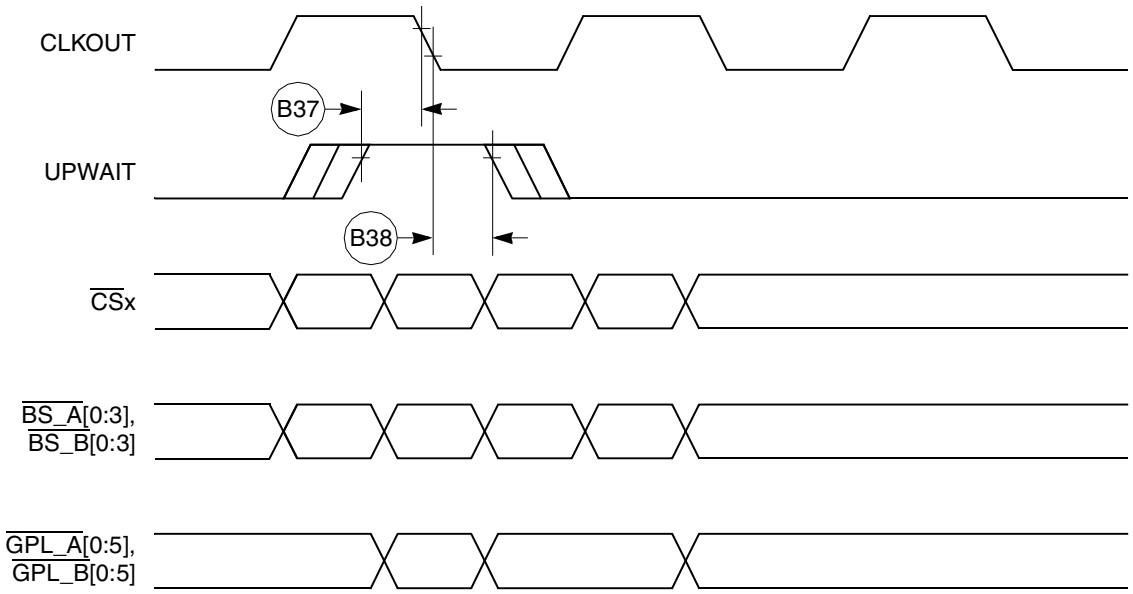


Figure 21. Asynchronous UPWAIT Asserted Detection in UPM-Handled Cycles Timing

Figure 22 provides the timing for the asynchronous negated UPWAIT signal controlled by the UPM.

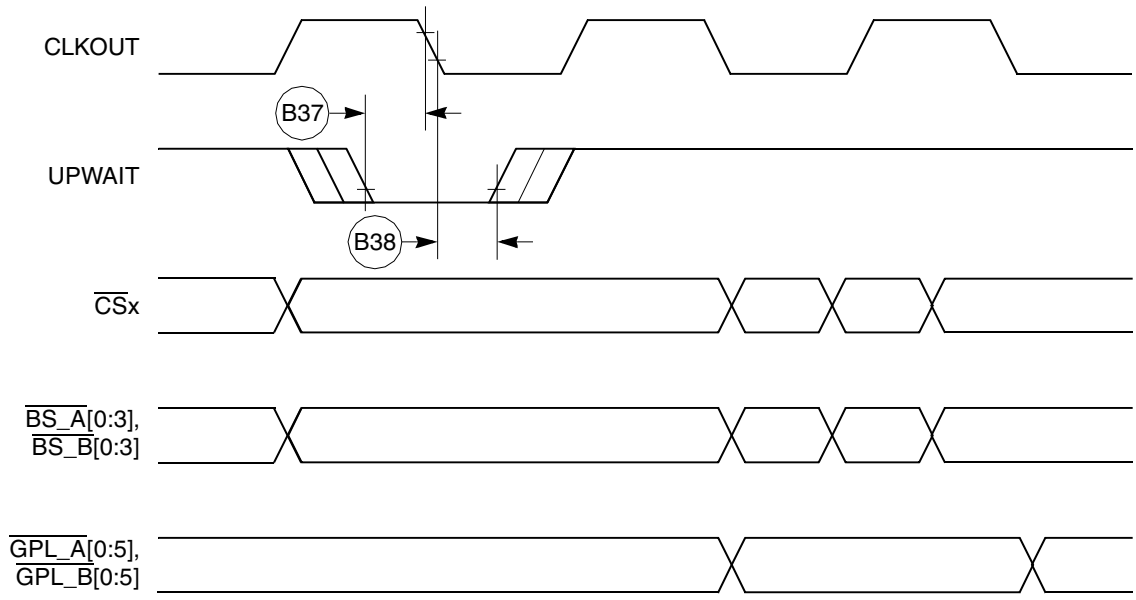


Figure 22. Asynchronous UPWAIT Negated Detection in UPM-Handled Cycles Timing

Figure 23 provides the timing for the synchronous external master access controlled by the GPCM.

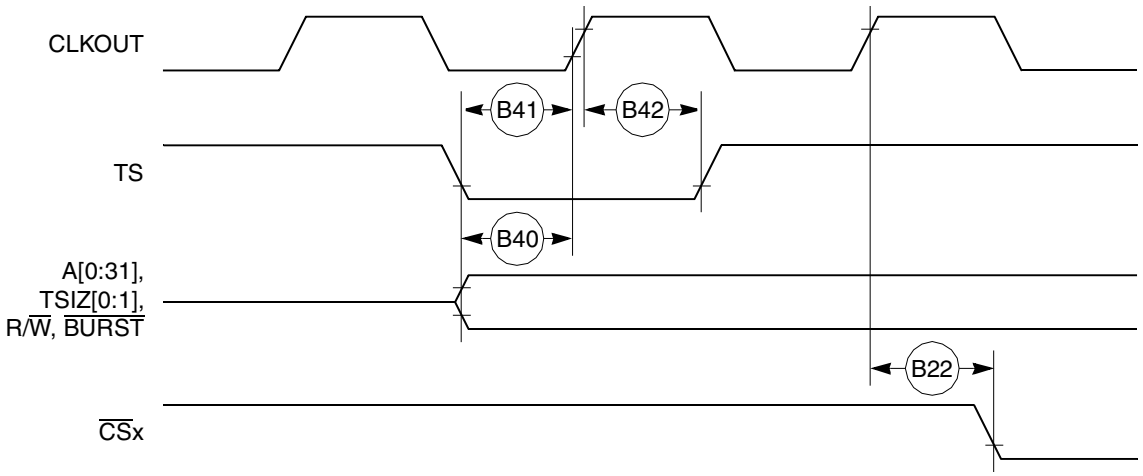


Figure 23. Synchronous External Master Access Timing (GPCM Handled—ACS = 00)

Figure 24 provides the timing for the asynchronous external master memory access controlled by the GPCM.

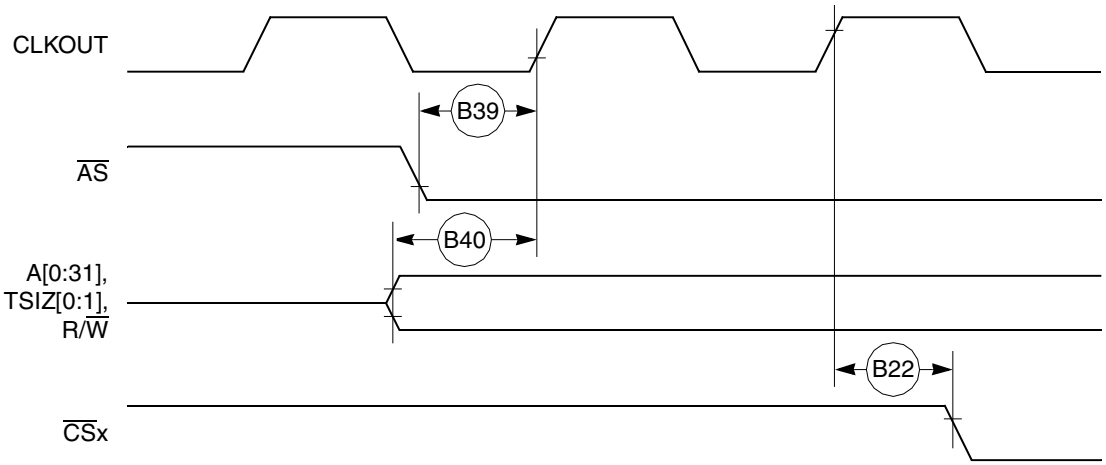


Figure 24. Asynchronous External Master Memory Access Timing (GPCM Controlled—ACS = 00)

Figure 25 provides the timing for the asynchronous external master control signals negation.

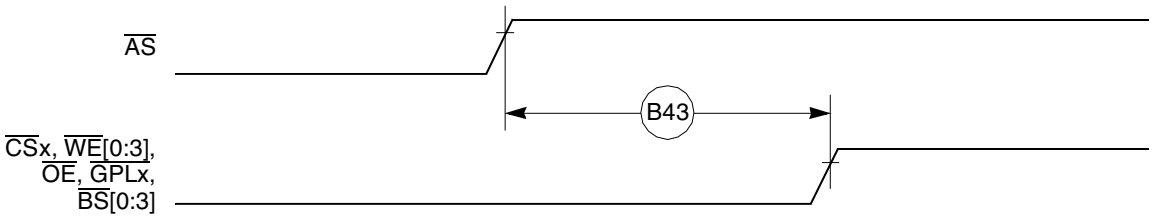


Figure 25. Asynchronous External Master—Control Signals Negation Timing

12.3 IDMA Controller AC Electrical Specifications

Table 18 provides the IDMA controller timings as shown in Figure 48 tthrough Figure 51.

Table 18. IDMA Controller Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
40	$\overline{\text{DREQ}}$ setup time to clock high	7	—	ns
41	$\overline{\text{DREQ}}$ hold time from clock high [1]	TBD	—	ns
42	$\overline{\text{SDACK}}$ assertion delay from clock high	—	12	ns
43	$\overline{\text{SDACK}}$ negation delay from clock low	—	12	ns
44	$\overline{\text{SDACK}}$ negation delay from $\overline{\text{TA}}$ low	—	20	ns
45	$\overline{\text{SDACK}}$ negation delay from clock high	—	15	ns
46	$\overline{\text{TA}}$ assertion to rising edge of the clock setup time (applies to external $\overline{\text{TA}}$)	7	—	ns

[1] Applies to high-to-low mode (EDM = 1).

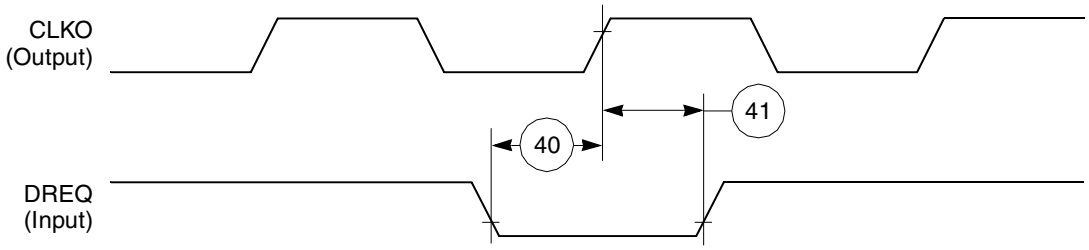


Figure 48. IDMA External Requests Timing Diagram

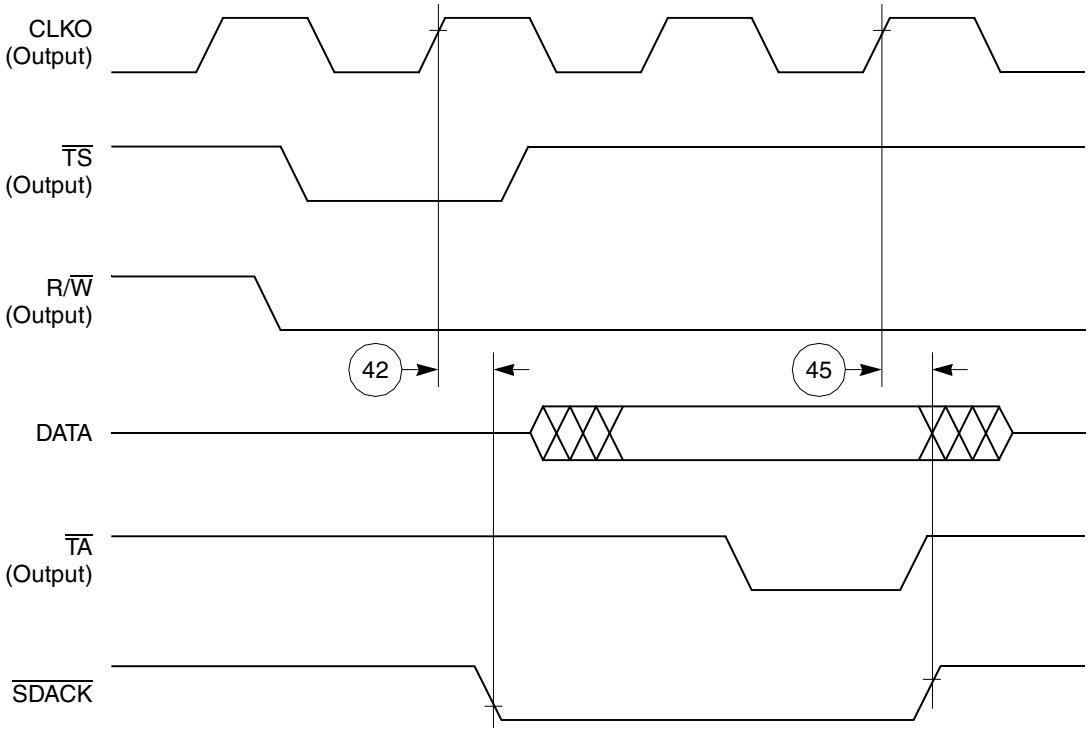


Figure 51. SDACK Timing Diagram—Peripheral Read, Internally-Generated TA

12.4 Baud Rate Generator AC Electrical Specifications

Table 19 provides the baud rate generator timings as shown in Figure 52.

Table 19. Baud Rate Generator Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
50	BRGO rise and fall time	—	10	ns
51	BRGO duty cycle	40	60	%
52	BRGO cycle	40	—	ns

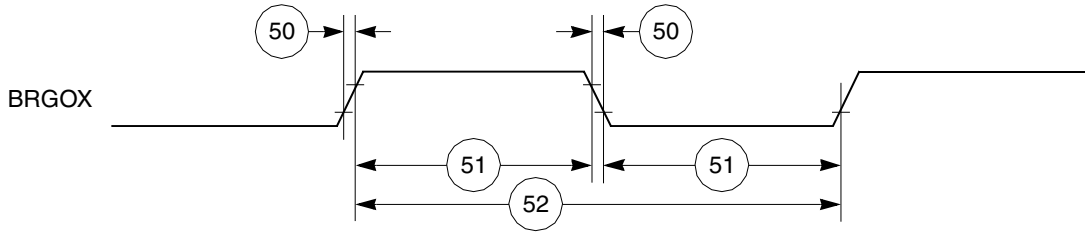


Figure 52. Baud Rate Generator Timing Diagram

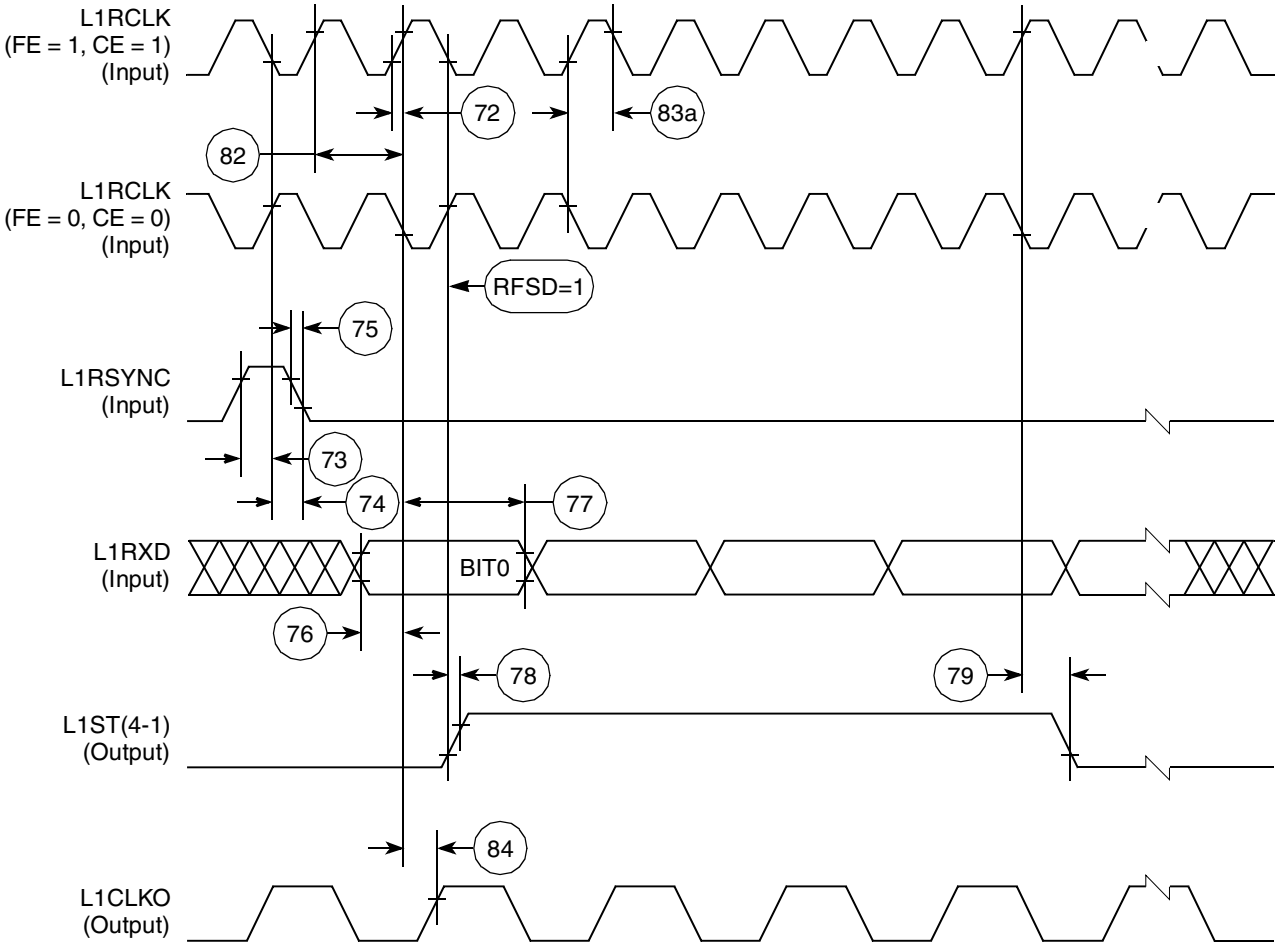


Figure 55. SI Receive Timing with Double-Speed Clocking (DSC = 1)

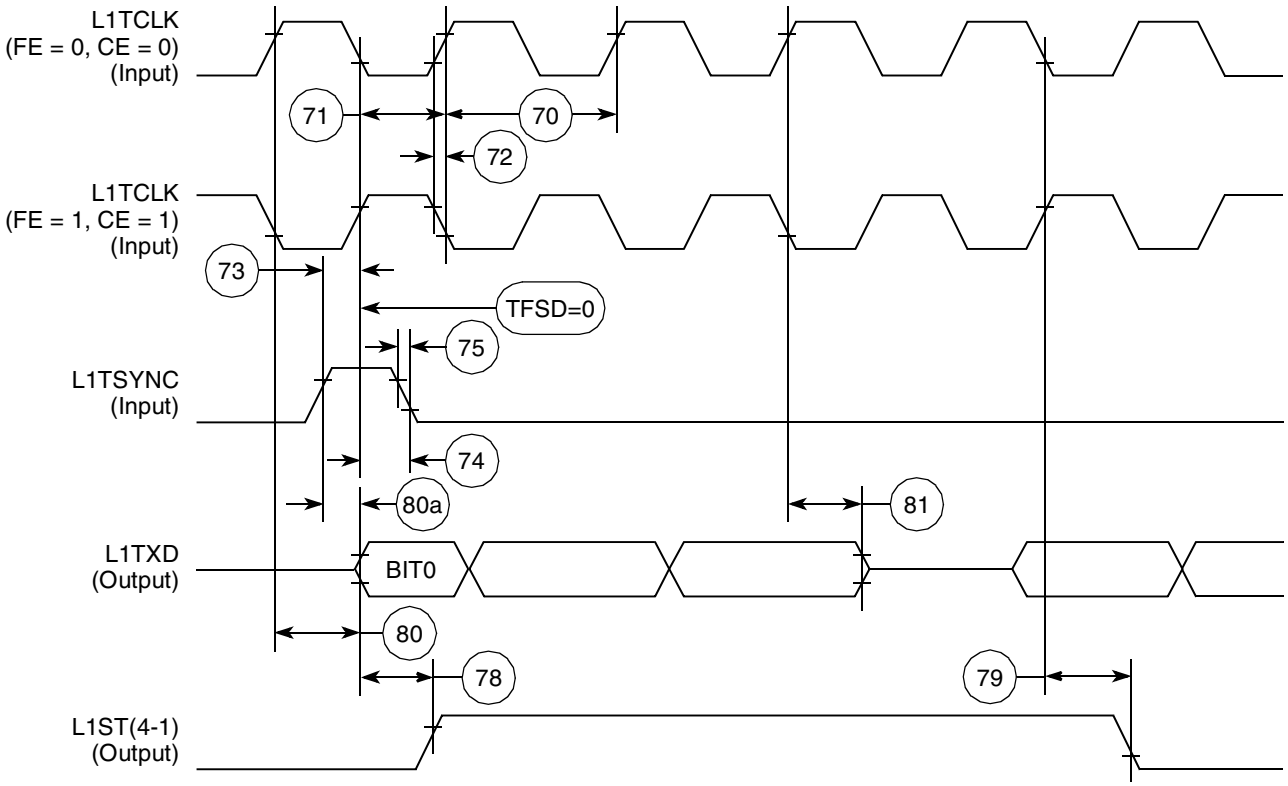


Figure 56. SI Transmit Timing Diagram (DSC = 0)

12.7 SCC in NMSI Mode Electrical Specifications

Table 22 provides the NMSI external clock timing.

Table 22. NMSI External Clock Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
100	RCLK1 and TCLK1 width high[1]	1/SYNCCLK	—	ns
101	RCLK1 and TCLK1 width low	1/SYNCCLK + 5	—	ns
102	RCLK1 and TCLK1 rise/fall time	—	15.00	ns
103	TXD1 active delay (from TCLK1 falling edge)	0.00	50.00	ns
104	$\overline{\text{RTS1}}$ active/inactive delay (from TCLK1 falling edge)	0.00	50.00	ns
105	$\overline{\text{CTS1}}$ setup time to TCLK1 rising edge	5.00	—	ns
106	RXD1 setup time to RCLK1 rising edge	5.00	—	ns
107	RXD1 hold time from RCLK1 rising edge[2]	5.00	—	ns
108	$\overline{\text{CD1}}$ setup time to RCLK1 rising edge	5.00	—	ns

1 The ratios SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater than or equal to 2.25/1.
2 Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as external sync signals.

Table 23 provides the NMSI internal clock timing.

Table 23. NMSI Internal Clock Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
100	RCLK1 and TCLK1 frequency[1]	0.00	SYNCCLK/3	MHz
102	RCLK1 and TCLK1 rise/fall time	—	—	ns
103	TXD1 active delay (from TCLK1 falling edge)	0.00	30.00	ns
104	$\overline{\text{RTS1}}$ active/inactive delay (from TCLK1 falling edge)	0.00	30.00	ns
105	$\overline{\text{CTS1}}$ setup time to TCLK1 rising edge	40.00	—	ns
106	RXD1 setup time to RCLK1 rising edge	40.00	—	ns
107	RXD1 hold time from RCLK1 rising edge[2]	0.00	—	ns
108	$\overline{\text{CD1}}$ setup time to RCLK1 rising edge	40.00	—	ns

1 The ratios SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater than or equal to 3/1.
2 Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as external sync signals

Figure 59 through Figure 61 show the NMSI timings.

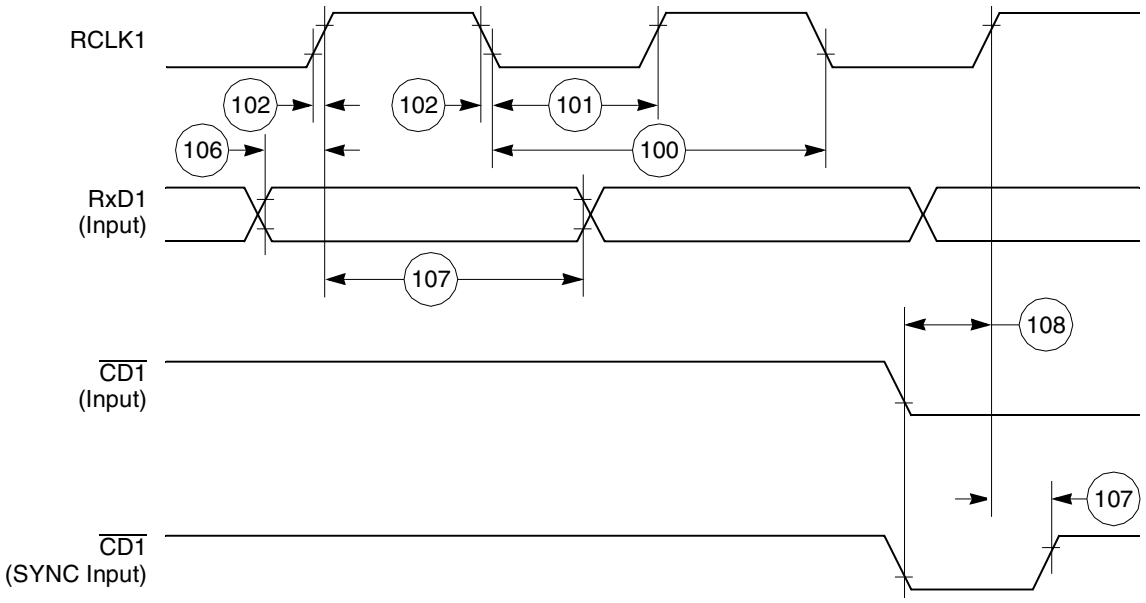


Figure 59. SCC NMSI Receive Timing Diagram

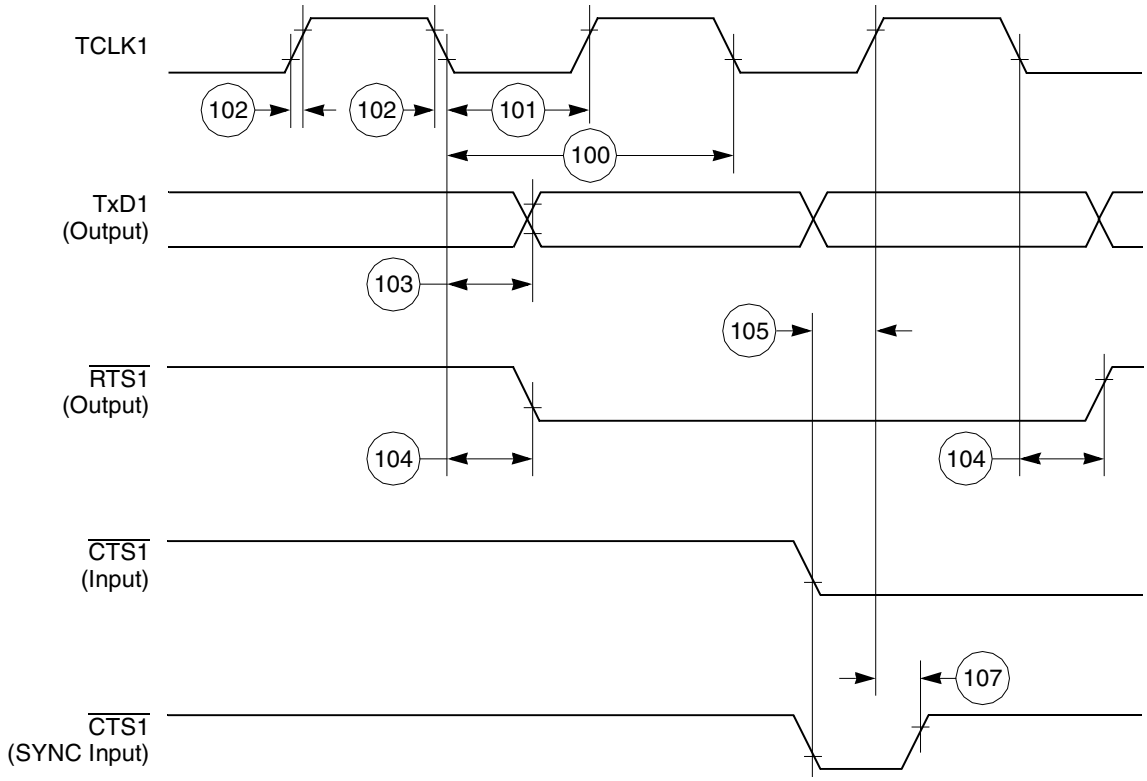
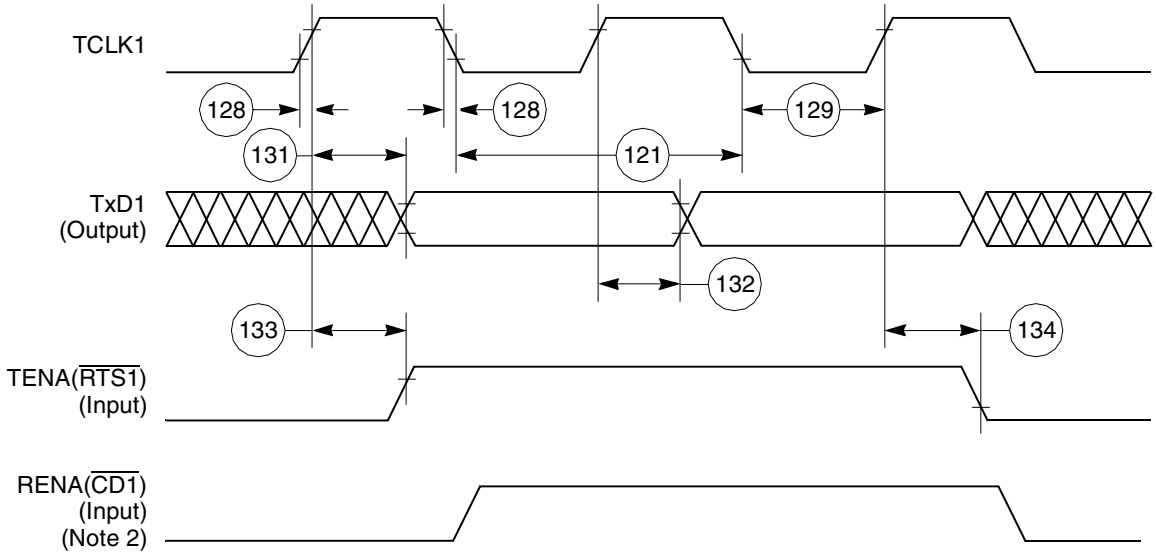


Figure 60. SCC NMSI Transmit Timing Diagram



Notes:
1. Transmit clock invert (TCI) bit in GSMR is set.
2. If RENA is negated before TENA or RENA is not asserted at all during transmit, then the CSL bit is set in the buffer descriptor at the end of the frame transmission.

Figure 64. Ethernet Transmit Timing Diagram

12.9 SMC Transparent AC Electrical Specifications

Table 25 provides the SMC transparent timings as shown in Figure 65.

Table 25. SMC Transparent Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
150	SMCLK clock period[1]	100	—	ns
151	SMCLK width low	50	—	ns
151A	SMCLK width high	50	—	ns
152	SMCLK rise/fall time	—	15	ns
153	SMTXD active delay (from SMCLK falling edge)	10	50	ns
154	SMRXD/SMSYNC setup time	20	—	ns
155	RXD1/SMSYNC hold time	5	—	ns

1 SyncCLK must be at least twice as fast as SMCLK.

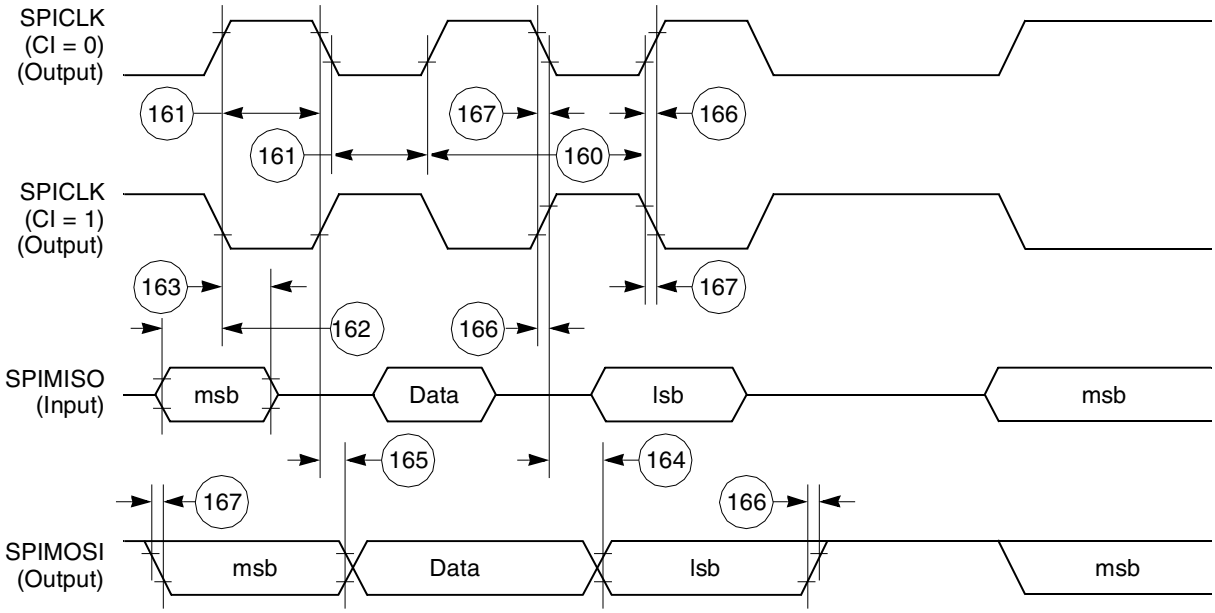


Figure 66. SPI Master (CP = 0) Timing Diagram

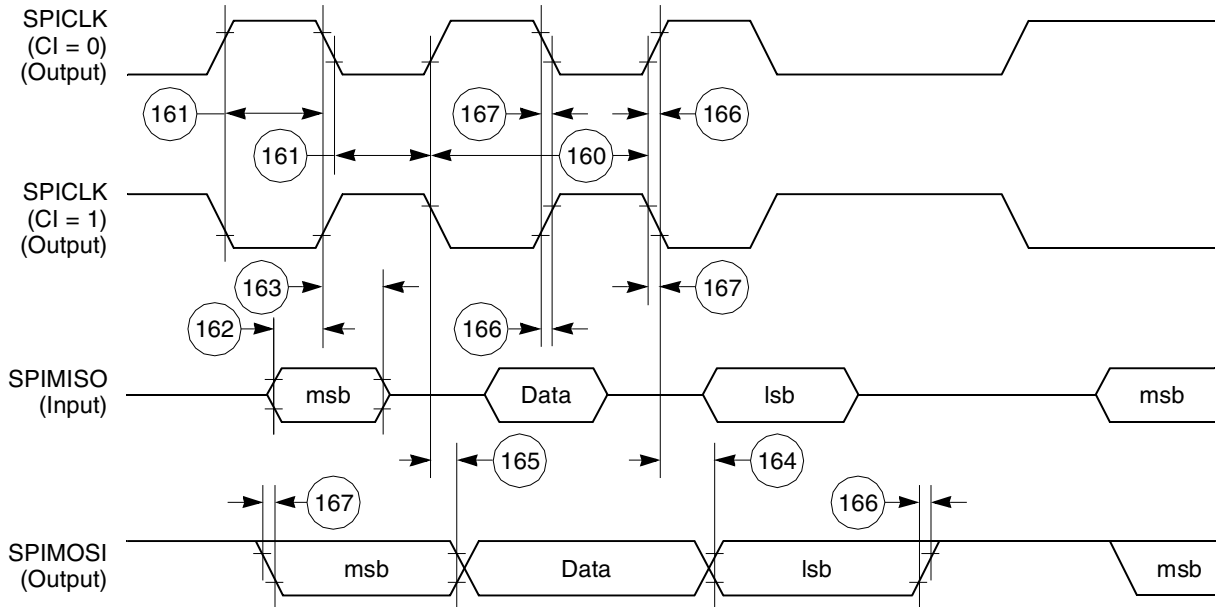


Figure 67. SPI Master (CP = 1) Timing Diagram

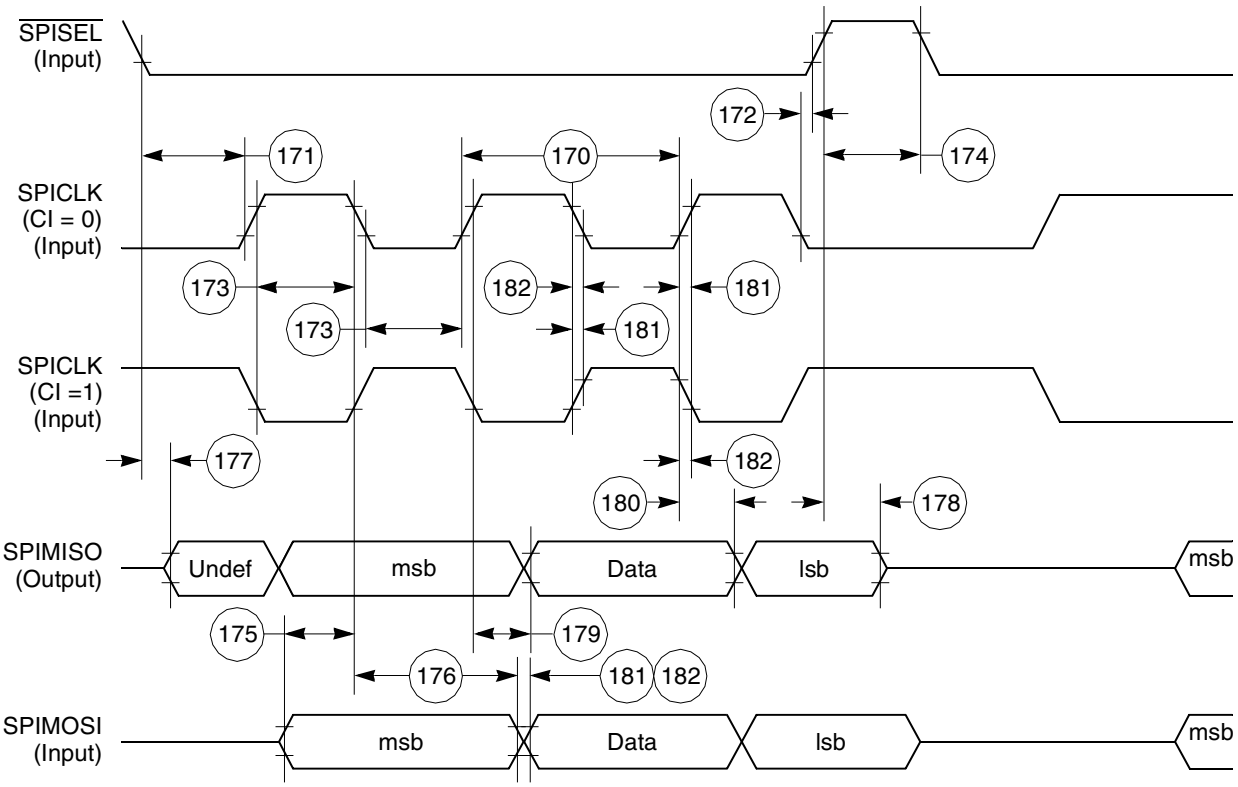


Figure 69. SPI Slave (CP = 1) Timing Diagram

12.12 I²C AC Electrical Specifications

Table 28 provides the I²C (SCL < 100 kHz) timings.

Table 28. I²C Timing (SCL < 100 kHz)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
200	SCL clock frequency (slave)	0	100	kHz
200	SCL clock frequency (master)[1]	1.5	100	kHz
202	Bus free time between transmissions	4.7	—	µs
203	Low period of SCL	4.7	—	µs
204	High period of SCL	4.0	—	µs
205	Start condition setup time	4.7	—	µs
206	Start condition hold time	4.0	—	µs
207	Data hold time	0	—	µs
208	Data setup time	250	—	ns
209	SDL/SCL rise time	—	1	µs

Figure 73 shows MII receive signal timing.

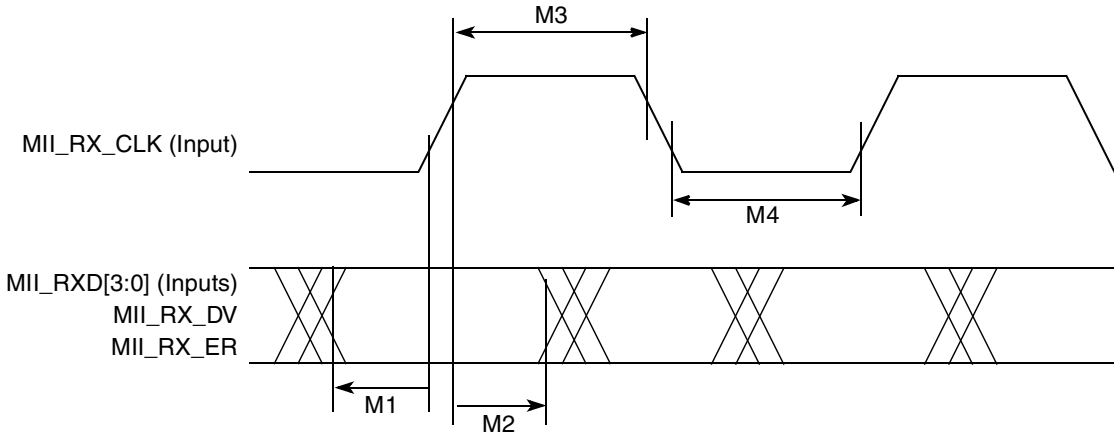


Figure 73. MII Receive Signal Timing Diagram

15.2 MII and Reduced MII Transmit Signal Timing

The transmitter functions correctly up to a MII_TX_CLK maximum frequency of 25 MHz + 1%. The RMII transmitter functions correctly up to a RMII_REFCLK maximum frequency of 50 MHz + 1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_TX_CLK frequency – 1%.

Table 35 provides information on the MII and RMII transmit signal timing.

Table 35. MII Transmit Signal Timing

Num	Characteristic	Min	Max	Unit
M5	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER invalid	5	—	ns
M6	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER valid	—	25	ns
M20_RMII	RMII_TXD[1:0], RMII_TX_EN to RMII_REFCLK setup	4	—	ns
M21_RMII	RMII_TXD[1:0], RMII_TX_EN data hold from RMII_REFCLK rising edge	2	—	ns
M7	MII_TX_CLK and RMII_REFCLK pulse width high	35%	65%	MII_TX_CLK or RMII_REFCLK period
M8	MII_TX_CLK and RMII_REFCLK pulse width low	35%	65%	MII_TX_CLK or RMII_REFCLK period

Table 39 contains a list of the MPC885 input and output signals and shows multiplexing and pin assignments.

Table 39. Pin Assignments

Name	Pin Number	Type
A[0:31]	M16, N18, N19, M19, M17, M18, L16, L19, L17, L18, K19, K18, K17, K16, J19, J17, J18, J16, E19, H18, H17, G19, F17, G17, H16, F19, D19, H19, E18, G18, F18, D18	Bidirectional Three-state
D[0:31]	P2, M1, L1, K2, N1, K4, H3, F2, P1, L4, L3, L2, N3, N2, K3, K1, J2, M4, J1, J3, H2, H1, J4, M3, G2, G1, G3, M2, H4, F1, E1, F3	Bidirectional Three-state
TSIZ0, $\overline{\text{REG}}$	G16	Bidirectional Three-state
TSIZ1	E17	Bidirectional Three-state
RD/$\overline{\text{WR}}$	D13	Bidirectional Three-state
$\overline{\text{BURST}}$	C10	Bidirectional Three-state
$\overline{\text{BDIP}}$, $\overline{\text{GPL\_B5}}$	A13	Output
$\overline{\text{TS}}$	A12	Bidirectional Active pull-up
$\overline{\text{TA}}$	C12	Bidirectional Active pull-up
$\overline{\text{TEA}}$	B12	Open-drain
$\overline{\text{BI}}$	D12	Bidirectional Active pull-up
$\overline{\text{IRQ2}}$, $\overline{\text{RSV}}$	B10	Bidirectional Three-state
$\overline{\text{IRQ4}}$, $\overline{\text{KR}}$, $\overline{\text{RETRY}}$, SPKROUT	C7	Bidirectional Three-state
$\overline{\text{CR}}$, $\overline{\text{IRQ3}}$	A11	Input
$\overline{\text{BR}}$	D11	Bidirectional
$\overline{\text{BG}}$	C11	Bidirectional
$\overline{\text{BB}}$	B11	Bidirectional Active pull-up
FRZ, $\overline{\text{IRQ6}}$	D10	Bidirectional
$\overline{\text{IRQ0}}$	N4	Input
$\overline{\text{IRQ1}}$	P3	Input
$\overline{\text{IRQ7}}$	P4	Input
$\overline{\text{CS}}$[0:5]	B14, C14, A15, D14, C16, A16	Output
$\overline{\text{CS6}}$, $\overline{\text{CE1\_B}}$	D15	Output
$\overline{\text{CS7}}$, $\overline{\text{CE2\_B}}$	B16	Output

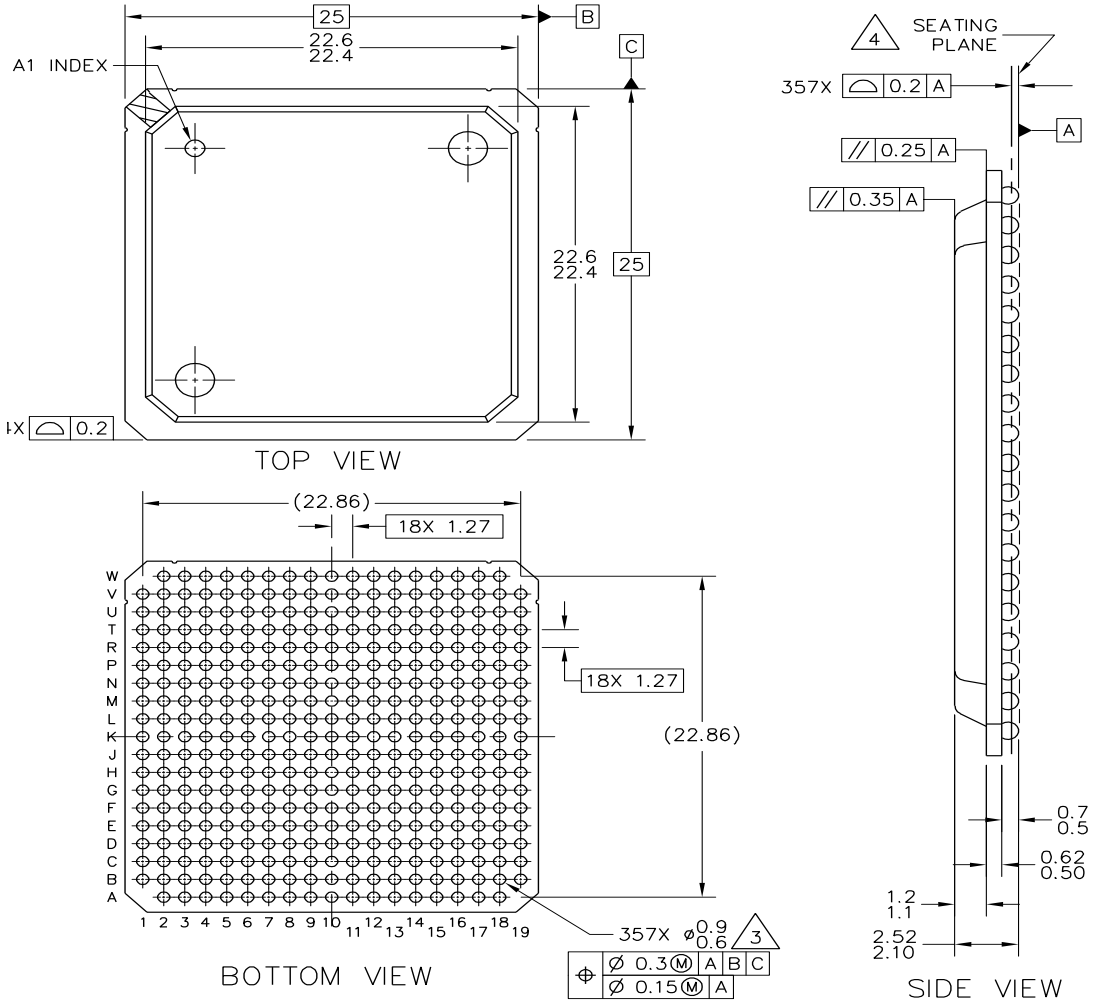
Table 39. Pin Assignments (continued)

Name	Pin Number	Type
PE14, RXD3, MII2-TXD0, RMII2-TXD0	V7	Bidirectional
TMS	V18	Input
TDI, DSDI	T16	Input
TCK, DSCK	U17	Input
$\overline{\text{TRST}}$	W18	Input
TDO, DSDO	T17	Output
MII1_CRS	T11	Input
MII_MDIO	P19	Bidirectional
MII1_TXEN, RMII1_TXEN	T5	Output
MII1_COL	U12	Input
V_{SSSYN1}	C2	PLL analog V_{DD} and GND
V_{SSSYN}	E4	Power
V_{DDLSYN}	B2	Power
GND	G6, G7, G8, G9, G10, G11, G12, G13, H7, H8, H9, H10, H11, H12, H13, H14, J7, J8, J9, J10, J11, J12, J13, K7, K8, K9, K10, K11, K12, K13, L7, L8, L9, L10, L11, L12, L13, M7, M8, M9, M10, M11, M12, M13, N7, N8, N9, N10, N11, N12, N13, N14, P7, P13, R16	Power
V_{DDL}	E5, E6, E9, E11, E14, G15, H5, J5, J15, K15, L5, M15, N5, R6, R9, R10, R12, R15	Power
V_{DDH}	E7, E8, E10, E12, E13, E15, F5, F6, F7, F8, F9, F10, F11, F12, F13, F14, F15, G5, G14, H6, H15, J6, J14, K5, K6, K14, L6, L14, L15, M5, M6, M14, N6, N15, P5, P6, P8, P9, P10, P11, P12, P14, P15, R5, R7, R8, R11, R13, R14	Power
N/C	N17	No connect

[1] ESAR mode only.

16.2 Mechanical Dimensions of the PBGA Package

Figure 78 shows the mechanical dimensions of the PBGA package.



NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M—1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

Figure 78. Mechanical Dimensions and Bottom Surface Nomenclature of the PBGA Package