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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	80MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (2), 10/100Mbps (2)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc880vr80

- Provides enhanced ATM functionality found on the MPC862 and MPC866 families and includes the following:
  - Improved operation, administration and maintenance (OAM) support
  - OAM performance monitoring (PM) support
  - Multiple APC priority levels available to support a range of traffic pace requirements
  - Port-to-port switching capability without the need for RAM-based microcode
  - Simultaneous MII (100BaseT) and UTOPIA (half- or full -duplex) capability
  - Optional statistical cell counters per PHY
  - UTOPIA L2-compliant interface with added FIFO buffering to reduce the total cell transmission time and multi-PHY support. (The earlier UTOPIA L1 specification is also supported.)
  - Parameter RAM for both SPI and I^{2}C can be relocated without RAM-based microcode
  - Supports full-duplex UTOPIA master (ATM side) and slave (PHY side) operations using a split bus
  - AAL2/VBR functionality is ROM-resident
- Up to 32-bit data bus (dynamic bus sizing for 8, 16, and 32 bits)
- Thirty-two address lines
- Memory controller (eight banks)
  - Contains complete dynamic RAM (DRAM) controller
  - Each bank can be a chip select or $\overline{\text{RAS}}$ to support a DRAM bank
  - Up to 30 wait states programmable per memory bank
  - Glueless interface to DRAM, SIMMS, SRAM, EPROMs, Flash EPROMs, and other memory devices
  - DRAM controller programmable to support most size and speed memory interfaces
  - Four $\overline{\text{CAS}}$ lines, four $\overline{\text{WE}}$ lines, and one $\overline{\text{OE}}$ line
  - Boot chip-select available at reset (options for 8-, 16-, or 32-bit memory)
  - Variable block sizes (32 Kbytes–256 Mbytes)
  - Selectable write protection
  - On-chip bus arbitration logic
- General-purpose timers
  - Four 16-bit timers or two 32-bit timers
  - Gate mode can enable/disable counting.
  - Interrupt can be masked on reference match and event capture
- Two fast Ethernet controllers (FEC)—Two 10/100 Mbps Ethernet/IEEE Std. 802.3™ CDMA/CS that interface through MII and/or RMII interfaces
- System integration unit (SIU)
  - Bus monitor
  - Software watchdog

- On-chip 16×16 multiply accumulate controller (MAC)
    - One operation per clock (two-clock latency, one-clock blockage)
    - MAC operates concurrently with other instructions
    - FIR loop—Four clocks per four multiplies
- Four baud rate generators
    - Independent (can be connected to any SCC or SMC)
    - Allow changes during operation
    - Autobaud support option
- Up to three serial communication controllers (SCCs) supporting the following protocols:
    - Serial ATM capability on SCCs
    - Optional UTOPIA port on SCC4
    - Ethernet/IEEE Std 802.3™ optional on the SCC(s) supporting full 10-Mbps operation
    - HDLC/SDLC
    - HDLC bus (implements an HDLC-based local area network (LAN))
    - Asynchronous HDLC to support point-to-point protocol (PPP)
    - AppleTalk
    - Universal asynchronous receiver transmitter (UART)
    - Synchronous UART
    - Serial infrared (IrDA)
    - Binary synchronous communication (BISYNC)
    - Totally transparent (bit streams)
    - Totally transparent (frame based with optional cyclic redundancy check (CRC))
- Up to two serial management channels (SMCs) supporting the following protocols:
    - UART (low-speed operation)
    - Transparent
    - General circuit interface (GCI) controller
    - Provide management for BRI devices as GCI controller in time-division multiplexed (TDM) channels
- Universal serial bus (USB)—Supports operation as a USB function endpoint, a USB host controller, or both for testing purposes (loop-back diagnostics)
    - USB 2.0 full-/low-speed compatible
    - The USB function mode has the following features:
        - Four independent endpoints support control, bulk, interrupt, and isochronous data transfers.
        - CRC16 generation and checking
        - CRC5 checking
        - NRZI encoding/decoding with bit stuffing
        - 12- or 1.5-Mbps data rate

MPC885/MPC880 PowerQUICC Hardware Specifications, Rev. 7

- – Flexible data buffers with multiple buffers per frame
- – Automatic retransmission upon transmit error
- — The USB host controller has the following features:
  - – Supports control, bulk, interrupt, and isochronous data transfers
  - – CRC16 generation and checking
  - – NRZI encoding/decoding with bit stuffing
  - – Supports both 12- and 1.5-Mbps data rates (automatic generation of preamble token and data rate configuration). Note that low-speed operation requires an external hub.
  - – Flexible data buffers with multiple buffers per frame
  - – Supports local loop back mode for diagnostics (12 Mbps only)
- Serial peripheral interface (SPI)
  - — Supports master and slave modes
  - — Supports multiple-master operation on the same bus
- Inter-integrated circuit (I^2C) port
  - — Supports master and slave modes
  - — Supports a multiple-master environment
- Time-slot assigner (TSA)
  - — Allows SCCs and SMCs to run in multiplexed and/or non-multiplexed operation
  - — Supports T1, CEPT, PCM highway, ISDN basic rate, ISDN primary rate, user defined
  - — 1- or 8-bit resolution
  - — Allows independent transmit and receive routing, frame synchronization, and clocking
  - — Allows dynamic changes
  - — Can be internally connected to four serial channels (two SCCs and two SMCs)
- Parallel interface port (PIP)
  - — Centronics interface support
  - — Supports fast connection between compatible ports on MPC885/MPC880 and other MPC8xx devices
- PCMCIA interface
  - — Master (socket) interface, release 2.1-compliant
  - — Supports two independent PCMCIA sockets
  - — 8 memory or I/O windows supported
- Debug interface
  - — Eight comparators: four operate on instruction address, two operate on data address, and two operate on data
  - — Supports conditions: $= \neq < >$
  - — Each watchpoint can generate a break point internally.
- Normal high and normal low power modes to conserve power

Table 6. DC Electrical Specifications (continued)

Characteristic	Symbol	Min	Max	Unit
Output high voltage, $I_{OH} = -2.0$ mA, except XTAL and open-drain pins	V_{OH}	2.4	—	V
Output low voltage $I_{OL} = 2.0$ mA (CLKOUT) $I_{OL} = 3.2$ mA[5] $I_{OL} = 5.3$ mA[6] $I_{OL} = 7.0$ mA (TXD1/PA14, TXD2/PA12) $I_{OL} = 8.9$ mA ($\overline{TS}$, $\overline{TA}$, $\overline{TEA}$, $\overline{BI}$, $\overline{BB}$, $\overline{HRESET}$, $\overline{SRESET}$)	V_{OL}	—	0.5	V

[1] The difference between V_{DDL} and V_{DDSYN} cannot be more than 100 mV.

[2] The signals PA[0:15], PB[14:31], PC[4:15], PD[3:15], PE(14:31), TDI, TDO, TCK, $\overline{TRST}$, TMS, MII1_TXEN, MII_MDIO are 5-V tolerant. The minimum voltage is still 2.0 V.

[3] V_{IL}(max) for the I^{2}C interface is 0.8 V rather than the 1.5 V as specified in the I^{2}C standard.

[4] Input capacitance is periodically sampled.

[5] A(0:31), TSIZ0/$\overline{REG}$, TSIZ1, D(0:31), $\overline{IRQ}$(2:4), $\overline{IRQ6}$, RD/$\overline{WR}$, $\overline{BURST}$, IP_B(3:7), PA(0:11), PA13, PA15, PB(14:31), PC(4:15), PD(3:15), PE(14:31), MII1_CRS, MII_MDIO, MII1_TXEN, and MII1_COL.

[6] $\overline{BDIP}$/GPL_B(5), $\overline{BR}$, $\overline{BG}$, FRZ/$\overline{IRQ6}$, $\overline{CS}$(0:7), $\overline{WE}$(0:3), $\overline{BS}$_A(0:3), $\overline{GPL\_A0}$/$\overline{GPL\_B0}$, $\overline{OE}$/GPL_A1/$\overline{GPL\_B1}$, $\overline{GPL\_A}$(2:3)/$\overline{GPL\_B}$(2:3)/$\overline{CS}$(2:3), UPWAITA/$\overline{GPL\_A4}$, UPWAITB/$\overline{GPL\_B4}$, $\overline{GPL\_A5}$, ALE_A, $\overline{CE1}$_A, $\overline{CE2}$_A, OP(0:3), and BADDR(28:30).

7 Thermal Calculation and Measurement

For the following discussions, $P_D = (V_{DDL} \times I_{DDL}) + PI/O$, where PI/O is the power dissipation of the I/O drivers.

NOTE

The V_{DDSYN} power dissipation is negligible.

7.1 Estimation with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, in °C can be obtained from the following equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_A = ambient temperature (°C)

$R_{\theta JA}$ = package junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in package

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. However, the answer is only an estimate; test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

7.6   References

Semiconductor Equipment and Materials International(415) 964-5111
805 East Middlefield Rd
Mountain View, CA 94043

MIL-SPEC and EIA/JESD (JEDEC) specifications800-854-7179 or
(Available from Global Engineering Documents)303-397-7956

JEDEC Specifications   http://www.jedec.org

1. C.E. Triplett and B. Joiner, "An Experimental Characterization of a 272 PBGA Within an
    Automotive Engine Controller Module," Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.

2. 2. B. Joiner and V. Adams, "Measurement and Simulation of Junction to Board Thermal
    Resistance and Its Application in Thermal Modeling," Proceedings of SemiTherm, San Diego,
    1999, pp. 212–220.

8   Power Supply and Power Sequencing

This section provides design considerations for the MPC885/MPC880 power supply. The
MPC885/MPC880 has a core voltage (V_{DDL}) and PLL voltage (V_{DDSYN}), which both operate at a lower
voltage than the I/O voltage V_{DDH}. The I/O section of the MPC885/MPC880 is supplied with 3.3 V across
V_{DDH} and V_{SS} (GND).

The signals PA[0:15], PB[14:31], PC[4:15], PD[3:15], TDI, TDO, TCK, TRST_B, TMS, MII_TXEN, and
MII_MDIO are 5 V tolerant. All inputs cannot be more than 2.5 V greater than V_{DDH}. In addition, 5-V
tolerant pins cannot exceed 5.5 V and remaining input pins cannot exceed 3.465 V. This restriction applies
to power up/down and normal operation.

One consequence of multiple power supplies is that when power is initially applied the voltage rails ramp
up at different rates. The rates depend on the nature of the power supply, the type of load on each power
supply, and the manner in which different voltages are derived. The following restrictions apply:

- V_{DDL} must not exceed V_{DDH} during power up and power down.
- V_{DDL} must not exceed 1.9 V, and V_{DDH} must not exceed 3.465 V.

These cautions are necessary for the long-term reliability of the part. If they are violated, the electrostatic
discharge (ESD) protection diodes are forward-biased, and excessive current can flow through these
diodes. If the system power supply design does not control the voltage sequencing, the circuit shown
Figure 5 can be added to meet these requirements. The MUR420 Schottky diodes control the maximum
potential difference between the external bus and core power supplies on power up, and the 1N5820 diodes
regulate the maximum potential difference on power down.

Table 9. Bus Operation Timings (continued)

| Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B32	CLKOUT falling edge to $\overline{BS}$ valid, as requested by control bit BST4 in the corresponding word in the UPM (MAX = 0.00 × B1 + 6.00)	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B32a	CLKOUT falling edge to $\overline{BS}$ valid, as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 0 (MAX = 0.25 × B1 + 6.80)	7.60	14.30	6.30	13.00	3.80	10.50	3.13	10.00	ns
B32b	CLKOUT rising edge to $\overline{BS}$ valid, as requested by control bit BST2 in the corresponding word in the UPM (MAX = 0.00 × B1 + 8.00)	1.50	8.00	1.50	8.00	1.50	8.00	1.50	8.00	ns
B32c	CLKOUT rising edge to $\overline{BS}$ valid, as requested by control bit BST3 in the corresponding word in the UPM (MAX = 0.25 × B1 + 6.80)	7.60	14.30	6.30	13.00	3.80	10.50	3.13	10.00	ns
B32d	CLKOUT falling edge to $\overline{BS}$ valid, as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 1 (MAX = 0.375 × B1 + 6.60)	13.30	18.00	11.30	16.00	7.60	12.30	4.49	11.30	ns
B33	CLKOUT falling edge to $\overline{GPL}$ valid, as requested by control bit GxT4 in the corresponding word in the UPM (MAX = 0.00 × B1 + 6.00)	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B33a	CLKOUT rising edge to $\overline{GPL}$ valid, as requested by control bit GxT3 in the corresponding word in the UPM (MAX = 0.25 × B1 + 6.80)	7.60	14.30	6.30	13.00	3.80	10.50	3.13	10.00	ns
B34	A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid, as requested by control bit CST4 in the corresponding word in the UPM (MIN = 0.25 × B1 − 2.00)	5.60	—	4.30	—	1.80	—	1.13	—	ns
B34a	A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid, as requested by control bit CST1 in the corresponding word in the UPM (MIN = 0.50 × B1 − 2.00)	13.20	—	10.50	—	5.60	—	4.25	—	ns
B34b	A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid, as requested by CST2 in the corresponding word in UPM (MIN = 0.75 × B1 − 2.00)	20.70	—	16.70	—	9.40	—	6.80	—	ns
B35	A(0:31), BADDR(28:30) to $\overline{CS}$ valid, as requested by control bit BST4 in the corresponding word in the UPM (MIN = 0.25 × B1 − 2.00)	5.60	—	4.30	—	1.80	—	1.13	—	ns
B35a	A(0:31), BADDR(28:30), and D(0:31) to $\overline{BS}$ valid, as requested by BST1 in the corresponding word in the UPM (MIN = 0.50 × B1 − 2.00)	13.20	—	10.50	—	5.60	—	4.25	—	ns
B35b	A(0:31), BADDR(28:30), and D(0:31) to $\overline{BS}$ valid, as requested by control bit BST2 in the corresponding word in the UPM (MIN = 0.75 × B1 − 2.00)	20.70	—	16.70	—	9.40	—	7.40	—	ns
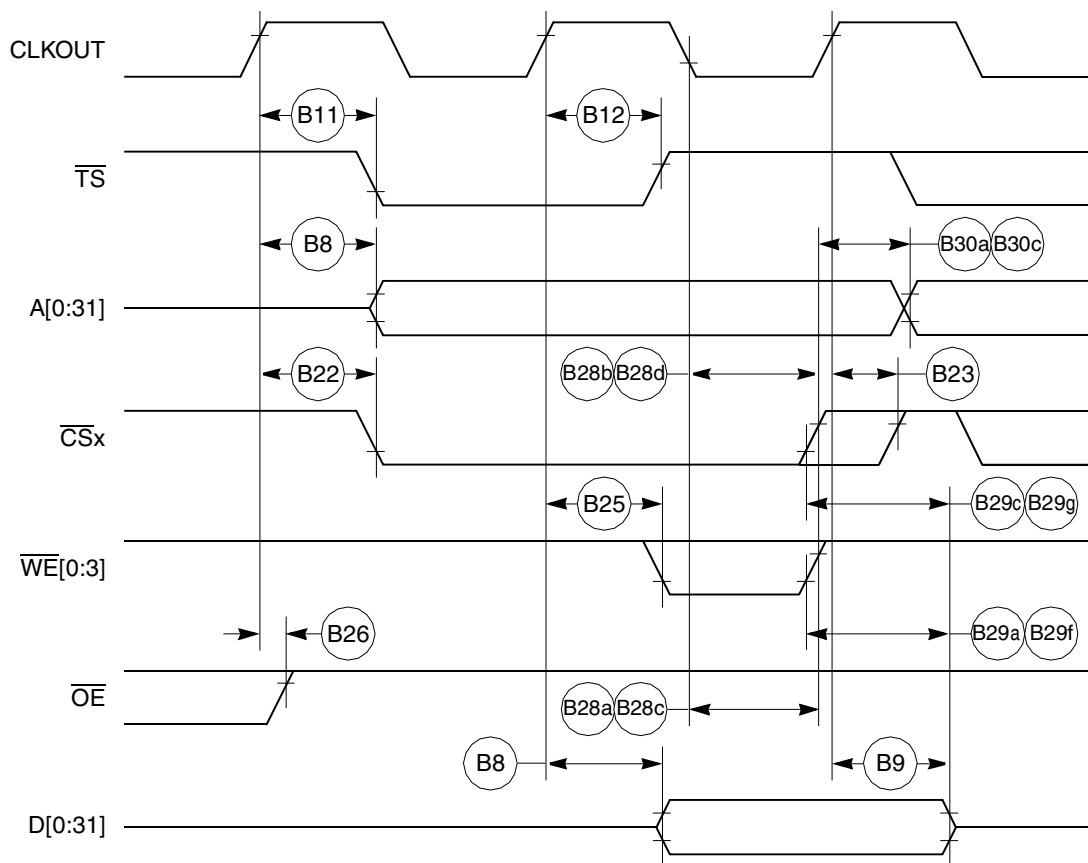
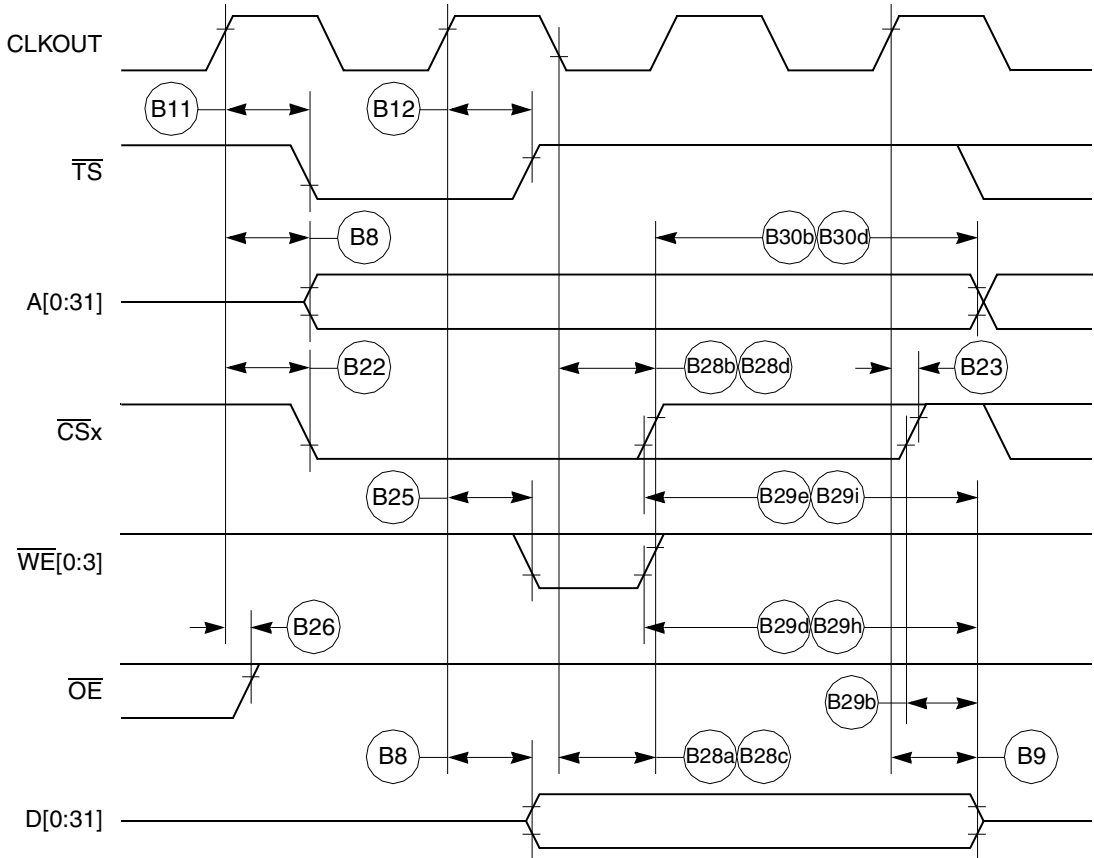**Figure 18. External Bus Write Timing (GPCM Controlled—TRLX = 0, CSNT = 1)**

Figure 19. External Bus Write Timing (GPCM Controlled—TRLX = 1, CSNT = 1)

Table 12 shows the PCMCIA port timing for the MPC885/MPC880.

Table 12. PCMCIA Port Timing

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
P57	CLKOUT to OPx valid (MAX = 0.00 × B1 + 19.00)	—	19.00	—	19.00	—	19.00	—	19.00	ns
P58	$\overline{\text{HRESET}}$ negated to OPx drive[1] (MIN = 0.75 × B1 + 3.00)	25.70	—	21.70	—	14.40	—	12.40	—	ns
P59	IP_Xx valid to CLKOUT rising edge (MIN = 0.00 × B1 + 5.00)	5.00	—	5.00	—	5.00	—	5.00	—	ns
P60	CLKOUT rising edge to IP_Xx invalid (MIN = 0.00 × B1 + 1.00)	1.00	—	1.00	—	1.00	—	1.00	—	ns

[1] OP2 and OP3 only.

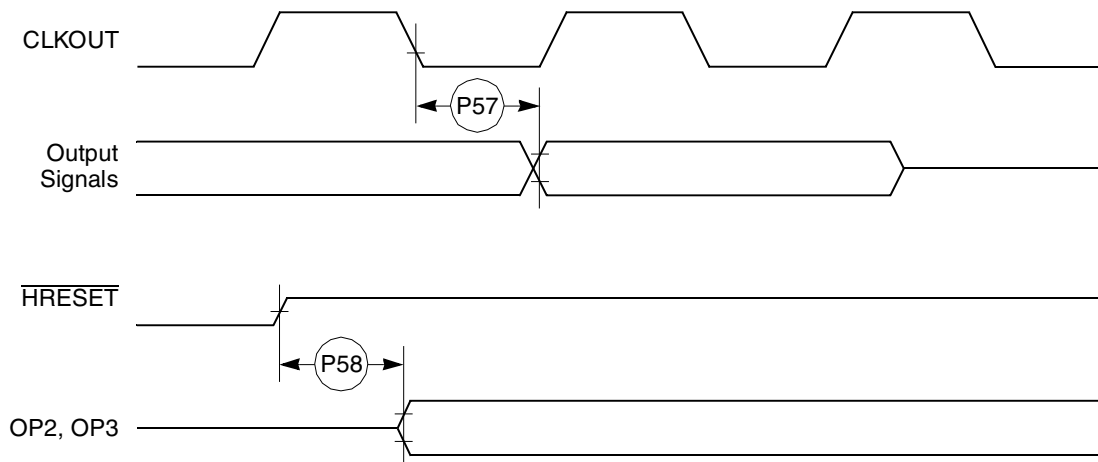Figure 31 provides the PCMCIA output port timing for the MPC885/MPC880.

Figure 31. PCMCIA Output Port Timing

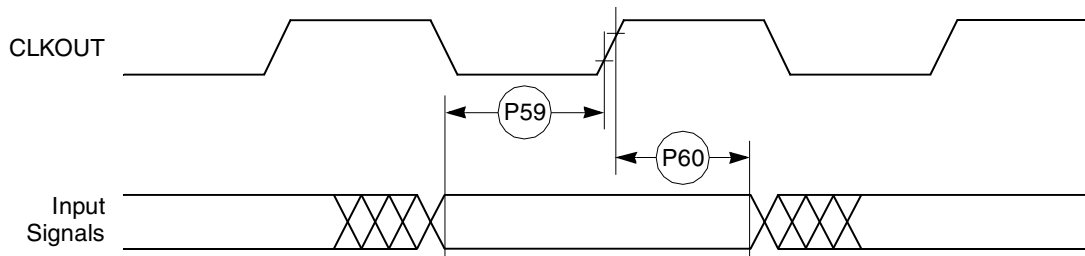Figure 32 provides the PCMCIA input port timing for the MPC885/MPC880.

Figure 32. PCMCIA Input Port Timing

Table 14 shows the reset timing for the MPC885/MPC880.

Table 14. Reset Timing

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
R69	CLKOUT to HRESET high impedance (MAX = 0.00 × B1 + 20.00)	—	20.00	—	20.00	—	20.00	—	20.00	ns
R70	CLKOUT to SRESET high impedance (MAX = 0.00 × B1 + 20.00)	—	20.00	—	20.00	—	20.00	—	20.00	ns
R71	RSTCONF pulse width (MIN = 17.00 × B1)	515.20	—	425.00	—	257.60	—	212.50	—	ns
R72	—	—	—	—	—	—	—	—	—	—
R73	Configuration data to HRESET rising edge setup time (MIN = 15.00 × B1 + 50.00)	504.50	—	425.00	—	277.30	—	237.50	—	ns
R74	Configuration data to RSTCONF rising edge setup time (MIN = 0.00 × B1 + 350.00)	350.00	—	350.00	—	350.00	—	350.00	—	ns
R75	Configuration data hold time after RSTCONF negation (MIN = 0.00 × B1 + 0.00)	0.00	—	0.00	—	0.00	—	0.00	—	ns
R76	Configuration data hold time after HRESET negation (MIN = 0.00 × B1 + 0.00)	0.00	—	0.00	—	0.00	—	0.00	—	ns
R77	HRESET and RSTCONF asserted to data out drive (MAX = 0.00 × B1 + 25.00)	—	25.00	—	25.00	—	25.00	—	25.00	ns
R78	RSTCONF negated to data out high impedance (MAX = 0.00 × B1 + 25.00)	—	25.00	—	25.00	—	25.00	—	25.00	ns
R79	CLKOUT of last rising edge before chip three-states HRESET to data out high impedance (MAX = 0.00 × B1 + 25.00)	—	25.00	—	25.00	—	25.00	—	25.00	ns
R80	DSDI, DSCK setup (MIN = 3.00 × B1)	90.90	—	75.00	—	45.50	—	37.50	—	ns
R81	DSDI, DSCK hold time (MIN = 0.00 × B1 + 0.00)	0.00	—	0.00	—	0.00	—	0.00	—	ns
R82	SRESET negated to CLKOUT rising edge for DSDI and DSCK sample (MIN = 8.00 × B1)	242.40	—	200.00	—	121.20	—	100.00	—	ns

12 CPM Electrical Characteristics

This section provides the AC and DC electrical specifications for the communications processor module (CPM) of the MPC885/MPC880.

12.1 PIP/PIO AC Electrical Specifications

Table 16 provides the PIP/PIO AC timings as shown in Figure 42 through Figure 46.

Table 16. PIP/PIO Timing

| Num	Characteristic	All Frequencies		Unit
		Min	Max	
21	Data-in setup time to STBI low	0	—	ns
22	Data-In hold time to STBI high	0	—	clk
23	STBI pulse width	1.5	—	clk
24	STBO pulse width	1 clk – 5 ns	—	ns
25	Data-out setup time to STBO low	2	—	clk
26	Data-out hold time from STBO high	5	—	clk
27	STBI low to STBO low (Rx interlock)	—	4.5	clk
28	STBI low to STBO high (Tx interlock)	2	—	clk
29	Data-in setup time to clock high	15	—	ns
30	Data-in hold time from clock high	7.5	—	ns
31	Clock low to data-out valid (CPU writes data, control, or direction)	—	25	ns
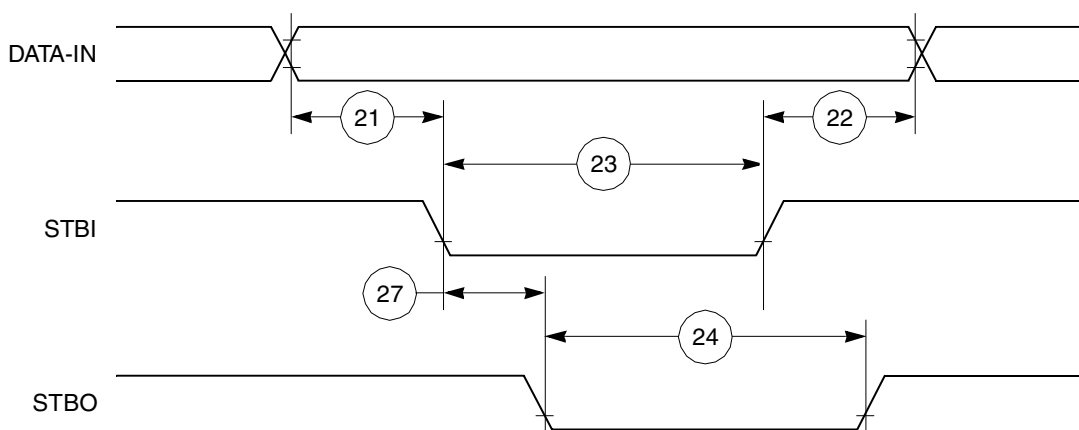
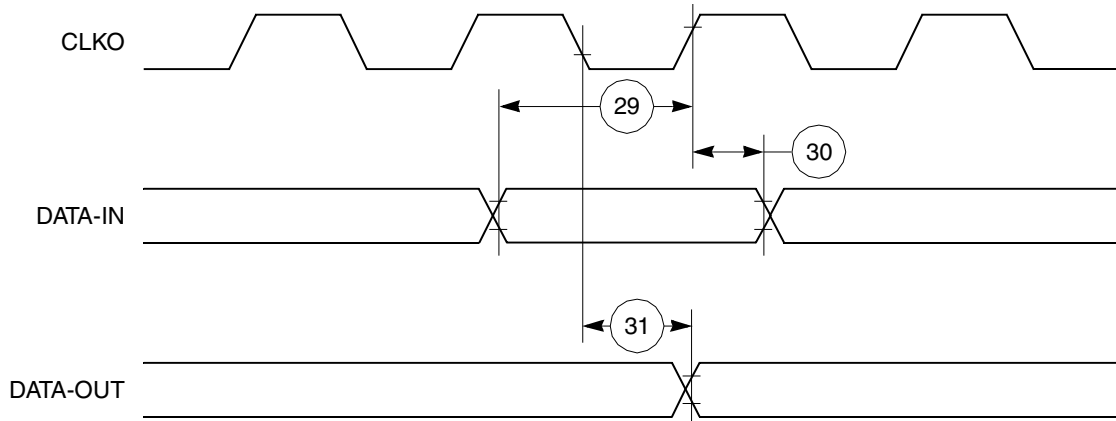**Figure 42. PIP Rx (Interlock Mode) Timing Diagram**

Figure 46. Parallel I/O Data-In/Data-Out Timing Diagram

12.2   Port C Interrupt AC Electrical Specifications

Table 17 provides the timings for port C interrupts.

Table 17. Port C Interrupt Timing

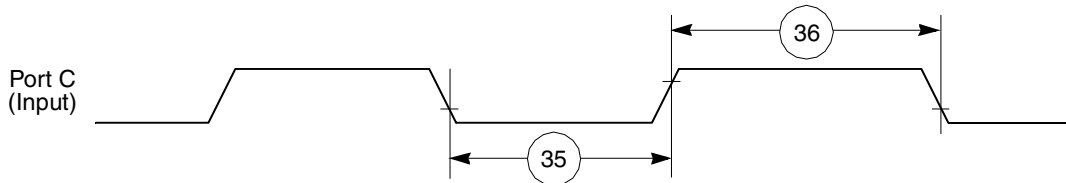| Num	Characteristic	33.34 MHz		Unit
		Min	Max	
35	Port C interrupt pulse width low (edge-triggered mode)	55	—	ns
36	Port C interrupt minimum time between active edges	55	—	ns

Figure 47 shows the port C interrupt detection timing.

Figure 47. Port C Interrupt Detection Timing
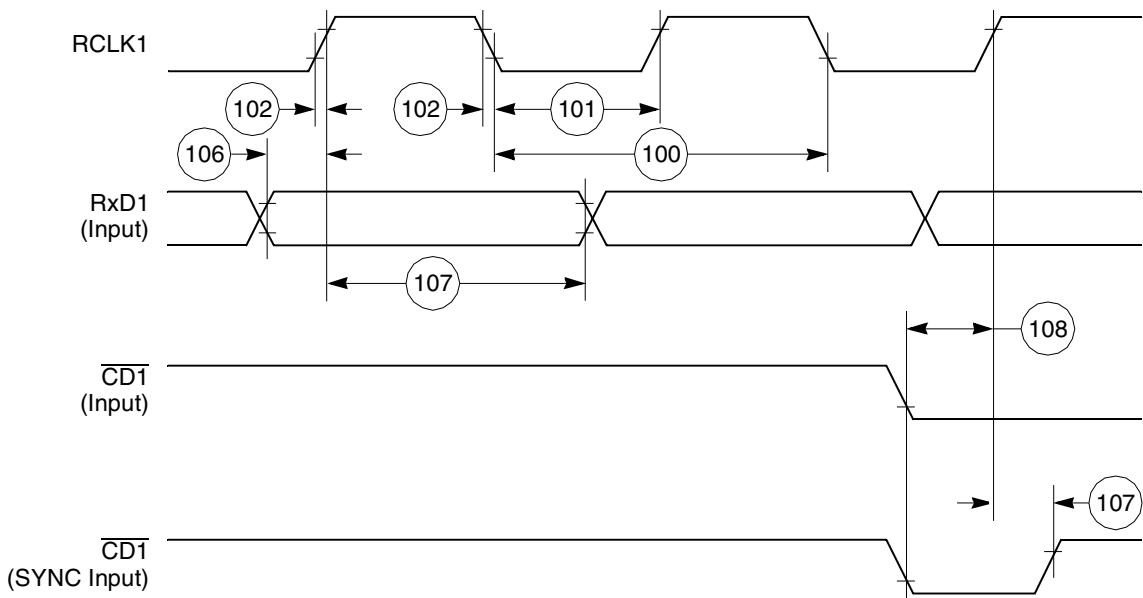
Figure 59 through Figure 61 show the NMSI timings.

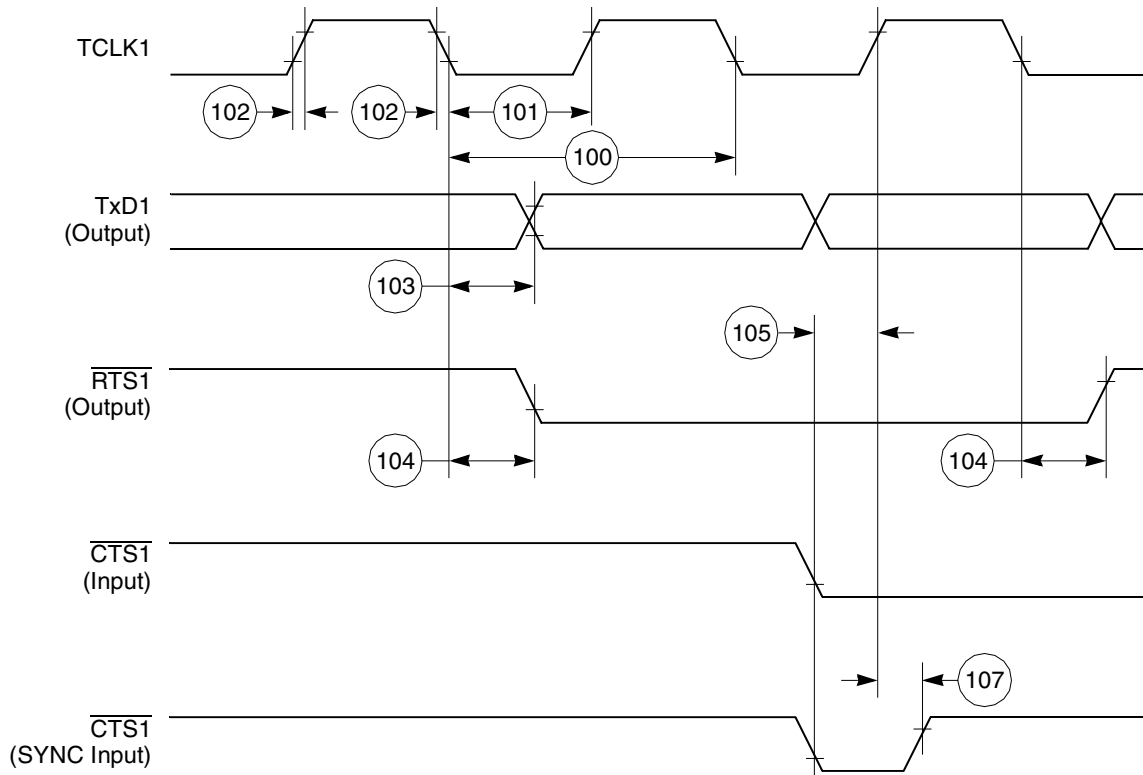**Figure 59. SCC NMSI Receive Timing Diagram**

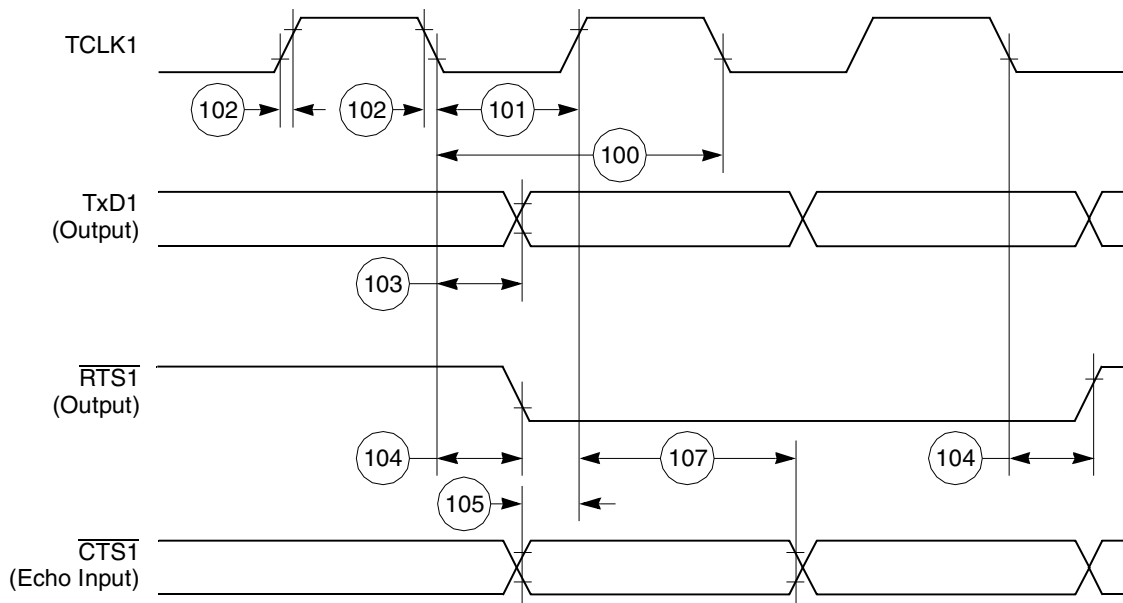**Figure 60. SCC NMSI Transmit Timing Diagram**

Figure 61. HDLC Bus Timing Diagram

12.8 Ethernet Electrical Specifications

Table 24 provides the Ethernet timings as shown in Figure 62 through Figure 64.

Table 24. Ethernet Timing

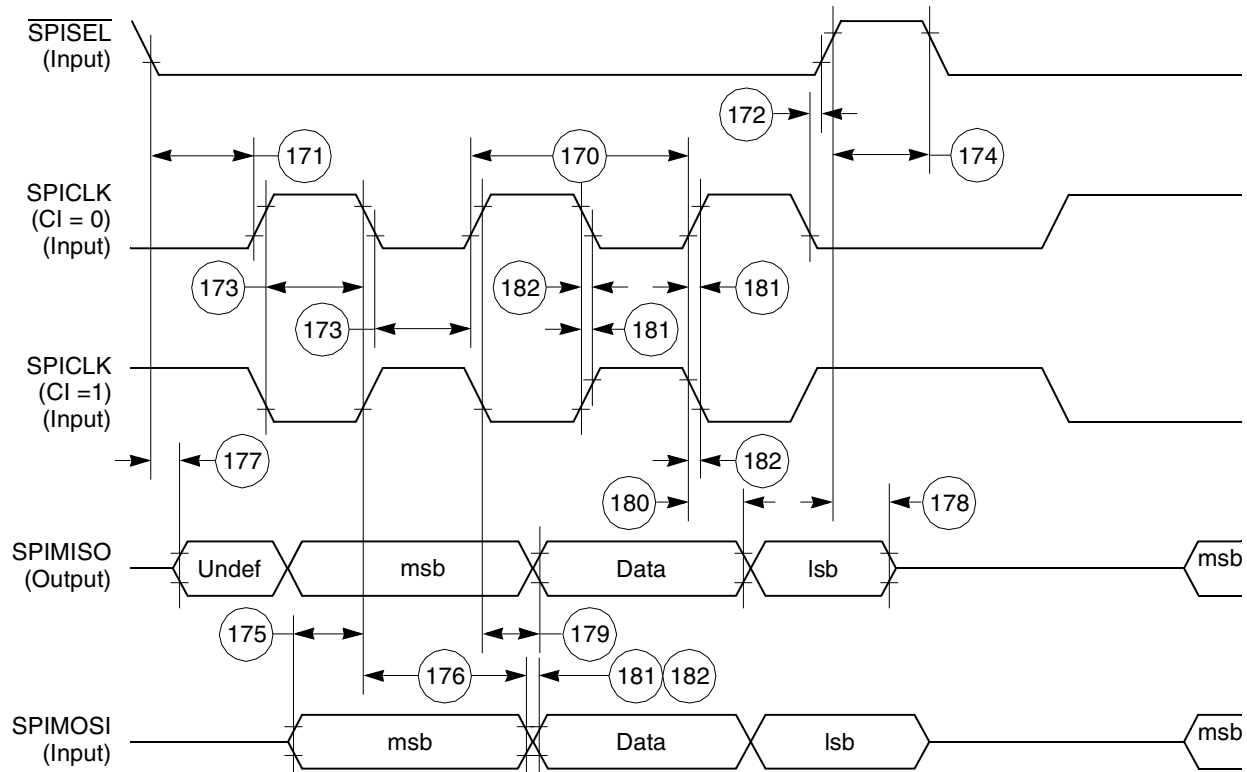| Num	Characteristic	All Frequencies		Unit
		Min	Max	
120	CLSN width high	40	—	ns
121	RCLK1 rise/fall time	—	15	ns
122	RCLK1 width low	40	—	ns
123	RCLK1 clock period[1]	80	120	ns
124	RXD1 setup time	20	—	ns
125	RXD1 hold time	5	—	ns
126	RENA active delay (from RCLK1 rising edge of the last data bit)	10	—	ns
127	RENA width low	100	—	ns
128	TCLK1 rise/fall time	—	15	ns
129	TCLK1 width low	40	—	ns
130	TCLK1 clock period[1]	99	101	ns
131	TXD1 active delay (from TCLK1 rising edge)	—	50	ns
132	TXD1 inactive delay (from TCLK1 rising edge)	6.5	50	ns
133	TENA active delay (from TCLK1 rising edge)	10	50	ns

Figure 69. SPI Slave (CP = 1) Timing Diagram

12.12 I²C AC Electrical Specifications

Table 28 provides the I²C (SCL < 100 kHz) timings.

Table 28. I²C Timing (SCL < 100 kHz)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
200	SCL clock frequency (slave)	0	100	kHz
200	SCL clock frequency (master)[1]	1.5	100	kHz
202	Bus free time between transmissions	4.7	—	μs
203	Low period of SCL	4.7	—	μs
204	High period of SCL	4.0	—	μs
205	Start condition setup time	4.7	—	μs
206	Start condition hold time	4.0	—	μs
207	Data hold time	0	—	μs
208	Data setup time	250	—	ns
209	SDL/SCL rise time	—	1	μs

Table 28. I²C Timing (SCL < 100 kHz) (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
210	SDL/SCL fall time	—	300	ns
211	Stop condition setup time	4.7	—	µs

[1] SCL frequency is given by SCL = BRGCLK_frequency/((BRG register + 3) × pre_scaler × 2).
The ratio SyncClk/(BRGCLK/pre_scaler) must be greater or equal to 4/1.

Table 29 provides the I²C (SCL > 100 kHz) timings.

Table 29. I²C Timing (SCL > 100 kHz)

Num	Characteristic	Expression	All Frequencies		Unit
			Min	Max	
200	SCL clock frequency (slave)	fSCL	0	BRGCLK/48	Hz
200	SCL clock frequency (master)[1]	fSCL	BRGCLK/16512	BRGCLK/48	Hz
202	Bus free time between transmissions	—	$1/(2.2 \times fSCL)$	—	s
203	Low period of SCL	—	$1/(2.2 \times fSCL)$	—	s
204	High period of SCL	—	$1/(2.2 \times fSCL)$	—	s
205	Start condition setup time	—	$1/(2.2 \times fSCL)$	—	s
206	Start condition hold time	—	$1/(2.2 \times fSCL)$	—	s
207	Data hold time	—	0	—	s
208	Data setup time	—	$1/(40 \times fSCL)$	—	s
209	SDL/SCL rise time	—	—	$1/(10 \times fSCL)$	s
210	SDL/SCL fall time	—	—	$1/(33 \times fSCL)$	s
211	Stop condition setup time	—	$1/2(2.2 \times fSCL)$	—	s

[1] SCL frequency is given by SCL = BrgClk_frequency/((BRG register + 3) × pre_scaler × 2).
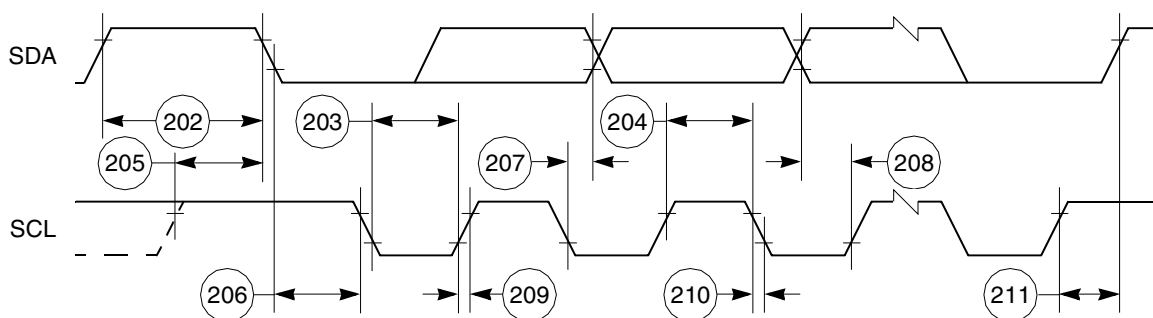The ratio SyncClk/(Brg_Clk/pre_scaler) must be greater or equal to 4/1.

Figure 70 shows the I²C bus timing.

Figure 70. I²C Bus Timing Diagram

13 UTOPIA AC Electrical Specifications

Table 30, Table 31, and Table 32, show the AC electrical specifications for the UTOPIA interface.

Table 30. UTOPIA Master (Muxed Mode) Electrical Specifications

Num	Signal Characteristic	Direction	Min	Max	Unit
U1	UtpClk rise/fall time (internal clock option)	Output		4	ns
	Duty cycle		50	50	%
	Frequency			33	MHz
U2	UTPB, SOC, $\overline{\text{RxEnb}}$, $\overline{\text{TxEnb}}$, RxAddr, and TxAddr active delay (PHREQ and PHSEL active delay in multi-PHY mode)	Output	2	16	ns
U3	UTPB, SOC, Rxclav, and Txclav setup time	Input	4		ns
U4	UTPB, SOC, Rxclav, and Txclav hold time	Input	1		ns

Table 31. UTOPIA Master (Split Bus Mode) Electrical Specifications

Num	Signal Characteristic	Direction	Min	Max	Unit
U1	UtpClk rise/fall time (Internal clock option)	Output		4	ns
	Duty cycle		50	50	%
	Frequency			33	MHz
U2	UTPB, SOC, $\overline{\text{RxEnb}}$, $\overline{\text{TxEnb}}$, RxAddr, and TxAddr active delay (PHREQ and PHSEL active delay in multi-PHY mode)	Output	2	16	ns
U3	UTPB_Aux, SOC_Aux, Rxclav, and Txclav setup time	Input	4		ns
U4	UTPB_Aux, SOC_Aux, Rxclav, and Txclav hold time	Input	1		ns

Table 32. UTOPIA Slave (Split Bus Mode) Electrical Specifications

Num	Signal Characteristic	Direction	Min	Max	Unit
U1	UtpClk rise/fall time (external clock option)	Input		4	ns
	Duty cycle		40	60	%
	Frequency			33	MHz
U2	UTPB, SOC, Rxclav, and Txclav active delay	Output	2	16	ns
U3	UTPB_AUX, SOC_Aux, $\overline{\text{RxEnb}}$, $\overline{\text{TxEnb}}$, RxAddr, and TxAddr setup time	Input	4		ns
U4	UTPB_AUX, SOC_Aux, $\overline{\text{RxEnb}}$, $\overline{\text{TxEnb}}$, RxAddr, and TxAddr hold time	Input	1		ns

14 USB Electrical Characteristics

This section provides the AC timings for the USB interface.

14.1 USB Interface AC Timing Specifications

The USB Port uses the transmit clock on SCC1. Table 33 lists the USB interface timings.

Table 33. USB Interface AC Timing Specifications

Name	Characteristic	All Frequencies		Unit
		Min	Max	
US1	USBCLK frequency of operation[1] Low speed Full speed		6 48	MHz MHz
US4	USBCLK duty cycle (measured at 1.5 V)	45	55	%

[1] USBCLK accuracy should be ±500 ppm or better. USBCLK may be stopped to conserve power.

15 FEC Electrical Characteristics

This section provides the AC electrical specifications for the fast Ethernet controller (FEC). Note that the timing specifications for the MII signals are independent of system clock frequency (part speed designation). Also, MII signals use TTL signal levels compatible with devices operating at either 5.0 or 3.3 V.

15.1 MII and Reduced MII Receive Signal Timing

The receiver functions correctly up to a MII_RX_CLK maximum frequency of 25 MHz + 1%. The reduced MII (RMII) receiver functions correctly up to a RMII_REFCLK maximum frequency of 50 MHz + 1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_RX_CLK frequency – 1%.

Table 34 provides information on the MII and RMII receive signal timing.

Table 34. MII Receive Signal Timing

Num	Characteristic	Min	Max	Unit
M1	MII_RXD[3:0], MII_RX_DV, MII_RX_ERR to MII_RX_CLK setup	5	—	ns
M2	MII_RX_CLK to MII_RXD[3:0], MII_RX_DV, MII_RX_ER hold	5	—	ns
M3	MII_RX_CLK pulse width high	35%	65%	MII_RX_CLK period
M4	MII_RX_CLK pulse width low	35%	65%	MII_RX_CLK period
M1_RMII	RMII_RXD[1:0], RMII_CRS_DV, RMII_RX_ERR to RMII_REFCLK setup	4	—	ns
M2_RMII	RMII_REFCLK to RMII_RXD[1:0], RMII_CRS_DV, RMII_RX_ERR hold	2	—	ns

16.2   Mechanical Dimensions of the PBGA Package

Figure 78 shows the mechanical dimensions of the PBGA package.
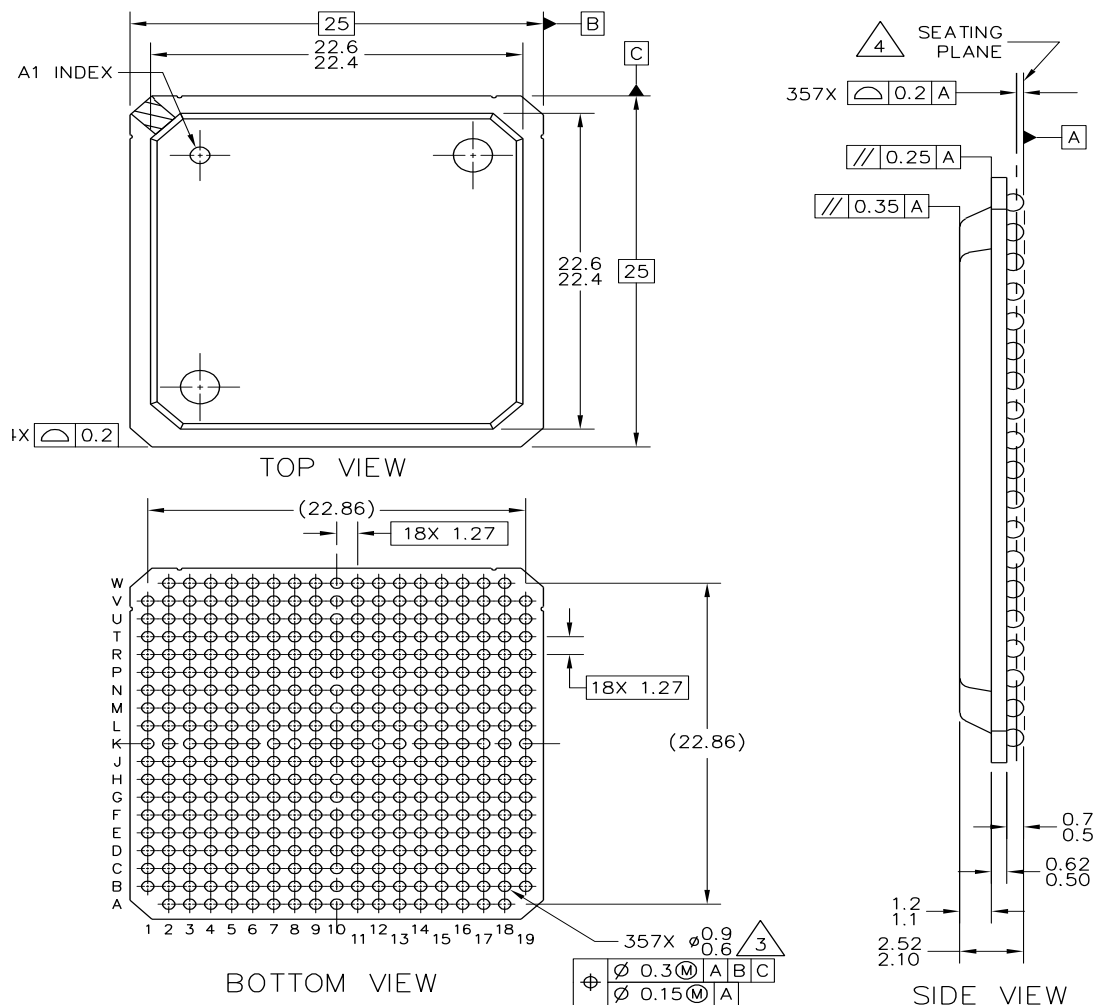
NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M—1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

Figure 78. Mechanical Dimensions and Bottom Surface Nomenclature of the PBGA Package

Table 40. Document Revision History (continued)

Revision Number	Date	Changes
0.4	5/2003	Changed the pin descriptions for PD8 and PD9.
0.3	05/2003	Corrected the signals that had overlines on them.
0.2	05/2003	Made the changes to the RMII Timing, Made sure all the V_{DDL}, V_{DDH}, and GND show up on the pinout diagram. Changed the SPI Master Timing Specs. 162 and 164.
0.1	04/2003	Added pinout and pinout assignments table. Added the USB timing to Section 14. Added the Reduced MII to Section 15. Removed the Data Parity. Made some changes to the Features list.
0	02/2003	Initial revision.