Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	133MHz
Co-Processors/DSP	Communications; CPM, Security; SEC
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (3), 10/100Mbps (2)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 100°C (TA)
Security Features	Cryptography
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc885cvr133

1 Overview

The MPC885/MPC880 is a versatile single-chip integrated microprocessor and peripheral combination that can be used in a variety of controller applications and communications and networking systems. The MPC885/MPC880 provides enhanced ATM functionality, an additional fast Ethernet controller, a USB, and an encryption block.

Table 1 shows the functionality supported by MPC885/MPC880.

Table 1. MPC885 Family

Part	Cache (Kbytes)		Ethernet		SCC	SMC	USB	ATM Support	Security Engine
	I Cache	D Cache	10BaseT	10/100					
MPC885	8	8	Up to 3	2	3	2	1	Serial ATM and UTOPIA interface	Yes
MPC880	8	8	Up to 2	2	2	2	1	Serial ATM and UTOPIA interface	No

2 Features

The MPC885/MPC880 is comprised of three modules that each use the 32-bit internal bus: a MPC8xx core, a system integration unit (SIU), and a communications processor module (CPM).

The following list summarizes the key MPC885/MPC880 features:

- Embedded MPC8xx core up to 133 MHz
- Maximum frequency operation of the external bus is 80 MHz (in 1:1 mode)
  - The 133-MHz core frequency supports 2:1 mode only.
  - The 66-/80-MHz core frequencies support both the 1:1 and 2:1 modes.
- Single-issue, 32-bit core (compatible with the Power Architecture definition) with thirty-two 32-bit general-purpose registers (GPRs)
  - The core performs branch prediction with conditional prefetch and without conditional execution.
  - 8-Kbyte data cache and 8-Kbyte instruction cache (see Table 1)
    - Instruction cache is two-way, set-associative with 256 sets in 2 blocks
    - Data cache is two-way, set-associative with 256 sets
    - Cache coherency for both instruction and data caches is maintained on 128-bit (4-word) cache blocks.
    - Caches are physically addressed, implement a least recently used (LRU) replacement algorithm, and are lockable on a cache block basis.
  - MMUs with 32-entry TLB, fully associative instruction and data TLBs
  - MMUs support multiple page sizes of 4, 16, and 512 Kbytes, and 8 Mbytes; 16 virtual address spaces and 16 protection groups
  - Advanced on-chip emulation debug mode

- On-chip 16 × 16 multiply accumulate controller (MAC)
  - One operation per clock (two-clock latency, one-clock blockage)
  - MAC operates concurrently with other instructions
  - FIR loop—Four clocks per four multiplies
- Four baud rate generators
  - Independent (can be connected to any SCC or SMC)
  - Allow changes during operation
  - Autobaud support option
- Up to three serial communication controllers (SCCs) supporting the following protocols:
  - Serial ATM capability on SCCs
  - Optional UTOPIA port on SCC4
  - Ethernet/IEEE Std 802.3™ optional on the SCC(s) supporting full 10-Mbps operation
  - HDLC/SDLC
  - HDLC bus (implements an HDLC-based local area network (LAN))
  - Asynchronous HDLC to support point-to-point protocol (PPP)
  - AppleTalk
  - Universal asynchronous receiver transmitter (UART)
  - Synchronous UART
  - Serial infrared (IrDA)
  - Binary synchronous communication (BISYNC)
  - Totally transparent (bit streams)
  - Totally transparent (frame based with optional cyclic redundancy check (CRC))
- Up to two serial management channels (SMCs) supporting the following protocols:
  - UART (low-speed operation)
  - Transparent
  - General circuit interface (GCI) controller
  - Provide management for BRI devices as GCI controller in time-division multiplexed (TDM) channels
- Universal serial bus (USB)—Supports operation as a USB function endpoint, a USB host controller, or both for testing purposes (loop-back diagnostics)
  - USB 2.0 full-/low-speed compatible
  - The USB function mode has the following features:
    - Four independent endpoints support control, bulk, interrupt, and isochronous data transfers.
    - CRC16 generation and checking
    - CRC5 checking
    - NRZI encoding/decoding with bit stuffing
    - 12- or 1.5-Mbps data rate

The MPC880 block diagram is shown in Figure 2.

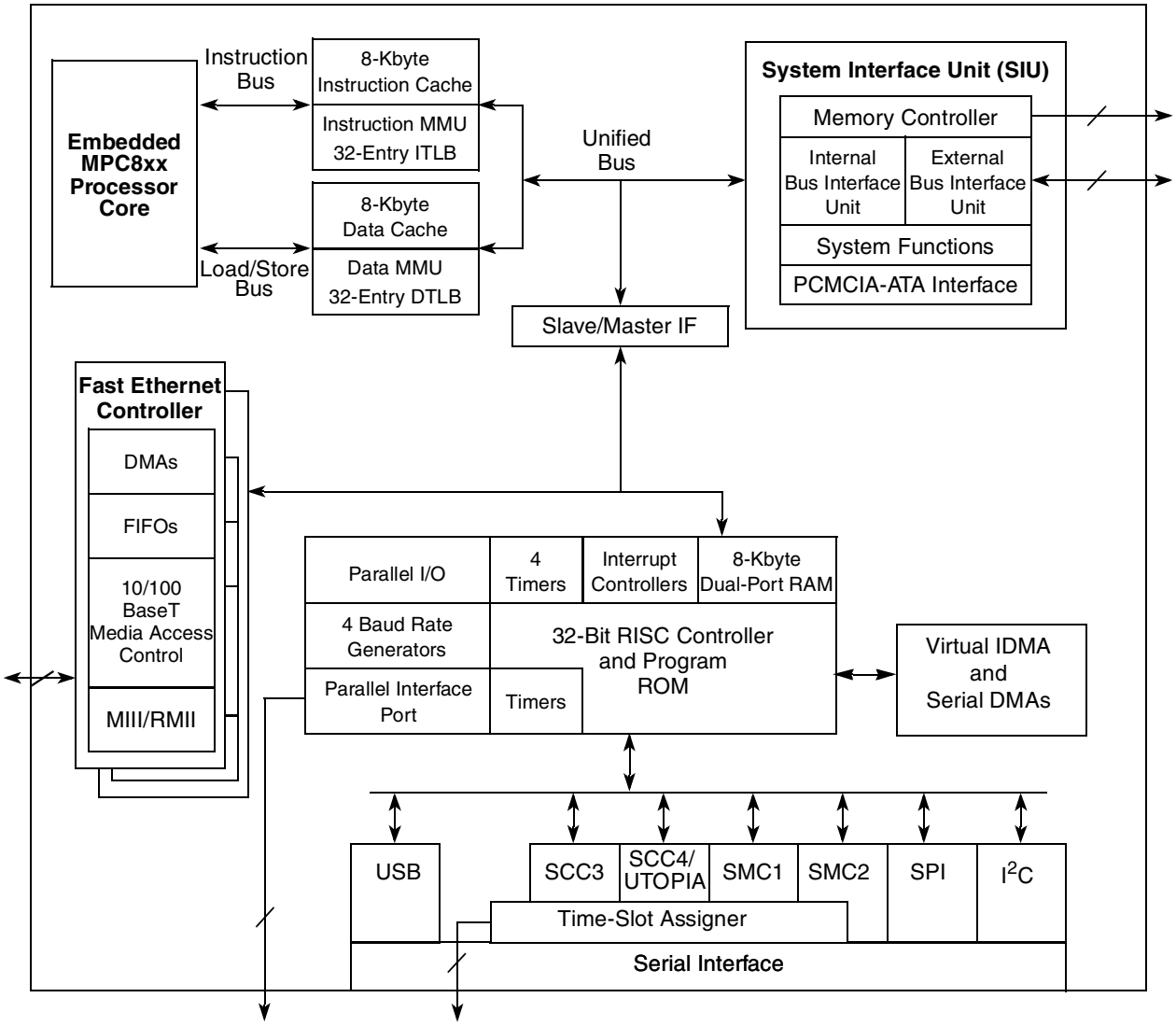

Figure 2. MPC880 Block Diagram

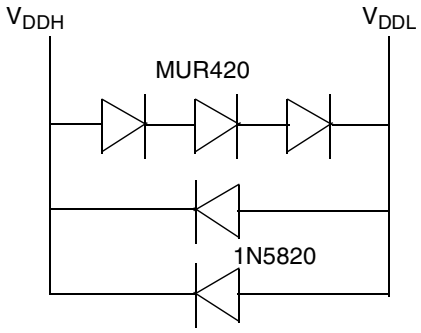

Figure 5. Example Voltage Sequencing Circuit

9 Layout Practices

Each V_{DD} pin on the MPC885/MPC880 should be provided with a low-impedance path to the board's supply. Each GND pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The V_{DD} power supply should be bypassed to ground using at least four 0.1 µF by-pass capacitors located as close as possible to the four sides of the package. Each board designed should be characterized and additional appropriate decoupling capacitors should be used if required. The capacitor leads and associated printed-circuit traces connecting to chip V_{DD} and GND should be kept to less than half an inch per capacitor lead. At a minimum, a four-layer board employing two inner layers as V_{DD} and GND planes should be used.

All output pins on the MPC885/MPC880 have fast rise and fall times. Printed-circuit (PC) trace interconnection length should be minimized in order to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{DD} and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins. For more information, please refer to the *MPC885 PowerQUICC™ Family Reference Manual*, Section 14.4.3, "Clock Synthesizer Power (V_{DDSYN}, V_{SSSYN}, V_{SSSYN1})."

10 Bus Signal Timing

The maximum bus speed supported by the MPC885/MPC880 is 80 MHz. Higher-speed parts must be operated in half-speed bus mode (for example, an MPC885/MPC880 used at 133 MHz must be configured for a 66 MHz bus). Table 7 shows the frequency ranges for standard part frequencies in 1:1 bus mode, and Table 8 shows the frequency ranges for standard part frequencies in 2:1 bus mode.

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B27a	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 1 (MIN = 1.50 × B1 – 2.00)	43.50	—	35.50	—	20.70	—	16.75	—	ns
B28	CLKOUT rising edge to $\overline{WE}$(0:3) negated GPCM write access CSNT = 0 (MAX = 0.00 × B1 + 9.00)	—	9.00	—	9.00	—	9.00	—	9.00	ns
B28a	CLKOUT falling edge to $\overline{WE}$(0:3) negated GPCM write access TRLX = 0, CSNT = 1, EBDF = 0 (MAX = 0.25 × B1 + 6.80)	7.60	14.30	6.30	13.00	3.80	10.50	3.13	9.93	ns
B28b	CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0, CSNT = 1 ACS = 10 or ACS = 11, EBDF = 0 (MAX = 0.25 × B1 + 6.80)	—	14.30	—	13.00	—	10.50	—	9.93	ns
B28c	CLKOUT falling edge to $\overline{WE}$(0:3) negated GPCM write access TRLX = 0, CSNT = 1 write access TRLX = 0, CSNT = 1, EBDF = 1 (MAX = 0.375 × B1 + 6.6)	10.90	18.00	10.90	18.00	5.20	12.30	4.69	11.29	ns
B28d	CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1 (MAX = 0.375 × B1 + 6.6)	—	18.00	—	18.00	—	12.30	—	11.30	ns
B29	$\overline{WE}$(0:3) negated to D(0:31) High-Z GPCM write access, CSNT = 0, EBDF = 0 (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	1.80	—	1.13	—	ns
B29a	$\overline{WE}$(0:3) negated to D(0:31) High-Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 0 (MIN = 0.50 × B1 – 2.00)	13.20	—	10.50	—	5.60	—	4.25	—	ns
B29b	$\overline{CS}$ negated to D(0:31) High-Z GPCM write access, ACS = 00, TRLX = 0 & CSNT = 0 (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	1.80	—	1.13	—	ns
B29c	$\overline{CS}$ negated to D(0:31) High-Z GPCM write access, TRLX = 0, CSNT = 1, ACS = 10, or ACS = 11 EBDF = 0 (MIN = 0.50 × B1 – 2.00)	13.20	—	10.50	—	5.60	—	4.25	—	ns
B29d	$\overline{WE}$(0:3) negated to D(0:31) High-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 0 (MIN = 1.50 × B1 – 2.00)	43.50	—	35.50	—	20.70	—	16.75	—	ns
B29e	$\overline{CS}$ negated to D(0:31) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11 EBDF = 0 (MIN = 1.50 × B1 – 2.00)	43.50	—	35.50	—	20.70	—	16.75	—	ns
B29f	$\overline{WE}$(0:3) negated to D(0:31) High-Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 1 (MIN = 0.375 × B1 – 6.30)[7]	5.00	—	3.00	—	0.00	—	0.00	—	ns
B29g	$\overline{CS}$ negated to D(0:31) High-Z GPCM write access, TRLX = 0, CSNT = 1 ACS = 10 or ACS = 11, EBDF = 1 (MIN = 0.375 × B1 – 6.30)[7]	5.00	—	3.00	—	0.00	—	0.00	—	ns

Figure 20 provides the timing for the external bus controlled by the UPM.

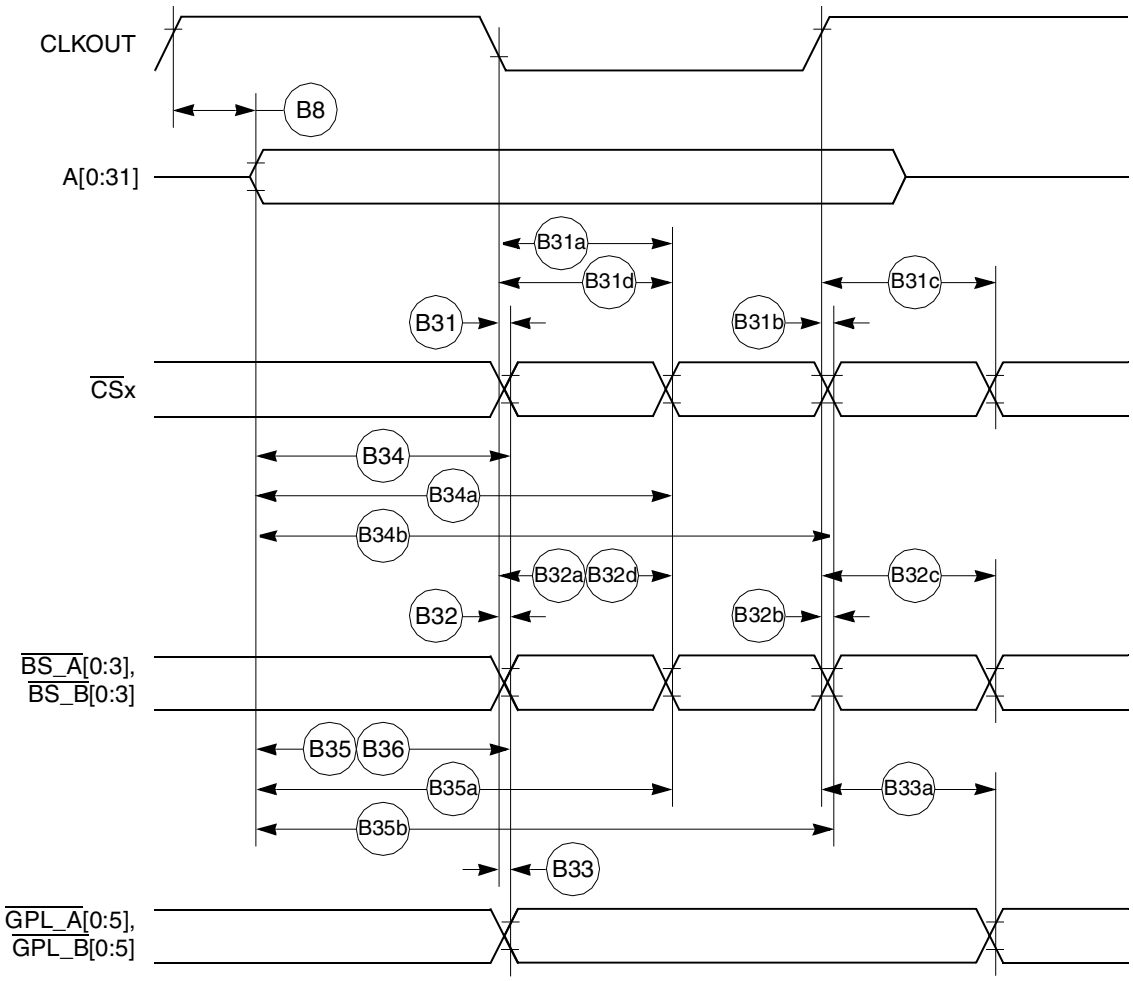

Figure 20. External Bus Timing (UPM-Controlled Signals)

Figure 21 provides the timing for the asynchronous asserted UPWAIT signal controlled by the UPM.

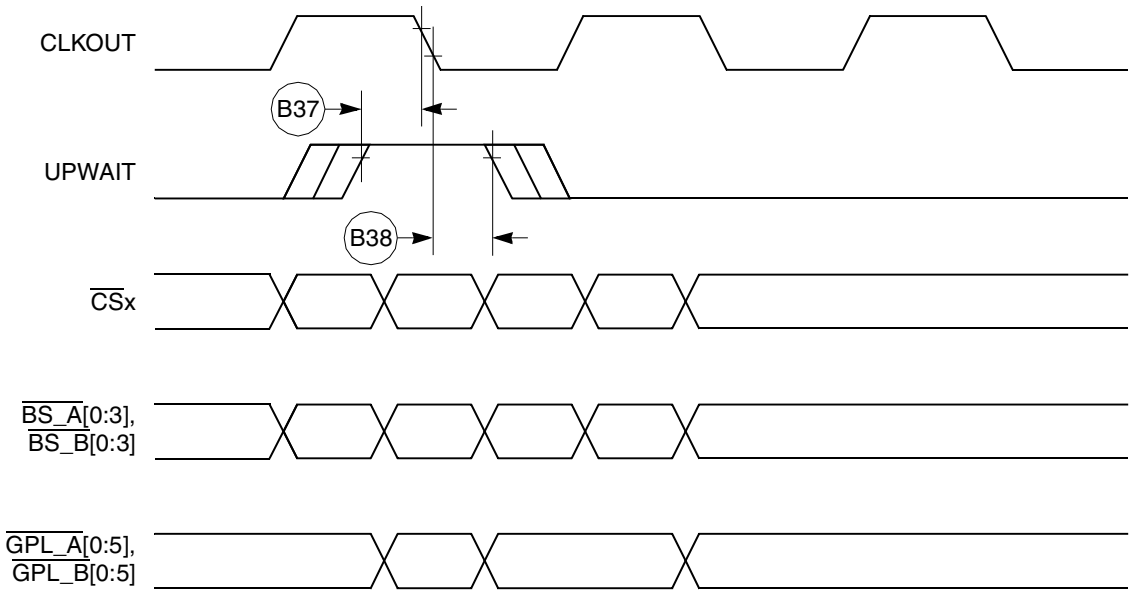

Figure 21. Asynchronous UPWAIT Asserted Detection in UPM-Handled Cycles Timing

Figure 22 provides the timing for the asynchronous negated UPWAIT signal controlled by the UPM.

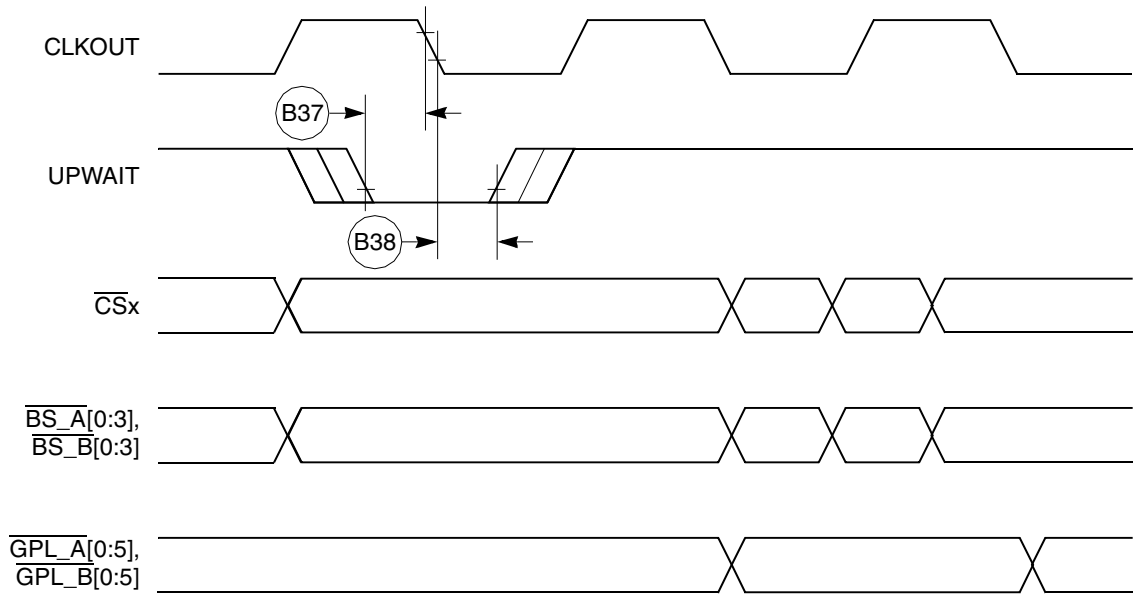

Figure 22. Asynchronous UPWAIT Negated Detection in UPM-Handled Cycles Timing

Figure 35 shows the reset timing for the data bus configuration.

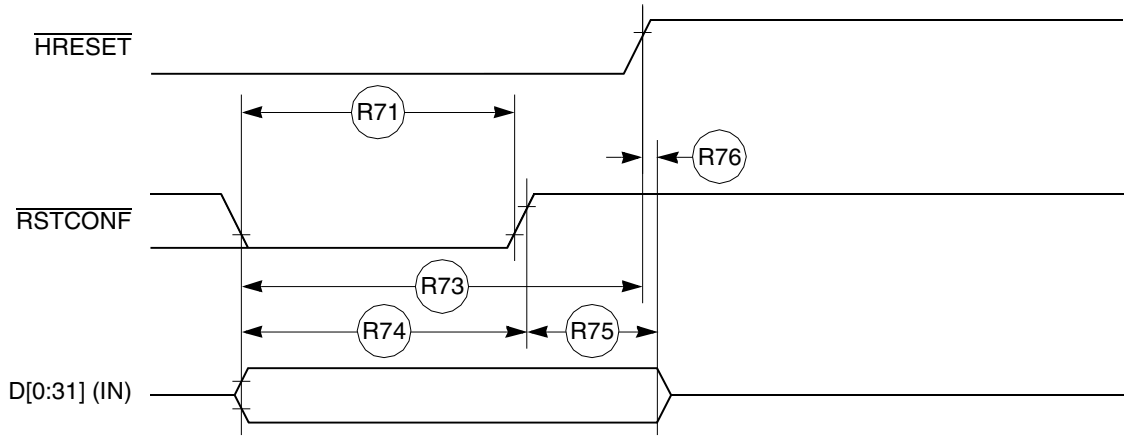

Figure 35. Reset Timing—Configuration from Data Bus

Figure 36 provides the reset timing for the data bus weak drive during configuration.

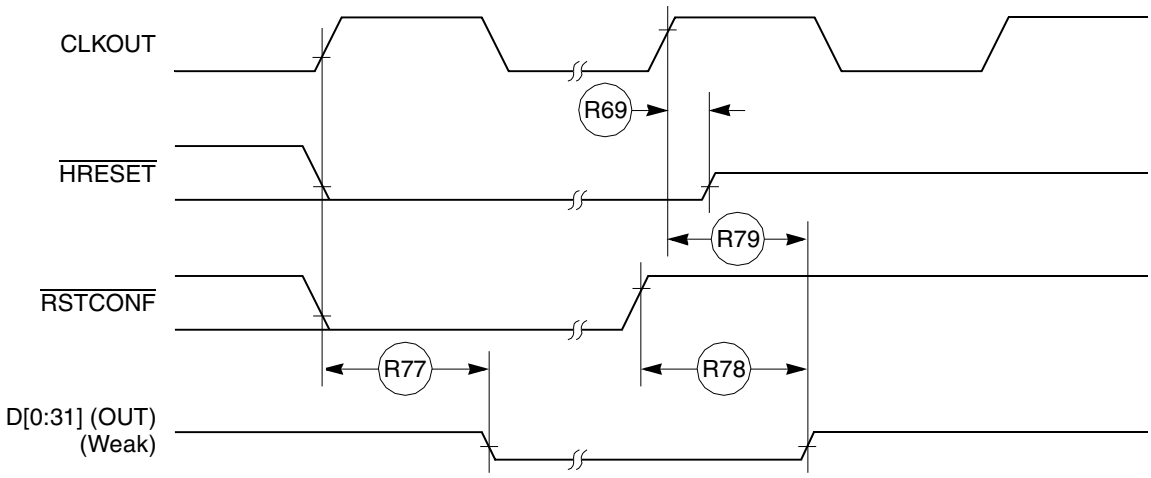

Figure 36. Reset Timing—Data Bus Weak Drive During Configuration

Figure 37 provides the reset timing for the debug port configuration.

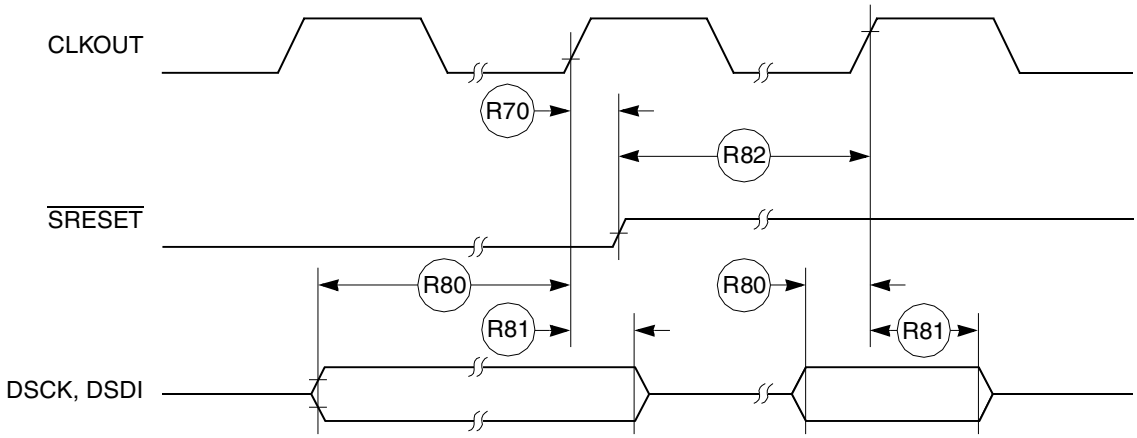

Figure 37. Reset Timing—Debug Port Configuration

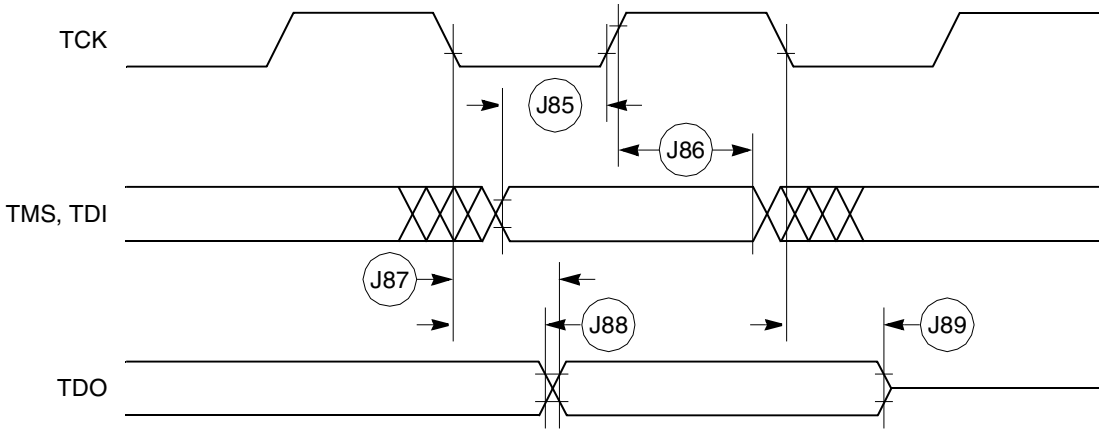

Figure 39. JTAG Test Access Port Timing Diagram

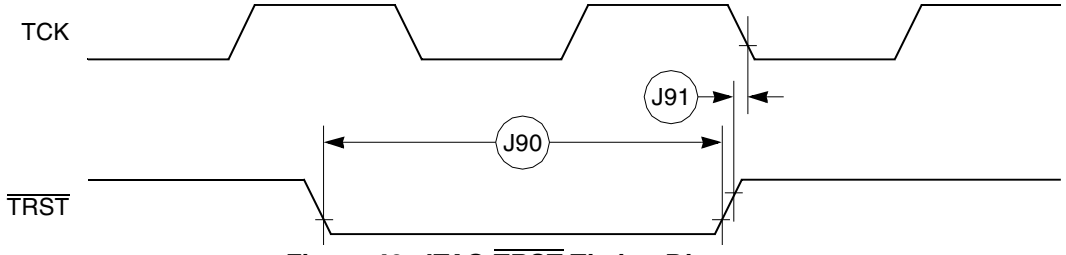

Figure 40. JTAG $\overline{\text{TRST}}$ Timing Diagram

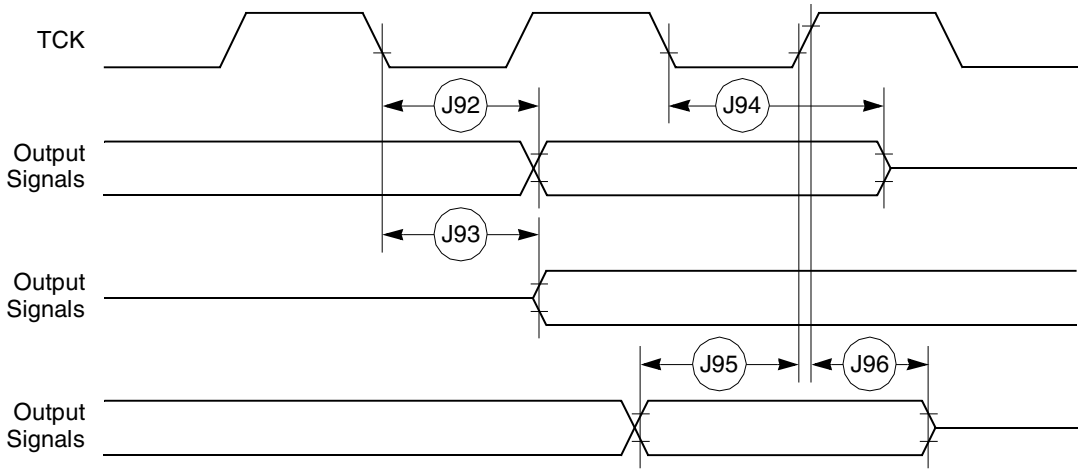

Figure 41. Boundary Scan (JTAG) Timing Diagram

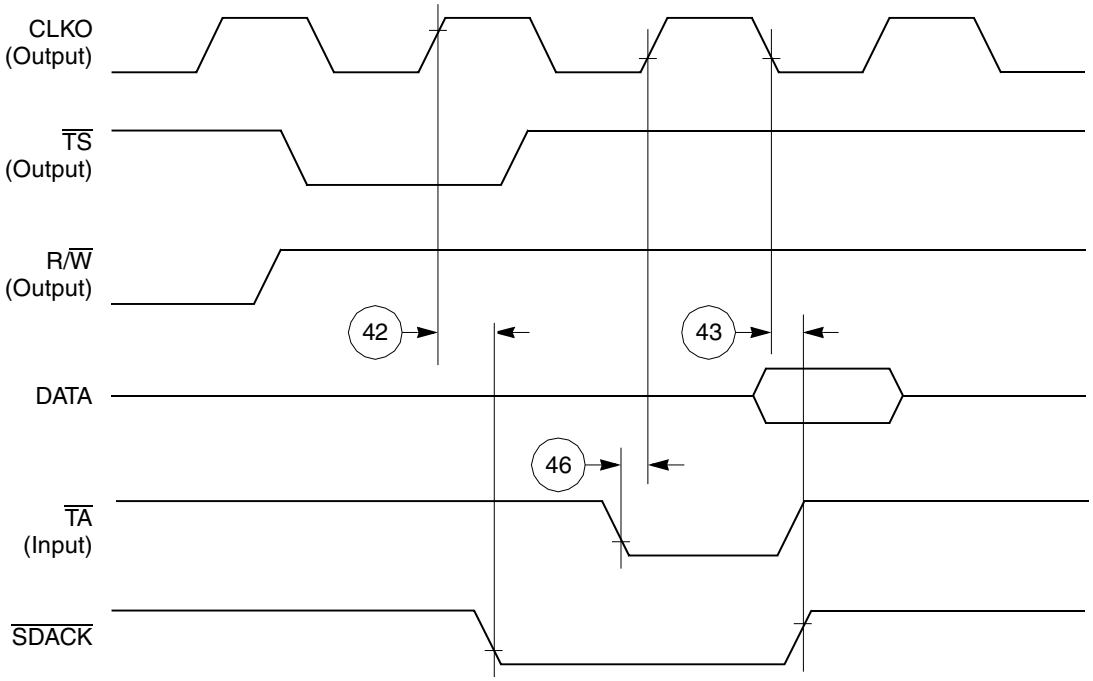

Figure 49. SDACK Timing Diagram—Peripheral Write, Externally-Generated TA

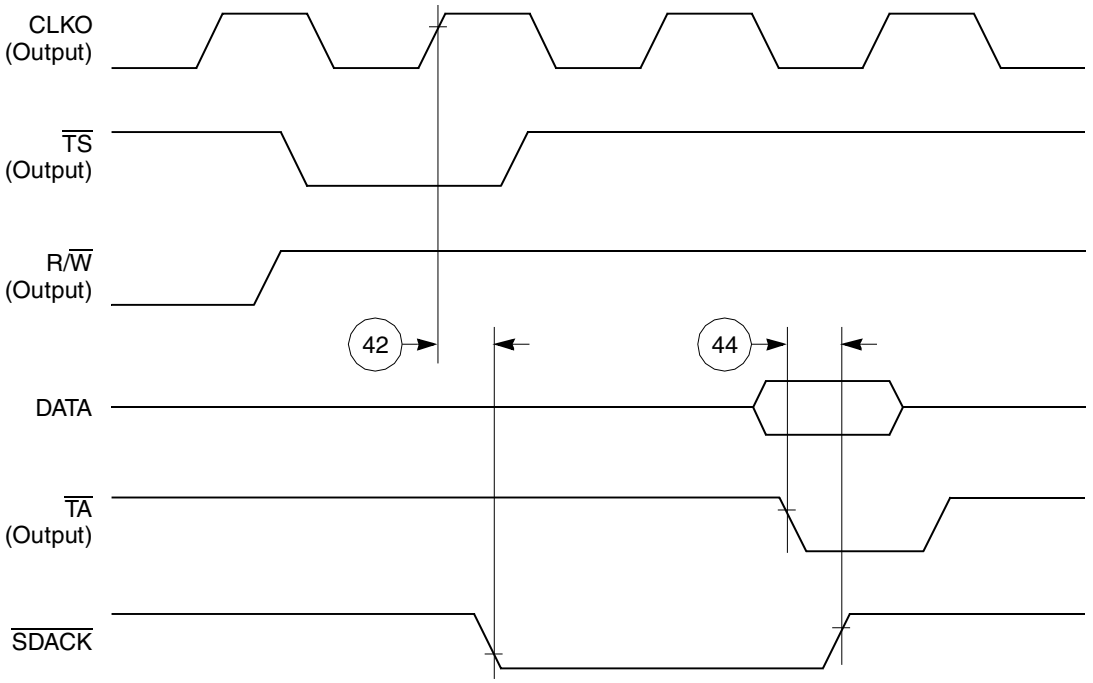

Figure 50. SDACK Timing Diagram—Peripheral Write, Internally-Generated TA

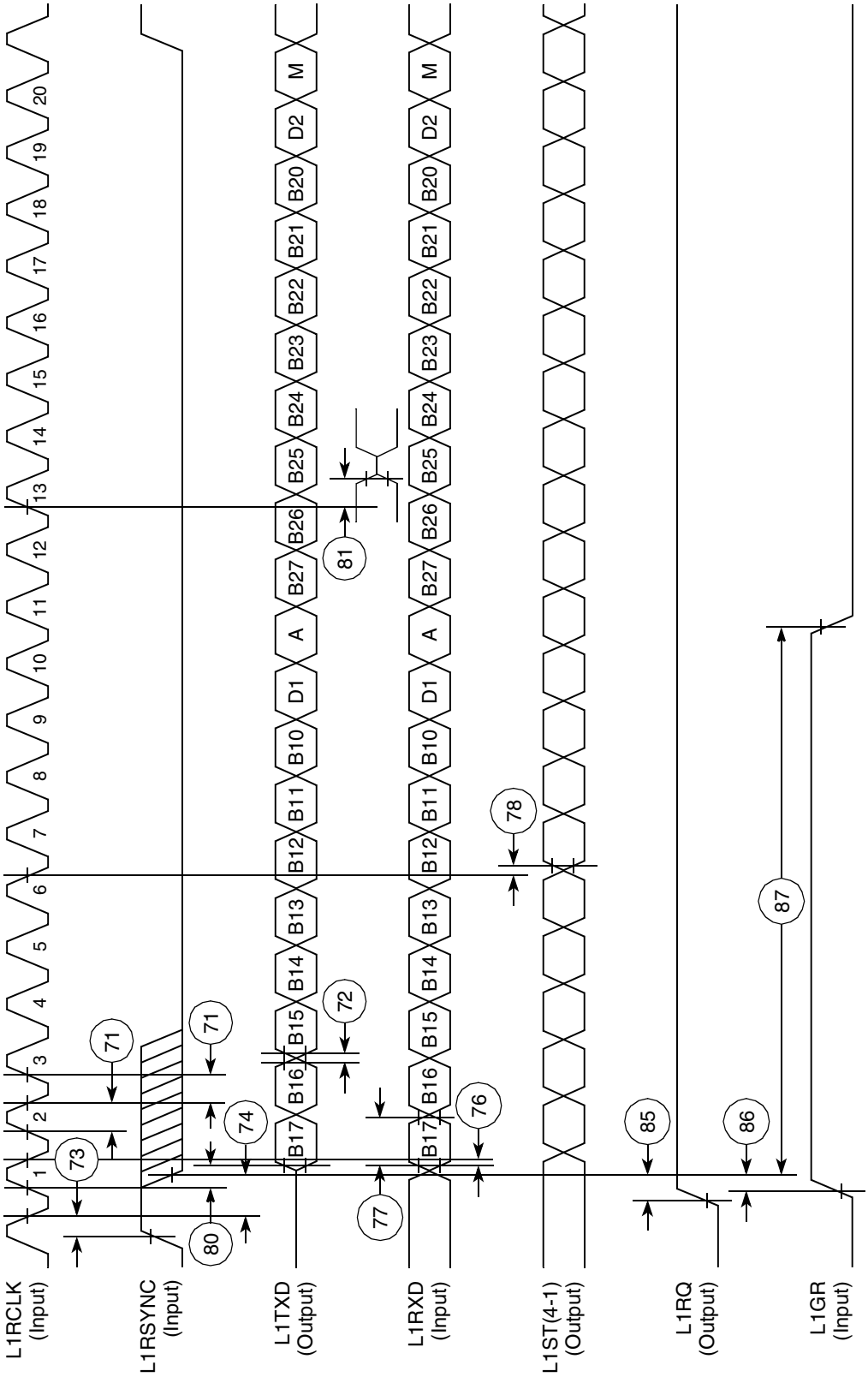

Figure 58. IDL Timing

12.7 SCC in NMSI Mode Electrical Specifications

Table 22 provides the NMSI external clock timing.

Table 22. NMSI External Clock Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
100	RCLK1 and TCLK1 width high[1]	1/SYNCCLK	—	ns
101	RCLK1 and TCLK1 width low	1/SYNCCLK + 5	—	ns
102	RCLK1 and TCLK1 rise/fall time	—	15.00	ns
103	TXD1 active delay (from TCLK1 falling edge)	0.00	50.00	ns
104	$\overline{\text{RTS1}}$ active/inactive delay (from TCLK1 falling edge)	0.00	50.00	ns
105	$\overline{\text{CTS1}}$ setup time to TCLK1 rising edge	5.00	—	ns
106	RXD1 setup time to RCLK1 rising edge	5.00	—	ns
107	RXD1 hold time from RCLK1 rising edge[2]	5.00	—	ns
108	$\overline{\text{CD1}}$ setup time to RCLK1 rising edge	5.00	—	ns

1 The ratios SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater than or equal to 2.25/1.
2 Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as external sync signals.

Table 23 provides the NMSI internal clock timing.

Table 23. NMSI Internal Clock Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
100	RCLK1 and TCLK1 frequency[1]	0.00	SYNCCLK/3	MHz
102	RCLK1 and TCLK1 rise/fall time	—	—	ns
103	TXD1 active delay (from TCLK1 falling edge)	0.00	30.00	ns
104	$\overline{\text{RTS1}}$ active/inactive delay (from TCLK1 falling edge)	0.00	30.00	ns
105	$\overline{\text{CTS1}}$ setup time to TCLK1 rising edge	40.00	—	ns
106	RXD1 setup time to RCLK1 rising edge	40.00	—	ns
107	RXD1 hold time from RCLK1 rising edge[2]	0.00	—	ns
108	$\overline{\text{CD1}}$ setup time to RCLK1 rising edge	40.00	—	ns

1 The ratios SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater than or equal to 3/1.
2 Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as external sync signals

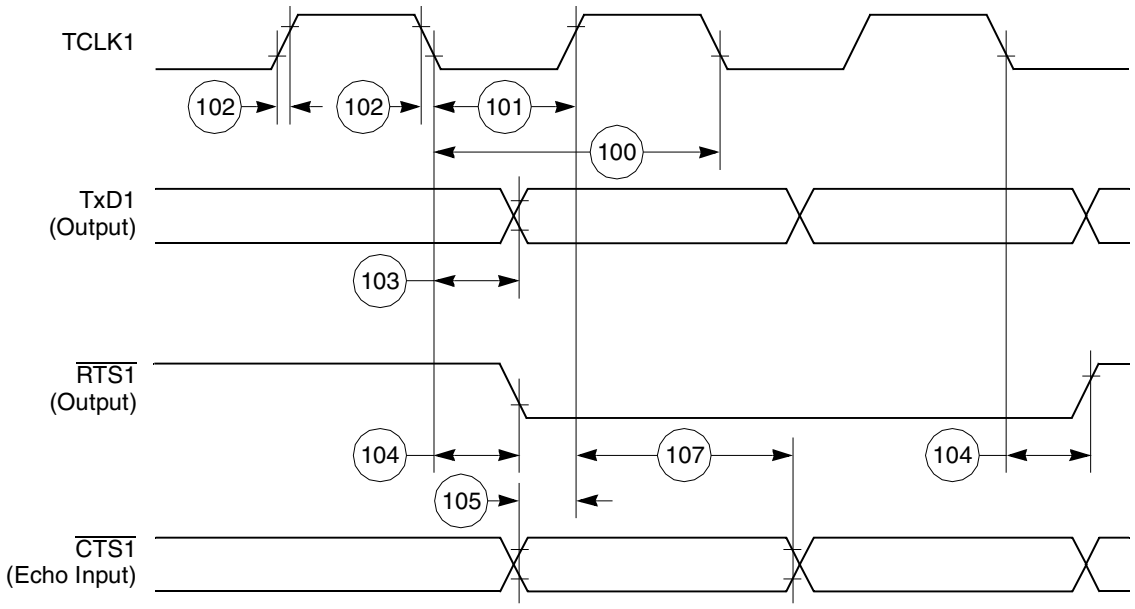

Figure 61. HDLC Bus Timing Diagram

12.8 Ethernet Electrical Specifications

Table 24 provides the Ethernet timings as shown in Figure 62 through Figure 64.

Table 24. Ethernet Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
120	CLSN width high	40	—	ns
121	RCLK1 rise/fall time	—	15	ns
122	RCLK1 width low	40	—	ns
123	RCLK1 clock period[1]	80	120	ns
124	RXD1 setup time	20	—	ns
125	RXD1 hold time	5	—	ns
126	RENA active delay (from RCLK1 rising edge of the last data bit)	10	—	ns
127	RENA width low	100	—	ns
128	TCLK1 rise/fall time	—	15	ns
129	TCLK1 width low	40	—	ns
130	TCLK1 clock period[1]	99	101	ns
131	TXD1 active delay (from TCLK1 rising edge)	—	50	ns
132	TXD1 inactive delay (from TCLK1 rising edge)	6.5	50	ns
133	TENA active delay (from TCLK1 rising edge)	10	50	ns

Table 24. Ethernet Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
134	TENA inactive delay (from TCLK1 rising edge)	10	50	ns
138	CLKO1 low to $\overline{\text{SDACK}}$ asserted[2]	—	20	ns
139	CLKO1 low to $\overline{\text{SDACK}}$ negated [2]	—	20	ns

[1] The ratios SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater than or equal to 2/1.
[2] $\overline{\text{SDACK}}$ is asserted whenever the SDMA writes the incoming frame DA into memory.

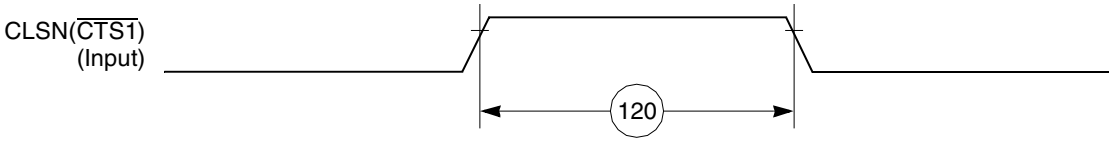

Figure 62. Ethernet Collision Timing Diagram

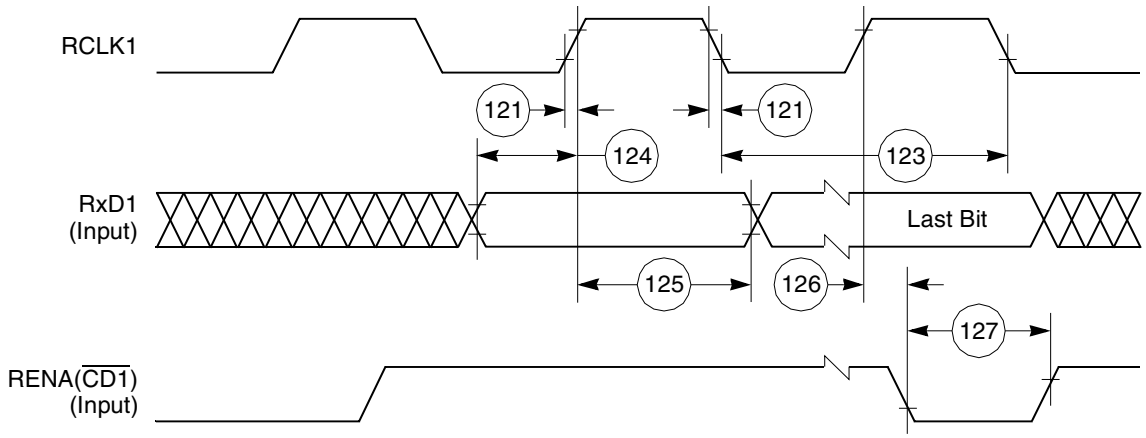

Figure 63. Ethernet Receive Timing Diagram

14 USB Electrical Characteristics

This section provides the AC timings for the USB interface.

14.1 USB Interface AC Timing Specifications

The USB Port uses the transmit clock on SCC1. Table 33 lists the USB interface timings.

Table 33. USB Interface AC Timing Specifications

Name	Characteristic	All Frequencies		Unit
		Min	Max	
US1	USBCLK frequency of operation[1] Low speed Full speed	 6 48		 MHz MHz
US4	USBCLK duty cycle (measured at 1.5 V)	45	55	%

[1] USBCLK accuracy should be ±500 ppm or better. USBCLK may be stopped to conserve power.

15 FEC Electrical Characteristics

This section provides the AC electrical specifications for the fast Ethernet controller (FEC). Note that the timing specifications for the MII signals are independent of system clock frequency (part speed designation). Also, MII signals use TTL signal levels compatible with devices operating at either 5.0 or 3.3 V.

15.1 MII and Reduced MII Receive Signal Timing

The receiver functions correctly up to a MII_RX_CLK maximum frequency of 25 MHz + 1%. The reduced MII (RMII) receiver functions correctly up to a RMII_REFCLK maximum frequency of 50 MHz + 1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_RX_CLK frequency – 1%.

Table 34 provides information on the MII and RMII receive signal timing.

Table 34. MII Receive Signal Timing

Num	Characteristic	Min	Max	Unit
M1	MII_RXD[3:0], MII_RX_DV, MII_RX_ERR to MII_RX_CLK setup	5	—	ns
M2	MII_RX_CLK to MII_RXD[3:0], MII_RX_DV, MII_RX_ER hold	5	—	ns
M3	MII_RX_CLK pulse width high	35%	65%	MII_RX_CLK period
M4	MII_RX_CLK pulse width low	35%	65%	MII_RX_CLK period
M1_RMII	RMII_RXD[1:0], RMII_CRS_DV, RMII_RX_ERR to RMII_REFCLK setup	4	—	ns
M2_RMII	RMII_REFCLK to RMII_RXD[1:0], RMII_CRS_DV, RMII_RX_ERR hold	2	—	ns

16 Mechanical Data and Ordering Information

Table 38 identifies the available packages and operating frequencies for the MPC885/MPC880 derivative devices.

Table 38. Available MPC885/MPC880 Packages/Frequencies

Package Type	Temperature (Tj)	Frequency (MHz)	Order Number
Plastic ball grid array ZP suffix — Leaded VR suffix — Lead-Free are available as needed	0°C to 95°C	66	KMPC885ZP66 KMPC880ZP66 MPC885ZP66 MPC880ZP66
		80	KMPC885ZP80 KMPC880ZP80 MPC885ZP80 MPC880ZP80
		133	KMPC885ZP133 KMPC880ZP133 MPC885ZP133 MPC880ZP133
Plastic ball grid array CZP suffix — Leaded CVR suffix — Lead-Free are available as needed	-40°C to 100°C	66	KMPC885CZP66 KMPC880CZP66 MPC885CZP66 MPC880CZP66
		133	KMPC885CZP133 KMPC880CZP133 MPC885CZP133 MPC880CZP133

Table 39. Pin Assignments (continued)

Name	Pin Number	Type
WE0, BS_B0, IORD	B18	Output
WE1, BS_B1, IOWR	E16	Output
WE2, BS_B2, PCOE	C17	Output
WE3, BS_B3, PCWE	B19	Output
BS_A[0:3]	D17, C18, C19, F16	Output
GPL_A0, GPL_B0	B17	Output
OE, GPL_A1, GPL_B1	A18	Output
GPL_A[2:3], GPL_B[2:3], CS[2:3]	D16, A17	Output
UPWAITA, GPL_A4	B13	Bidirectional
UPWAITB, GPL_B4	A14	Bidirectional
GPL_A5	C13	Output
PORESET	B3	Input
RSTCONF	D4	Input
HRESET	B4	Open-drain
SRESET	A3	Open-drain
XTAL	A4	Analog output
EXTAL	D5	Analog input (3.3 V only)
CLKOUT	G4	Output
EXTCLK	A5	Input (3.3 V only)
TEXP	C4	Output
ALE_A	B7	Output
CE1_A	B15	Output
CE2_A	C15	Output
WAIT_A, SOC_Split[1]	A2	Input
WAIT_B	C3	Input
IP_A0, UTPB_Split0[1]	B1	Input
IP_A1, UTPB_Split1[1]	C1	Input
IP_A2, IOIS16_A, UTPB_Split2[1]	F4	Input
IP_A3, UTPB_Split3[1]	E3	Input
IP_A4, UTPB_Split4[1]	D2	Input
IP_A5, UTPB_Split5[1]	D1	Input
IP_A6, UTPB_Split6[1]	E2	Input
IP_A7, UTPB_Split7[1]	D3	Input

Table 39. Pin Assignments (continued)

Name	Pin Number	Type
PD5, CLK8, L1TCLKB, UTPB6	V6	Bidirectional
PD4, CLK4, UTPB7	W4	Bidirectional
PD3, CLK7, TIN4, SOC	T9	Bidirectional
PE31, CLK8, L1TCLKB, MII1-RXCLK	U9	Bidirectional (Optional: open-drain)
PE30, L1RXDB, MII1-RXD2	W7	Bidirectional (Optional: open-drain)
PE29, MII2-CRS	T8	Bidirectional (Optional: open-drain)
PE28, $\overline{\text{TOUT3}}$, MII2-COL	V5	Bidirectional (Optional: open-drain)
PE27, $\overline{\text{RTS3}}$, L1RQB, MII2-RXER, RMII2-RXER	V4	Bidirectional (Optional: open-drain)
PE26, L1CLKOB, MII2-RXDV, RMII2-CRS_DV	T1	Bidirectional (Optional: open-drain)
PE25, RXD4, MII2-RXD3, L1ST2	T3	Bidirectional (Optional: open-drain)
PE24, SMRXD1, BRGO1, MII2-RXD2	V8	Bidirectional (Optional: open-drain)
PE23, $\overline{\text{SMSYN2}}$, TXD4, MII2-RXCLK, L1ST1	V2	Bidirectional (Optional: open-drain)
PE22, $\overline{\text{TOUT2}}$, MII2-RXD1, RMII2-RXD1, $\overline{\text{SDACK1}}$	V1	Bidirectional (Optional: open-drain)
PE21, SMRXD2, $\overline{\text{TOUT1}}$, MII2-RXD0, RMII2-RXD0, $\overline{\text{RTS3}}$	V9	Bidirectional (Optional: open-drain)
PE20, L1RSYNCA, SMTXD2, $\overline{\text{CTS3}}$, MII2-TXER	R4	Bidirectional (Optional: open-drain)
PE19, L1TXDB, MII2-TXEN, RMII2-TXEN	T6	Bidirectional (Optional: open-drain)
PE18, L1TSYNCA, SMTXD1, MII2-TXD3	R1	Bidirectional (Optional: open-drain)
PE17, TIN3, CLK5, BRGO3, $\overline{\text{SMSYN1}}$, MII2-TXD2	W8	Bidirectional (Optional: open-drain)
PE16, L1RCLKB, CLK6, TXD3, MII2-TXCLK, RMII2-REFCLK	T7	Bidirectional (Optional: open-drain)
PE15, $\overline{\text{TGATE1}}$, MII2-TXD1, RMII2-TXD1	W6	Bidirectional

17 Document Revision History

Table 40 lists significant changes between revisions of this hardware specification.

Table 40. Document Revision History

Revision Number	Date	Changes
7	07/2010	In Table 9, "Bus Operation Timings," changed the following: • Updated TRLX condition value for B22a/b/c to "TRLX = [0 or 1]" • Removed TRLX condition for B23 • Updated condition and equation for B30 to "Invalid GPCM read/write access (MIN = 0.25 × B1 – 2.00)" • Updated note 8 to "The timing B30 refers to $\overline{CS}$ when ACS = 00 and to $\overline{CS}$ and $\overline{WE}$(0:3) when CSNT = 0."
6	05/2010	Added minimum load for CLKOUT in Section 10, "Bus Signal Timing."
5	03/2009	Updated formatting of Table 12 , "PCMCIA Port Timing," Table 13, "Debug Port Timing," Table 14, "Reset Timing," and Table 15, "JTAG Timing."
4	08/2007	• On page 1, updated first paragraph and added a second paragraph. • After Table 2, inserted a new figure showing the undershoot/overshoot voltage (Figure 3) and renumbered the rest of the figures. • In Table 9, for reset timings B29f and B29g added footnote indicating that the formula only applies to bus operation up to 50 MHz. • In Figure 6, changed all reference voltage measurement points from 0.2 and 0.8 V to 50% level. • In Table 18, changed num 46 description to read, "$\overline{TA}$ assertion to rising edge ..." • In Figure 49, changed $\overline{TA}$ to reflect the rising edge of the clock.
3.0	7/22/2004	• Added sentence to Spec B1A about EXTCLK and CLKOUT being in Alignment for Integer Values • Added a footnote to Spec 41 specifying that EDM = 1 • Added RMII1_EN under M1II_EN in Table 36 Pin Assignments • Added a tablefootnote to Table 6 DC Electrical Specifications about meeting the VIL Max of the I2C Standard • Put the new part numbers in the Ordering Information Section
2.0	12/2003	• Changed the maximum operating frequency to 133 MHz. • Put in the orderable part numbers that are orderable. • Put the timing in the 80 MHz column. • Rounded the timings to hundredths in the 80 MHz column. • Put the pin numbers in footnotes by the maximum currents in Table 6. • Changed 22 and 41 in the Timing. • Put in the Thermal numbers.
1.0	9/2003	• Added the DSP information in the Features list • Fixed table formatting. • Nontechnical edits. • Released to the external web.
0.9	8/2003	Changed the USB description to full-/low-speed compatible.
0.8	8/2003	Added the Reference to USB 2.0 to the Features list and removed 1.1 from USB on the block diagrams.
0.7	7/2003	Added the RxClav and TxClav signals to PC15.
0.6	6/2003	Changed the pin descriptions per the June 22 spec.
0.5	5/2003	Changed some more typos, put in the phsel and phreq pins. Corrected the USB timing.

How to Reach Us:

Home Page:
www.freescale.com

Web Support:
http://www.freescale.com/support

USA/Europe or Locations Not Listed:
Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
1-800-521-6274 or
+1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo 153-0064
Japan
0120 191014 or
+81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor
Literature Distribution Center
1-800 441-2447 or
+1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor
@hibbertgroup.com

Document Number: MPC885EC
Rev. 7
07/2010