



Welcome to [E-XFL.COM](#)

Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	66MHz
Co-Processors/DSP	Communications; CPM, Security; SEC
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (3), 10/100Mbps (2)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 100°C (TA)
Security Features	Cryptography
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc885cvr66

1 Overview

The MPC885/MPC880 is a versatile single-chip integrated microprocessor and peripheral combination that can be used in a variety of controller applications and communications and networking systems. The MPC885/MPC880 provides enhanced ATM functionality, an additional fast Ethernet controller, a USB, and an encryption block.

[Table 1](#) shows the functionality supported by MPC885/MPC880.

Table 1. MPC885 Family

Part	Cache (Kbytes)		Ethernet		SCC	SMC	USB	ATM Support	Security Engine
	I Cache	D Cache	10BaseT	10/100					
MPC885	8	8	Up to 3	2	3	2	1	Serial ATM and UTOPIA interface	Yes
MPC880	8	8	Up to 2	2	2	2	1	Serial ATM and UTOPIA interface	No

2 Features

The MPC885/MPC880 is comprised of three modules that each use the 32-bit internal bus: a MPC8xx core, a system integration unit (SIU), and a communications processor module (CPM).

The following list summarizes the key MPC885/MPC880 features:

- Embedded MPC8xx core up to 133 MHz
- Maximum frequency operation of the external bus is 80 MHz (in 1:1 mode)
 - The 133-MHz core frequency supports 2:1 mode only.
 - The 66-/80-MHz core frequencies support both the 1:1 and 2:1 modes.
- Single-issue, 32-bit core (compatible with the Power Architecture definition) with thirty-two 32-bit general-purpose registers (GPRs)
 - The core performs branch prediction with conditional prefetch and without conditional execution.
 - 8-Kbyte data cache and 8-Kbyte instruction cache (see [Table 1](#))
 - Instruction cache is two-way, set-associative with 256 sets in 2 blocks
 - Data cache is two-way, set-associative with 256 sets
 - Cache coherency for both instruction and data caches is maintained on 128-bit (4-word) cache blocks.
 - Caches are physically addressed, implement a least recently used (LRU) replacement algorithm, and are lockable on a cache block basis.
 - MMUs with 32-entry TLB, fully associative instruction and data TLBs
 - MMUs support multiple page sizes of 4, 16, and 512 Kbytes, and 8 Mbytes; 16 virtual address spaces and 16 protection groups
 - Advanced on-chip emulation debug mode

- Periodic interrupt timer (PIT)
- Clock synthesizer
- Decrementer and time base
- Reset controller
- IEEE Std 1149.1™ test access port (JTAG)
- Security engine is optimized to handle all the algorithms associated with IPsec, SSL/TLS, SRTP, IEEE Std 802.11i™, and iSCSI processing. Available on the MPC885, the security engine contains a crypto-channel, a controller, and a set of crypto hardware accelerators (CHAs). The CHAs are:
 - Data encryption standard execution unit (DEU)
 - DES, 3DES
 - Two key (K1, K2, K1) or three key (K1, K2, K3)
 - ECB and CBC modes for both DES and 3DES
 - Advanced encryption standard unit (AESU)
 - Implements the Rijndael symmetric key cipher
 - ECB, CBC, and counter modes
 - 128-, 192-, and 256- bit key lengths
 - Message digest execution unit (MDEU)
 - SHA with 160- or 256-bit message digest
 - MD5 with 128-bit message digest
 - HMAC with either algorithm
 - Crypto-channel supporting multi-command descriptor chains
 - Integrated controller managing internal resources and bus mastering
 - Buffer size of 256 bytes for the DEU, AESU, and MDEU, with flow control for large data sizes
- Interrupts
 - Six external interrupt request (IRQ) lines
 - 12 port pins with interrupt capability
 - 23 internal interrupt sources
 - Programmable priority between SCCs
 - Programmable highest priority request
- Communications processor module (CPM)
 - RISC controller
 - Communication-specific commands (for example, GRACEFUL STOP TRANSMIT, ENTER HUNT MODE, and RESTART TRANSMIT)
 - Supports continuous mode transmission and reception on all serial channels
 - 8-Kbytes of dual-port RAM
 - Several serial DMA (SDMA) channels to support the CPM
 - Three parallel I/O registers with open-drain capability

- On-chip 16 × 16 multiply accumulate controller (MAC)
 - One operation per clock (two-clock latency, one-clock blockage)
 - MAC operates concurrently with other instructions
 - FIR loop—Four clocks per four multiplies
- Four baud rate generators
 - Independent (can be connected to any SCC or SMC)
 - Allow changes during operation
 - Autobaud support option
- Up to three serial communication controllers (SCCs) supporting the following protocols:
 - Serial ATM capability on SCCs
 - Optional UTOPIA port on SCC4
 - Ethernet/IEEE Std 802.3™ optional on the SCC(s) supporting full 10-Mbps operation
 - HDLC/SDLC
 - HDLC bus (implements an HDLC-based local area network (LAN))
 - Asynchronous HDLC to support point-to-point protocol (PPP)
 - AppleTalk
 - Universal asynchronous receiver transmitter (UART)
 - Synchronous UART
 - Serial infrared (IrDA)
 - Binary synchronous communication (BISYNC)
 - Totally transparent (bit streams)
 - Totally transparent (frame based with optional cyclic redundancy check (CRC))
- Up to two serial management channels (SMCs) supporting the following protocols:
 - UART (low-speed operation)
 - Transparent
 - General circuit interface (GCI) controller
 - Provide management for BRI devices as GCI controller in time-division multiplexed (TDM) channels
- Universal serial bus (USB)—Supports operation as a USB function endpoint, a USB host controller, or both for testing purposes (loop-back diagnostics)
 - USB 2.0 full-/low-speed compatible
 - The USB function mode has the following features:
 - Four independent endpoints support control, bulk, interrupt, and isochronous data transfers.
 - CRC16 generation and checking
 - CRC5 checking
 - NRZI encoding/decoding with bit stuffing
 - 12- or 1.5-Mbps data rate

- Flexible data buffers with multiple buffers per frame
 - Automatic retransmission upon transmit error
- The USB host controller has the following features:
 - Supports control, bulk, interrupt, and isochronous data transfers
 - CRC16 generation and checking
 - NRZI encoding/decoding with bit stuffing
 - Supports both 12- and 1.5-Mbps data rates (automatic generation of preamble token and data rate configuration). Note that low-speed operation requires an external hub.
 - Flexible data buffers with multiple buffers per frame
 - Supports local loop back mode for diagnostics (12 Mbps only)
- Serial peripheral interface (SPI)
 - Supports master and slave modes
 - Supports multiple-master operation on the same bus
- Inter-integrated circuit (I²C) port
 - Supports master and slave modes
 - Supports a multiple-master environment
- Time-slot assigner (TSA)
 - Allows SCCs and SMCs to run in multiplexed and/or non-multiplexed operation
 - Supports T1, CEPT, PCM highway, ISDN basic rate, ISDN primary rate, user defined
 - 1- or 8-bit resolution
 - Allows independent transmit and receive routing, frame synchronization, and clocking
 - Allows dynamic changes
 - Can be internally connected to four serial channels (two SCCs and two SMCs)
- Parallel interface port (PIP)
 - Centronics interface support
 - Supports fast connection between compatible ports on MPC885/MPC880 and other MPC8xx devices
- PCMCIA interface
 - Master (socket) interface, release 2.1-compliant
 - Supports two independent PCMCIA sockets
 - 8 memory or I/O windows supported
- Debug interface
 - Eight comparators: four operate on instruction address, two operate on data address, and two operate on data
 - Supports conditions: = ≠ < >
 - Each watchpoint can generate a break point internally.
- Normal high and normal low power modes to conserve power

The MPC880 block diagram is shown in [Figure 2](#).

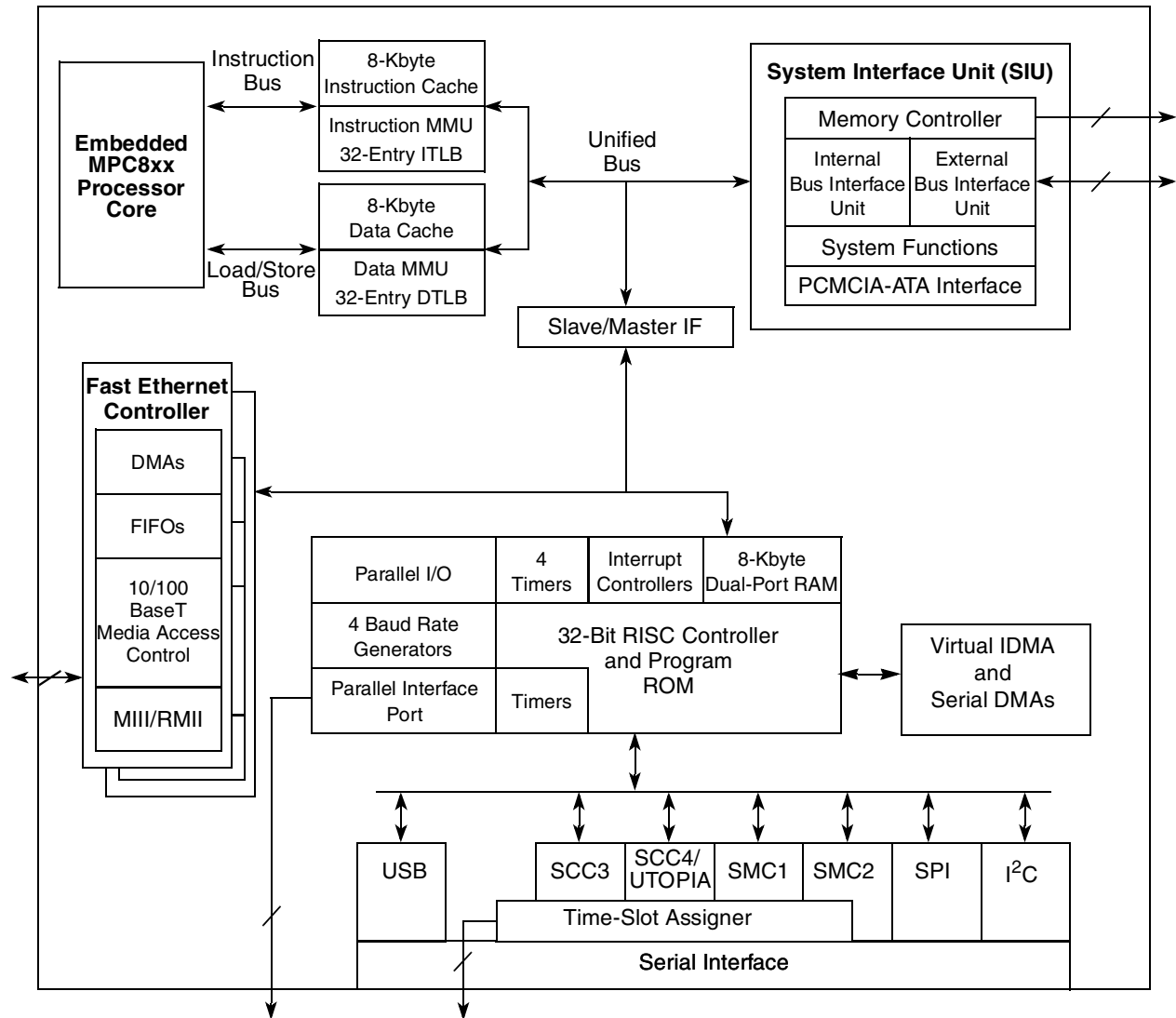


Figure 2. MPC880 Block Diagram

Table 6. DC Electrical Specifications (continued)

Characteristic	Symbol	Min	Max	Unit
Output high voltage, $I_{OH} = -2.0$ mA, except XTAL and open-drain pins	V_{OH}	2.4	—	V
Output low voltage $I_{OL} = 2.0$ mA (CLKOUT) $I_{OL} = 3.2$ mA ⁵ $I_{OL} = 5.3$ mA ⁶ $I_{OL} = 7.0$ mA (TXD1/PA14, TXD2/PA12) $I_{OL} = 8.9$ mA (\overline{TS} , \overline{TA} , \overline{TEA} , \overline{BI} , \overline{BB} , \overline{HRESET} , \overline{SRESET})	V_{OL}	—	0.5	V

¹ The difference between V_{DDL} and V_{DDSYN} cannot be more than 100 mV.

² The signals PA[0:15], PB[14:31], PC[4:15], PD[3:15], PE(14:31), TDI, TDO, TCK, \overline{TRST} , TMS, MII1_TXEN, MII_MDIO are 5-V tolerant. The minimum voltage is still 2.0 V.

³ V_{IL} (max) for the I²C interface is 0.8 V rather than the 1.5 V as specified in the I²C standard.

⁴ Input capacitance is periodically sampled.

⁵ A(0:31), TSIZ0/REG, TSIZ1, D(0:31), $\overline{IRQ6}$, RD/ \overline{WR} , \overline{BURST} , IP_B(3:7), PA(0:11), PA13, PA15, PB(14:31), PC(4:15), PD(3:15), PE(14:31), MII1_CRS, MII_MDIO, MII1_TXEN, and MII1_COL.

⁶ $\overline{BDIP}/\overline{GPL_B}(5)$, \overline{BR} , \overline{BG} , $\overline{FRZ}/\overline{IRQ6}$, $\overline{CS}(0:7)$, $\overline{WE}(0:3)$, $\overline{BS_A}(0:3)$, $\overline{GPL_A0}/\overline{GPL_B0}$, $\overline{OE}/\overline{GPL_A1}/\overline{GPL_B1}$, $\overline{GPL_A}(2:3)/\overline{GPL_B}(2:3)/\overline{CS}(2:3)$, UPWAITA/ $\overline{GPL_A4}$, UPWAITB/ $\overline{GPL_B4}$, $\overline{GPL_A5}$, $\overline{ALE_A}$, $\overline{CE1_A}$, $\overline{CE2_A}$, OP(0:3), and BADDR(28:30).

7 Thermal Calculation and Measurement

For the following discussions, $P_D = (V_{DDL} \times I_{DDL}) + P_{I/O}$, where $P_{I/O}$ is the power dissipation of the I/O drivers.

NOTE

The V_{DDSYN} power dissipation is negligible.

7.1 Estimation with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J , in °C can be obtained from the following equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_A = ambient temperature (°C)

$R_{\theta JA}$ = package junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in package

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. However, the answer is only an estimate; test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B32	CLKOUT falling edge to \overline{BS} valid, as requested by control bit BST4 in the corresponding word in the UPM (MAX = $0.00 \times B1 + 6.00$)	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B32a	CLKOUT falling edge to \overline{BS} valid, as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 0 (MAX = $0.25 \times B1 + 6.80$)	7.60	14.30	6.30	13.00	3.80	10.50	3.13	10.00	ns
B32b	CLKOUT rising edge to \overline{BS} valid, as requested by control bit BST2 in the corresponding word in the UPM (MAX = $0.00 \times B1 + 8.00$)	1.50	8.00	1.50	8.00	1.50	8.00	1.50	8.00	ns
B32c	CLKOUT rising edge to \overline{BS} valid, as requested by control bit BST3 in the corresponding word in the UPM (MAX = $0.25 \times B1 + 6.80$)	7.60	14.30	6.30	13.00	3.80	10.50	3.13	10.00	ns
B32d	CLKOUT falling edge to \overline{BS} valid, as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 1 (MAX = $0.375 \times B1 + 6.60$)	13.30	18.00	11.30	16.00	7.60	12.30	4.49	11.30	ns
B33	CLKOUT falling edge to \overline{GPL} valid, as requested by control bit GxT4 in the corresponding word in the UPM (MAX = $0.00 \times B1 + 6.00$)	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B33a	CLKOUT rising edge to \overline{GPL} valid, as requested by control bit GxT3 in the corresponding word in the UPM (MAX = $0.25 \times B1 + 6.80$)	7.60	14.30	6.30	13.00	3.80	10.50	3.13	10.00	ns
B34	A(0:31), BADDR(28:30), and D(0:31) to \overline{CS} valid, as requested by control bit CST4 in the corresponding word in the UPM (MIN = $0.25 \times B1 - 2.00$)	5.60	—	4.30	—	1.80	—	1.13	—	ns
B34a	A(0:31), BADDR(28:30), and D(0:31) to \overline{CS} valid, as requested by control bit CST1 in the corresponding word in the UPM (MIN = $0.50 \times B1 - 2.00$)	13.20	—	10.50	—	5.60	—	4.25	—	ns
B34b	A(0:31), BADDR(28:30), and D(0:31) to \overline{CS} valid, as requested by CST2 in the corresponding word in UPM (MIN = $0.75 \times B1 - 2.00$)	20.70	—	16.70	—	9.40	—	6.80	—	ns
B35	A(0:31), BADDR(28:30) to \overline{CS} valid, as requested by control bit BST4 in the corresponding word in the UPM (MIN = $0.25 \times B1 - 2.00$)	5.60	—	4.30	—	1.80	—	1.13	—	ns
B35a	A(0:31), BADDR(28:30), and D(0:31) to \overline{BS} valid, as requested by BST1 in the corresponding word in the UPM (MIN = $0.50 \times B1 - 2.00$)	13.20	—	10.50	—	5.60	—	4.25	—	ns
B35b	A(0:31), BADDR(28:30), and D(0:31) to \overline{BS} valid, as requested by control bit BST2 in the corresponding word in the UPM (MIN = $0.75 \times B1 - 2.00$)	20.70	—	16.70	—	9.40	—	7.40	—	ns

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B36	A(0:31), BADDR(28:30), and D(0:31) to \overline{GPL} valid, as requested by control bit GxT4 in the corresponding word in the UPM (MIN = $0.25 \times B1 - 2.00$)	5.60	—	4.30	—	1.80	—	1.13	—	ns
B37	UPWAIT valid to CLKOUT falling edge ⁹ (MIN = $0.00 \times B1 + 6.00$)	6.00	—	6.00	—	6.00	—	6.00	—	ns
B38	CLKOUT falling edge to UPWAIT valid ⁹ (MIN = $0.00 \times B1 + 1.00$)	1.00	—	1.00	—	1.00	—	1.00	—	ns
B39	\overline{AS} valid to CLKOUT rising edge ¹⁰ (MIN = $0.00 \times B1 + 7.00$)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B40	A(0:31), TSIZ(0:1), RD/ \overline{WR} , \overline{BURST} , valid to CLKOUT rising edge (MIN = $0.00 \times B1 + 7.00$)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B41	\overline{TS} valid to CLKOUT rising edge (setup time) (MIN = $0.00 \times B1 + 7.00$)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B42	CLKOUT rising edge to \overline{TS} valid (hold time) (MIN = $0.00 \times B1 + 2.00$)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B43	\overline{AS} negation to memory controller signals negation (MAX = TBD)	—	TBD	—	TBD	—	TBD	—	TBD	ns

¹ For part speeds above 50 MHz, use 9.80 ns for B11a.

² The timing required for \overline{BR} input is relevant when the MPC885/MPC880 is selected to work with the internal bus arbiter. The timing for \overline{BG} input is relevant when the MPC885/MPC880 is selected to work with the external bus arbiter.

³ For part speeds above 50 MHz, use 2 ns for B17.

⁴ The D(0:31) input timings B18 and B19 refer to the rising edge of the CLKOUT in which the \overline{TA} input signal is asserted.

⁵ For part speeds above 50 MHz, use 2 ns for B19.

⁶ The D(0:31) input timings B20 and B21 refer to the falling edge of the CLKOUT. This timing is valid only for read accesses controlled by chip-selects under control of the user-programmable machine (UPM) in the memory controller, for data beats where DLT3 = 1 in the RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

⁷ This formula applies to bus operation up to 50 MHz.

⁸ The timing B30 refers to \overline{CS} when ACS = 00 and to \overline{CS} and $\overline{WE}(0:3)$ when CSNT = 0.

⁹ The signal UPWAIT is considered asynchronous to the CLKOUT and synchronized internally. The timings specified in B37 and B38 are specified to enable the freeze of the UPM output signals as described in [Figure 21](#).

¹⁰ The \overline{AS} signal is considered asynchronous to the CLKOUT. The timing B39 is specified in order to allow the behavior specified in [Figure 24](#).

Figure 10 provides the timing for the synchronous input signals.

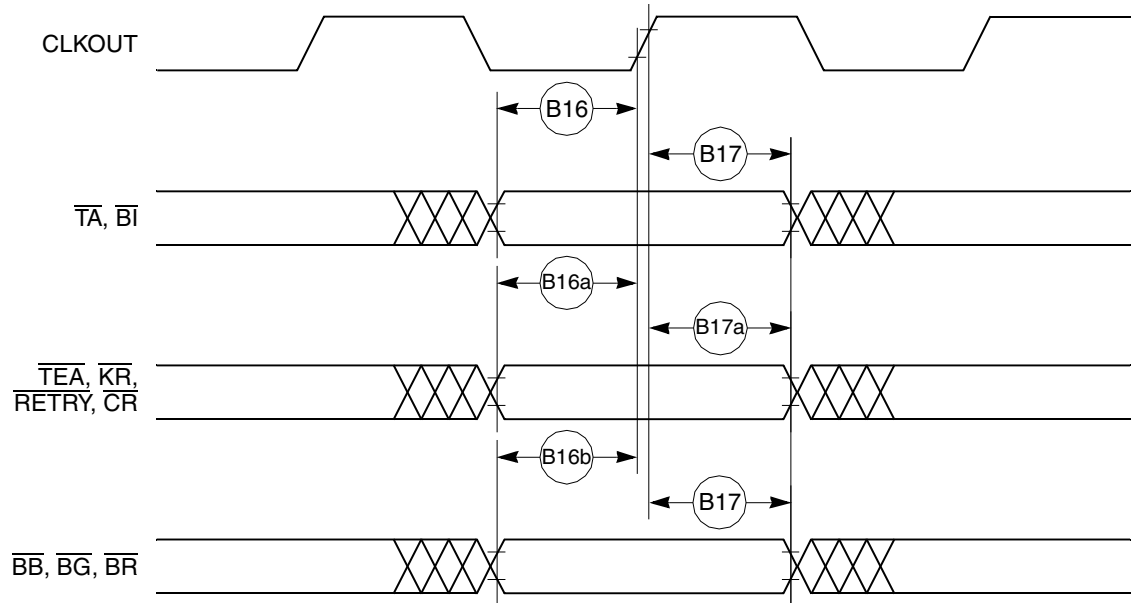


Figure 10. Synchronous Input Signals Timing

Figure 11 provides normal case timing for input data. It also applies to normal read accesses under the control of the user-programmable machine (UPM) in the memory controller.

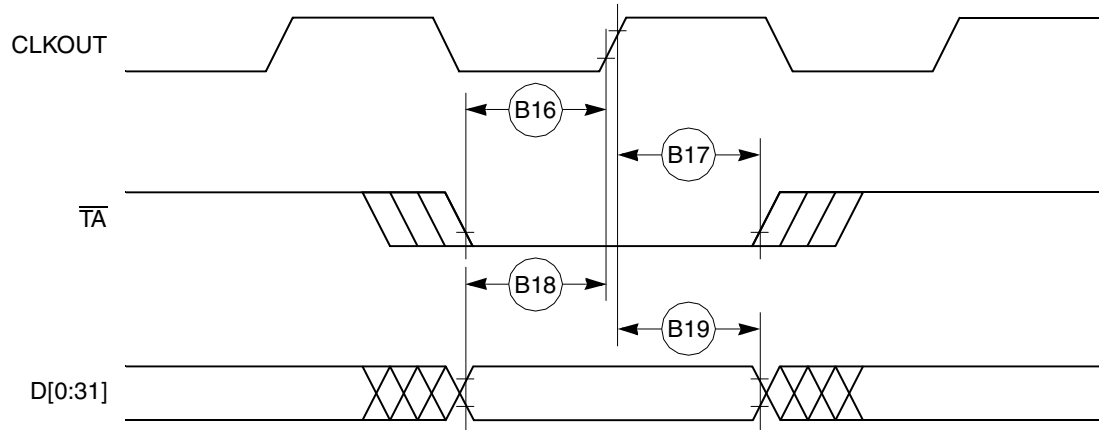


Figure 11. Input Data Timing in Normal Case

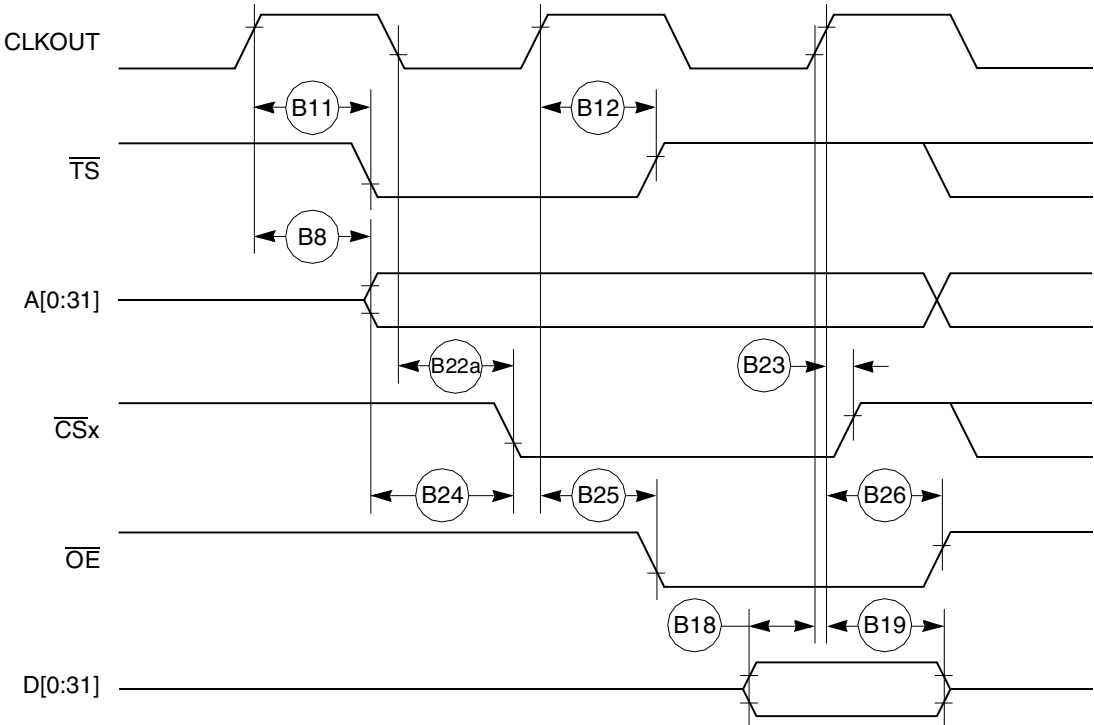


Figure 14. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 10)

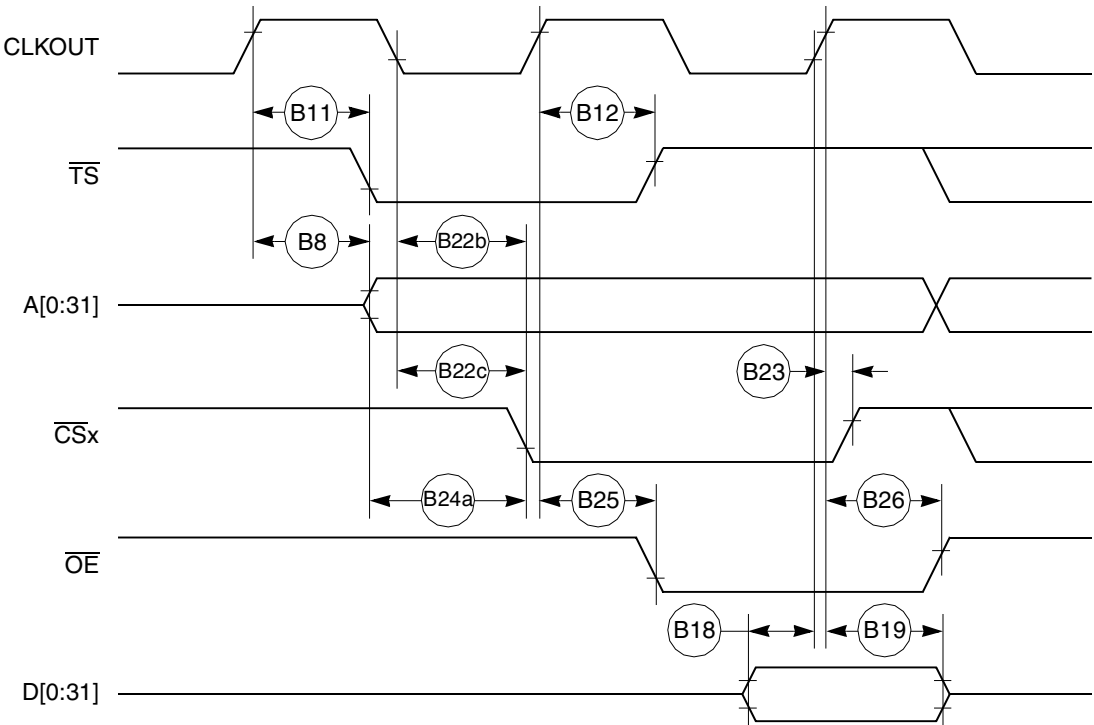


Figure 15. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 11)

Table 14 shows the reset timing for the MPC885/MPC880.

Table 14. Reset Timing

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
R69	CLKOUT to $\overline{\text{HRESET}}$ high impedance (MAX = $0.00 \times B1 + 20.00$)	—	20.00	—	20.00	—	20.00	—	20.00	ns
R70	CLKOUT to $\overline{\text{SRESET}}$ high impedance (MAX = $0.00 \times B1 + 20.00$)	—	20.00	—	20.00	—	20.00	—	20.00	ns
R71	$\overline{\text{RSTCONF}}$ pulse width (MIN = $17.00 \times B1$)	515.20	—	425.00	—	257.60	—	212.50	—	ns
R72	—	—	—	—	—	—	—	—	—	—
R73	Configuration data to $\overline{\text{HRESET}}$ rising edge setup time (MIN = $15.00 \times B1 + 50.00$)	504.50	—	425.00	—	277.30	—	237.50	—	ns
R74	Configuration data to $\overline{\text{RSTCONF}}$ rising edge setup time (MIN = $0.00 \times B1 + 350.00$)	350.00	—	350.00	—	350.00	—	350.00	—	ns
R75	Configuration data hold time after $\overline{\text{RSTCONF}}$ negation (MIN = $0.00 \times B1 + 0.00$)	0.00	—	0.00	—	0.00	—	0.00	—	ns
R76	Configuration data hold time after $\overline{\text{HRESET}}$ negation (MIN = $0.00 \times B1 + 0.00$)	0.00	—	0.00	—	0.00	—	0.00	—	ns
R77	$\overline{\text{HRESET}}$ and $\overline{\text{RSTCONF}}$ asserted to data out drive (MAX = $0.00 \times B1 + 25.00$)	—	25.00	—	25.00	—	25.00	—	25.00	ns
R78	$\overline{\text{RSTCONF}}$ negated to data out high impedance (MAX = $0.00 \times B1 + 25.00$)	—	25.00	—	25.00	—	25.00	—	25.00	ns
R79	CLKOUT of last rising edge before chip three-states $\overline{\text{HRESET}}$ to data out high impedance (MAX = $0.00 \times B1 + 25.00$)	—	25.00	—	25.00	—	25.00	—	25.00	ns
R80	DSDI, DSCK setup (MIN = $3.00 \times B1$)	90.90	—	75.00	—	45.50	—	37.50	—	ns
R81	DSDI, DSCK hold time (MIN = $0.00 \times B1 + 0.00$)	0.00	—	0.00	—	0.00	—	0.00	—	ns
R82	$\overline{\text{SRESET}}$ negated to CLKOUT rising edge for DSDI and DSCK sample (MIN = $8.00 \times B1$)	242.40	—	200.00	—	121.20	—	100.00	—	ns

11 IEEE 1149.1 Electrical Specifications

Table 15 provides the JTAG timings for the MPC885/MPC880 shown in Figure 38 through Figure 41.

Table 15. JTAG Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
J82	TCK cycle time	100.00	—	ns
J83	TCK clock pulse width measured at 1.5 V	40.00	—	ns
J84	TCK rise and fall times	0.00	10.00	ns
J85	TMS, TDI data setup time	5.00	—	ns
J86	TMS, TDI data hold time	25.00	—	ns
J87	TCK low to TDO data valid	—	27.00	ns
J88	TCK low to TDO data invalid	0.00	—	ns
J89	TCK low to TDO high impedance	—	20.00	ns
J90	$\overline{\text{TRST}}$ assert time	100.00	—	ns
J91	$\overline{\text{TRST}}$ setup time to TCK low	40.00	—	ns
J92	TCK falling edge to output valid	—	50.00	ns
J93	TCK falling edge to output valid out of high impedance	—	50.00	ns
J94	TCK falling edge to output high impedance	—	50.00	ns
J95	Boundary scan input valid to TCK rising edge	50.00	—	ns
J96	TCK rising edge to boundary scan input invalid	50.00	—	ns

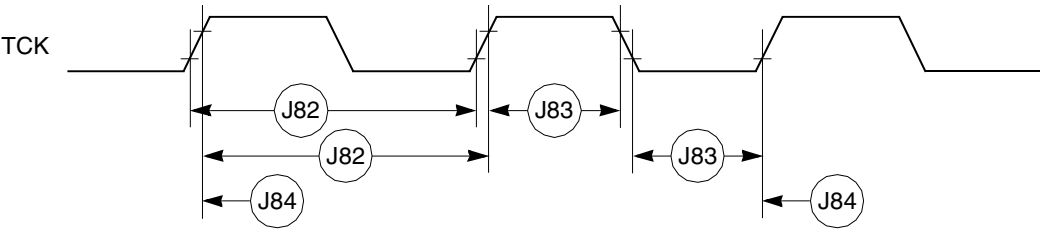


Figure 38. JTAG Test Clock Input Timing

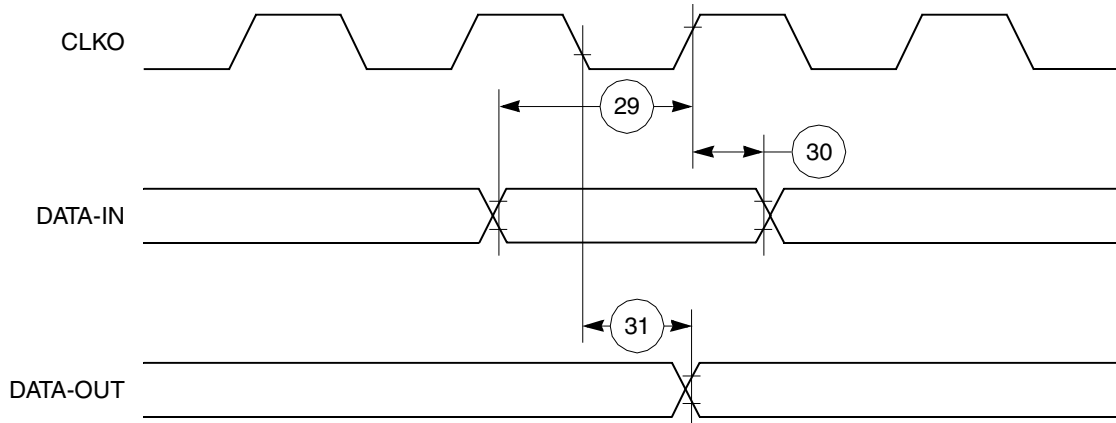


Figure 46. Parallel I/O Data-In/Data-Out Timing Diagram

12.2 Port C Interrupt AC Electrical Specifications

Table 17 provides the timings for port C interrupts.

Table 17. Port C Interrupt Timing

Num	Characteristic	33.34 MHz		Unit
		Min	Max	
35	Port C interrupt pulse width low (edge-triggered mode)	55	—	ns
36	Port C interrupt minimum time between active edges	55	—	ns

Figure 47 shows the port C interrupt detection timing.

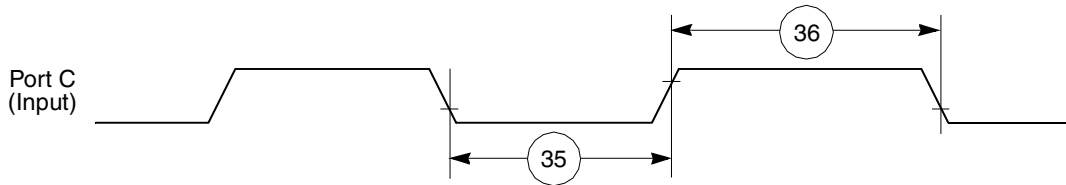


Figure 47. Port C Interrupt Detection Timing

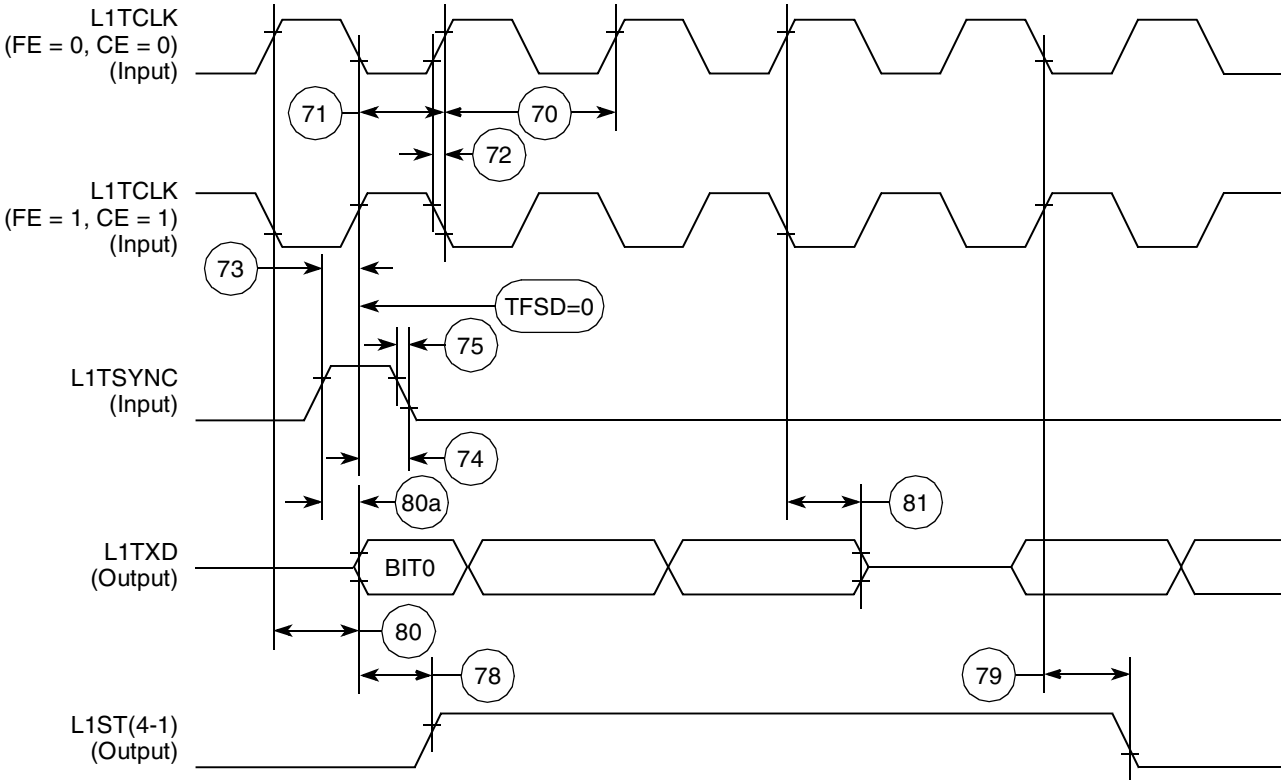


Figure 56. SI Transmit Timing Diagram (DSC = 0)

13 UTOPIA AC Electrical Specifications

Table 30, Table 31, and Table 32, show the AC electrical specifications for the UTOPIA interface.

Table 30. UTOPIA Master (Muxed Mode) Electrical Specifications

Num	Signal Characteristic	Direction	Min	Max	Unit
U1	UtpClk rise/fall time (internal clock option)	Output		4	ns
	Duty cycle		50	50	%
	Frequency			33	MHz
U2	UTPB, SOC, $\overline{\text{RxEnb}}$, $\overline{\text{TxEnb}}$, RxAddr, and TxAddr $\overline{\text{}}$ active delay (PHREQ and PHSEL active delay in multi-PHY mode)	Output	2	16	ns
U3	UTPB, SOC, Rxclav, and Txclav setup time	Input	4		ns
U4	UTPB, SOC, Rxclav, and Txclav hold time	Input	1		ns

Table 31. UTOPIA Master (Split Bus Mode) Electrical Specifications

Num	Signal Characteristic	Direction	Min	Max	Unit
U1	UtpClk rise/fall time (Internal clock option)	Output		4	ns
	Duty cycle		50	50	%
	Frequency			33	MHz
U2	UTPB, SOC, $\overline{\text{RxEnb}}$, $\overline{\text{TxEnb}}$, RxAddr, and TxAddr active delay (PHREQ and PHSEL active delay in multi-PHY mode)	Output	2	16	ns
U3	UTPB_Aux, SOC_Aux, Rxclav, and Txclav setup time	Input	4		ns
U4	UTPB_Aux, SOC_Aux, Rxclav, and Txclav hold time	Input	1		ns

Table 32. UTOPIA Slave (Split Bus Mode) Electrical Specifications

Num	Signal Characteristic	Direction	Min	Max	Unit
U1	UtpClk rise/fall time (external clock option)	Input		4	ns
	Duty cycle		40	60	%
	Frequency			33	MHz
U2	UTPB, SOC, Rxclav, and Txclav active delay	Output	2	16	ns
U3	UTPB_AUX, SOC_Aux, $\overline{\text{RxEnb}}$, $\overline{\text{TxEnb}}$, RxAddr, and TxAddr setup time	Input	4		ns
U4	UTPB_AUX, SOC_Aux, $\overline{\text{RxEnb}}$, $\overline{\text{TxEnb}}$, RxAddr, and TxAddr hold time	Input	1		ns

Figure 73 shows MII receive signal timing.

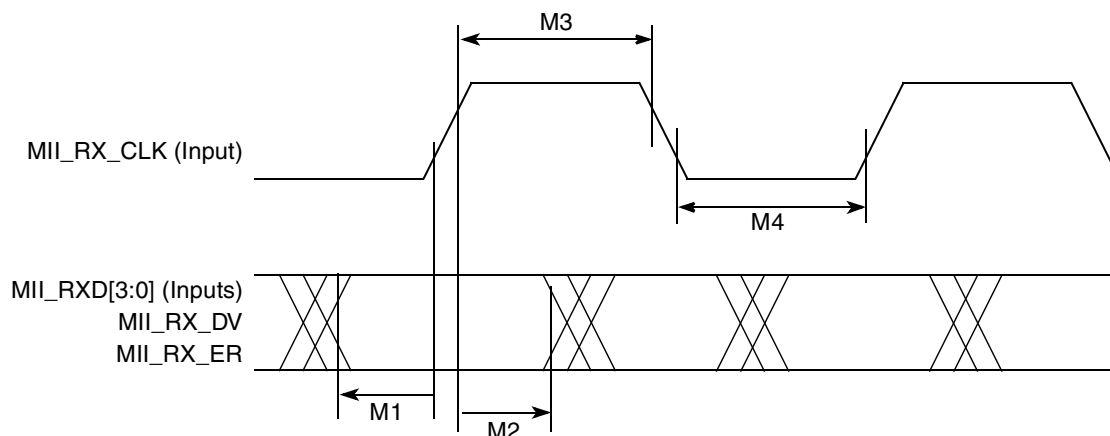


Figure 73. MII Receive Signal Timing Diagram

15.2 MII and Reduced MII Transmit Signal Timing

The transmitter functions correctly up to a MII_TX_CLK maximum frequency of 25 MHz + 1%. The RMII transmitter functions correctly up to a RMII_REFCLK maximum frequency of 50 MHz + 1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_TX_CLK frequency - 1%.

Table 35 provides information on the MII and RMII transmit signal timing.

Table 35. MII Transmit Signal Timing

Num	Characteristic	Min	Max	Unit
M5	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER invalid	5	—	ns
M6	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER valid	—	25	ns
M20_RMII	RMII_TXD[1:0], RMII_TX_EN to RMII_REFCLK setup	4	—	ns
M21_RMII	RMII_TXD[1:0], RMII_TX_EN data hold from RMII_REFCLK rising edge	2	—	ns
M7	MII_TX_CLK and RMII_REFCLK pulse width high	35%	65%	MII_TX_CLK or RMII_REFCLK period
M8	MII_TX_CLK and RMII_REFCLK pulse width low	35%	65%	MII_TX_CLK or RMII_REFCLK period

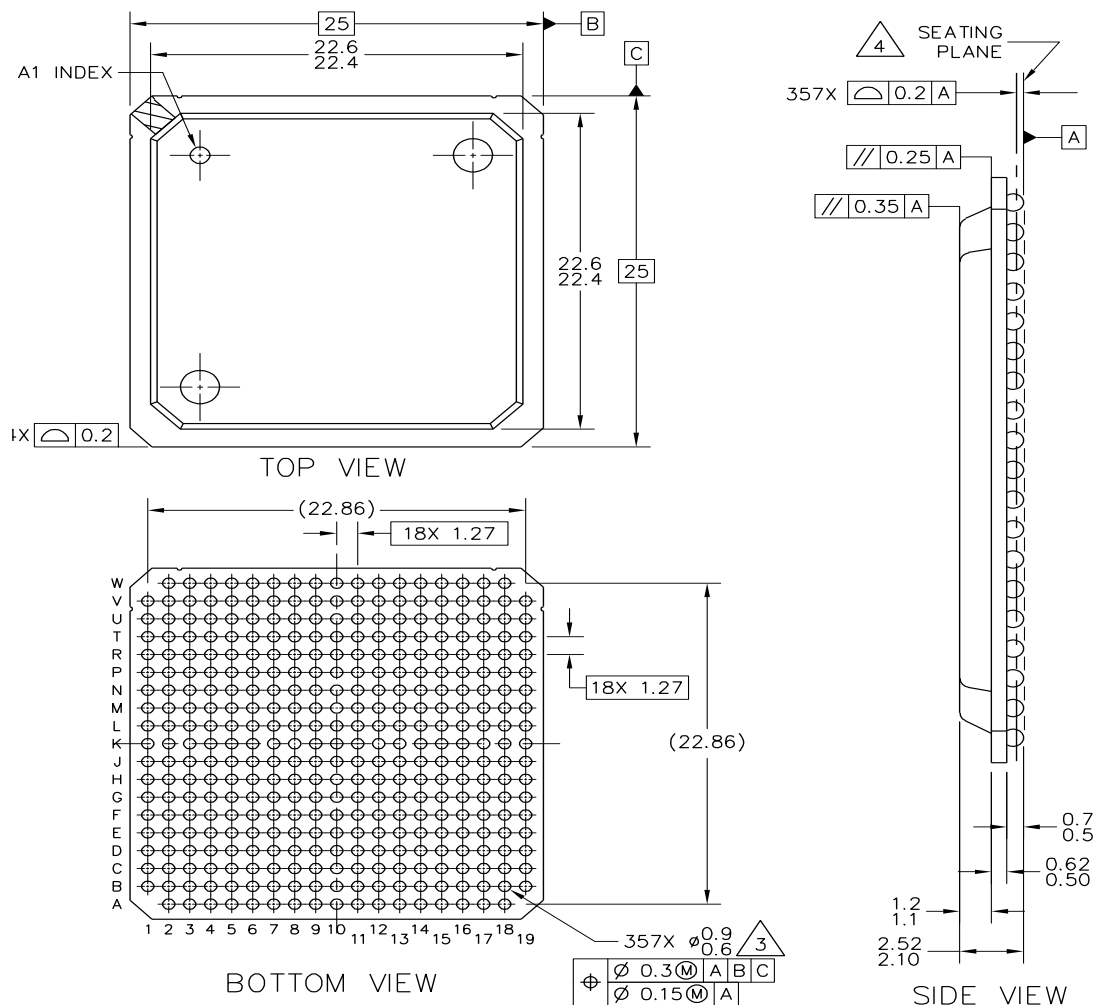
Table 39 contains a list of the MPC885 input and output signals and shows multiplexing and pin assignments.

Table 39. Pin Assignments

Name	Pin Number	Type
A[0:31]	M16, N18, N19, M19, M17, M18, L16, L19, L17, L18, K19, K18, K17, K16, J19, J17, J18, J16, E19, H18, H17, G19, F17, G17, H16, F19, D19, H19, E18, G18, F18, D18	Bidirectional Three-state
D[0:31]	P2, M1, L1, K2, N1, K4, H3, F2, P1, L4, L3, L2, N3, N2, K3, K1, J2, M4, J1, J3, H2, H1, J4, M3, G2, G1, G3, M2, H4, F1, E1, F3	Bidirectional Three-state
TSIZ0, $\overline{\text{REG}}$	G16	Bidirectional Three-state
TSIZ1	E17	Bidirectional Three-state
RD/ $\overline{\text{WR}}$	D13	Bidirectional Three-state
$\overline{\text{BURST}}$	C10	Bidirectional Three-state
$\overline{\text{BDIP}}$, $\overline{\text{GPL_B5}}$	A13	Output
$\overline{\text{TS}}$	A12	Bidirectional Active pull-up
$\overline{\text{TA}}$	C12	Bidirectional Active pull-up
$\overline{\text{TEA}}$	B12	Open-drain
$\overline{\text{BI}}$	D12	Bidirectional Active pull-up
$\overline{\text{IRQ2}}$, $\overline{\text{RSV}}$	B10	Bidirectional Three-state
$\overline{\text{IRQ4}}$, $\overline{\text{KR}}$, $\overline{\text{RETRY}}$, $\overline{\text{SPKROUT}}$	C7	Bidirectional Three-state
$\overline{\text{CR}}$, $\overline{\text{IRQ3}}$	A11	Input
$\overline{\text{BR}}$	D11	Bidirectional
$\overline{\text{BG}}$	C11	Bidirectional
$\overline{\text{BB}}$	B11	Bidirectional Active pull-up
FRZ, $\overline{\text{IRQ6}}$	D10	Bidirectional
$\overline{\text{IRQ0}}$	N4	Input
$\overline{\text{IRQ1}}$	P3	Input
$\overline{\text{IRQ7}}$	P4	Input
$\overline{\text{CS}}[0:5]$	B14, C14, A15, D14, C16, A16	Output
$\overline{\text{CS6}}$, $\overline{\text{CE1_B}}$	D15	Output
$\overline{\text{CS7}}$, $\overline{\text{CE2_B}}$	B16	Output

16.2 Mechanical Dimensions of the PBGA Package

Figure 78 shows the mechanical dimensions of the PBGA package.



NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M—1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

Figure 78. Mechanical Dimensions and Bottom Surface Nomenclature of the PBGA Package

17 Document Revision History

Table 40 lists significant changes between revisions of this hardware specification.

Table 40. Document Revision History

Revision Number	Date	Changes
7	07/2010	In Table 9, "Bus Operation Timings," changed the following: <ul style="list-style-type: none"> Updated TRLX condition value for B22a/b/c to "TRLX = [0 or 1]" Removed TRLX condition for B23 Updated condition and equation for B30 to "Invalid GPCM read/write access (MIN = $0.25 \times B1 - 2.00$)" Updated note 8 to "The timing B30 refers to \overline{CS} when ACS = 00 and to \overline{CS} and $\overline{WE}(0:3)$ when CSNT = 0."
6	05/2010	Added minimum load for CLKOUT in Section 10, "Bus Signal Timing."
5	03/2009	Updated formatting of Table 12, "PCMCIA Port Timing," Table 13, "Debug Port Timing," Table 14, "Reset Timing," and Table 15, "JTAG Timing."
4	08/2007	<ul style="list-style-type: none"> On page 1, updated first paragraph and added a second paragraph. After Table 2, inserted a new figure showing the undershoot/overshoot voltage (Figure 3) and renumbered the rest of the figures. In Table 9, for reset timings B29f and B29g added footnote indicating that the formula only applies to bus operation up to 50 MHz. In Figure 6, changed all reference voltage measurement points from 0.2 and 0.8 V to 50% level. In Table 18, changed num 46 description to read, "\overline{TA} assertion to rising edge ..." In Figure 49, changed \overline{TA} to reflect the rising edge of the clock.
3.0	7/22/2004	<ul style="list-style-type: none"> Added sentence to Spec B1A about EXTCLK and CLKOUT being in Alignment for Integer Values Added a footnote to Spec 41 specifying that EDM = 1 Added RMII1_EN under M1II_EN in Table 36 Pin Assignments Added a tablefootnote to Table 6 DC Electrical Specifications about meeting the VIL Max of the I2C Standard Put the new part numbers in the Ordering Information Section
2.0	12/2003	<ul style="list-style-type: none"> Changed the maximum operating frequency to 133 MHz. Put in the orderable part numbers that are orderable. Put the timing in the 80 MHz column. Rounded the timings to hundredths in the 80 MHz column. Put the pin numbers in footnotes by the maximum currents in Table 6. Changed 22 and 41 in the Timing. Put in the Thermal numbers.
1.0	9/2003	<ul style="list-style-type: none"> Added the DSP information in the Features list Fixed table formatting. Nontechnical edits. Released to the external web.
0.9	8/2003	Changed the USB description to full-/low-speed compatible.
0.8	8/2003	Added the Reference to USB 2.0 to the Features list and removed 1.1 from USB on the block diagrams.
0.7	7/2003	Added the RxClav and TxClav signals to PC15.
0.6	6/2003	Changed the pin descriptions per the June 22 spec.
0.5	5/2003	Changed some more typos, put in the phsel and phreq pins. Corrected the USB timing.

How to Reach Us:

Home Page:

www.freescale.com

Web Support:

<http://www.freescale.com/support>

USA/Europe or Locations Not Listed:

Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
1-800-521-6274 or
+1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:

Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo 153-0064
Japan
0120 191014 or
+81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

For Literature Requests Only:

Freescale Semiconductor
Literature Distribution Center
1-800 441-2447 or
+1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale, the Freescale logo, and PowerQUICC, are trademarks of Freescale Semiconductor, Inc. Reg. U.S. Pat. & Tm. Off. All other product or service names are the property of their respective owners. The Power Architecture and Power.org word marks and the Power and Power.org logos and related marks are trademarks and service marks licensed by Power.org.

© 2010 Freescale Semiconductor, Inc.

