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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	133MHz
Co-Processors/DSP	Communications; CPM, Security; SEC
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (3), 10/100Mbps (2)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	Cryptography
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc885zp133

1 Overview

The MPC885/MPC880 is a versatile single-chip integrated microprocessor and peripheral combination that can be used in a variety of controller applications and communications and networking systems. The MPC885/MPC880 provides enhanced ATM functionality, an additional fast Ethernet controller, a USB, and an encryption block.

Table 1 shows the functionality supported by MPC885/MPC880.

Table 1. MPC885 Family

Part	Cache (Kbytes)		Ethernet		SCC	SMC	USB	ATM Support	Security Engine
	I Cache	D Cache	10BaseT	10/100					
MPC885	8	8	Up to 3	2	3	2	1	Serial ATM and UTOPIA interface	Yes
MPC880	8	8	Up to 2	2	2	2	1	Serial ATM and UTOPIA interface	No

2 Features

The MPC885/MPC880 is comprised of three modules that each use the 32-bit internal bus: a MPC8xx core, a system integration unit (SIU), and a communications processor module (CPM).

The following list summarizes the key MPC885/MPC880 features:

- Embedded MPC8xx core up to 133 MHz
- Maximum frequency operation of the external bus is 80 MHz (in 1:1 mode)
  - The 133-MHz core frequency supports 2:1 mode only.
  - The 66-/80-MHz core frequencies support both the 1:1 and 2:1 modes.
- Single-issue, 32-bit core (compatible with the Power Architecture definition) with thirty-two 32-bit general-purpose registers (GPRs)
  - The core performs branch prediction with conditional prefetch and without conditional execution.
  - 8-Kbyte data cache and 8-Kbyte instruction cache (see Table 1)
    - Instruction cache is two-way, set-associative with 256 sets in 2 blocks
    - Data cache is two-way, set-associative with 256 sets
    - Cache coherency for both instruction and data caches is maintained on 128-bit (4-word) cache blocks.
    - Caches are physically addressed, implement a least recently used (LRU) replacement algorithm, and are lockable on a cache block basis.
  - MMUs with 32-entry TLB, fully associative instruction and data TLBs
  - MMUs support multiple page sizes of 4, 16, and 512 Kbytes, and 8 Mbytes; 16 virtual address spaces and 16 protection groups
  - Advanced on-chip emulation debug mode

Table 6. DC Electrical Specifications (continued)

Characteristic	Symbol	Min	Max	Unit
Output high voltage, I_{OH} = –2.0 mA, except XTAL and open-drain pins	V_{OH}	2.4	—	V
Output low voltage I_{OL} = 2.0 mA (CLKOUT) I_{OL} = 3.2 mA[5] I_{OL} = 5.3 mA[6] I_{OL} = 7.0 mA (TXD1/PA14, TXD2/PA12) I_{OL} = 8.9 mA ($\overline{TS}$, $\overline{TA}$, $\overline{TEA}$, $\overline{BI}$, $\overline{BB}$, $\overline{HRESET}$, $\overline{SRESET}$)	V_{OL}	—	0.5	V

1 The difference between V_{DDL} and V_{DDSYN} cannot be more than 100 mV.

2 The signals PA[0:15], PB[14:31], PC[4:15], PD[3:15], PE(14:31), TDI, TDO, TCK, $\overline{TRST}$, TMS, MII1_TXEN, MII_MDIO are 5-V tolerant. The minimum voltage is still 2.0 V.

3 V_{IL}(max) for the I^2C interface is 0.8 V rather than the 1.5 V as specified in the I^2C standard.

4 Input capacitance is periodically sampled.

5 A(0:31), TSIZ0/$\overline{REG}$, TSIZ1, D(0:31), $\overline{IRQ}$(2:4), $\overline{IRQ6}$, RD/$\overline{WR}$, $\overline{BURST}$, IP_B(3:7), PA(0:11), PA13, PA15, PB(14:31), PC(4:15), PD(3:15), PE(14:31), MII1_CRS, MII_MDIO, MII1_TXEN, and MII1_COL.

6 $\overline{BDIP}$/$\overline{GPL\_B}$(5), $\overline{BR}$, $\overline{BG}$, FRZ/$\overline{IRQ6}$, $\overline{CS}$(0:7), $\overline{WE}$(0:3), $\overline{BS}$_A(0:3), $\overline{GPL\_A0}$/$\overline{GPL\_B0}$, $\overline{OE}$/$\overline{GPL\_A1}$/$\overline{GPL\_B1}$, $\overline{GPL\_A}$(2:3)/$\overline{GPL\_B}$(2:3)/$\overline{CS}$(2:3), UPWAITA/$\overline{GPL\_A4}$, UPWAITB/$\overline{GPL\_B4}$, $\overline{GPL\_A5}$, ALE_A, $\overline{CE}$1_A, $\overline{CE}$2_A, OP(0:3), and BADDR(28:30).

7 Thermal Calculation and Measurement

For the following discussions, $P_D = (V_{DDL} \times I_{DDL}) + PI/O$, where PI/O is the power dissipation of the I/O drivers.

NOTE

The V_{DDSYN} power dissipation is negligible.

7.1 Estimation with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, in °C can be obtained from the following equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_A = ambient temperature (ºC)

$R_{\theta JA}$ = package junction-to-ambient thermal resistance (ºC/W)

P_D = power dissipation in package

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. However, the answer is only an estimate; test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B32	CLKOUT falling edge to $\overline{BS}$ valid, as requested by control bit BST4 in the corresponding word in the UPM (MAX = 0.00 × B1 + 6.00)	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B32a	CLKOUT falling edge to $\overline{BS}$ valid, as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 0 (MAX = 0.25 × B1 + 6.80)	7.60	14.30	6.30	13.00	3.80	10.50	3.13	10.00	ns
B32b	CLKOUT rising edge to $\overline{BS}$ valid, as requested by control bit BST2 in the corresponding word in the UPM (MAX = 0.00 × B1 + 8.00)	1.50	8.00	1.50	8.00	1.50	8.00	1.50	8.00	ns
B32c	CLKOUT rising edge to $\overline{BS}$ valid, as requested by control bit BST3 in the corresponding word in the UPM (MAX = 0.25 × B1 + 6.80)	7.60	14.30	6.30	13.00	3.80	10.50	3.13	10.00	ns
B32d	CLKOUT falling edge to $\overline{BS}$ valid, as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 1 (MAX = 0.375 × B1 + 6.60)	13.30	18.00	11.30	16.00	7.60	12.30	4.49	11.30	ns
B33	CLKOUT falling edge to $\overline{GPL}$ valid, as requested by control bit GxT4 in the corresponding word in the UPM (MAX = 0.00 × B1 + 6.00)	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B33a	CLKOUT rising edge to $\overline{GPL}$ valid, as requested by control bit GxT3 in the corresponding word in the UPM (MAX = 0.25 × B1 + 6.80)	7.60	14.30	6.30	13.00	3.80	10.50	3.13	10.00	ns
B34	A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid, as requested by control bit CST4 in the corresponding word in the UPM (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	1.80	—	1.13	—	ns
B34a	A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid, as requested by control bit CST1 in the corresponding word in the UPM (MIN = 0.50 × B1 – 2.00)	13.20	—	10.50	—	5.60	—	4.25	—	ns
B34b	A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid, as requested by CST2 in the corresponding word in UPM (MIN = 0.75 × B1 – 2.00)	20.70	—	16.70	—	9.40	—	6.80	—	ns
B35	A(0:31), BADDR(28:30) to $\overline{CS}$ valid, as requested by control bit BST4 in the corresponding word in the UPM (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	1.80	—	1.13	—	ns
B35a	A(0:31), BADDR(28:30), and D(0:31) to $\overline{BS}$ valid, as requested by BST1 in the corresponding word in the UPM (MIN = 0.50 × B1 – 2.00)	13.20	—	10.50	—	5.60	—	4.25	—	ns
B35b	A(0:31), BADDR(28:30), and D(0:31) to $\overline{BS}$ valid, as requested by control bit BST2 in the corresponding word in the UPM (MIN = 0.75 × B1 – 2.00)	20.70	—	16.70	—	9.40	—	7.40	—	ns

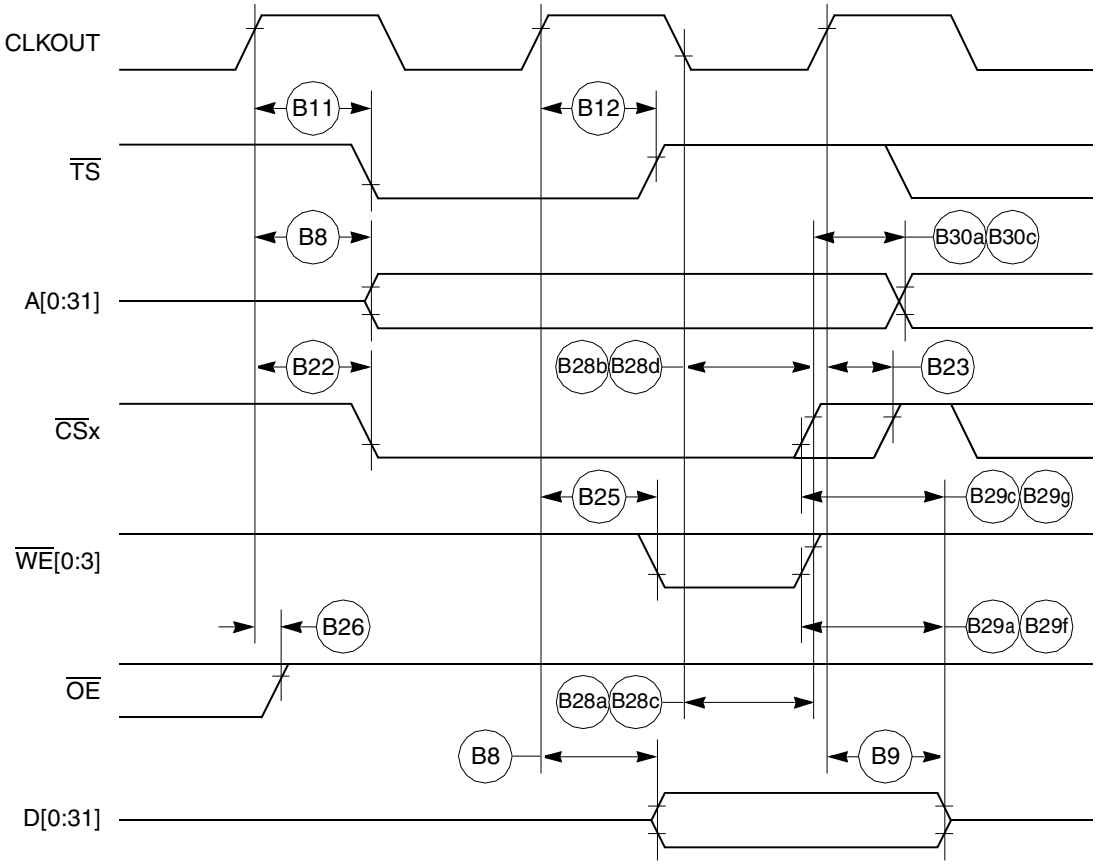

Figure 18. External Bus Write Timing (GPCM Controlled—TRLX = 0, CSNT = 1)

Figure 21 provides the timing for the asynchronous asserted UPWAIT signal controlled by the UPM.

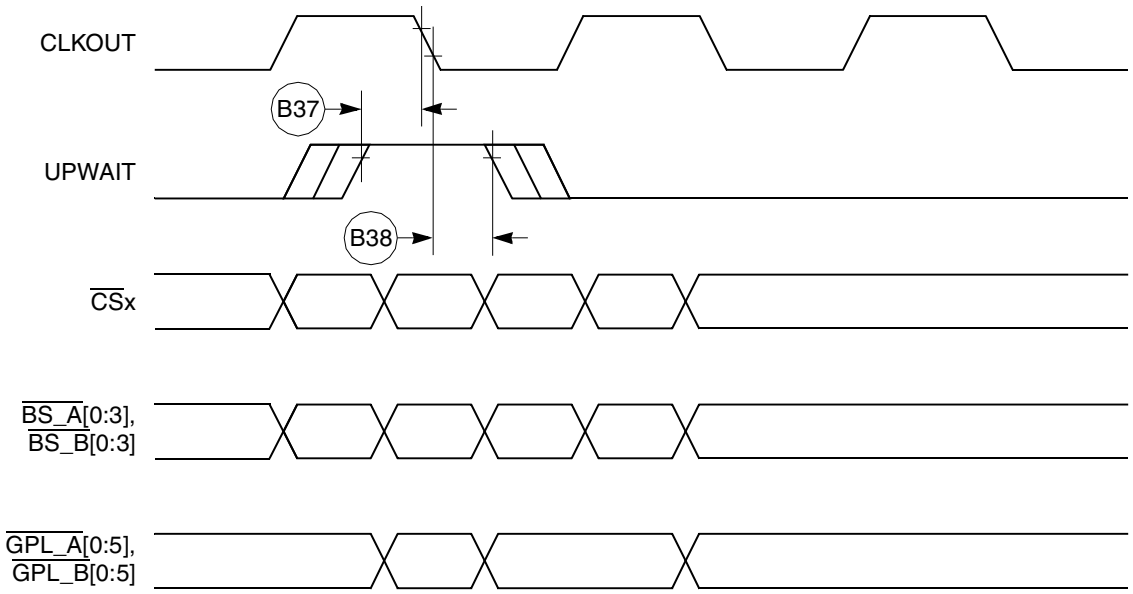

Figure 21. Asynchronous UPWAIT Asserted Detection in UPM-Handled Cycles Timing

Figure 22 provides the timing for the asynchronous negated UPWAIT signal controlled by the UPM.

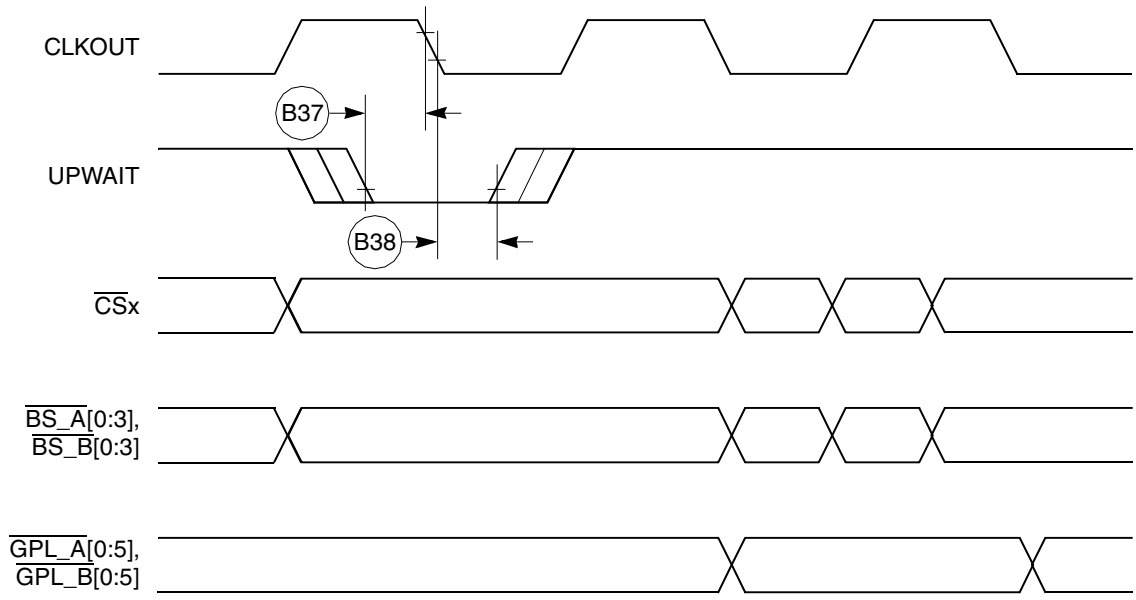

Figure 22. Asynchronous UPWAIT Negated Detection in UPM-Handled Cycles Timing

Figure 23 provides the timing for the synchronous external master access controlled by the GPCM.

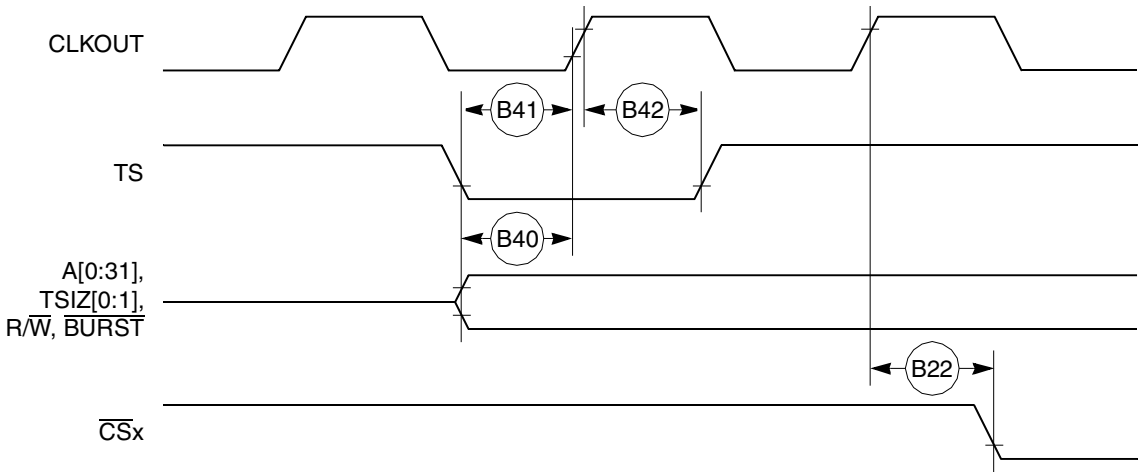

Figure 23. Synchronous External Master Access Timing (GPCM Handled—ACS = 00)

Figure 24 provides the timing for the asynchronous external master memory access controlled by the GPCM.

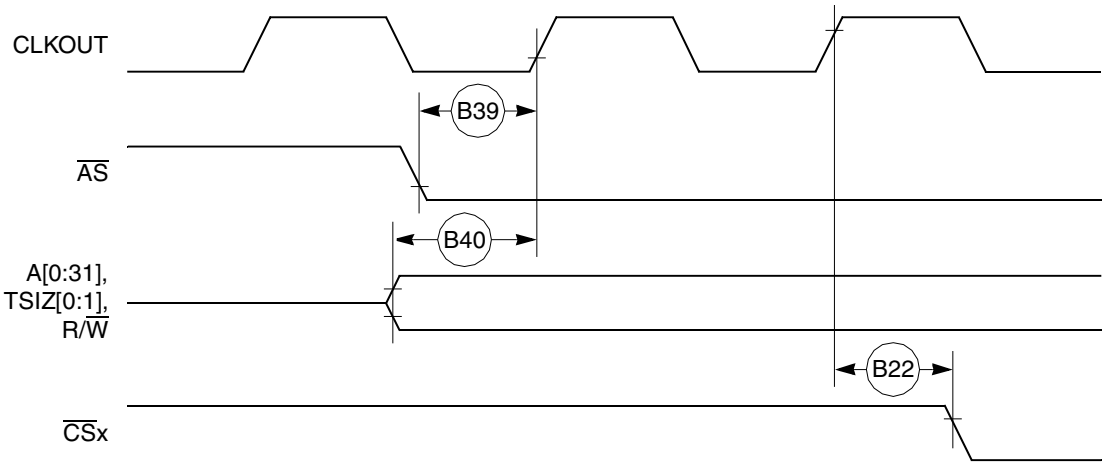

Figure 24. Asynchronous External Master Memory Access Timing (GPCM Controlled—ACS = 00)

Figure 25 provides the timing for the asynchronous external master control signals negation.

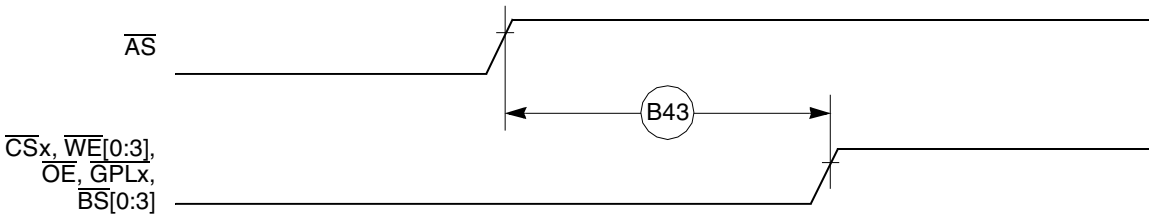

Figure 25. Asynchronous External Master—Control Signals Negation Timing

Figure 29 provides the PCMCIA access cycle timing for the external bus write.

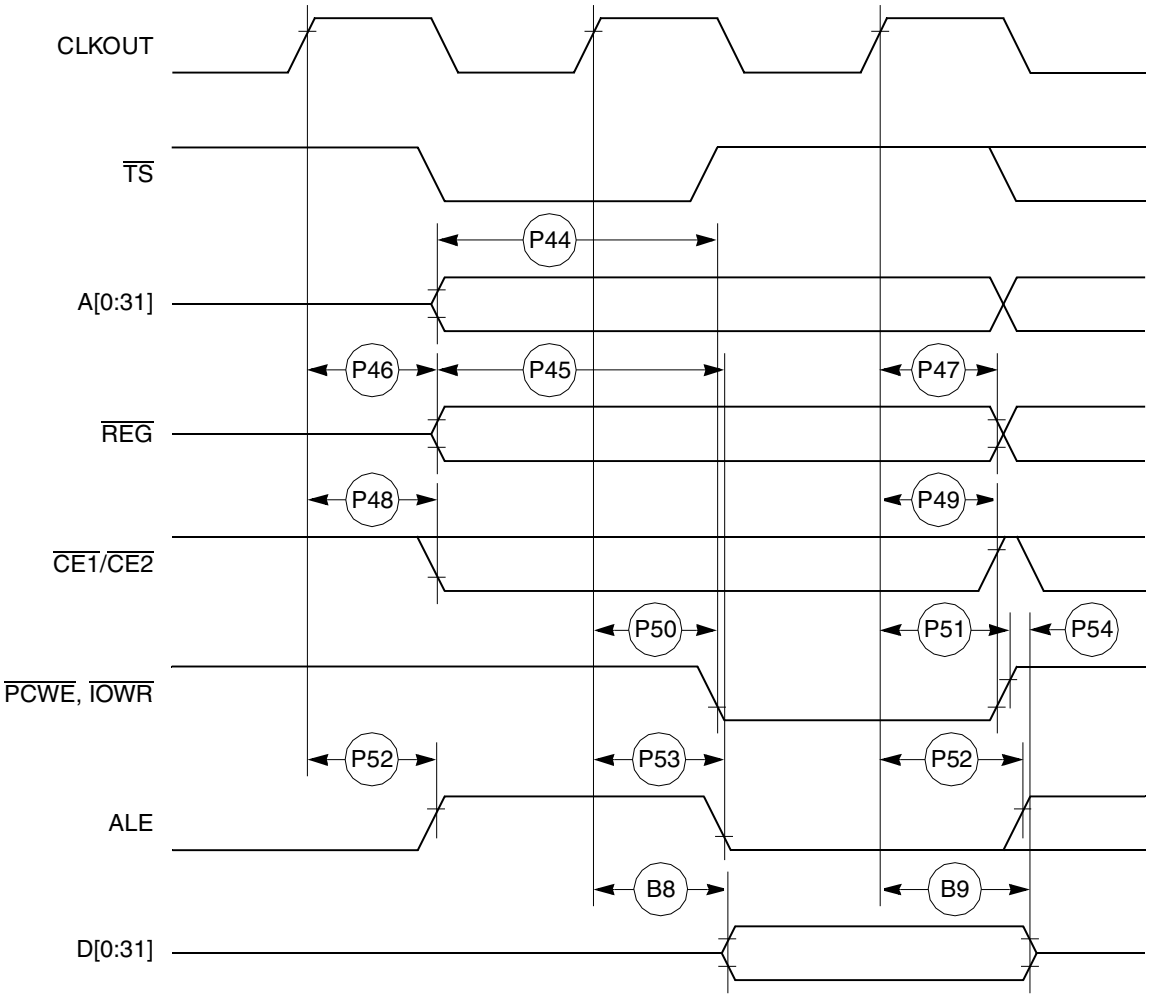

Figure 29. PCMCIA Access Cycles Timing External Bus Write

Figure 30 provides the PCMCIA WAIT signals detection timing.

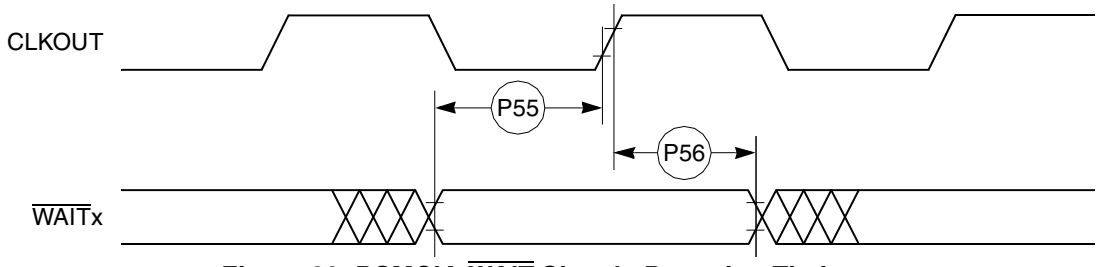

Figure 30. PCMCIA WAIT Signals Detection Timing

Table 14 shows the reset timing for the MPC885/MPC880.

Table 14. Reset Timing

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
R69	CLKOUT to $\overline{\text{HRESET}}$ high impedance (MAX = 0.00 × B1 + 20.00)	—	20.00	—	20.00	—	20.00	—	20.00	ns
R70	CLKOUT to $\overline{\text{SRESET}}$ high impedance (MAX = 0.00 × B1 + 20.00)	—	20.00	—	20.00	—	20.00	—	20.00	ns
R71	$\overline{\text{RSTCONF}}$ pulse width (MIN = 17.00 × B1)	515.20	—	425.00	—	257.60	—	212.50	—	ns
R72	—	—	—	—	—	—	—	—	—	—
R73	Configuration data to HRESET rising edge setup time (MIN = 15.00 × B1 + 50.00)	504.50	—	425.00	—	277.30	—	237.50	—	ns
R74	Configuration data to $\overline{\text{RSTCONF}}$ rising edge setup time (MIN = 0.00 × B1 + 350.00)	350.00	—	350.00	—	350.00	—	350.00	—	ns
R75	Configuration data hold time after $\overline{\text{RSTCONF}}$ negation (MIN = 0.00 × B1 + 0.00)	0.00	—	0.00	—	0.00	—	0.00	—	ns
R76	Configuration data hold time after $\overline{\text{HRESET}}$ negation (MIN = 0.00 × B1 + 0.00)	0.00	—	0.00	—	0.00	—	0.00	—	ns
R77	$\overline{\text{HRESET}}$ and $\overline{\text{RSTCONF}}$ asserted to data out drive (MAX = 0.00 × B1 + 25.00)	—	25.00	—	25.00	—	25.00	—	25.00	ns
R78	$\overline{\text{RSTCONF}}$ negated to data out high impedance (MAX = 0.00 × B1 + 25.00)	—	25.00	—	25.00	—	25.00	—	25.00	ns
R79	CLKOUT of last rising edge before chip three-states $\overline{\text{HRESET}}$ to data out high impedance (MAX = 0.00 × B1 + 25.00)	—	25.00	—	25.00	—	25.00	—	25.00	ns
R80	DSDI, DSCK setup (MIN = 3.00 × B1)	90.90	—	75.00	—	45.50	—	37.50	—	ns
R81	DSDI, DSCK hold time (MIN = 0.00 × B1 + 0.00)	0.00	—	0.00	—	0.00	—	0.00	—	ns
R82	$\overline{\text{SRESET}}$ negated to CLKOUT rising edge for DSDI and DSCK sample (MIN = 8.00 × B1)	242.40	—	200.00	—	121.20	—	100.00	—	ns

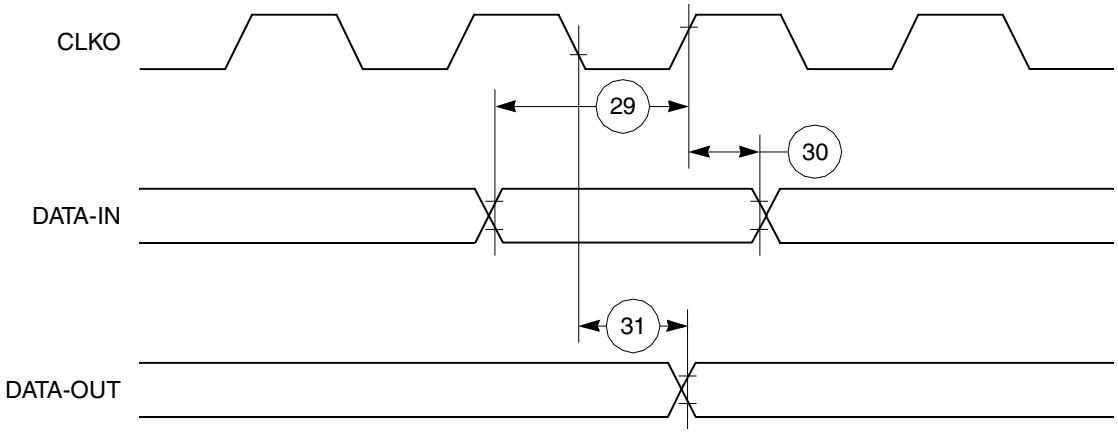

Figure 46. Parallel I/O Data-In/Data-Out Timing Diagram

12.2 Port C Interrupt AC Electrical Specifications

Table 17 provides the timings for port C interrupts.

Table 17. Port C Interrupt Timing

Num	Characteristic	33.34 MHz		Unit
		Min	Max	
35	Port C interrupt pulse width low (edge-triggered mode)	55	—	ns
36	Port C interrupt minimum time between active edges	55	—	ns

Figure 47 shows the port C interrupt detection timing.

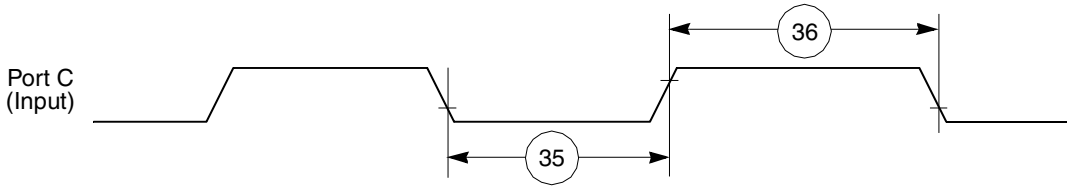

Figure 47. Port C Interrupt Detection Timing

Table 21. SI Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
76	L1RXD valid to L1CLK edge (L1RXD setup time)	17.00	—	ns
77	L1CLK edge to L1RXD invalid (L1RXD hold time)	13.00	—	ns
78	L1CLK edge to L1ST(1–4) valid[4]	10.00	45.00	ns
78A	L1SYNC valid to L1ST(1–4) valid	10.00	45.00	ns
79	L1CLK edge to L1ST(1–4) invalid	10.00	45.00	ns
80	L1CLK edge to L1TXD valid	10.00	55.00	ns
80A	L1TSYNC valid to L1TXD valid[4]	10.00	55.00	ns
81	L1CLK edge to L1TXD high impedance	0.00	42.00	ns
82	L1RCLK, L1TCLK frequency (DSC =1)	—	16.00 or SYNCCLK/2	MHz
83	L1RCLK, L1TCLK width low (DSC =1)	P + 10	—	ns
83a	L1RCLK, L1TCLK width high (DSC = 1)[3]	P + 10	—	ns
84	L1CLK edge to L1CLKO valid (DSC = 1)	—	30.00	ns
85	$\overline{\text{L1RQ}}$ valid before falling edge of L1TSYNC[4]	1.00	—	L1TCLK
86	L1GR setup time[2]	42.00	—	ns
87	L1GR hold time	42.00	—	ns
88	L1CLK edge to L1SYNC valid (FSD = 00) CNT = 0000, BYT = 0, DSC = 0)	—	0.00	ns

1 The ratio SyncCLK/L1RCLK must be greater than 2.5/1.
2 These specs are valid for IDL mode only.
3 Where P = 1/CLKOUT. Thus for a 25-MHz CLKO1 rate, P = 40 ns.
4 These strobes and TxD on the first bit of the frame become valid after L1CLK edge or L1SYNC, whichever comes later.

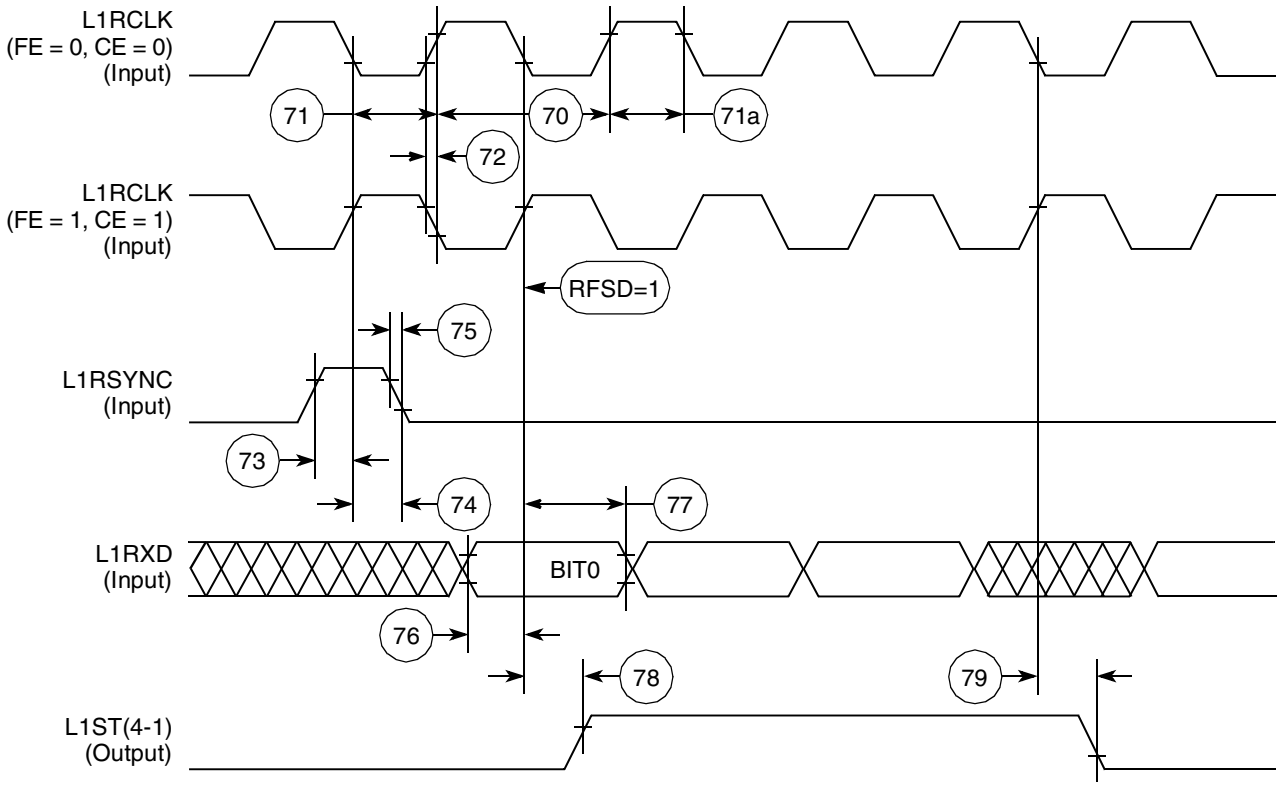

Figure 54. SI Receive Timing Diagram with Normal Clocking (DSC = 0)

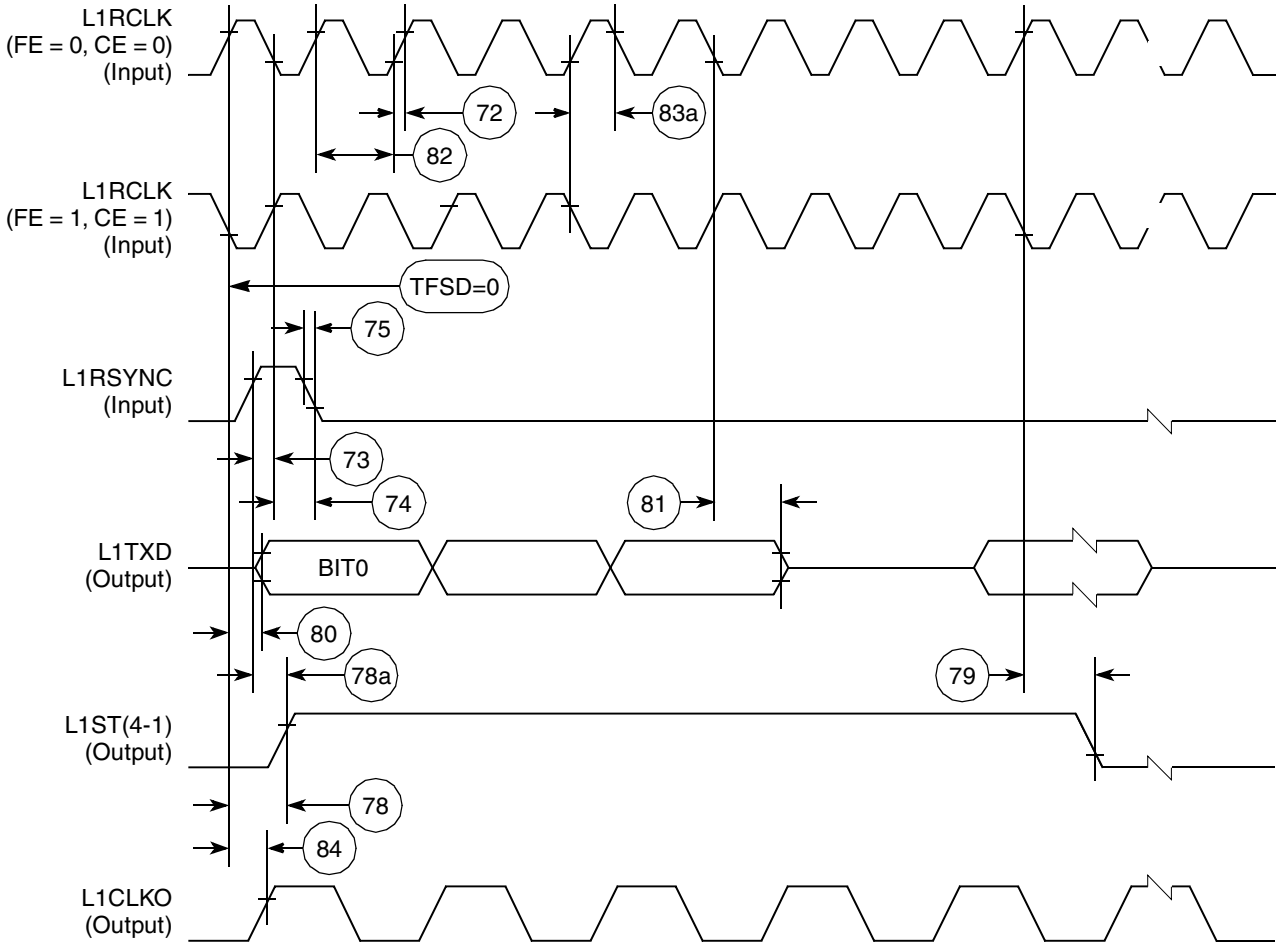

Figure 57. SI Transmit Timing with Double Speed Clocking (DSC = 1)

12.7 SCC in NMSI Mode Electrical Specifications

Table 22 provides the NMSI external clock timing.

Table 22. NMSI External Clock Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
100	RCLK1 and TCLK1 width high[1]	1/SYNCCLK	—	ns
101	RCLK1 and TCLK1 width low	1/SYNCCLK + 5	—	ns
102	RCLK1 and TCLK1 rise/fall time	—	15.00	ns
103	TXD1 active delay (from TCLK1 falling edge)	0.00	50.00	ns
104	$\overline{\text{RTS1}}$ active/inactive delay (from TCLK1 falling edge)	0.00	50.00	ns
105	$\overline{\text{CTS1}}$ setup time to TCLK1 rising edge	5.00	—	ns
106	RXD1 setup time to RCLK1 rising edge	5.00	—	ns
107	RXD1 hold time from RCLK1 rising edge[2]	5.00	—	ns
108	$\overline{\text{CD1}}$ setup time to RCLK1 rising edge	5.00	—	ns

1 The ratios SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater than or equal to 2.25/1.
2 Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as external sync signals.

Table 23 provides the NMSI internal clock timing.

Table 23. NMSI Internal Clock Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
100	RCLK1 and TCLK1 frequency[1]	0.00	SYNCCLK/3	MHz
102	RCLK1 and TCLK1 rise/fall time	—	—	ns
103	TXD1 active delay (from TCLK1 falling edge)	0.00	30.00	ns
104	$\overline{\text{RTS1}}$ active/inactive delay (from TCLK1 falling edge)	0.00	30.00	ns
105	$\overline{\text{CTS1}}$ setup time to TCLK1 rising edge	40.00	—	ns
106	RXD1 setup time to RCLK1 rising edge	40.00	—	ns
107	RXD1 hold time from RCLK1 rising edge[2]	0.00	—	ns
108	$\overline{\text{CD1}}$ setup time to RCLK1 rising edge	40.00	—	ns

1 The ratios SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater than or equal to 3/1.
2 Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as external sync signals

Table 24. Ethernet Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
134	TENA inactive delay (from TCLK1 rising edge)	10	50	ns
138	CLKO1 low to $\overline{\text{SDACK}}$ asserted[2]	—	20	ns
139	CLKO1 low to $\overline{\text{SDACK}}$ negated [2]	—	20	ns

[1] The ratios SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater than or equal to 2/1.
[2] $\overline{\text{SDACK}}$ is asserted whenever the SDMA writes the incoming frame DA into memory.

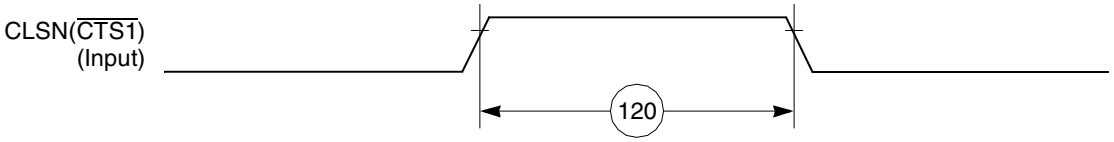

Figure 62. Ethernet Collision Timing Diagram

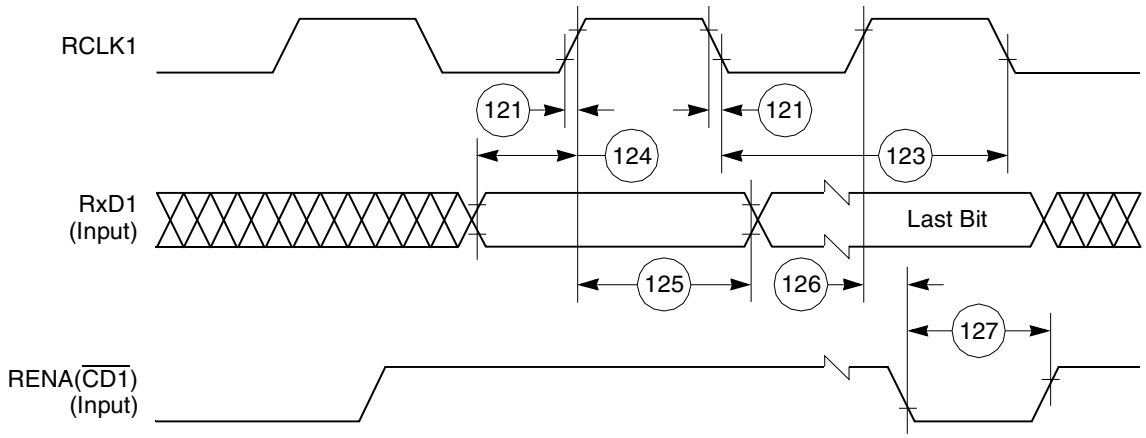

Figure 63. Ethernet Receive Timing Diagram

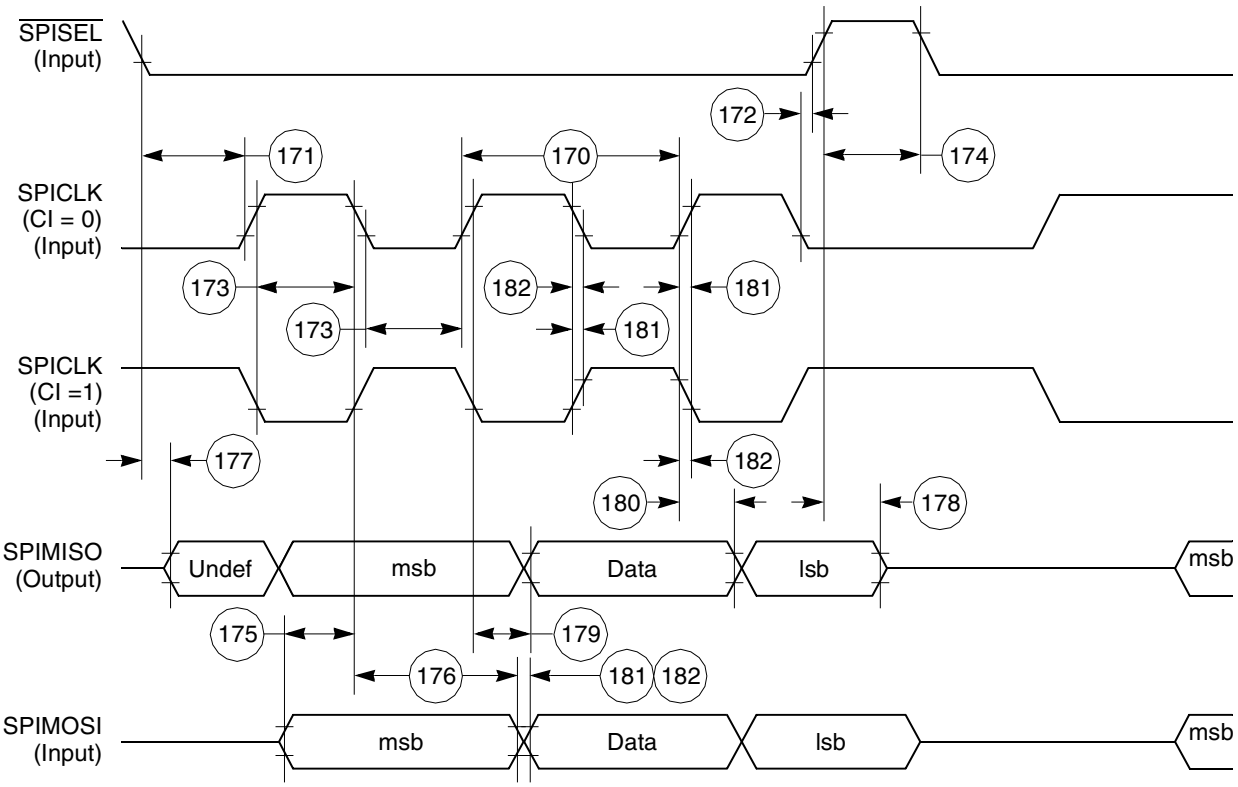

Figure 69. SPI Slave (CP = 1) Timing Diagram

12.12 I²C AC Electrical Specifications

Table 28 provides the I²C (SCL < 100 kHz) timings.

Table 28. I²C Timing (SCL < 100 kHz)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
200	SCL clock frequency (slave)	0	100	kHz
200	SCL clock frequency (master)[1]	1.5	100	kHz
202	Bus free time between transmissions	4.7	—	µs
203	Low period of SCL	4.7	—	µs
204	High period of SCL	4.0	—	µs
205	Start condition setup time	4.7	—	µs
206	Start condition hold time	4.0	—	µs
207	Data hold time	0	—	µs
208	Data setup time	250	—	ns
209	SDL/SCL rise time	—	1	µs

Figure 71 shows signal timings during UTOPIA receive operations.

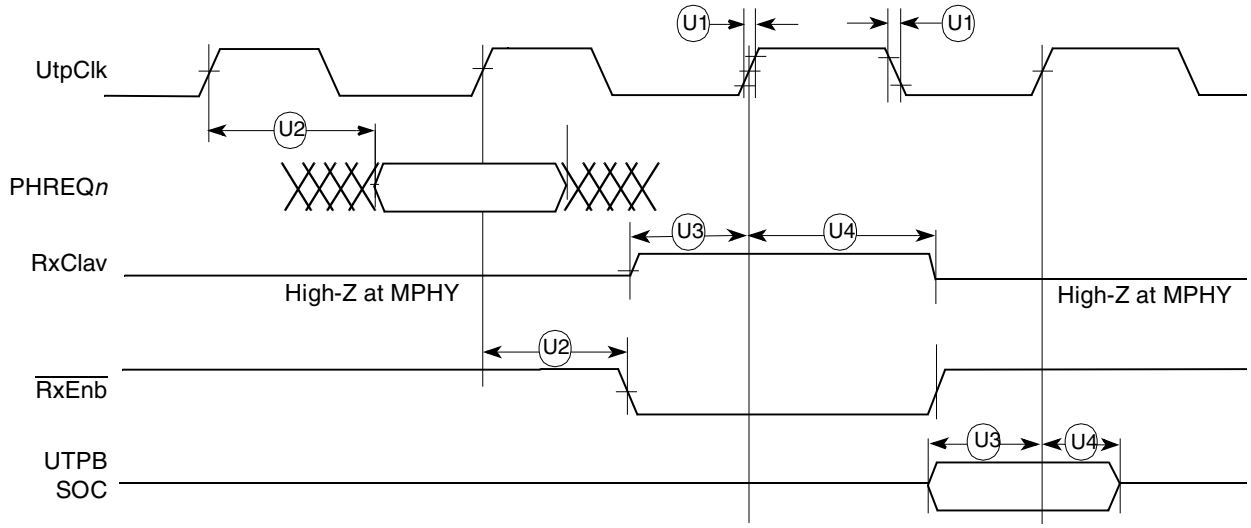

Figure 71. UTOPIA Receive Timing

Figure 72 shows signal timings during UTOPIA transmit operations.

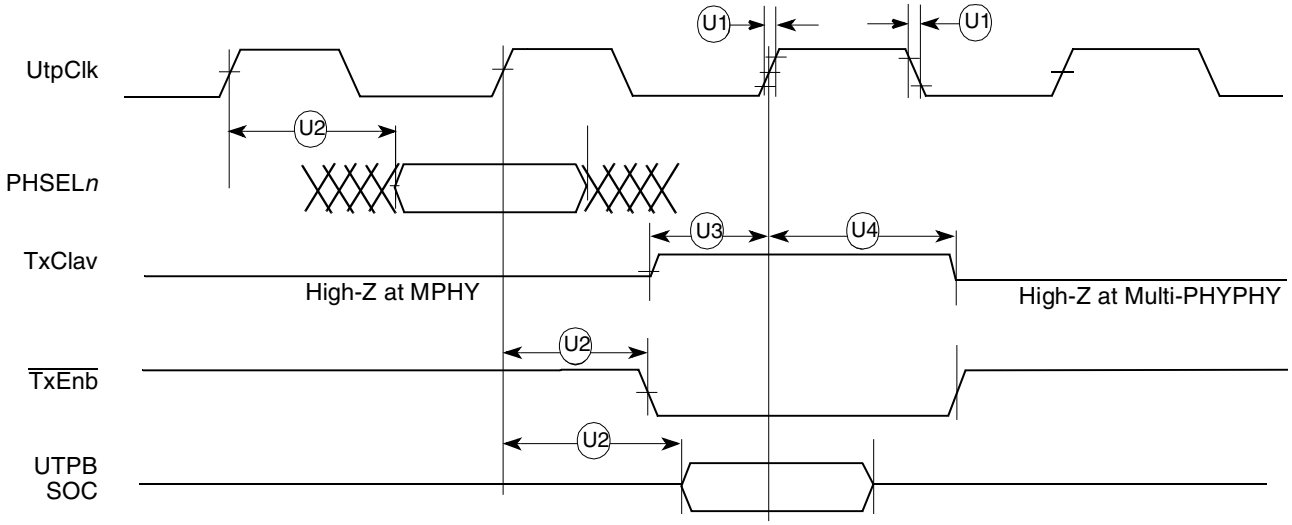

Figure 72. UTOPIA Transmit Timing

Table 39. Pin Assignments (continued)

Name	Pin Number	Type
WE0, BS_B0, IORD	B18	Output
WE1, BS_B1, IOWR	E16	Output
WE2, BS_B2, PCOE	C17	Output
WE3, BS_B3, PCWE	B19	Output
BS_A[0:3]	D17, C18, C19, F16	Output
GPL_A0, GPL_B0	B17	Output
OE, GPL_A1, GPL_B1	A18	Output
GPL_A[2:3], GPL_B[2:3], CS[2:3]	D16, A17	Output
UPWAITA, GPL_A4	B13	Bidirectional
UPWAITB, GPL_B4	A14	Bidirectional
GPL_A5	C13	Output
PORESET	B3	Input
RSTCONF	D4	Input
HRESET	B4	Open-drain
SRESET	A3	Open-drain
XTAL	A4	Analog output
EXTAL	D5	Analog input (3.3 V only)
CLKOUT	G4	Output
EXTCLK	A5	Input (3.3 V only)
TEXP	C4	Output
ALE_A	B7	Output
CE1_A	B15	Output
CE2_A	C15	Output
WAIT_A, SOC_Split[1]	A2	Input
WAIT_B	C3	Input
IP_A0, UTPB_Split0[1]	B1	Input
IP_A1, UTPB_Split1[1]	C1	Input
IP_A2, IOIS16_A, UTPB_Split2[1]	F4	Input
IP_A3, UTPB_Split3[1]	E3	Input
IP_A4, UTPB_Split4[1]	D2	Input
IP_A5, UTPB_Split5[1]	D1	Input
IP_A6, UTPB_Split6[1]	E2	Input
IP_A7, UTPB_Split7[1]	D3	Input

Table 39. Pin Assignments (continued)

Name	Pin Number	Type
PD5, CLK8, L1TCLKB, UTPB6	V6	Bidirectional
PD4, CLK4, UTPB7	W4	Bidirectional
PD3, CLK7, TIN4, SOC	T9	Bidirectional
PE31, CLK8, L1TCLKB, MII1-RXCLK	U9	Bidirectional (Optional: open-drain)
PE30, L1RXDB, MII1-RXD2	W7	Bidirectional (Optional: open-drain)
PE29, MII2-CRS	T8	Bidirectional (Optional: open-drain)
PE28, $\overline{\text{TOUT3}}$, MII2-COL	V5	Bidirectional (Optional: open-drain)
PE27, $\overline{\text{RTS3}}$, L1RQB, MII2-RXER, RMII2-RXER	V4	Bidirectional (Optional: open-drain)
PE26, L1CLKOB, MII2-RXDV, RMII2-CRS_DV	T1	Bidirectional (Optional: open-drain)
PE25, RXD4, MII2-RXD3, L1ST2	T3	Bidirectional (Optional: open-drain)
PE24, SMRXD1, BRGO1, MII2-RXD2	V8	Bidirectional (Optional: open-drain)
PE23, $\overline{\text{SMSYN2}}$, TXD4, MII2-RXCLK, L1ST1	V2	Bidirectional (Optional: open-drain)
PE22, $\overline{\text{TOUT2}}$, MII2-RXD1, RMII2-RXD1, $\overline{\text{SDACK1}}$	V1	Bidirectional (Optional: open-drain)
PE21, SMRXD2, $\overline{\text{TOUT1}}$, MII2-RXD0, RMII2-RXD0, $\overline{\text{RTS3}}$	V9	Bidirectional (Optional: open-drain)
PE20, L1RSYNCA, SMTXD2, $\overline{\text{CTS3}}$, MII2-TXER	R4	Bidirectional (Optional: open-drain)
PE19, L1TXDB, MII2-TXEN, RMII2-TXEN	T6	Bidirectional (Optional: open-drain)
PE18, L1TSYNCA, SMTXD1, MII2-TXD3	R1	Bidirectional (Optional: open-drain)
PE17, TIN3, CLK5, BRGO3, $\overline{\text{SMSYN1}}$, MII2-TXD2	W8	Bidirectional (Optional: open-drain)
PE16, L1RCLKB, CLK6, TXD3, MII2-TXCLK, RMII2-REFCLK	T7	Bidirectional (Optional: open-drain)
PE15, $\overline{\text{TGATE1}}$, MII2-TXD1, RMII2-TXD1	W6	Bidirectional

Table 39. Pin Assignments (continued)

Name	Pin Number	Type
PE14, RXD3, MII2-TXD0, RMII2-TXD0	V7	Bidirectional
TMS	V18	Input
TDI, DSDI	T16	Input
TCK, DSCK	U17	Input
$\overline{\text{TRST}}$	W18	Input
TDO, DSDO	T17	Output
MII1_CRS	T11	Input
MII_MDIO	P19	Bidirectional
MII1_TXEN, RMII1_TXEN	T5	Output
MII1_COL	U12	Input
V_{SSSYN1}	C2	PLL analog V_{DD} and GND
V_{SSSYN}	E4	Power
V_{DDLSYN}	B2	Power
GND	G6, G7, G8, G9, G10, G11, G12, G13, H7, H8, H9, H10, H11, H12, H13, H14, J7, J8, J9, J10, J11, J12, J13, K7, K8, K9, K10, K11, K12, K13, L7, L8, L9, L10, L11, L12, L13, M7, M8, M9, M10, M11, M12, M13, N7, N8, N9, N10, N11, N12, N13, N14, P7, P13, R16	Power
V_{DDL}	E5, E6, E9, E11, E14, G15, H5, J5, J15, K15, L5, M15, N5, R6, R9, R10, R12, R15	Power
V_{DDH}	E7, E8, E10, E12, E13, E15, F5, F6, F7, F8, F9, F10, F11, F12, F13, F14, F15, G5, G14, H6, H15, J6, J14, K5, K6, K14, L6, L14, L15, M5, M6, M14, N6, N15, P5, P6, P8, P9, P10, P11, P12, P14, P15, R5, R7, R8, R11, R13, R14	Power
N/C	N17	No connect

[1] ESAR mode only.

17 Document Revision History

Table 40 lists significant changes between revisions of this hardware specification.

Table 40. Document Revision History

Revision Number	Date	Changes
7	07/2010	In Table 9, "Bus Operation Timings," changed the following: • Updated TRLX condition value for B22a/b/c to "TRLX = [0 or 1]" • Removed TRLX condition for B23 • Updated condition and equation for B30 to "Invalid GPCM read/write access (MIN = 0.25 × B1 – 2.00)" • Updated note 8 to "The timing B30 refers to $\overline{CS}$ when ACS = 00 and to $\overline{CS}$ and $\overline{WE}$(0:3) when CSNT = 0."
6	05/2010	Added minimum load for CLKOUT in Section 10, "Bus Signal Timing."
5	03/2009	Updated formatting of Table 12 , "PCMCIA Port Timing," Table 13, "Debug Port Timing," Table 14, "Reset Timing," and Table 15, "JTAG Timing."
4	08/2007	• On page 1, updated first paragraph and added a second paragraph. • After Table 2, inserted a new figure showing the undershoot/overshoot voltage (Figure 3) and renumbered the rest of the figures. • In Table 9, for reset timings B29f and B29g added footnote indicating that the formula only applies to bus operation up to 50 MHz. • In Figure 6, changed all reference voltage measurement points from 0.2 and 0.8 V to 50% level. • In Table 18, changed num 46 description to read, "$\overline{TA}$ assertion to rising edge ..." • In Figure 49, changed $\overline{TA}$ to reflect the rising edge of the clock.
3.0	7/22/2004	• Added sentence to Spec B1A about EXTCLK and CLKOUT being in Alignment for Integer Values • Added a footnote to Spec 41 specifying that EDM = 1 • Added RMII1_EN under M1II_EN in Table 36 Pin Assignments • Added a tablefootnote to Table 6 DC Electrical Specifications about meeting the VIL Max of the I2C Standard • Put the new part numbers in the Ordering Information Section
2.0	12/2003	• Changed the maximum operating frequency to 133 MHz. • Put in the orderable part numbers that are orderable. • Put the timing in the 80 MHz column. • Rounded the timings to hundredths in the 80 MHz column. • Put the pin numbers in footnotes by the maximum currents in Table 6. • Changed 22 and 41 in the Timing. • Put in the Thermal numbers.
1.0	9/2003	• Added the DSP information in the Features list • Fixed table formatting. • Nontechnical edits. • Released to the external web.
0.9	8/2003	Changed the USB description to full-/low-speed compatible.
0.8	8/2003	Added the Reference to USB 2.0 to the Features list and removed 1.1 from USB on the block diagrams.
0.7	7/2003	Added the RxClav and TxClav signals to PC15.
0.6	6/2003	Changed the pin descriptions per the June 22 spec.
0.5	5/2003	Changed some more typos, put in the phsel and phreq pins. Corrected the USB timing.