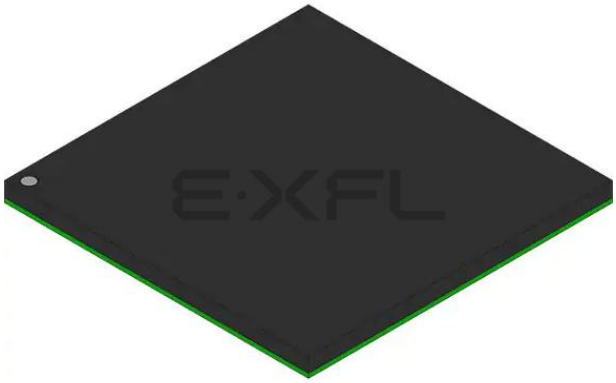

Welcome to E-XFL.COM

## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | MPC8xx |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 133MHz |
| Co-Processors/DSP | Communications; CPM |
| RAM Controllers | DRAM |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10Mbps (2), 10/100Mbps (2) |
| SATA | - |
| USB | USB 2.0 (1) |
| Voltage - I/O | 3.3V |
| Operating Temperature | -40°C ~ 100°C (TA) |
| Security Features | - |
| Package / Case | 357-BBGA |
| Supplier Device Package | 357-PBGA (25x25) |
| Purchase URL | https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc880cvr133 |

- Provides enhanced ATM functionality found on the MPC862 and MPC866 families and includes the following:
  - Improved operation, administration and maintenance (OAM) support
  - OAM performance monitoring (PM) support
  - Multiple APC priority levels available to support a range of traffic pace requirements
  - Port-to-port switching capability without the need for RAM-based microcode
  - Simultaneous MII (100BaseT) and UTOPIA (half- or full -duplex) capability
  - Optional statistical cell counters per PHY
  - UTOPIA L2-compliant interface with added FIFO buffering to reduce the total cell transmission time and multi-PHY support. (The earlier UTOPIA L1 specification is also supported.)
  - Parameter RAM for both SPI and $I^2C$ can be relocated without RAM-based microcode
  - Supports full-duplex UTOPIA master (ATM side) and slave (PHY side) operations using a split bus
  - AAL2/VBR functionality is ROM-resident
- Up to 32-bit data bus (dynamic bus sizing for 8, 16, and 32 bits)
- Thirty-two address lines
- Memory controller (eight banks)
  - Contains complete dynamic RAM (DRAM) controller
  - Each bank can be a chip select or $\overline{\text{RAS}}$ to support a DRAM bank
  - Up to 30 wait states programmable per memory bank
  - Glueless interface to DRAM, SIMMS, SRAM, EPROMs, Flash EPROMs, and other memory devices
  - DRAM controller programmable to support most size and speed memory interfaces
  - Four $\overline{\text{CAS}}$ lines, four $\overline{\text{WE}}$ lines, and one $\overline{\text{OE}}$ line
  - Boot chip-select available at reset (options for 8-, 16-, or 32-bit memory)
  - Variable block sizes (32 Kbytes–256 Mbytes)
  - Selectable write protection
  - On-chip bus arbitration logic
- General-purpose timers
  - Four 16-bit timers or two 32-bit timers
  - Gate mode can enable/disable counting.
  - Interrupt can be masked on reference match and event capture
- Two fast Ethernet controllers (FEC)—Two 10/100 Mbps Ethernet/IEEE Std. 802.3™ CDMA/CS that interface through MII and/or RMII interfaces
- System integration unit (SIU)
  - Bus monitor
  - Software watchdog

The MPC880 block diagram is shown in Figure 2.

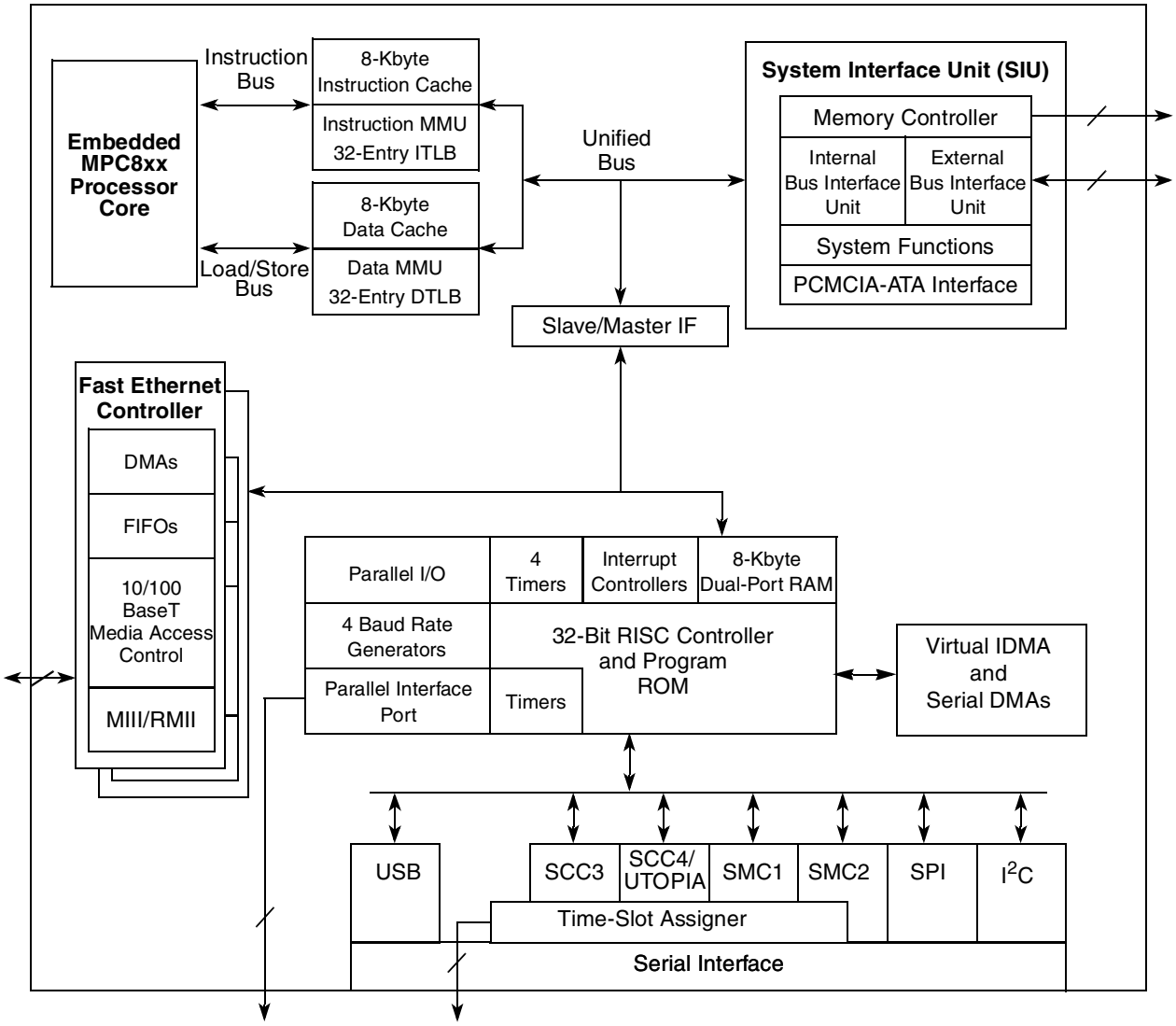


**Figure 2. MPC880 Block Diagram**

Figure 6 provides the control timing diagram.

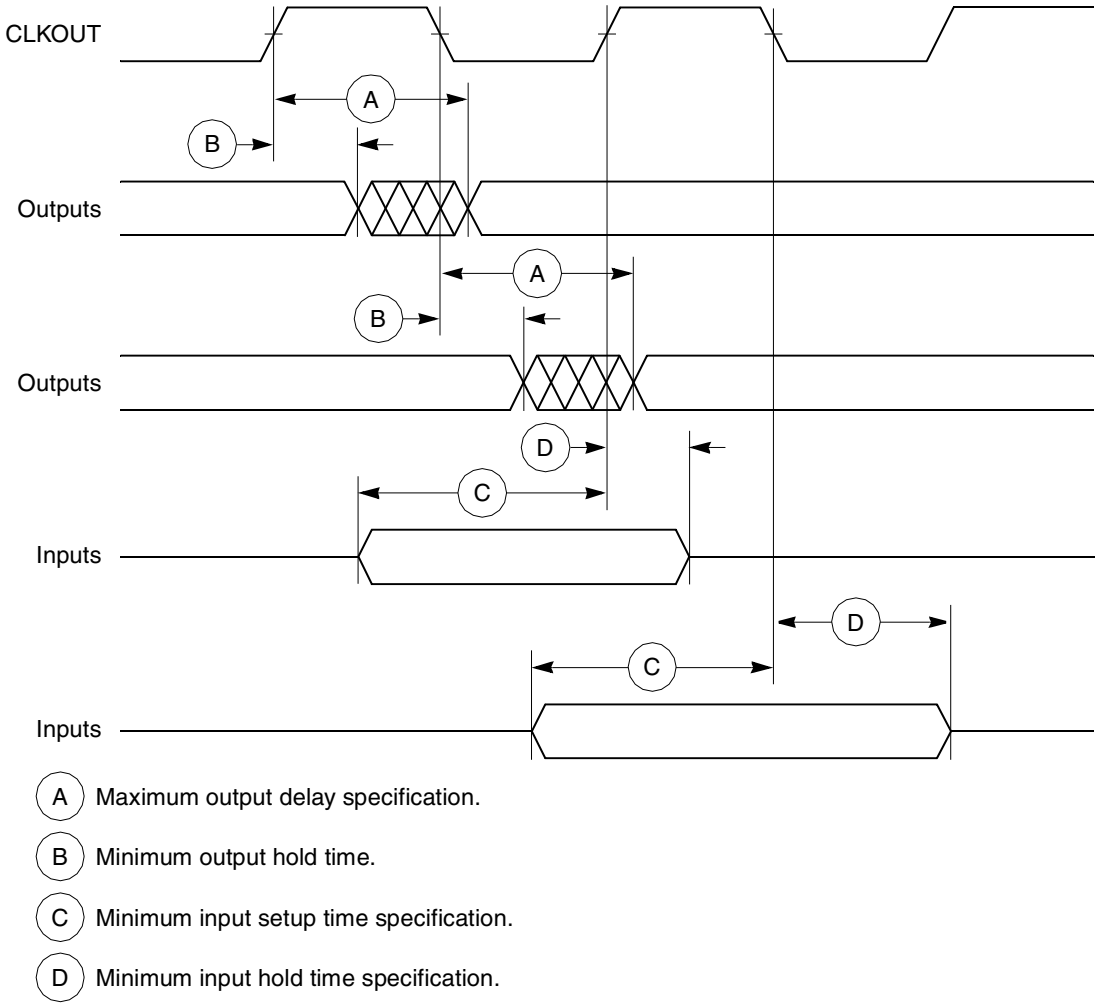


**Figure 6. Control Timing**

Figure 7 provides the timing for the external clock.

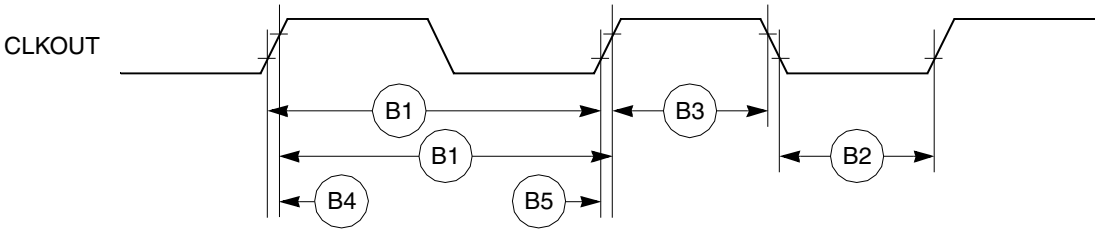


**Figure 7. External Clock Timing**

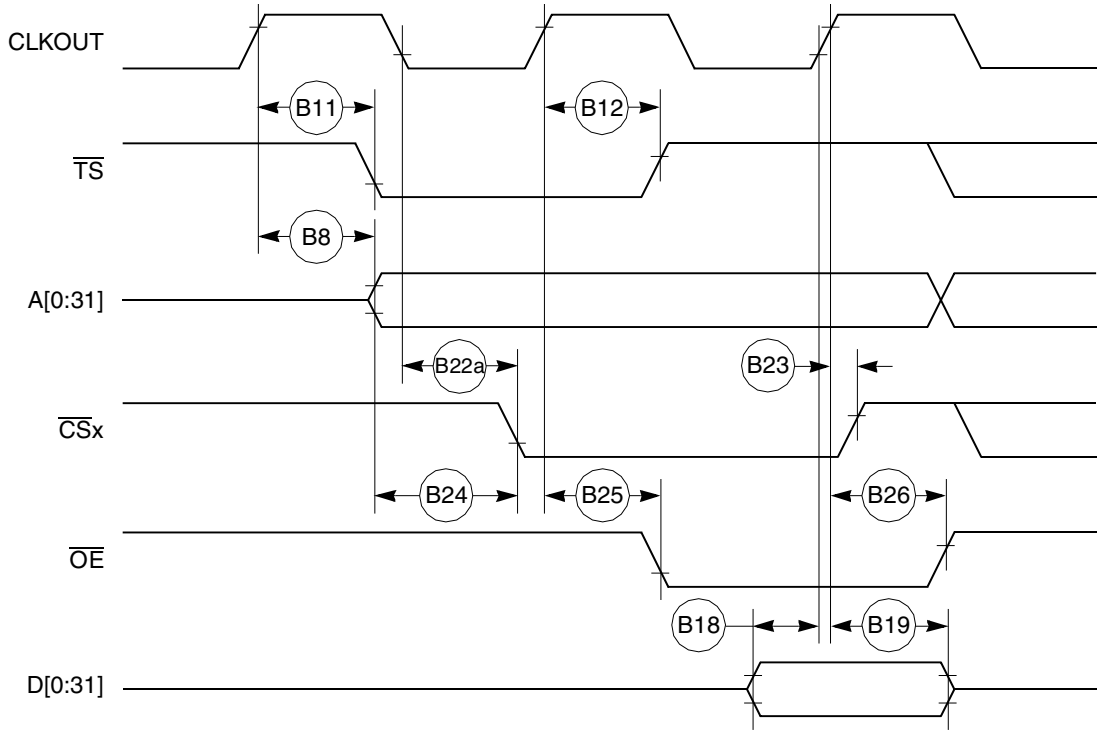


**Figure 14. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 10)**

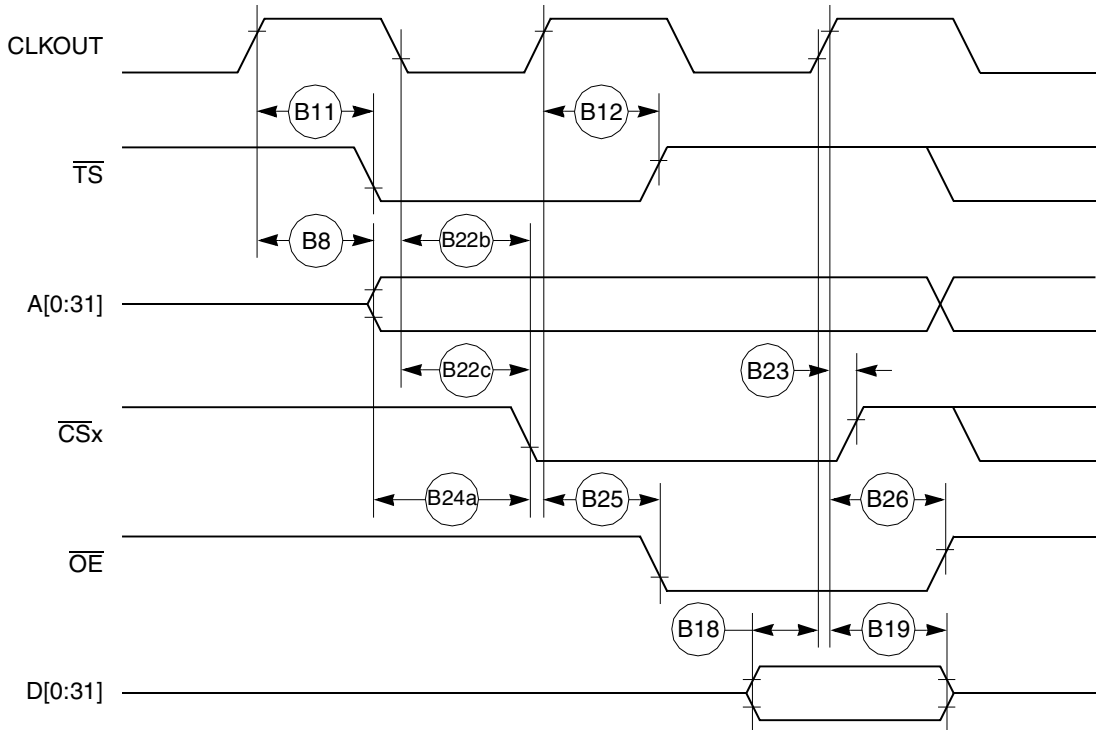


**Figure 15. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 11)**

Figure 17 through Figure 19 provide the timing for the external bus write controlled by various GPCM factors.

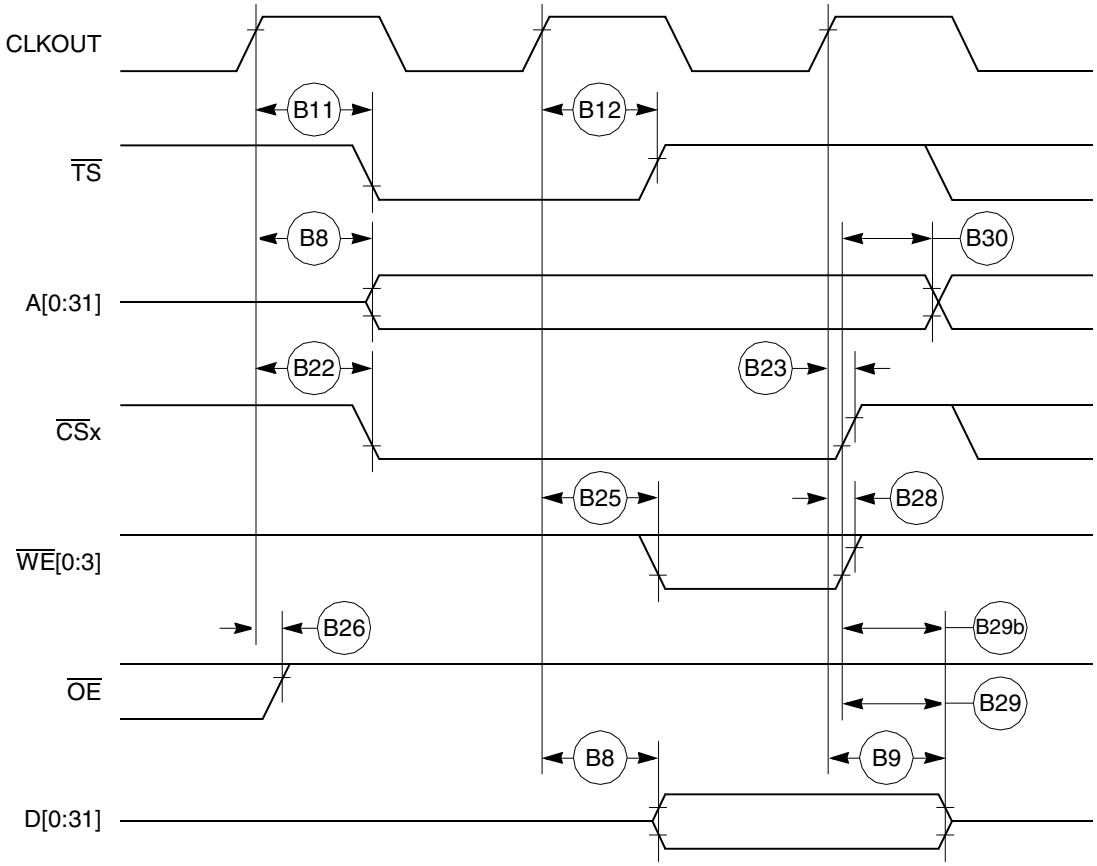


**Figure 17. External Bus Write Timing (GPCM Controlled—TRLX = 0, CSNT = 0)**

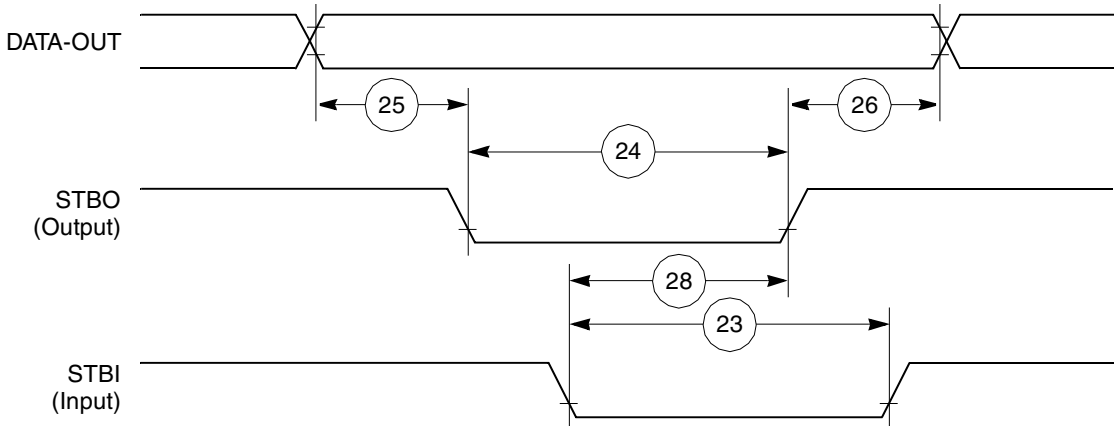


**Figure 43. PIP Tx (Interlock Mode) Timing Diagram**

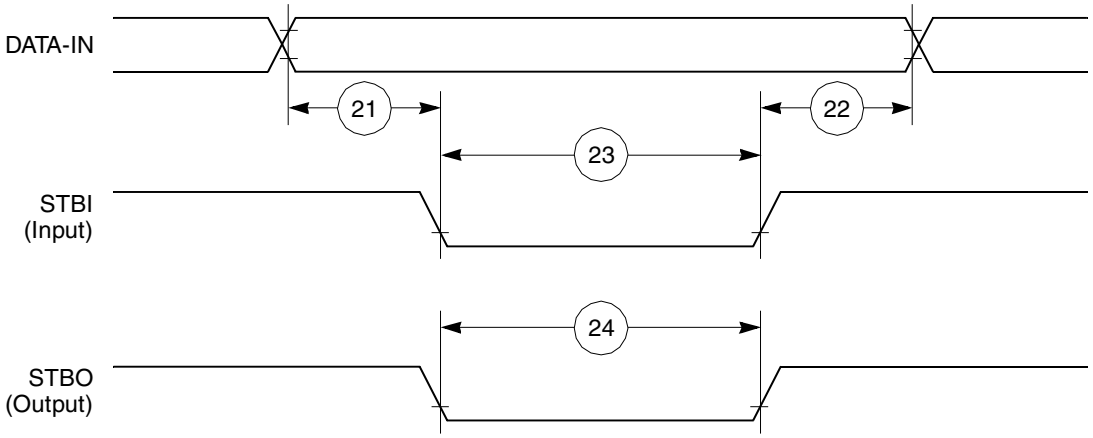


**Figure 44. PIP Rx (Pulse Mode) Timing Diagram**

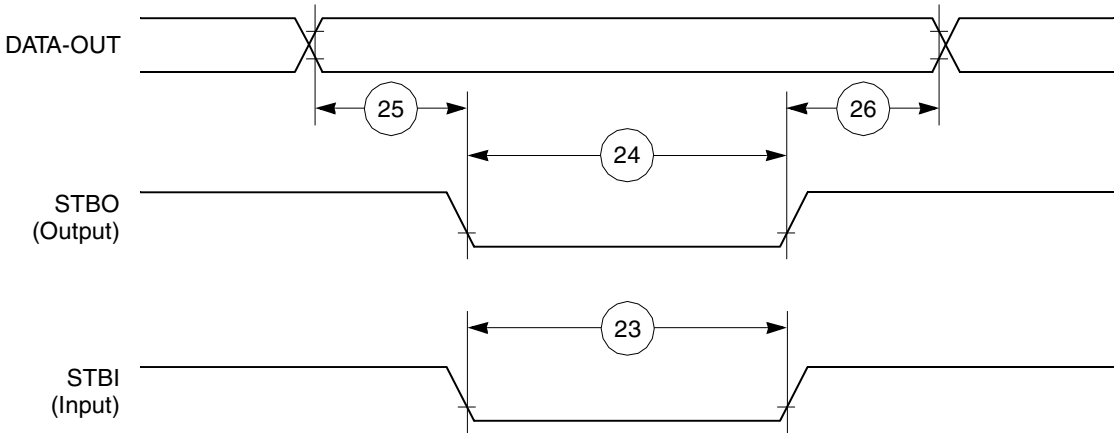


**Figure 45. PIP TX (Pulse Mode) Timing Diagram**

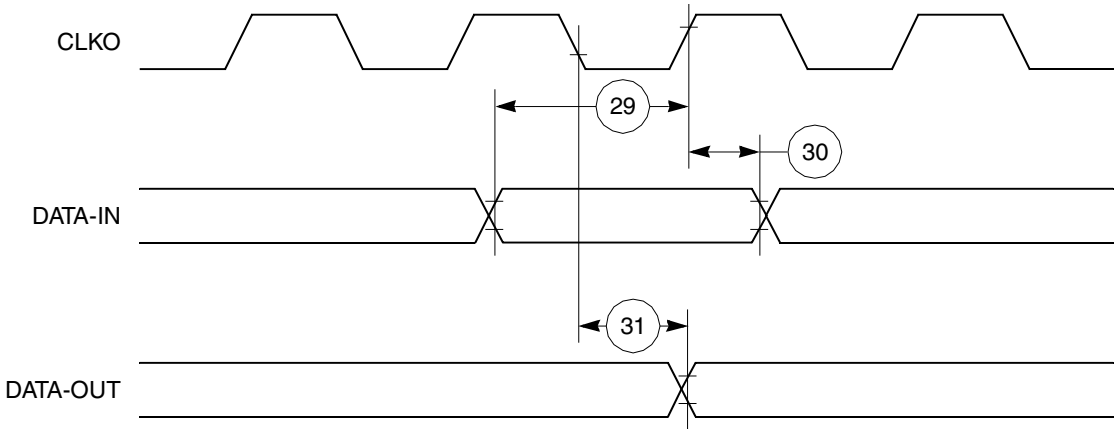


**Figure 46. Parallel I/O Data-In/Data-Out Timing Diagram**

## 12.2 Port C Interrupt AC Electrical Specifications

Table 17 provides the timings for port C interrupts.

**Table 17. Port C Interrupt Timing**

| Num | Characteristic | 33.34 MHz | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 35 | Port C interrupt pulse width low (edge-triggered mode) | 55 | — | ns |
| 36 | Port C interrupt minimum time between active edges | 55 | — | ns |

Figure 47 shows the port C interrupt detection timing.

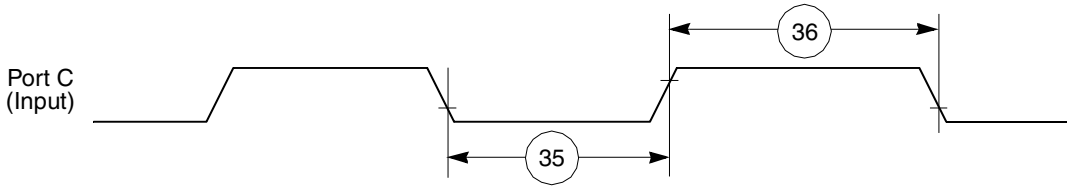


**Figure 47. Port C Interrupt Detection Timing**

**Table 21. SI Timing (continued)**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 76 | L1RXD valid to L1CLK edge (L1RXD setup time) | 17.00 | — | ns |
| 77 | L1CLK edge to L1RXD invalid (L1RXD hold time) | 13.00 | — | ns |
| 78 | L1CLK edge to L1ST(1–4) valid[4] | 10.00 | 45.00 | ns |
| 78A | L1SYNC valid to L1ST(1–4) valid | 10.00 | 45.00 | ns |
| 79 | L1CLK edge to L1ST(1–4) invalid | 10.00 | 45.00 | ns |
| 80 | L1CLK edge to L1TXD valid | 10.00 | 55.00 | ns |
| 80A | L1TSYNC valid to L1TXD valid[4] | 10.00 | 55.00 | ns |
| 81 | L1CLK edge to L1TXD high impedance | 0.00 | 42.00 | ns |
| 82 | L1RCLK, L1TCLK frequency (DSC =1) | — | 16.00 or SYNCCLK/2 | MHz |
| 83 | L1RCLK, L1TCLK width low (DSC =1) | P + 10 | — | ns |
| 83a | L1RCLK, L1TCLK width high (DSC = 1)[3] | P + 10 | — | ns |
| 84 | L1CLK edge to L1CLKO valid (DSC = 1) | — | 30.00 | ns |
| 85 | $\overline{\text{L1RQ}}$ valid before falling edge of L1TSYNC[4] | 1.00 | — | L1TCLK |
| 86 | L1GR setup time[2] | 42.00 | — | ns |
| 87 | L1GR hold time | 42.00 | — | ns |
| 88 | L1CLK edge to L1SYNC valid (FSD = 00) CNT = 0000, BYT = 0, DSC = 0) | — | 0.00 | ns |

1 The ratio SyncCLK/L1RCLK must be greater than 2.5/1.
2 These specs are valid for IDL mode only.
3 Where P = 1/CLKOUT. Thus for a 25-MHz CLKO1 rate, P = 40 ns.
4 These strobes and TxD on the first bit of the frame become valid after L1CLK edge or L1SYNC, whichever comes later.

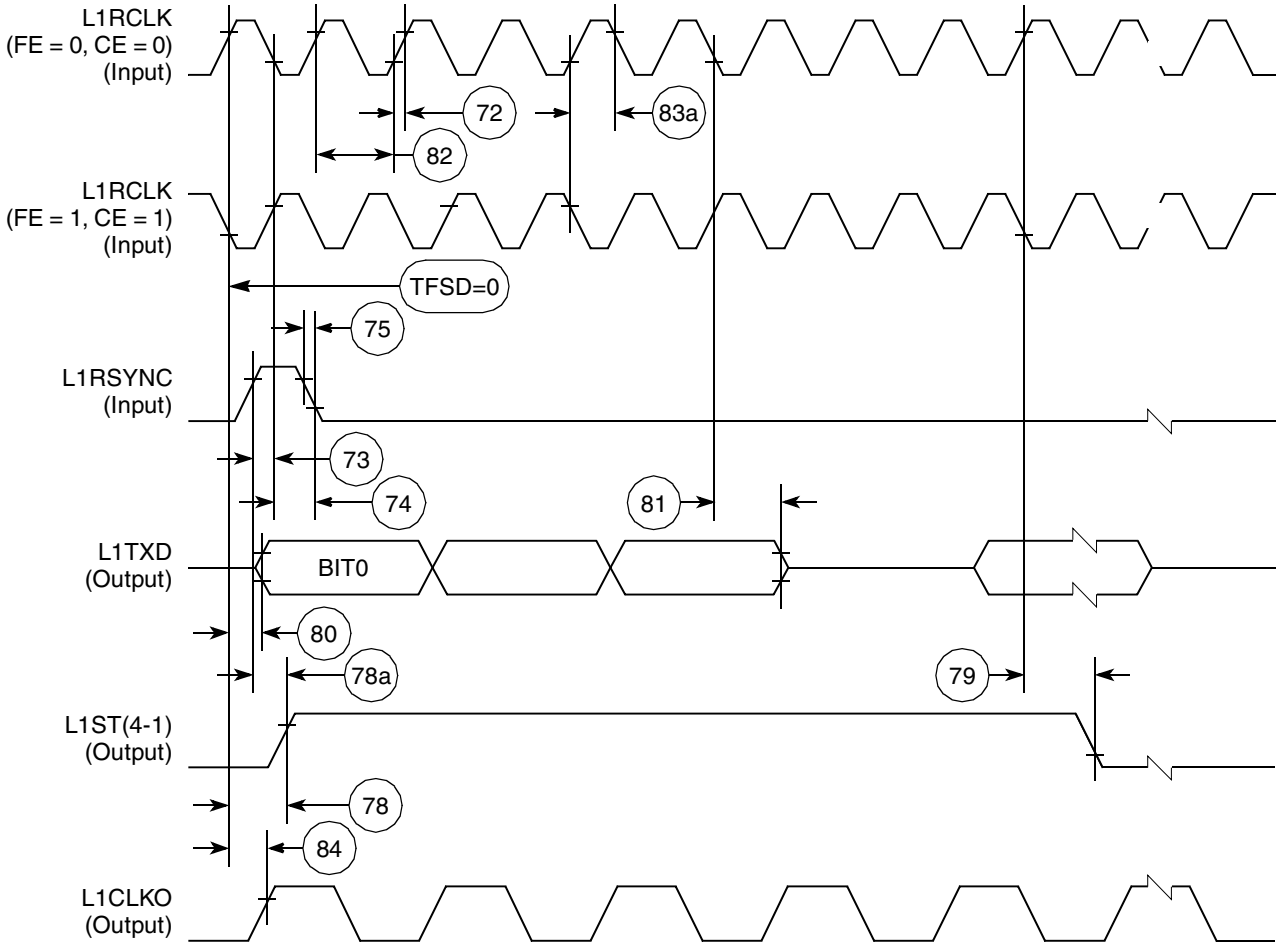


**Figure 57. SI Transmit Timing with Double Speed Clocking (DSC = 1)**

## 12.7 SCC in NMSI Mode Electrical Specifications

Table 22 provides the NMSI external clock timing.

**Table 22. NMSI External Clock Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 100 | RCLK1 and TCLK1 width high[1] | 1/SYNCCLK | — | ns |
| 101 | RCLK1 and TCLK1 width low | 1/SYNCCLK + 5 | — | ns |
| 102 | RCLK1 and TCLK1 rise/fall time | — | 15.00 | ns |
| 103 | TXD1 active delay (from TCLK1 falling edge) | 0.00 | 50.00 | ns |
| 104 | $\overline{\text{RTS1}}$ active/inactive delay (from TCLK1 falling edge) | 0.00 | 50.00 | ns |
| 105 | $\overline{\text{CTS1}}$ setup time to TCLK1 rising edge | 5.00 | — | ns |
| 106 | RXD1 setup time to RCLK1 rising edge | 5.00 | — | ns |
| 107 | RXD1 hold time from RCLK1 rising edge[2] | 5.00 | — | ns |
| 108 | $\overline{\text{CD1}}$ setup time to RCLK1 rising edge | 5.00 | — | ns |

1 The ratios SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater than or equal to 2.25/1.
2 Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as external sync signals.

Table 23 provides the NMSI internal clock timing.

**Table 23. NMSI Internal Clock Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 100 | RCLK1 and TCLK1 frequency[1] | 0.00 | SYNCCLK/3 | MHz |
| 102 | RCLK1 and TCLK1 rise/fall time | — | — | ns |
| 103 | TXD1 active delay (from TCLK1 falling edge) | 0.00 | 30.00 | ns |
| 104 | $\overline{\text{RTS1}}$ active/inactive delay (from TCLK1 falling edge) | 0.00 | 30.00 | ns |
| 105 | $\overline{\text{CTS1}}$ setup time to TCLK1 rising edge | 40.00 | — | ns |
| 106 | RXD1 setup time to RCLK1 rising edge | 40.00 | — | ns |
| 107 | RXD1 hold time from RCLK1 rising edge[2] | 0.00 | — | ns |
| 108 | $\overline{\text{CD1}}$ setup time to RCLK1 rising edge | 40.00 | — | ns |

1 The ratios SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater than or equal to 3/1.
2 Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as external sync signals

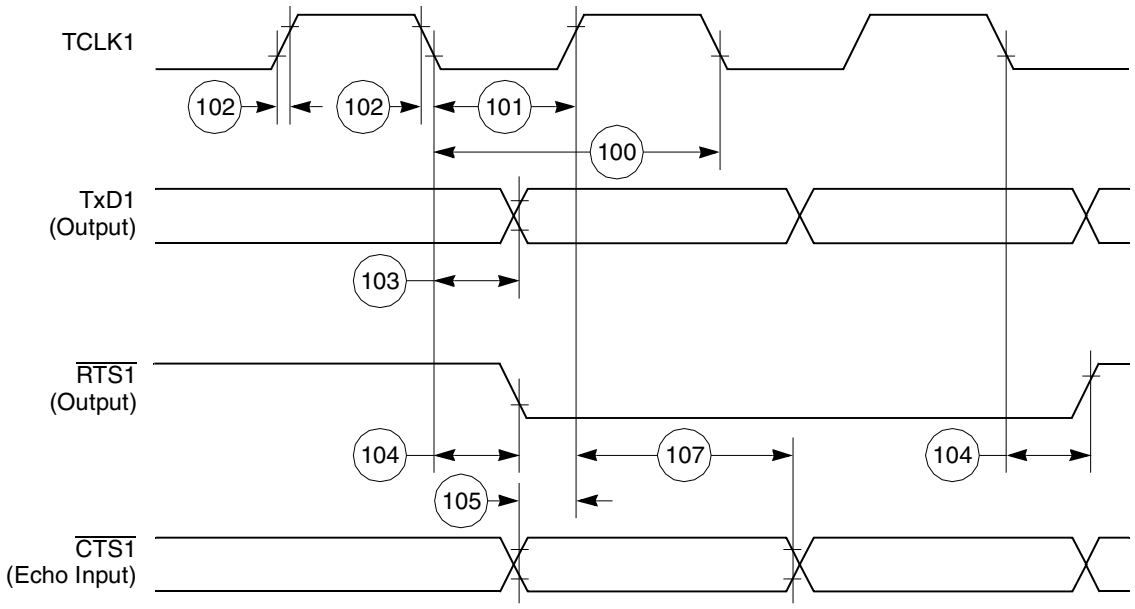


**Figure 61. HDLC Bus Timing Diagram**

## 12.8 Ethernet Electrical Specifications

Table 24 provides the Ethernet timings as shown in Figure 62 through Figure 64.

**Table 24. Ethernet Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 120 | CLSN width high | 40 | — | ns |
| 121 | RCLK1 rise/fall time | — | 15 | ns |
| 122 | RCLK1 width low | 40 | — | ns |
| 123 | RCLK1 clock period[1] | 80 | 120 | ns |
| 124 | RXD1 setup time | 20 | — | ns |
| 125 | RXD1 hold time | 5 | — | ns |
| 126 | RENA active delay (from RCLK1 rising edge of the last data bit) | 10 | — | ns |
| 127 | RENA width low | 100 | — | ns |
| 128 | TCLK1 rise/fall time | — | 15 | ns |
| 129 | TCLK1 width low | 40 | — | ns |
| 130 | TCLK1 clock period[1] | 99 | 101 | ns |
| 131 | TXD1 active delay (from TCLK1 rising edge) | — | 50 | ns |
| 132 | TXD1 inactive delay (from TCLK1 rising edge) | 6.5 | 50 | ns |
| 133 | TENA active delay (from TCLK1 rising edge) | 10 | 50 | ns |

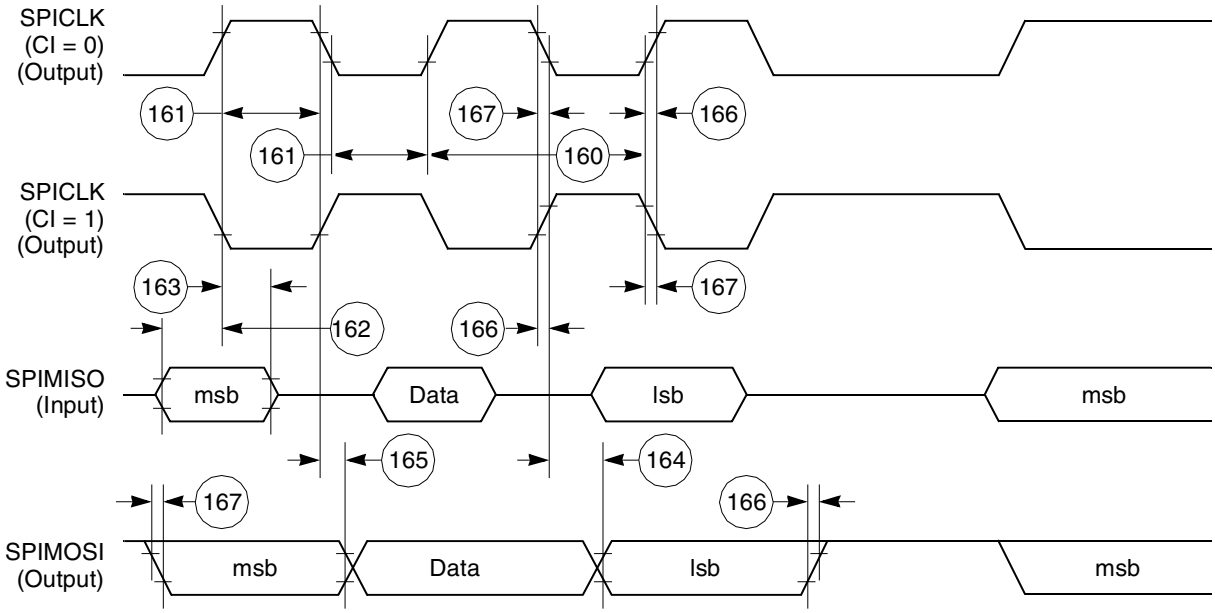


**Figure 66. SPI Master (CP = 0) Timing Diagram**

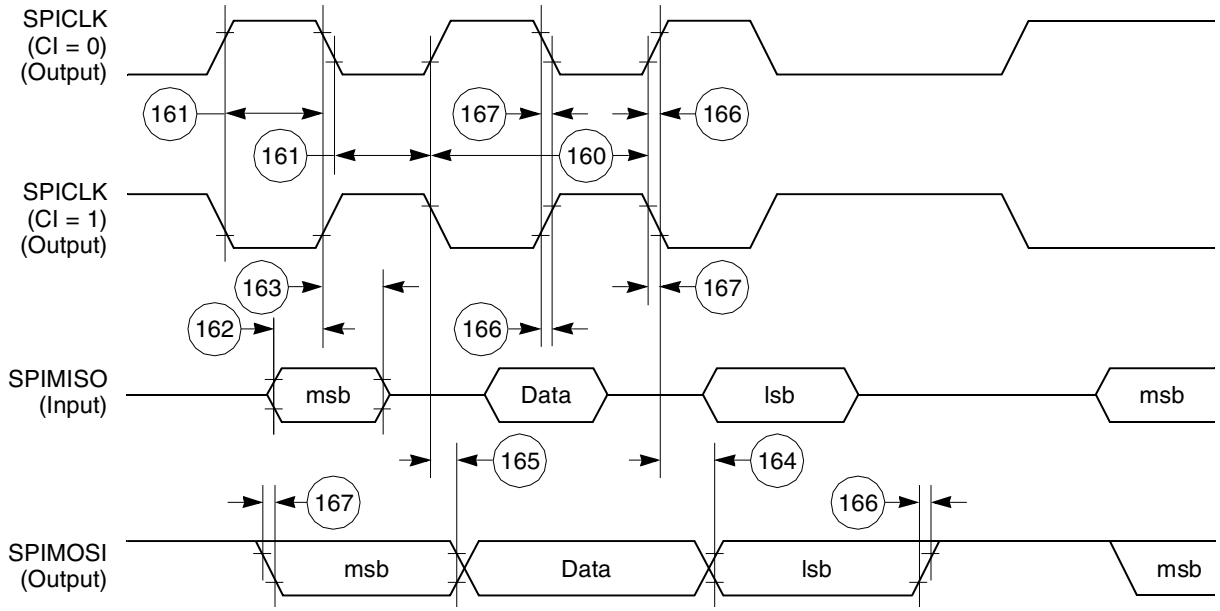


**Figure 67. SPI Master (CP = 1) Timing Diagram**

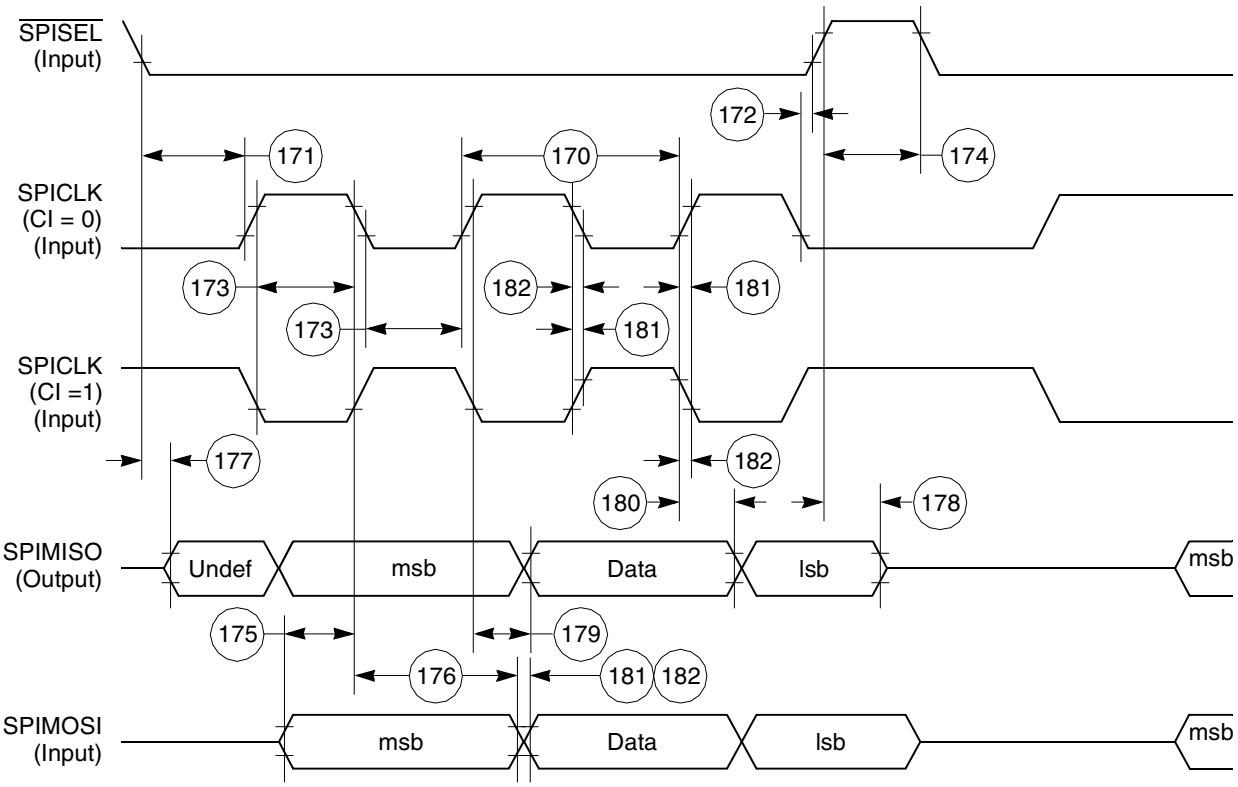


**Figure 69. SPI Slave (CP = 1) Timing Diagram**

## 12.12 I²C AC Electrical Specifications

Table 28 provides the I²C (SCL < 100 kHz) timings.

**Table 28. I²C Timing (SCL < 100 kHz)**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 200 | SCL clock frequency (slave) | 0 | 100 | kHz |
| 200 | SCL clock frequency (master)[1] | 1.5 | 100 | kHz |
| 202 | Bus free time between transmissions | 4.7 | — | µs |
| 203 | Low period of SCL | 4.7 | — | µs |
| 204 | High period of SCL | 4.0 | — | µs |
| 205 | Start condition setup time | 4.7 | — | µs |
| 206 | Start condition hold time | 4.0 | — | µs |
| 207 | Data hold time | 0 | — | µs |
| 208 | Data setup time | 250 | — | ns |
| 209 | SDL/SCL rise time | — | 1 | µs |

# 13 UTOPIA AC Electrical Specifications

Table 30, Table 31, and Table 32, show the AC electrical specifications for the UTOPIA interface.

**Table 30. UTOPIA Master (Muxed Mode) Electrical Specifications**

| Num | Signal Characteristic | Direction | Min | Max | Unit |
|---|---|---|---|---|---|
| U1 | UtpClk rise/fall time (internal clock option) | Output | | 4 | ns |
| | Duty cycle | | 50 | 50 | % |
| | Frequency | | | 33 | MHz |
| U2 | UTPB, SOC, $\overline{\text{RxEnb}}$, $\overline{\text{TxEnb}}$, RxAddr, and TxAddr active delay (PHREQ and PHSEL active delay in multi-PHY mode) | Output | 2 | 16 | ns |
| U3 | UTPB, SOC, Rxclav, and Txclav setup time | Input | 4 | | ns |
| U4 | UTPB, SOC, Rxclav, and Txclav hold time | Input | 1 | | ns |

**Table 31. UTOPIA Master (Split Bus Mode) Electrical Specifications**

| Num | Signal Characteristic | Direction | Min | Max | Unit |
|---|---|---|---|---|---|
| U1 | UtpClk rise/fall time (Internal clock option) | Output | | 4 | ns |
| | Duty cycle | | 50 | 50 | % |
| | Frequency | | | 33 | MHz |
| U2 | UTPB, SOC, $\overline{\text{RxEnb}}$, $\overline{\text{TxEnb}}$, RxAddr, and TxAddr active delay (PHREQ and PHSEL active delay in multi-PHY mode) | Output | 2 | 16 | ns |
| U3 | UTPB_Aux, SOC_Aux, Rxclav, and Txclav setup time | Input | 4 | | ns |
| U4 | UTPB_Aux, SOC_Aux, Rxclav, and Txclav hold time | Input | 1 | | ns |

**Table 32. UTOPIA Slave (Split Bus Mode) Electrical Specifications**

| Num | Signal Characteristic | Direction | Min | Max | Unit |
|---|---|---|---|---|---|
| U1 | UtpClk rise/fall time (external clock option) | Input | | 4 | ns |
| | Duty cycle | | 40 | 60 | % |
| | Frequency | | | 33 | MHz |
| U2 | UTPB, SOC, Rxclav, and Txclav active delay | Output | 2 | 16 | ns |
| U3 | UTPB_AUX, SOC_Aux, $\overline{\text{RxEnb}}$, $\overline{\text{TxEnb}}$, RxAddr, and TxAddr setup time | Input | 4 | | ns |
| U4 | UTPB_AUX, SOC_Aux, $\overline{\text{RxEnb}}$, $\overline{\text{TxEnb}}$, RxAddr, and TxAddr hold time | Input | 1 | | ns |

Figure 71 shows signal timings during UTOPIA receive operations.

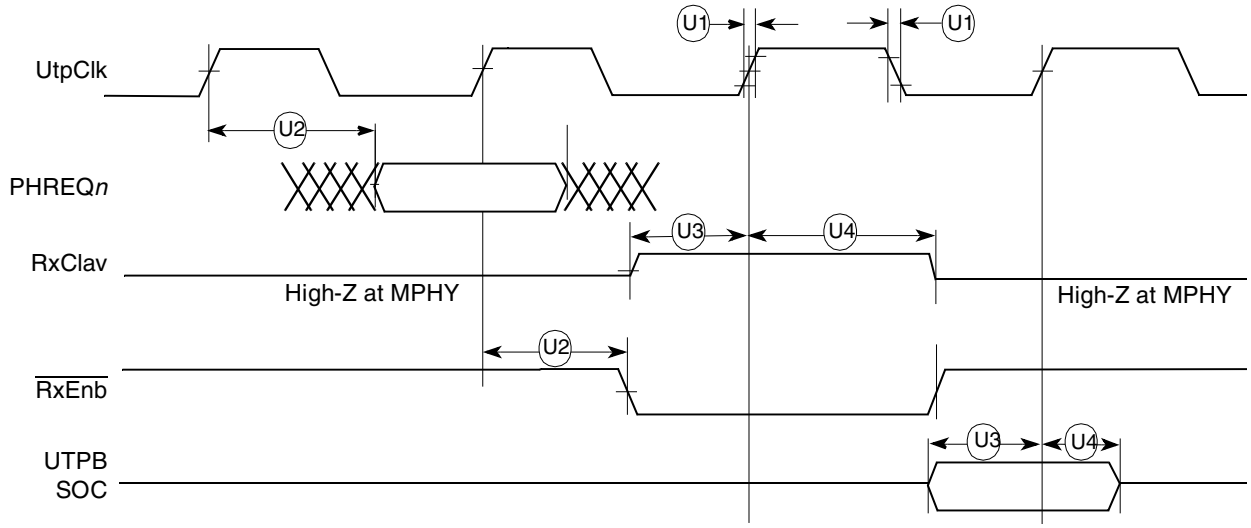


**Figure 71. UTOPIA Receive Timing**

Figure 72 shows signal timings during UTOPIA transmit operations.

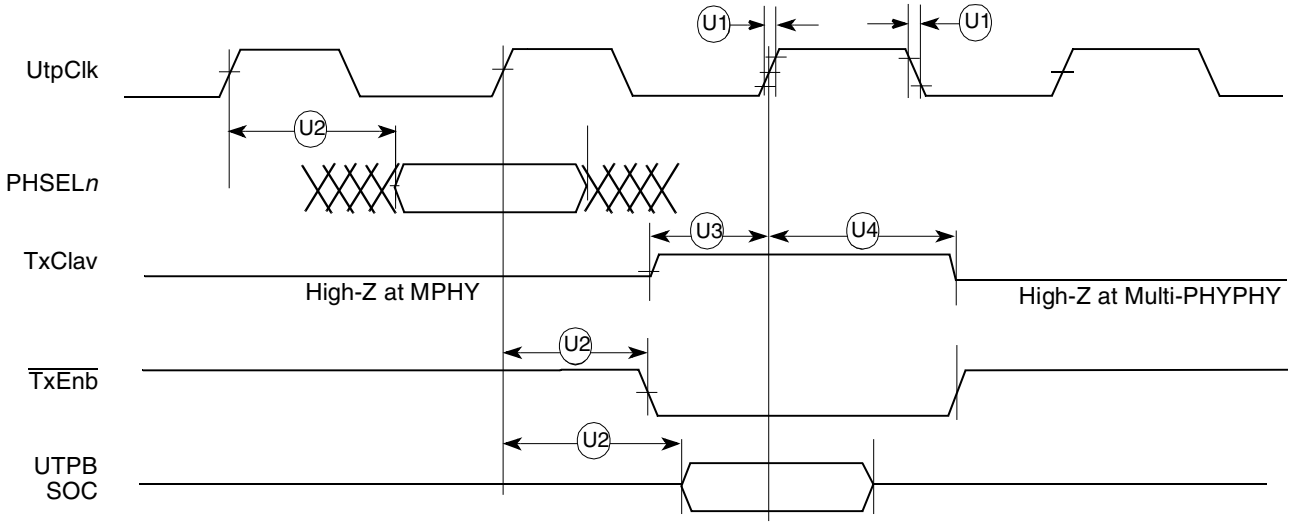


**Figure 72. UTOPIA Transmit Timing**

# 16 Mechanical Data and Ordering Information

Table 38 identifies the available packages and operating frequencies for the MPC885/MPC880 derivative devices.

**Table 38. Available MPC885/MPC880 Packages/Frequencies**

| Package Type | Temperature (Tj) | Frequency (MHz) | Order Number |
|---|---|---|---|
| Plastic ball grid array<br>ZP suffix — Leaded<br>VR suffix — Lead-Free are available as needed | 0°C to 95°C | 66 | KMPC885ZP66<br>KMPC880ZP66<br>MPC885ZP66<br>MPC880ZP66 |
| | | 80 | KMPC885ZP80<br>KMPC880ZP80<br>MPC885ZP80<br>MPC880ZP80 |
| | | 133 | KMPC885ZP133<br>KMPC880ZP133<br>MPC885ZP133<br>MPC880ZP133 |
| Plastic ball grid array<br>CZP suffix — Leaded<br>CVR suffix — Lead-Free are available as needed | -40°C to 100°C | 66 | KMPC885CZP66<br>KMPC880CZP66<br>MPC885CZP66<br>MPC880CZP66 |
| | | 133 | KMPC885CZP133<br>KMPC880CZP133<br>MPC885CZP133<br>MPC880CZP133 |

## 16.1 Pin Assignments

Figure 77 shows the top-view pinout of the PBGA package. For additional information, see the *MPC885 PowerQUICC™ Family Reference Manual*.

**NOTE:** This is the top view of the device.

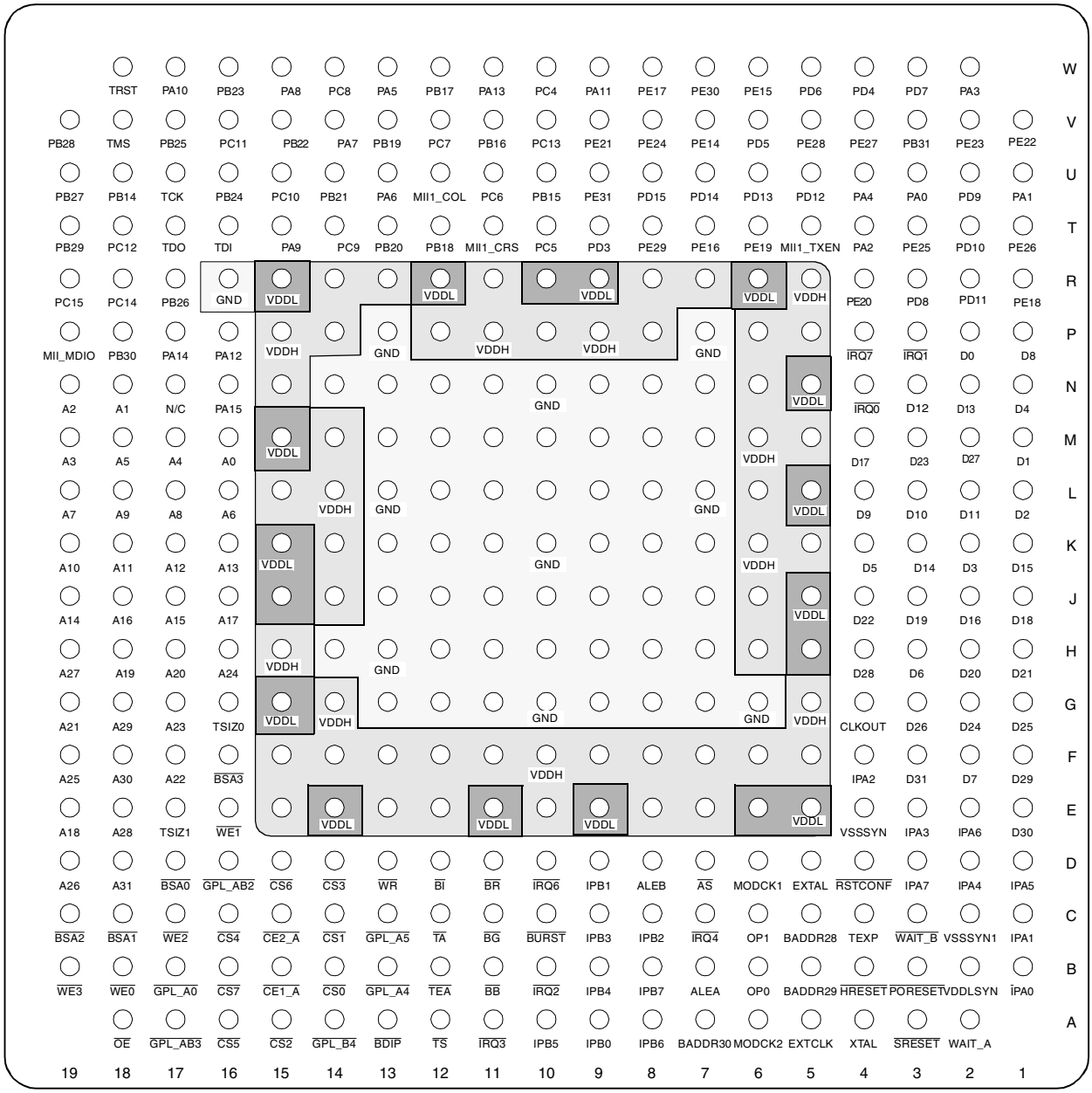


**Figure 77. Pinout of the PBGA Package**

**Table 39. Pin Assignments (continued)**

| Name | Pin Number | Type |
|---|---|---|
| ALE_B, DSCK/AT1 | D8 | Bidirectional<br>Three-state |
| IP_B[0:1], IWP[0:1], VFLS[0:1] | A9, D9 | Bidirectional |
| IP_B2, $\overline{\text{IOIS16\_B}}$, AT2 | C8 | Bidirectional<br>Three-state |
| IP_B3, IWP2, VF2 | C9 | Bidirectional |
| IP_B4, LWP0, VF0 | B9 | Bidirectional |
| IP_B5, LWP1, VF1 | A10 | Bidirectional |
| IP_B6, DSDI, AT0 | A8 | Bidirectional<br>Three-state |
| IP_B7, $\overline{\text{PTR}}$, AT3 | B8 | Bidirectional<br>Three-state |
| OP0, UtpClk_Split[1] | B6 | Bidirectional |
| OP1 | C6 | Output |
| OP2, MODCK1, $\overline{\text{STS}}$ | D6 | Bidirectional |
| OP3, MODCK2, DSDO | A6 | Bidirectional |
| BADDR30, $\overline{\text{REG}}$ | A7 | Output |
| BADDR[28:29] | C5, B5 | Output |
| $\overline{\text{AS}}$ | D7 | Input |
| PA15, USBRXD | N16 | Bidirectional |
| PA14, $\overline{\text{USBOE}}$ | P17 | Bidirectional<br>(Optional: open-drain) |
| PA13, RXD2 | W11 | Bidirectional |
| PA12, TXD2 | P16 | Bidirectional<br>(Optional: open-drain) |
| PA11, RXD4, MII1-TXD0, RMII1-TXD0 | W9 | Bidirectional<br>(Optional: open-drain) |
| PA10, MII1-TXER, TIN4, CLK7 | W17 | Bidirectional<br>(Optional: open-drain) |
| PA9, L1TXDA, RXD3 | T15 | Bidirectional<br>(Optional: open-drain) |
| PA8, L1RXDA, TXD3 | W15 | Bidirectional<br>(Optional: open-drain) |
| PA7, CLK1, L1RCLKA, BRGO1, TIN1 | V14 | Bidirectional |
| PA6, CLK2, $\overline{\text{TOUT1}}$ | U13 | Bidirectional |
| PA5, CLK3, L1TCLKA, BRGO2, TIN2 | W13 | Bidirectional |

**Table 39. Pin Assignments (continued)**

| Name | Pin Number | Type |
|---|---|---|
| PD5, CLK8, L1TCLKB, UTPB6 | V6 | Bidirectional |
| PD4, CLK4, UTPB7 | W4 | Bidirectional |
| PD3, CLK7, TIN4, SOC | T9 | Bidirectional |
| PE31, CLK8, L1TCLKB, MII1-RXCLK | U9 | Bidirectional (Optional: open-drain) |
| PE30, L1RXDB, MII1-RXD2 | W7 | Bidirectional (Optional: open-drain) |
| PE29, MII2-CRS | T8 | Bidirectional (Optional: open-drain) |
| PE28, $\overline{\text{TOUT3}}$, MII2-COL | V5 | Bidirectional (Optional: open-drain) |
| PE27, $\overline{\text{RTS3}}$, L1RQB, MII2-RXER, RMII2-RXER | V4 | Bidirectional (Optional: open-drain) |
| PE26, L1CLKOB, MII2-RXDV, RMII2-CRS_DV | T1 | Bidirectional (Optional: open-drain) |
| PE25, RXD4, MII2-RXD3, L1ST2 | T3 | Bidirectional (Optional: open-drain) |
| PE24, SMRXD1, BRGO1, MII2-RXD2 | V8 | Bidirectional (Optional: open-drain) |
| PE23, $\overline{\text{SMSYN2}}$, TXD4, MII2-RXCLK, L1ST1 | V2 | Bidirectional (Optional: open-drain) |
| PE22, $\overline{\text{TOUT2}}$, MII2-RXD1, RMII2-RXD1, $\overline{\text{SDACK1}}$ | V1 | Bidirectional (Optional: open-drain) |
| PE21, SMRXD2, $\overline{\text{TOUT1}}$, MII2-RXD0, RMII2-RXD0, $\overline{\text{RTS3}}$ | V9 | Bidirectional (Optional: open-drain) |
| PE20, L1RSYNCA, SMTXD2, $\overline{\text{CTS3}}$, MII2-TXER | R4 | Bidirectional (Optional: open-drain) |
| PE19, L1TXDB, MII2-TXEN, RMII2-TXEN | T6 | Bidirectional (Optional: open-drain) |
| PE18, L1TSYNCA, SMTXD1, MII2-TXD3 | R1 | Bidirectional (Optional: open-drain) |
| PE17, TIN3, CLK5, BRGO3, $\overline{\text{SMSYN1}}$, MII2-TXD2 | W8 | Bidirectional (Optional: open-drain) |
| PE16, L1RCLKB, CLK6, TXD3, MII2-TXCLK, RMII2-REFCLK | T7 | Bidirectional (Optional: open-drain) |
| PE15, $\overline{\text{TGATE1}}$, MII2-TXD1, RMII2-TXD1 | W6 | Bidirectional |

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