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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	66MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (2), 10/100Mbps (2)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 100°C (TA)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc880czp66

  - Flexible data buffers with multiple buffers per frame
  - Automatic retransmission upon transmit error
- The USB host controller has the following features:
  - Supports control, bulk, interrupt, and isochronous data transfers
  - CRC16 generation and checking
  - NRZI encoding/decoding with bit stuffing
  - Supports both 12- and 1.5-Mbps data rates (automatic generation of preamble token and data rate configuration). Note that low-speed operation requires an external hub.
  - Flexible data buffers with multiple buffers per frame
  - Supports local loop back mode for diagnostics (12 Mbps only)

- Serial peripheral interface (SPI)
  - Supports master and slave modes
  - Supports multiple-master operation on the same bus
- Inter-integrated circuit (I^2C) port
  - Supports master and slave modes
  - Supports a multiple-master environment
- Time-slot assigner (TSA)
  - Allows SCCs and SMCs to run in multiplexed and/or non-multiplexed operation
  - Supports T1, CEPT, PCM highway, ISDN basic rate, ISDN primary rate, user defined
  - 1- or 8-bit resolution
  - Allows independent transmit and receive routing, frame synchronization, and clocking
  - Allows dynamic changes
  - Can be internally connected to four serial channels (two SCCs and two SMCs)
- Parallel interface port (PIP)
  - Centronics interface support
  - Supports fast connection between compatible ports on MPC885/MPC880 and other MPC8xx devices
- PCMCIA interface
  - Master (socket) interface, release 2.1-compliant
  - Supports two independent PCMCIA sockets
  - 8 memory or I/O windows supported
- Debug interface
  - Eight comparators: four operate on instruction address, two operate on data address, and two operate on data
  - Supports conditions: $= \neq < >$
  - Each watchpoint can generate a break point internally.
- Normal high and normal low power modes to conserve power

- 1.8-V core and 3.3-V I/O operation
- The MPC885/MPC880 comes in a 357-pin ball grid array (PBGA) package

The MPC885 block diagram is shown in Figure 1.

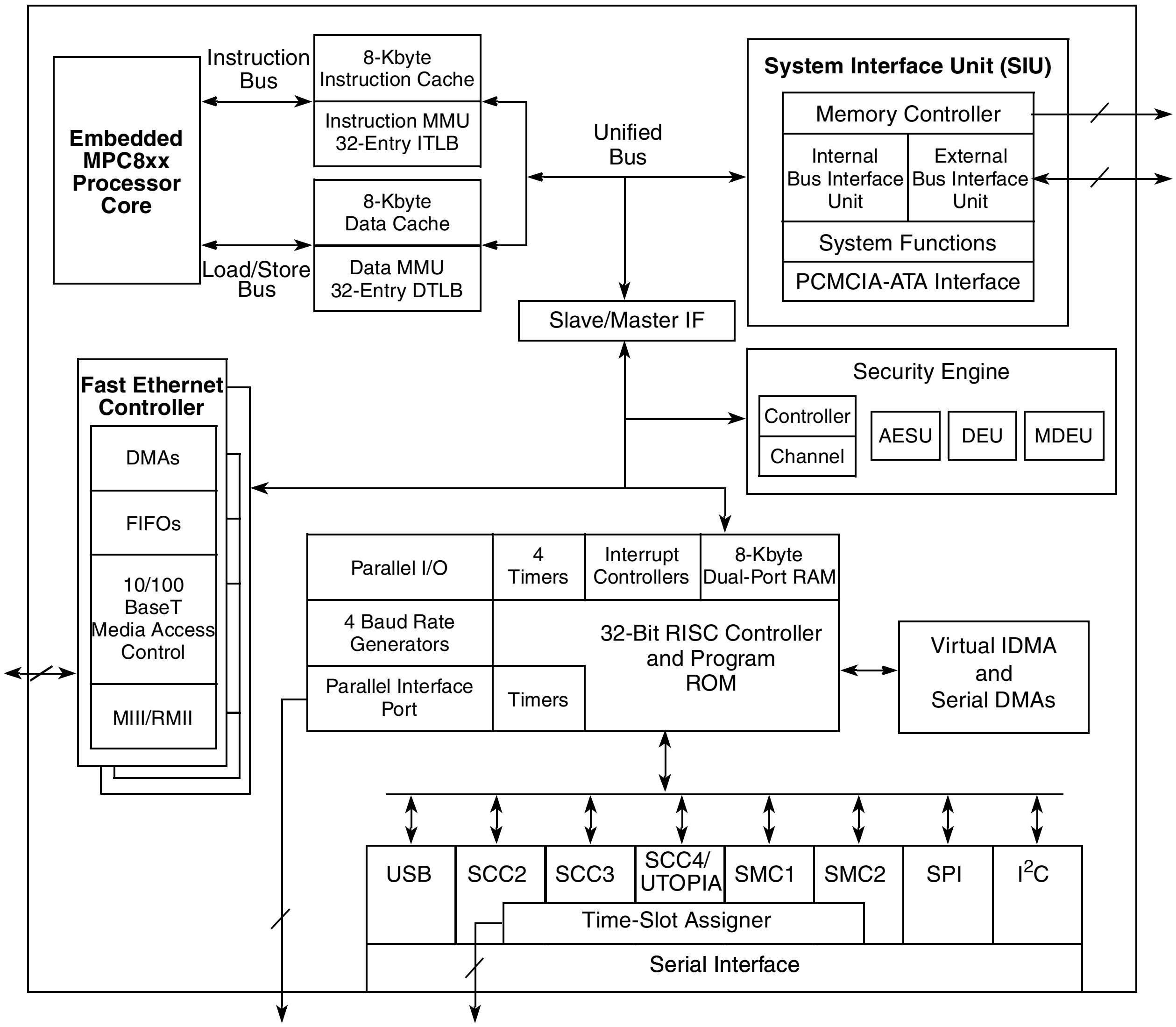

Figure 1. MPC885 Block Diagram

The MPC880 block diagram is shown in Figure 2.

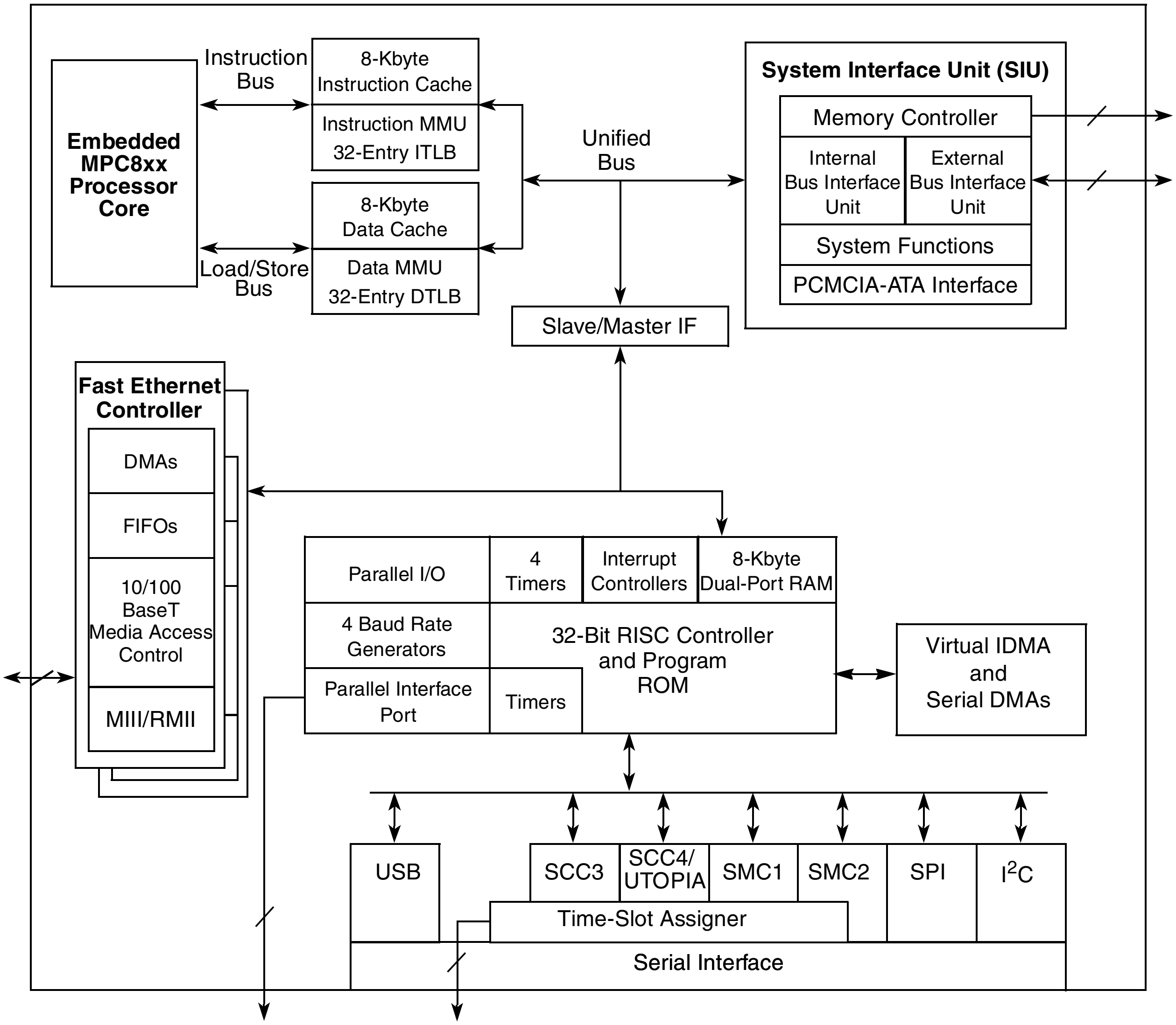

Figure 2. MPC880 Block Diagram

Table 3. Operating Temperatures

Rating	Symbol	Value	Unit
Temperature[1] (standard)	$T_{A(min)}$	0	°C
	$T_{J(max)}$	95	°C
Temperature (extended)	$T_{A(min)}$	–40	°C
	$T_{J(max)}$	100	°C

1 Minimum temperatures are guaranteed as ambient temperature, T_A. Maximum temperatures are guaranteed as junction temperature, T_J.

This device contains circuitry protecting against damage due to high-static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{DD}).

4 Thermal Characteristics

Table 4 shows the thermal characteristics for the MPC885/MPC880.

Table 4. MPC885/MPC880 Thermal Resistance Data

Rating	Environment		Symbol	Value	Unit
Junction-to-ambient[1]	Natural convection	Single-layer board (1s)	$R_{\theta JA}$[2]	37	°C/W
		Four-layer board (2s2p)	$R_{\theta JMA}$[3]	25	
	Airflow (200 ft/min)	Single-layer board (1s)	$R_{\theta JMA}$[3]	30	
		Four-layer board (2s2p)	$R_{\theta JMA}$[3]	22	
Junction-to-board[4]	—	—	$R_{\theta JB}$	17	
Junction-to-case [5]	—	—	$R_{\theta JC}$	10	
Junction-to-package top[6]	Natural convection	—	Ψ_{JT}	2	
	Airflow (200 ft/min)	—	Ψ_{JT}	2	

1 Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.

2 Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature. For exposed pad packages where the pad would be expected to be soldered, junction-to-case thermal resistance is a simulated value from the junction to the exposed pad without contact resistance.

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

7.2 Estimation with Junction-to-Case Thermal Resistance

Historically, thermal resistance has frequently been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (ºC/W)

$R_{\theta JC}$ = junction-to-case thermal resistance (ºC/W)

$R_{\theta CA}$ = case-to-ambient thermal resistance (ºC/W)

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user adjusts the thermal environment to affect the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the airflow around the device, add a heat sink, change the mounting arrangement on the printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device. This thermal model is most useful for ceramic packages with heat sinks where some 90% of the heat flows through the case and the heat sink to the ambient environment. For most packages, a better model is required.

7.3 Estimation with Junction-to-Board Thermal Resistance

A simple package thermal model that has demonstrated reasonable accuracy (about 20%) is a two-resistor model consisting of a junction-to-board and a junction-to-case thermal resistance. The junction-to-case covers the situation where a heat sink is used or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed-circuit board. It has been observed that the thermal performance of most plastic packages and especially PBGA packages is strongly dependent on the board temperature; see Figure 4.

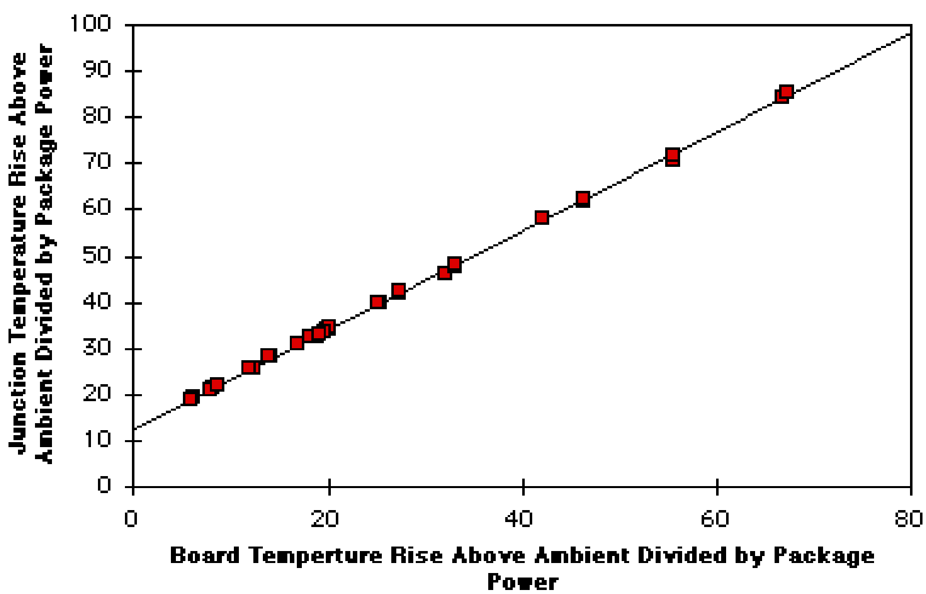

Figure 4. Effect of Board Temperature Rise on Thermal Behavior

If the board temperature is known, an estimate of the junction temperature in the environment can be made using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

$R_{\theta JB}$ = junction-to-board thermal resistance (ºC/W)

T_B = board temperature (ºC)

P_D = power dissipation in package

If the board temperature is known and the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. For this method to work, the board and board mounting must be similar to the test board used to determine the junction-to-board thermal resistance, namely a 2s2p (board with a power and a ground plane) and vias attaching the thermal balls to the ground plane.

7.4 Estimation Using Simulation

When the board temperature is not known, a thermal simulation of the application is needed. The simple two resistor model can be used with the thermal simulation of the application [2], or a more accurate and complex model of the package can be used in the thermal simulation.

7.5 Experimental Determination

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

Ψ_{JT} = thermal characterization parameter

T_T = thermocouple temperature on top of package

P_D = power dissipation in package

The thermal characterization parameter is measured per the JESD51-2 specification published by JEDEC using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by the cooling effects of the thermocouple wire.

7.6 References

Semiconductor Equipment and Materials International(415) 964-5111
805 East Middlefield Rd
Mountain View, CA 94043

MIL-SPEC and EIA/JESD (JEDEC) specifications800-854-7179 or
(Available from Global Engineering Documents)303-397-7956

JEDEC Specifications http://www.jedec.org

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
2. 2. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

8 Power Supply and Power Sequencing

This section provides design considerations for the MPC885/MPC880 power supply. The MPC885/MPC880 has a core voltage (V_{DDL}) and PLL voltage (V_{DDSYN}), which both operate at a lower voltage than the I/O voltage V_{DDH}. The I/O section of the MPC885/MPC880 is supplied with 3.3 V across V_{DDH} and V_{SS} (GND).

The signals PA[0:15], PB[14:31], PC[4:15], PD[3:15], TDI, TDO, TCK, TRST_B, TMS, MII_TXEN, and MII_MDIO are 5 V tolerant. All inputs cannot be more than 2.5 V greater than V_{DDH}. In addition, 5-V tolerant pins cannot exceed 5.5 V and remaining input pins cannot exceed 3.465 V. This restriction applies to power up/down and normal operation.

One consequence of multiple power supplies is that when power is initially applied the voltage rails ramp up at different rates. The rates depend on the nature of the power supply, the type of load on each power supply, and the manner in which different voltages are derived. The following restrictions apply:

- V_{DDL} must not exceed V_{DDH} during power up and power down.
- V_{DDL} must not exceed 1.9 V, and V_{DDH} must not exceed 3.465 V.

These cautions are necessary for the long-term reliability of the part. If they are violated, the electrostatic discharge (ESD) protection diodes are forward-biased, and excessive current can flow through these diodes. If the system power supply design does not control the voltage sequencing, the circuit shown Figure 5 can be added to meet these requirements. The MUR420 Schottky diodes control the maximum potential difference between the external bus and core power supplies on power up, and the 1N5820 diodes regulate the maximum potential difference on power down.

Figure 12 provides the timing for the input data controlled by the UPM for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

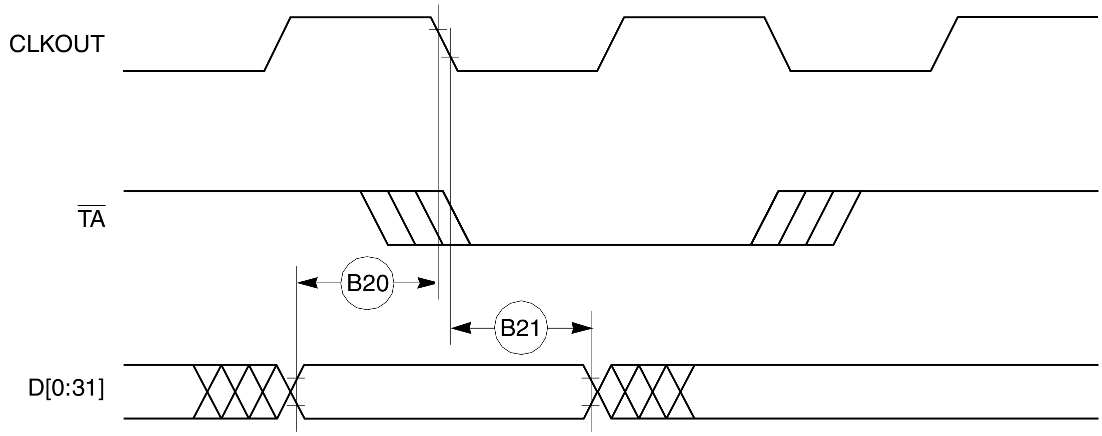

Figure 12. Input Data Timing when Controlled by UPM in the Memory Controller and DLT3 = 1

Figure 13 through Figure 16 provide the timing for the external bus read controlled by various GPCM factors.

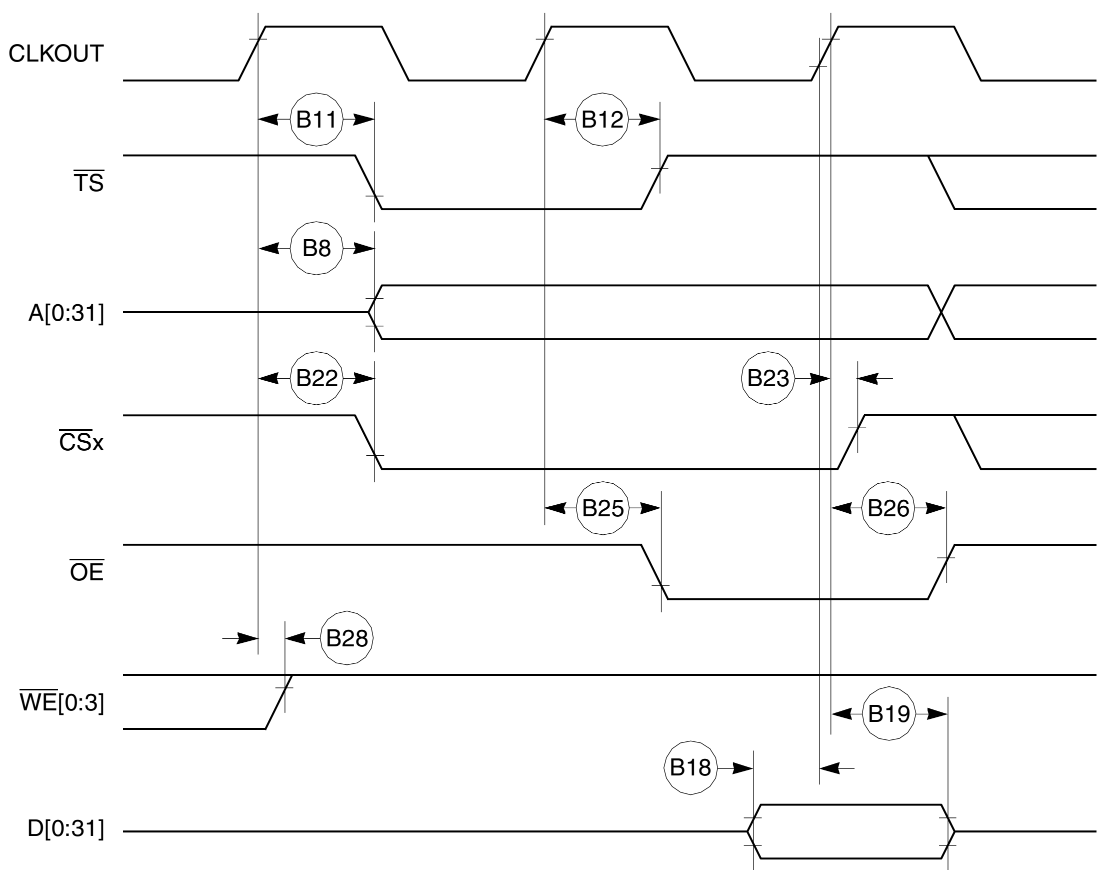

Figure 13. External Bus Read Timing (GPCM Controlled—ACS = 00)

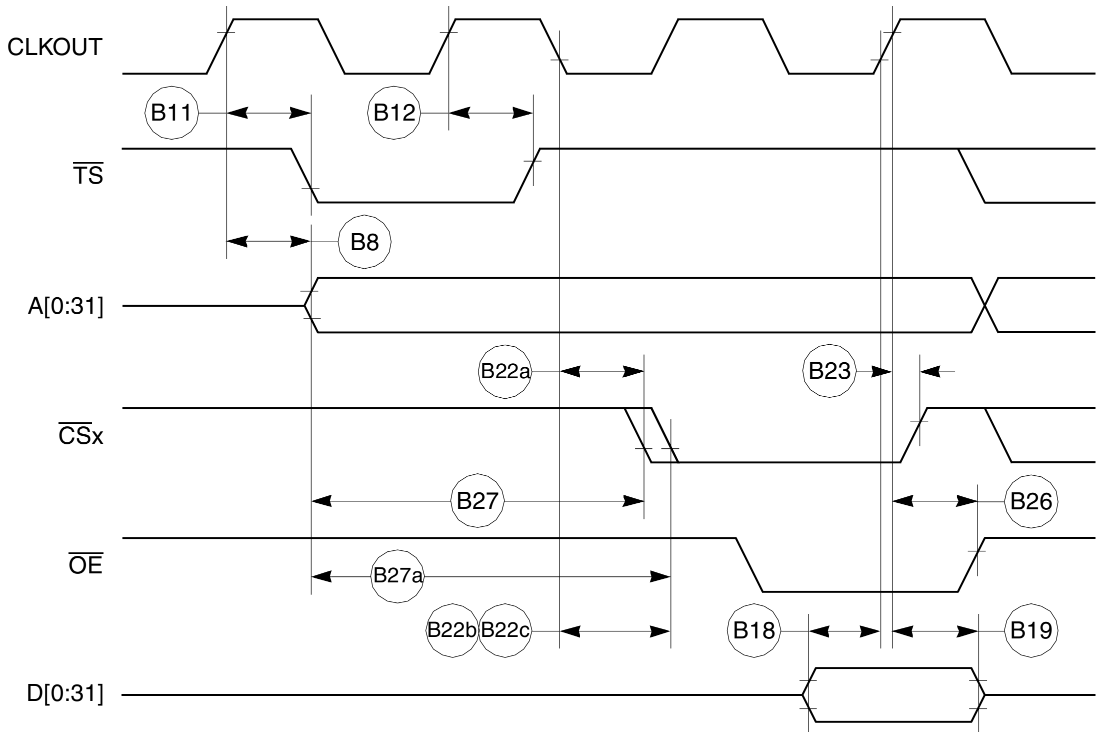

Figure 16. External Bus Read Timing (GPCM Controlled—TRLX = 1, ACS = 10, ACS = 11)

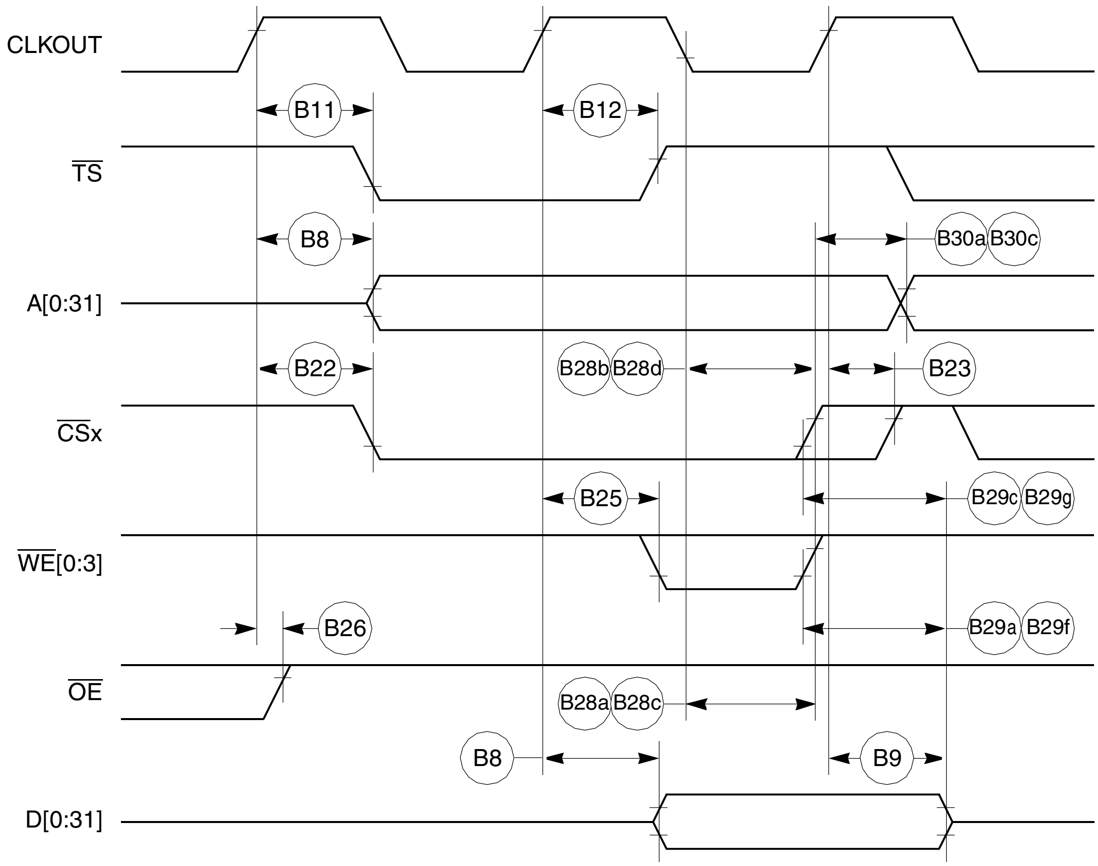

Figure 18. External Bus Write Timing (GPCM Controlled—TRLX = 0, CSNT = 1)

Figure 23 provides the timing for the synchronous external master access controlled by the GPCM.

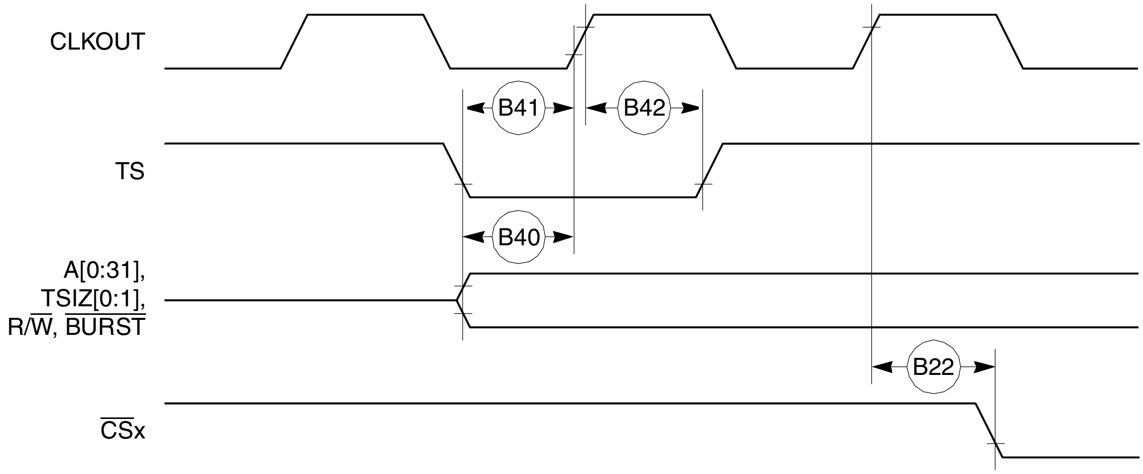

Figure 23. Synchronous External Master Access Timing (GPCM Handled—ACS = 00)

Figure 24 provides the timing for the asynchronous external master memory access controlled by the GPCM.

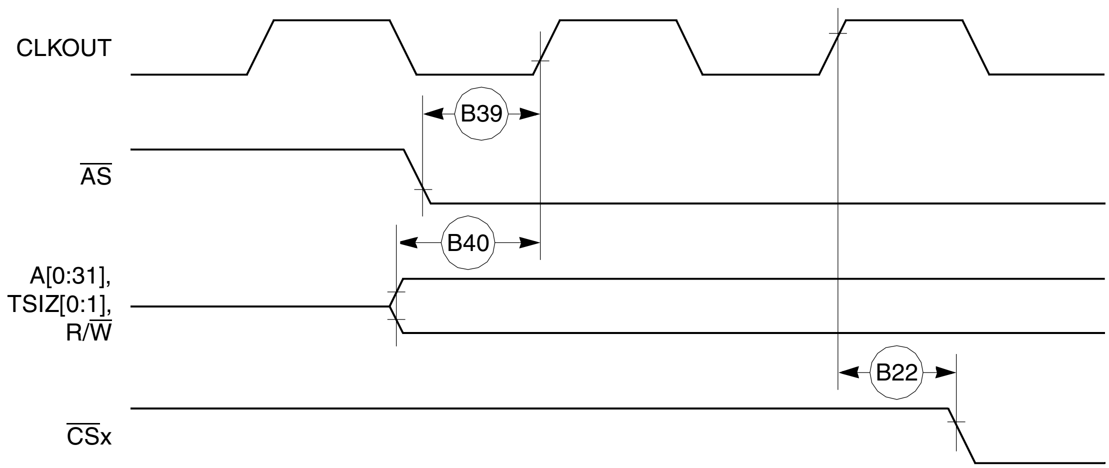

Figure 24. Asynchronous External Master Memory Access Timing (GPCM Controlled—ACS = 00)

Figure 25 provides the timing for the asynchronous external master control signals negation.

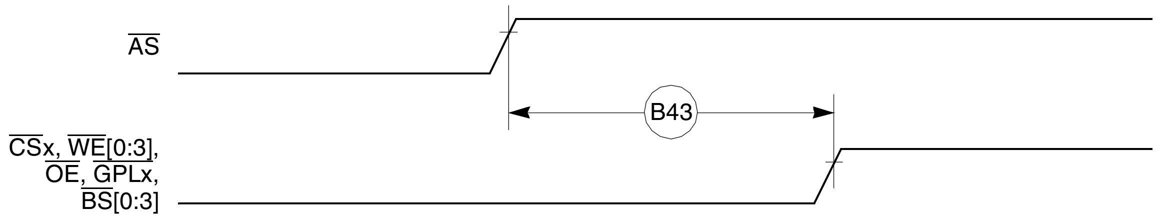

Figure 25. Asynchronous External Master—Control Signals Negation Timing

Table 10 provides the interrupt timing for the MPC885/MPC880.

Table 10. Interrupt Timing

Num	Characteristic[1]	All Frequencies		Unit
		Min	Max	
I39	$\overline{IRQ}$x valid to CLKOUT rising edge (setup time)	6.00		ns
I40	$\overline{IRQ}$x hold time after CLKOUT	2.00		ns
I41	$\overline{IRQ}$x pulse width low	3.00		ns
I42	$\overline{IRQ}$x pulse width high	3.00		ns
I43	$\overline{IRQ}$x edge-to-edge time	$4 \times T_{CLOCKOUT}$		—

[1] The I39 and I40 timings describe the testing conditions under which the $\overline{IRQ}$ lines are tested when being defined as level sensitive. The $\overline{IRQ}$ lines are synchronized internally and do not have to be asserted or negated with reference to the CLKOUT. The I41, I42, and I43 timings are specified to allow correct functioning of the $\overline{IRQ}$ lines detection circuitry and have no direct relation with the total system interrupt latency that the MPC885/MPC880 is able to support.

Figure 26 provides the interrupt detection timing for the external level-sensitive lines.

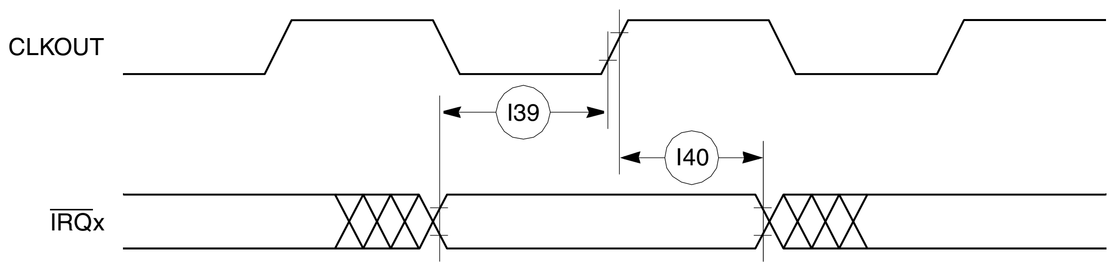

Figure 26. Interrupt Detection Timing for External Level Sensitive Lines

Figure 27 provides the interrupt detection timing for the external edge-sensitive lines.

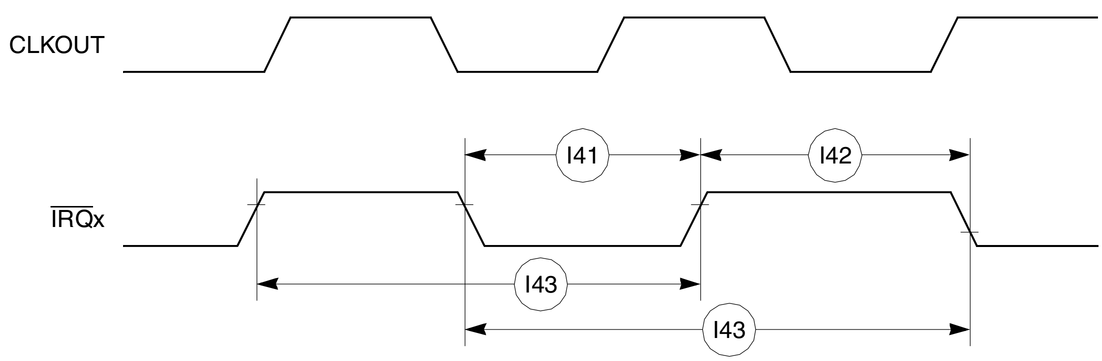

Figure 27. Interrupt Detection Timing for External Edge Sensitive Lines

Table 13 shows the debug port timing for the MPC885/MPC880.

Table 13. Debug Port Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
D61	DSCK cycle time	$3 \times T_{CLOCKOUT}$	—	—
D62	DSCK clock pulse width	$1.25 \times T_{CLOCKOUT}$	—	—
D63	DSCK rise and fall times	0.00	3.00	ns
D64	DSDI input data setup time	8.00	—	ns
D65	DSDI data hold time	5.00	—	ns
D66	DSCK low to DSDO data valid	0.00	15.00	ns
D67	DSCK low to DSDO invalid	0.00	2.00	ns

Figure 33 provides the input timing for the debug port clock.

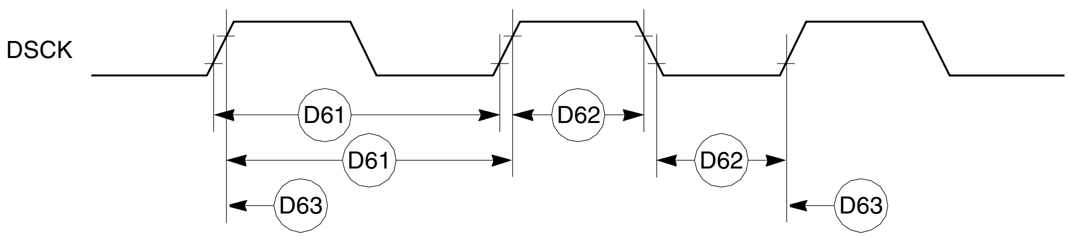

Figure 33. Debug Port Clock Input Timing

Figure 34 provides the timing for the debug port.

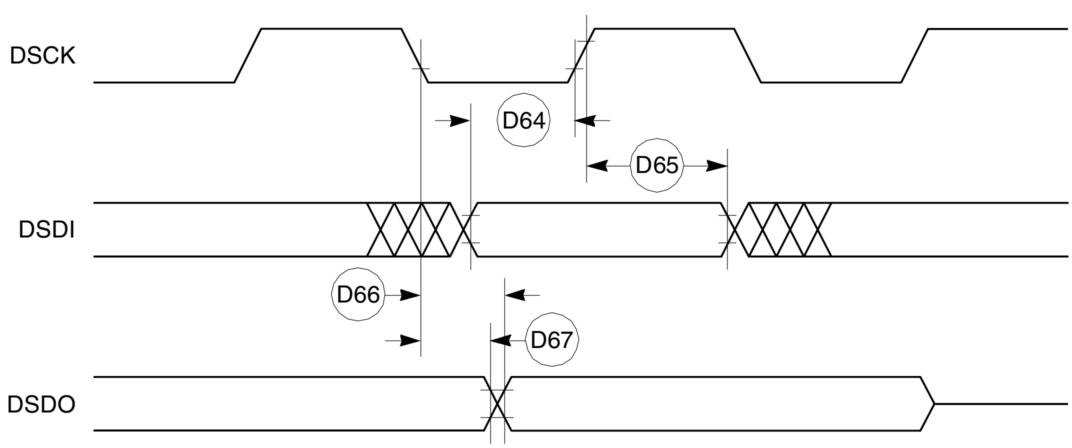

Figure 34. Debug Port Timings

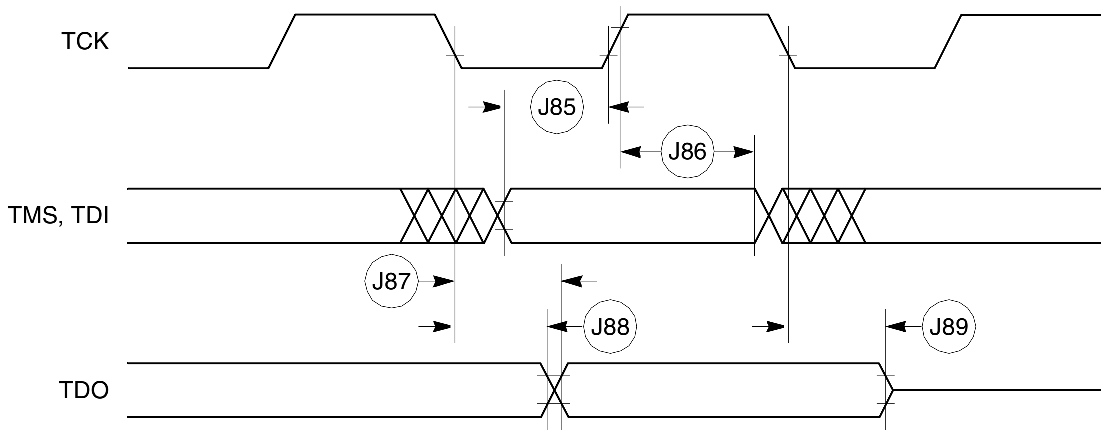

Figure 39. JTAG Test Access Port Timing Diagram

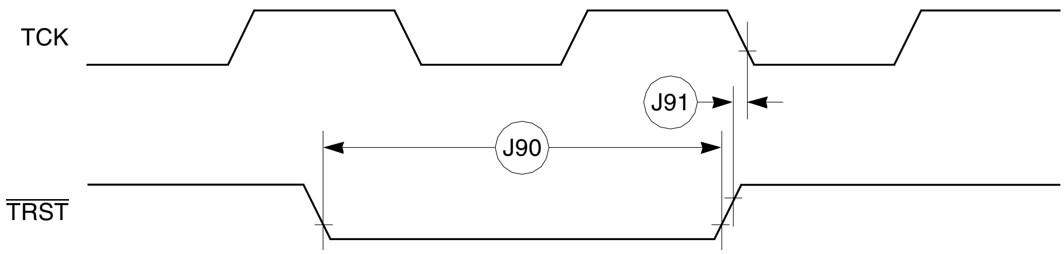

Figure 40. JTAG $\overline{\text{TRST}}$ Timing Diagram

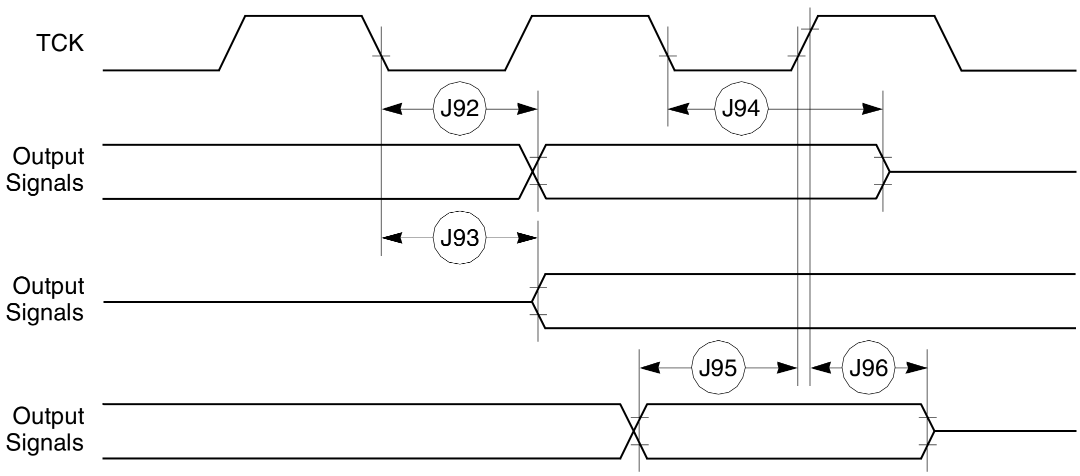

Figure 41. Boundary Scan (JTAG) Timing Diagram

12.3 IDMA Controller AC Electrical Specifications

Table 18 provides the IDMA controller timings as shown in Figure 48 tthrough Figure 51.

Table 18. IDMA Controller Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
40	DREQ setup time to clock high	7	—	ns
41	DREQ hold time from clock high [1]	TBD	—	ns
42	SDACK assertion delay from clock high	—	12	ns
43	SDACK negation delay from clock low	—	12	ns
44	SDACK negation delay from TA low	—	20	ns
45	SDACK negation delay from clock high	—	15	ns
46	TA assertion to rising edge of the clock setup time (applies to external TA)	7	—	ns

[1] Applies to high-to-low mode (EDM = 1).

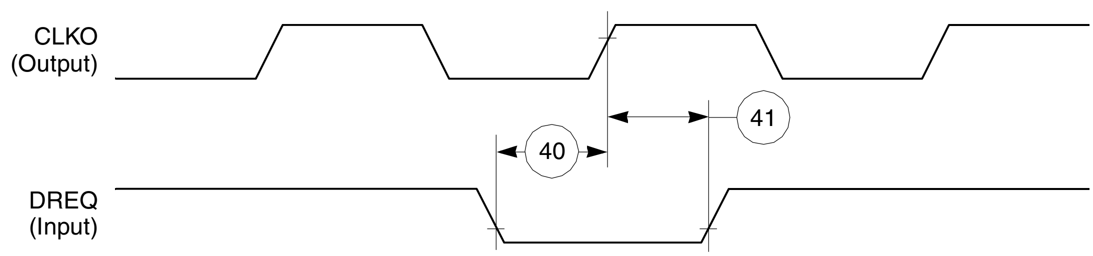

Figure 48. IDMA External Requests Timing Diagram

12.7 SCC in NMSI Mode Electrical Specifications

Table 22 provides the NMSI external clock timing.

Table 22. NMSI External Clock Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
100	RCLK1 and TCLK1 width high[1]	1/SYNCCLK	—	ns
101	RCLK1 and TCLK1 width low	1/SYNCCLK + 5	—	ns
102	RCLK1 and TCLK1 rise/fall time	—	15.00	ns
103	TXD1 active delay (from TCLK1 falling edge)	0.00	50.00	ns
104	$\overline{RTS1}$ active/inactive delay (from TCLK1 falling edge)	0.00	50.00	ns
105	$\overline{CTS1}$ setup time to TCLK1 rising edge	5.00	—	ns
106	RXD1 setup time to RCLK1 rising edge	5.00	—	ns
107	RXD1 hold time from RCLK1 rising edge[2]	5.00	—	ns
108	$\overline{CD1}$ setup time to RCLK1 rising edge	5.00	—	ns

[1] The ratios SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater than or equal to 2.25/1.
[2] Also applies to $\overline{CD}$ and $\overline{CTS}$ hold time when they are used as external sync signals.

Table 23 provides the NMSI internal clock timing.

Table 23. NMSI Internal Clock Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
100	RCLK1 and TCLK1 frequency[1]	0.00	SYNCCLK/3	MHz
102	RCLK1 and TCLK1 rise/fall time	—	—	ns
103	TXD1 active delay (from TCLK1 falling edge)	0.00	30.00	ns
104	$\overline{RTS1}$ active/inactive delay (from TCLK1 falling edge)	0.00	30.00	ns
105	$\overline{CTS1}$ setup time to TCLK1 rising edge	40.00	—	ns
106	RXD1 setup time to RCLK1 rising edge	40.00	—	ns
107	RXD1 hold time from RCLK1 rising edge[2]	0.00	—	ns
108	$\overline{CD1}$ setup time to RCLK1 rising edge	40.00	—	ns

[1] The ratios SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater than or equal to 3/1.
[2] Also applies to $\overline{CD}$ and $\overline{CTS}$ hold time when they are used as external sync signals

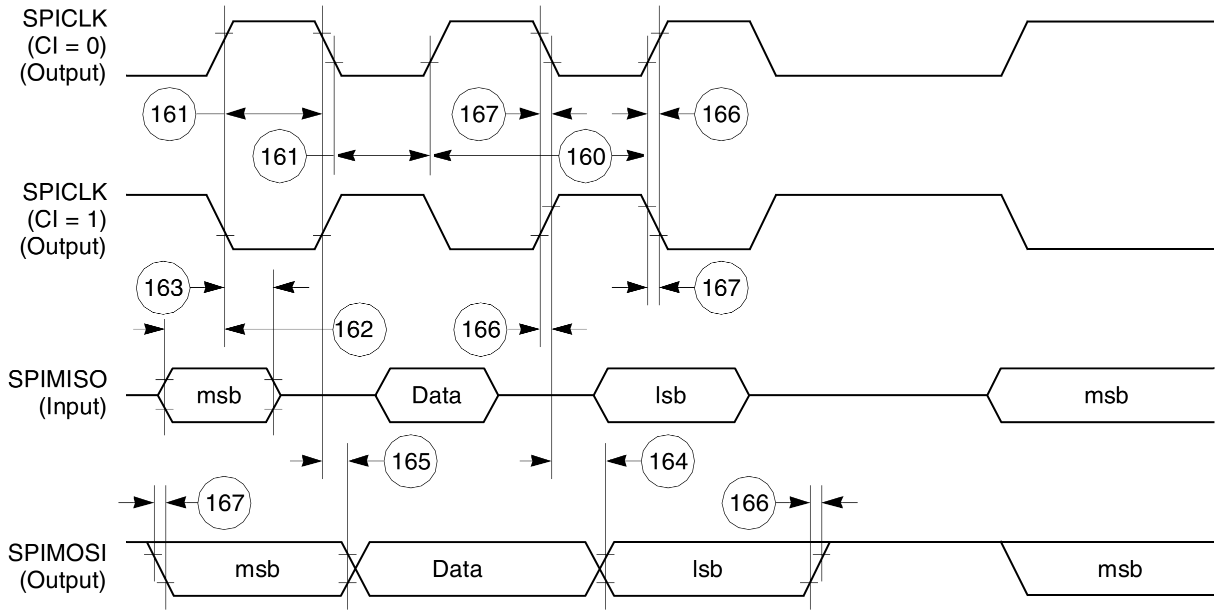

Figure 66. SPI Master (CP = 0) Timing Diagram

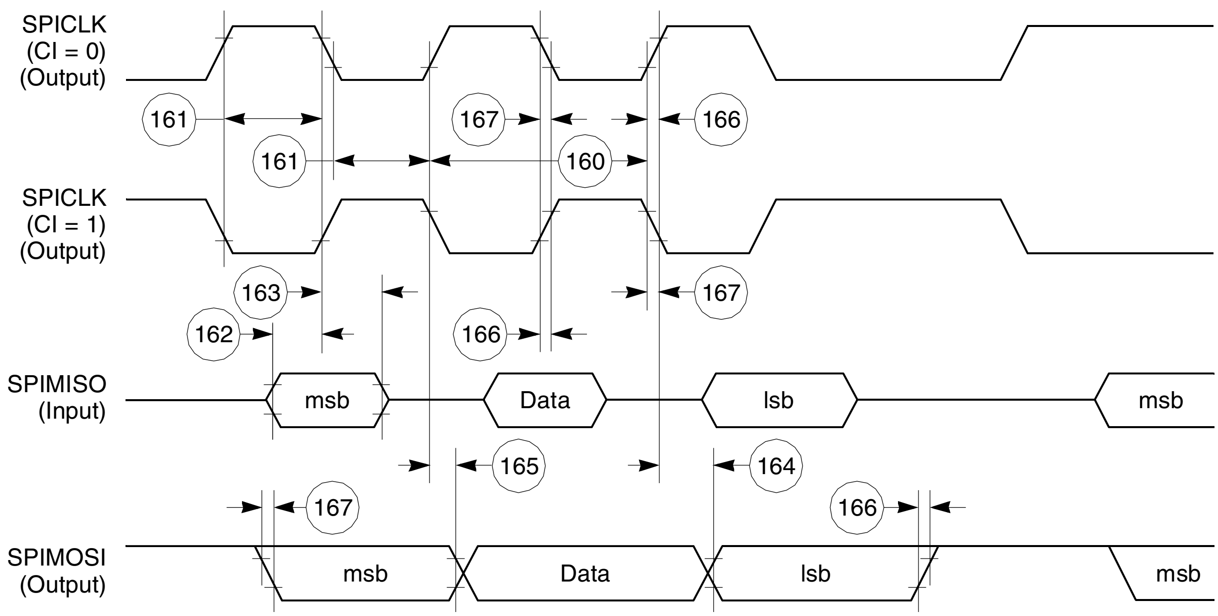

Figure 67. SPI Master (CP = 1) Timing Diagram

16.1 Pin Assignments

Figure 77 shows the top-view pinout of the PBGA package. For additional information, see the *MPC885 PowerQUICC™ Family Reference Manual*.

NOTE: This is the top view of the device.

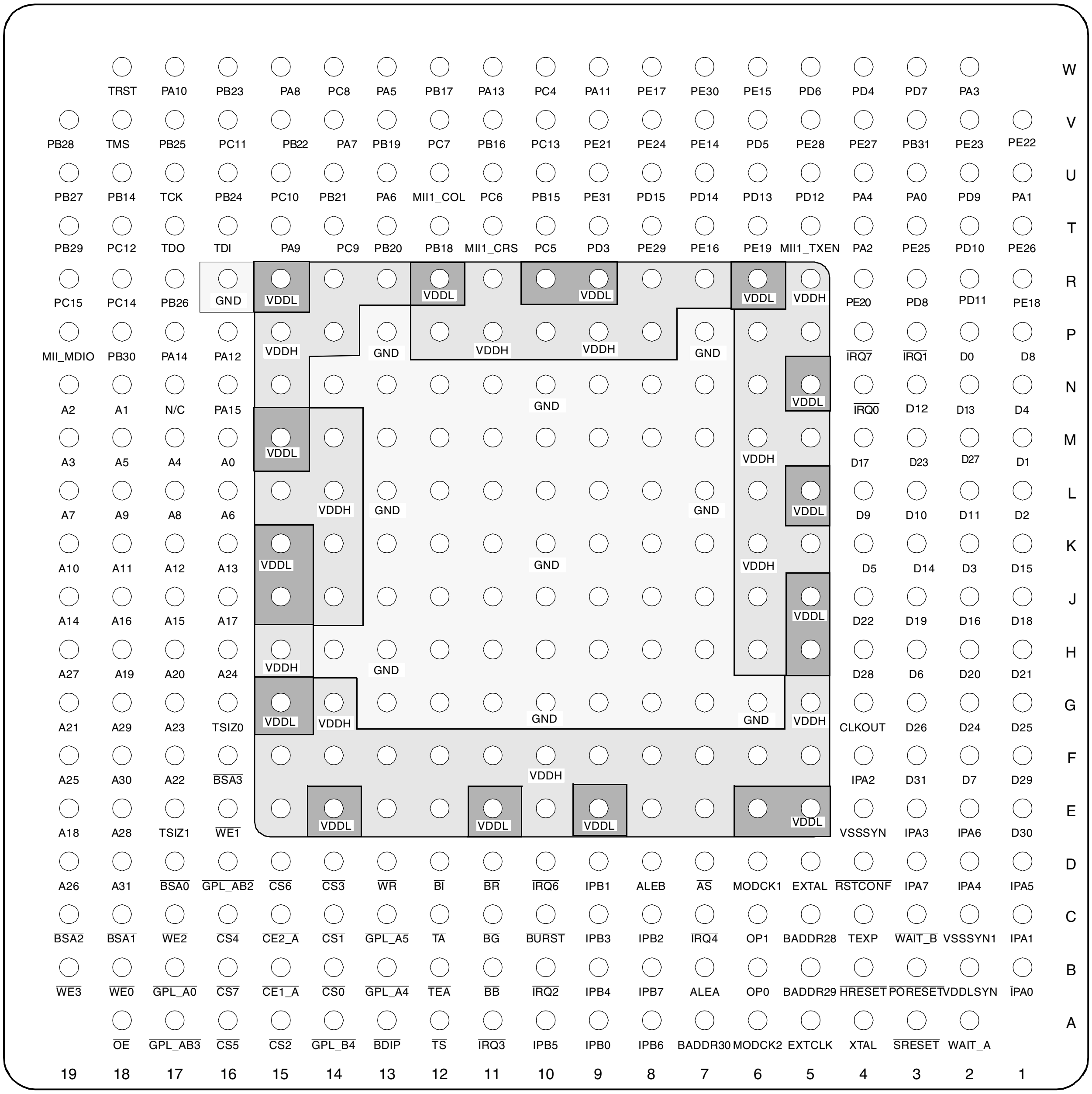

Figure 77. Pinout of the PBGA Package

Table 39. Pin Assignments (continued)

Name	Pin Number	Type
PA4, $\overline{CTS4}$, MII1-TXD1, RMII1-TXD1	U4	Bidirectional
PA3, MII1-RXER, RMII1-RXER, BRGO3	W2	Bidirectional
PA2, MII1-RXDV, RMII1-CRS_DV, TXD4	T4	Bidirectional
PA1, MII1-RXD0, RMII1-RXD0, BRGO4	U1	Bidirectional
PA0, MII1-RXD1, RMII1-RXD1, $\overline{TOUT4}$	U3	Bidirectional
PB31, $\overline{SPISEL}$, MII1-TXCLK, RMII1-REFCLK	V3	Bidirectional (Optional: open-drain)
PB30, SPICLK	P18	Bidirectional (Optional: open-drain)
PB29, SPIMOSI	T19	Bidirectional (Optional: open-drain)
PB28, SPIMISO, BRGO4	V19	Bidirectional (Optional: open-drain)
PB27, I2CSDA, BRGO1	U19	Bidirectional (Optional: open-drain)
PB26, I2CSCL, BRGO2	R17	Bidirectional (Optional: open-drain)
PB25, RXADDR3[1], TXADDR3, SMTXD1	V17	Bidirectional (Optional: open-drain)
PB24, TXADDR3[1], RXADDR3, SMRXD1	U16	Bidirectional (Optional: open-drain)
PB23, TXADDR2[1], RXADDR2, $\overline{SDACK1}$, $\overline{SMSYN1}$	W16	Bidirectional (Optional: open-drain)
PB22, TXADDR4[1], RXADDR4, $\overline{SDACK2}$, $\overline{SMSYN2}$	V15	Bidirectional (Optional: open-drain)
PB21, SMTXD2, TXADDR1[1], BRG01, RXADDR1, PHSEL[1]	U14	Bidirectional (Optional: open-drain)
PB20, SMRXD2, L1CLKOA, TXADDR0[1], RXADDR0, PHSEL[0]	T13	Bidirectional (Optional: open-drain)
PB19, MII1-RXD3, $\overline{RTS4}$	V13	Bidirectional (Optional: open-drain)
PB18, RXADDR4[1], TXADDR4, $\overline{RTS2}$, L1ST2	T12	Bidirectional (Optional: open-drain)

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