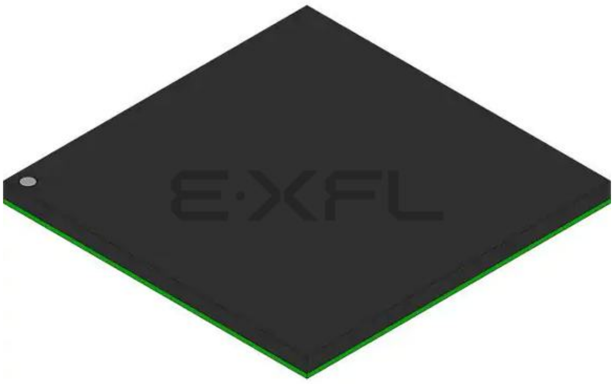

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	133MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (2), 10/100Mbps (2)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	Cryptography
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc880zp133

Email: info@E-XFL.COM Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

1 Overview

The MPC885/MPC880 is a versatile single-chip integrated microprocessor and peripheral combination that can be used in a variety of controller applications and communications and networking systems. The MPC885/MPC880 provides enhanced ATM functionality, an additional fast Ethernet controller, a USB, and an encryption block.

Table 1 shows the functionality supported by MPC885/MPC880.

Table 1. MPC885 Family

Part	Cache (Kbytes)		Ethernet		SCC	SMC	USB	ATM Support	Security Engine
	I Cache	D Cache	10BaseT	10/100					
MPC885	8	8	Up to 3	2	3	2	1	Serial ATM and UTOPIA interface	Yes
MPC880	8	8	Up to 2	2	2	2	1	Serial ATM and UTOPIA interface	No

2 Features

The MPC885/MPC880 is comprised of three modules that each use the 32-bit internal bus: a MPC8xx core, a system integration unit (SIU), and a communications processor module (CPM).

The following list summarizes the key MPC885/MPC880 features:

- Embedded MPC8xx core up to 133 MHz
- Maximum frequency operation of the external bus is 80 MHz (in 1:1 mode)
  - The 133-MHz core frequency supports 2:1 mode only.
  - The 66-/80-MHz core frequencies support both the 1:1 and 2:1 modes.
- Single-issue, 32-bit core (compatible with the Power Architecture definition) with thirty-two 32-bit general-purpose registers (GPRs)
  - The core performs branch prediction with conditional prefetch and without conditional execution.
  - 8-Kbyte data cache and 8-Kbyte instruction cache (see Table 1)
    - Instruction cache is two-way, set-associative with 256 sets in 2 blocks
    - Data cache is two-way, set-associative with 256 sets
    - Cache coherency for both instruction and data caches is maintained on 128-bit (4-word) cache blocks.
    - Caches are physically addressed, implement a least recently used (LRU) replacement algorithm, and are lockable on a cache block basis.
  - MMUs with 32-entry TLB, fully associative instruction and data TLBs
  - MMUs support multiple page sizes of 4, 16, and 512 Kbytes, and 8 Mbytes; 16 virtual address spaces and 16 protection groups
  - Advanced on-chip emulation debug mode

3 Maximum Tolerated Ratings

This section provides the maximum tolerated voltage and temperature ranges for the MPC885/MPC880. Table 2 displays the maximum tolerated ratings, and Table 3 displays the operating temperatures.

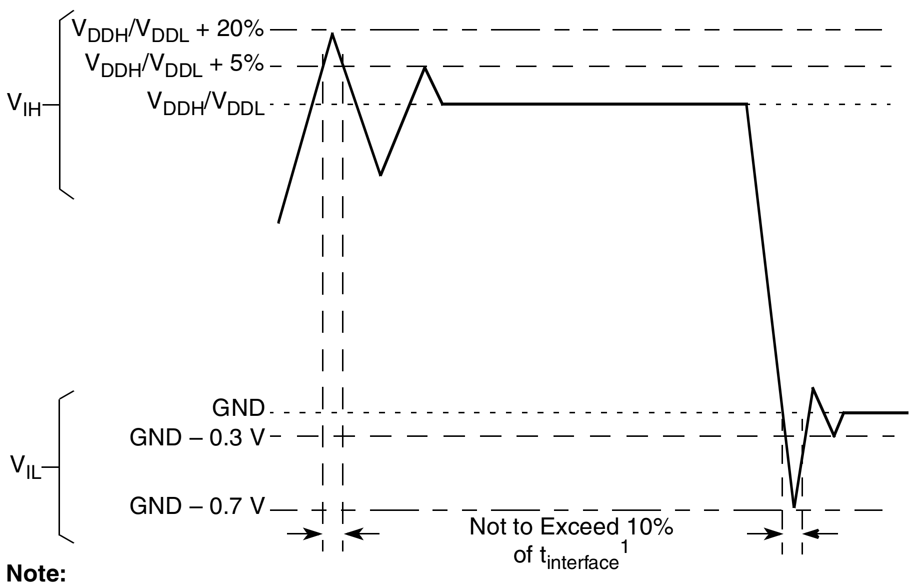
Table 2. Maximum Tolerated Ratings

Rating	Symbol	Value	Unit
Supply voltage[1]	V_{DDH}	–0.3 to 4.0	V
	V_{DDL}	–0.3 to 2.0	V
	VDDSYN	–0.3 to 2.0	V
	Difference between V_{DDL} and V_{DDSYN}	<100	mV
Input voltage[2]	V_{in}	GND – 0.3 to V_{DDH}	V
Storage temperature range	T_{stg}	–55 to +150	°C

[1] The power supply of the device must start its ramp from 0.0 V.

[2] Functional operating conditions are provided with the DC electrical specifications in Table 6. Absolute maximum ratings are stress ratings only; functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device. See Section 8, "Power Supply and Power Sequencing."
Caution: All inputs that tolerate 5 V cannot be more than 2.5 V greater than V_{DDH}. This restriction applies to power up and normal operation (that is, if the MPC885/MPC880 is unpowered, a voltage greater than 2.5 V must not be applied to its inputs).

Figure 3 shows the undershoot and overshoot voltages at the interfaces of the MPC885/MPC880.



Note:
1. $t_{interface}$ refers to the clock period associated with the bus clock interface.

Figure 3. Undershoot/Overshoot Voltage for V_{DDH} and V_{DDL}

Table 3. Operating Temperatures

Rating	Symbol	Value	Unit
Temperature[1] (standard)	$T_{A(min)}$	0	°C
	$T_{J(max)}$	95	°C
Temperature (extended)	$T_{A(min)}$	–40	°C
	$T_{J(max)}$	100	°C

[1] Minimum temperatures are guaranteed as ambient temperature, T_A. Maximum temperatures are guaranteed as junction temperature, T_J.

This device contains circuitry protecting against damage due to high-static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{DD}).

4 Thermal Characteristics

Table 4 shows the thermal characteristics for the MPC885/MPC880.

Table 4. MPC885/MPC880 Thermal Resistance Data

Rating	Environment		Symbol	Value	Unit
Junction-to-ambient[1]	Natural convection	Single-layer board (1s)	$R_{\theta JA}$[2]	37	°C/W
		Four-layer board (2s2p)	$R_{\theta JMA}$[3]	25	
	Airflow (200 ft/min)	Single-layer board (1s)	$R_{\theta JMA}$[3]	30	
		Four-layer board (2s2p)	$R_{\theta JMA}$[3]	22	
Junction-to-board[4]	—	—	$R_{\theta JB}$	17	
Junction-to-case [5]	—	—	$R_{\theta JC}$	10	
Junction-to-package top[6]	Natural convection	—	Ψ_{JT}	2	
	Airflow (200 ft/min)	—	Ψ_{JT}	2	

[1] Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.
[2] Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.
[3] Per JEDEC JESD51-6 with the board horizontal.
[4] Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
[5] Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature. For exposed pad packages where the pad would be expected to be soldered, junction-to-case thermal resistance is a simulated value from the junction to the exposed pad without contact resistance.
[6] Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B16b	$\overline{BB}$, $\overline{BG}$, $\overline{BR}$, valid to CLKOUT (setup time)[2] (4MIN = 0.00 × B1 + 0.00)	4.00	—	4.00	—	4.00	—	4.00	—	ns
B17	CLKOUT to $\overline{TA}$, $\overline{TEA}$, $\overline{BI}$, $\overline{BB}$, $\overline{BG}$, $\overline{BR}$ valid (hold time) (MIN = 0.00 × B1 + 1.00[3])	1.00	—	1.00	—	2.00	—	2.00	—	ns
B17a	CLKOUT to $\overline{KR}$, $\overline{RETRY}$, $\overline{CR}$ valid (hold time) (MIN = 0.00 × B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B18	D(0:31) valid to CLKOUT rising edge (setup time)[4] (MIN = 0.00 × B1 + 6.00)	6.00	—	6.00	—	6.00	—	6.00	—	ns
B19	CLKOUT rising edge to D(0:31) valid (hold time)[4] (MIN = 0.00 × B1 + 1.00[5])	1.00	—	1.00	—	2.00	—	2.00	—	ns
B20	D(0:31) valid to CLKOUT falling edge (setup time)[6] (MIN = 0.00 × B1 + 4.00)	4.00	—	4.00	—	4.00	—	4.00	—	ns
B21	CLKOUT falling edge to D(0:31) valid (hold time)[6] (MIN = 0.00 × B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B22	CLKOUT rising edge to $\overline{CS}$ asserted GPCM ACS = 00 (MAX = 0.25 × B1 + 6.3)	7.60	13.80	6.30	12.50	3.80	10.00	3.13	9.43	ns
B22a	CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = [0 or 1] (MAX = 0.00 × B1 + 8.00)	—	8.00	—	8.00	—	8.00	—	8.00	ns
B22b	CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = [0 or 1], EBDF = 0 (MAX = 0.25 × B1 + 6.3)	7.60	13.80	6.30	12.50	3.80	10.00	3.13	9.43	ns
B22c	CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = [0 or 1], EBDF = 1 (MAX = 0.375 × B1 + 6.6)	10.90	18.00	10.90	16.00	5.20	12.30	4.69	10.93	ns
B23	CLKOUT rising edge to $\overline{CS}$ negated GPCM read access, GPCM write access ACS = 00 and CSNT = 0 (MAX = 0.00 × B1 + 8.00)	2.00	8.00	2.00	8.00	2.00	8.00	2.00	8.00	ns
B24	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 0 (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	1.80	—	1.13	—	ns
B24a	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 11 TRLX = 0 (MIN = 0.50 × B1 – 2.00)	13.20	—	10.50	—	5.60	—	4.25	—	ns
B25	CLKOUT rising edge to $\overline{OE}$, $\overline{WE}$(0:3) asserted (MAX = 0.00 × B1 + 9.00)	—	9.00	—	9.00	—	9.00	—	9.00	ns
B26	CLKOUT rising edge to $\overline{OE}$ negated (MAX = 0.00 × B1 + 9.00)	2.00	9.00	2.00	9.00	2.00	9.00	2.00	9.00	ns
B27	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 1 (MIN = 1.25 × B1 – 2.00)	35.90	—	29.30	—	16.90	—	13.60	—	ns

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B36	A(0:31), BADDR(28:30), and D(0:31) to $\overline{\text{GPL}}$ valid, as requested by control bit GxT4 in the corresponding word in the UPM (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	1.80	—	1.13	—	ns
B37	UPWAIT valid to CLKOUT falling edge[9] (MIN = 0.00 × B1 + 6.00)	6.00	—	6.00	—	6.00	—	6.00	—	ns
B38	CLKOUT falling edge to UPWAIT valid [9] (MIN = 0.00 × B1 + 1.00)	1.00	—	1.00	—	1.00	—	1.00	—	ns
B39	$\overline{\text{AS}}$ valid to CLKOUT rising edge[10] (MIN = 0.00 × B1 + 7.00)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B40	A(0:31), TSIZ(0:1), RD/$\overline{\text{WR}}$, $\overline{\text{BURST}}$, valid to CLKOUT rising edge (MIN = 0.00 × B1 + 7.00)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B41	$\overline{\text{TS}}$ valid to CLKOUT rising edge (setup time) (MIN = 0.00 × B1 + 7.00)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B42	CLKOUT rising edge to $\overline{\text{TS}}$ valid (hold time) (MIN = 0.00 × B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B43	$\overline{\text{AS}}$ negation to memory controller signals negation (MAX = TBD)	—	TBD	—	TBD	—	TBD	—	TBD	ns

1 For part speeds above 50 MHz, use 9.80 ns for B11a.

2 The timing required for $\overline{\text{BR}}$ input is relevant when the MPC885/MPC880 is selected to work with the internal bus arbiter. The timing for $\overline{\text{BG}}$ input is relevant when the MPC885/MPC880 is selected to work with the external bus arbiter.

3 For part speeds above 50 MHz, use 2 ns for B17.

4 The D(0:31) input timings B18 and B19 refer to the rising edge of the CLKOUT in which the $\overline{\text{TA}}$ input signal is asserted.

5 For part speeds above 50 MHz, use 2 ns for B19.

6 The D(0:31) input timings B20 and B21 refer to the falling edge of the CLKOUT. This timing is valid only for read accesses controlled by chip-selects under control of the user-programmable machine (UPM) in the memory controller, for data beats where DLT3 = 1 in the RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

7 This formula applies to bus operation up to 50 MHz.

8 The timing B30 refers to $\overline{\text{CS}}$ when ACS = 00 and to $\overline{\text{CS}}$ and $\overline{\text{WE}}$(0:3) when CSNT = 0.

9 The signal UPWAIT is considered asynchronous to the CLKOUT and synchronized internally. The timings specified in B37 and B38 are specified to enable the freeze of the UPM output signals as described in Figure 21.

10 The $\overline{\text{AS}}$ signal is considered asynchronous to the CLKOUT. The timing B39 is specified in order to allow the behavior specified in Figure 24.

Figure 12 provides the timing for the input data controlled by the UPM for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

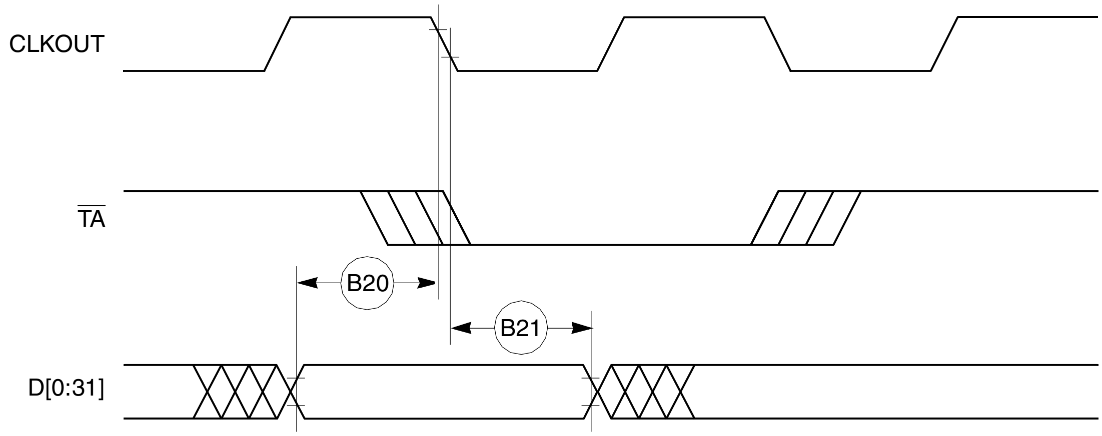


Figure 12. Input Data Timing when Controlled by UPM in the Memory Controller and DLT3 = 1

Figure 13 through Figure 16 provide the timing for the external bus read controlled by various GPCM factors.

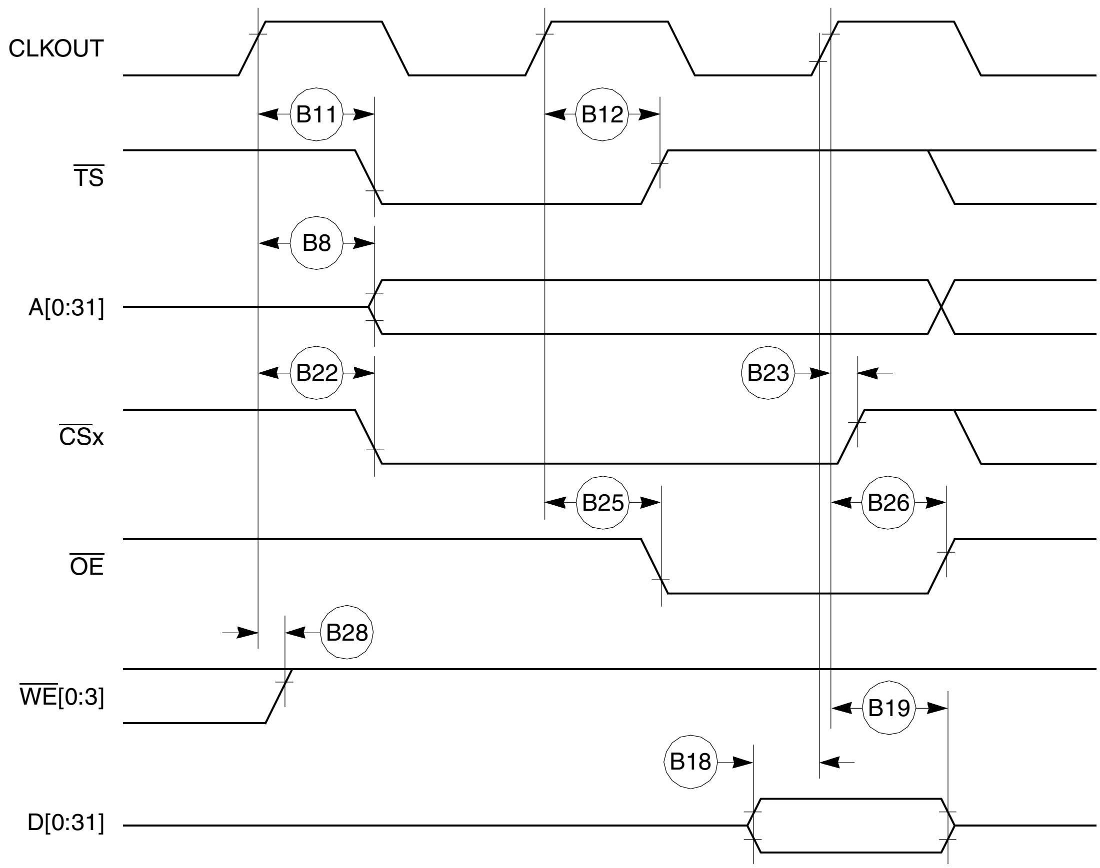


Figure 13. External Bus Read Timing (GPCM Controlled—ACS = 00)

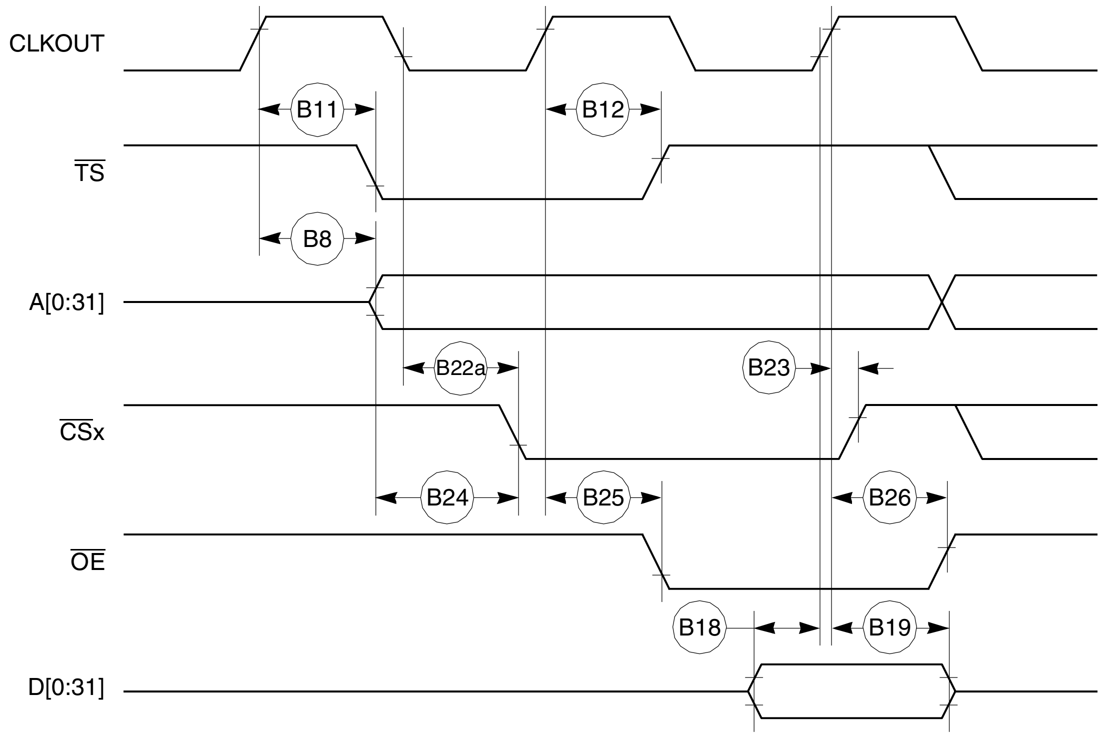


Figure 14. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 10)

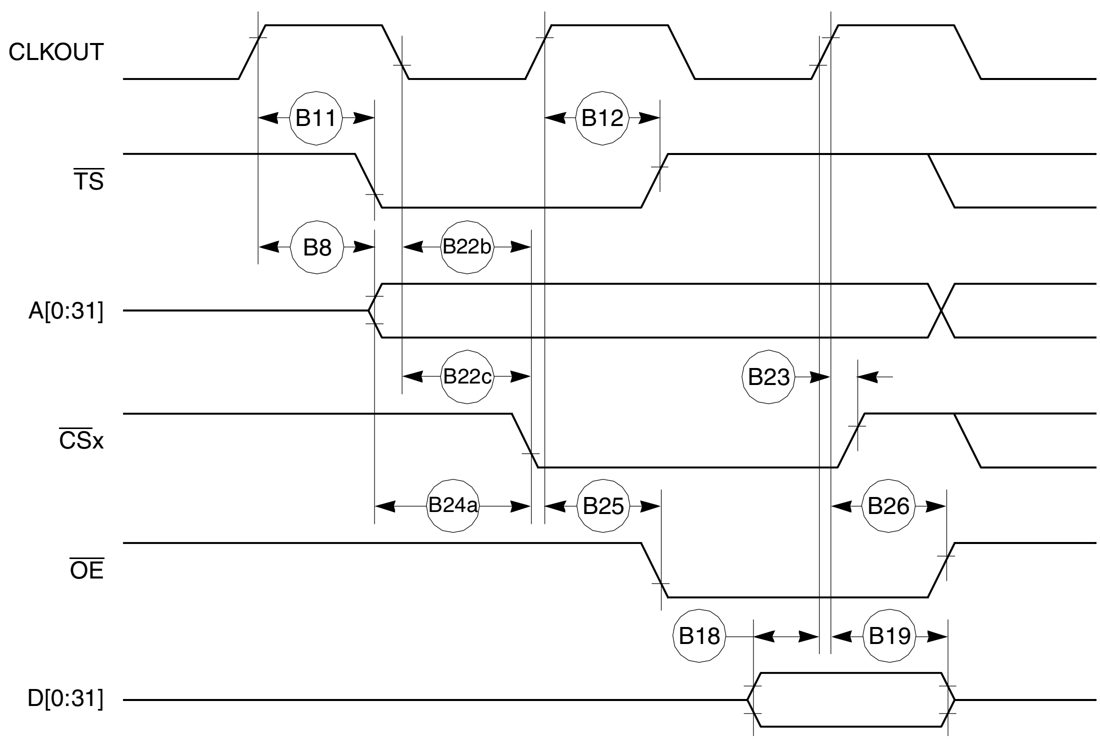


Figure 15. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 11)

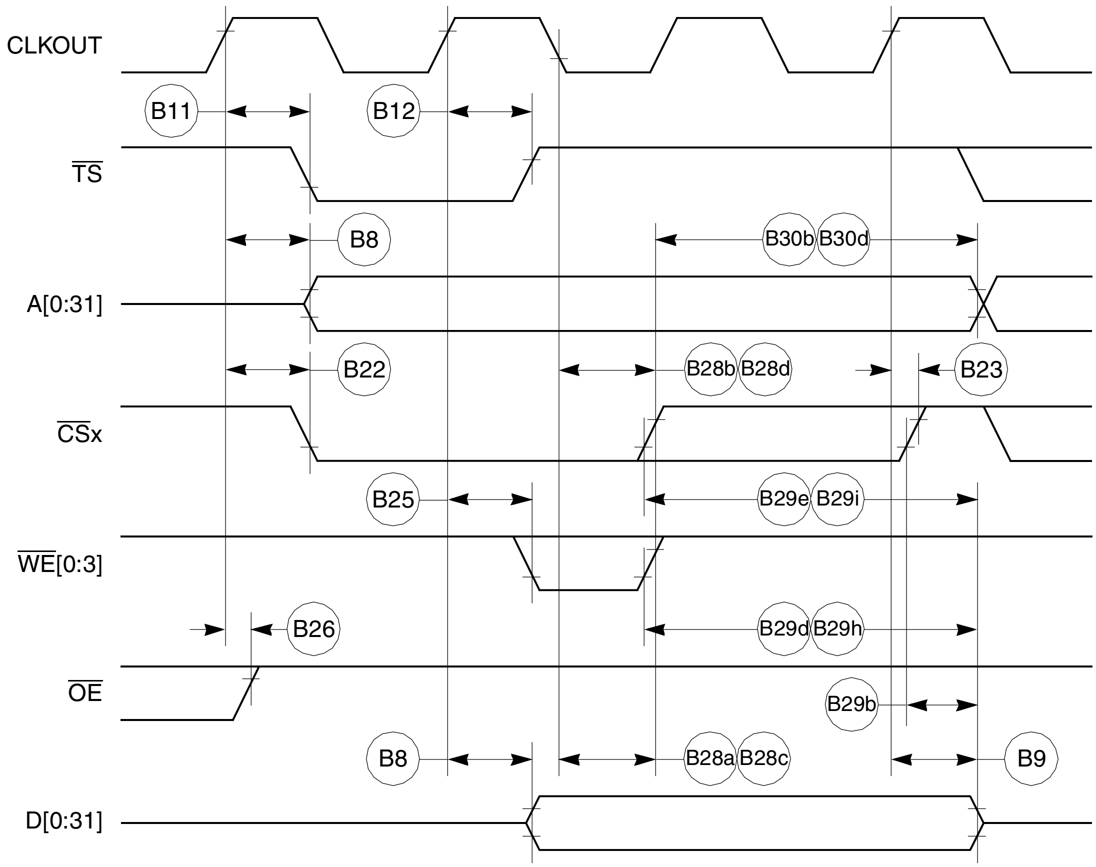


Figure 19. External Bus Write Timing (GPCM Controlled—TRLX = 1, CSNT = 1)

Figure 29 provides the PCMCIA access cycle timing for the external bus write.

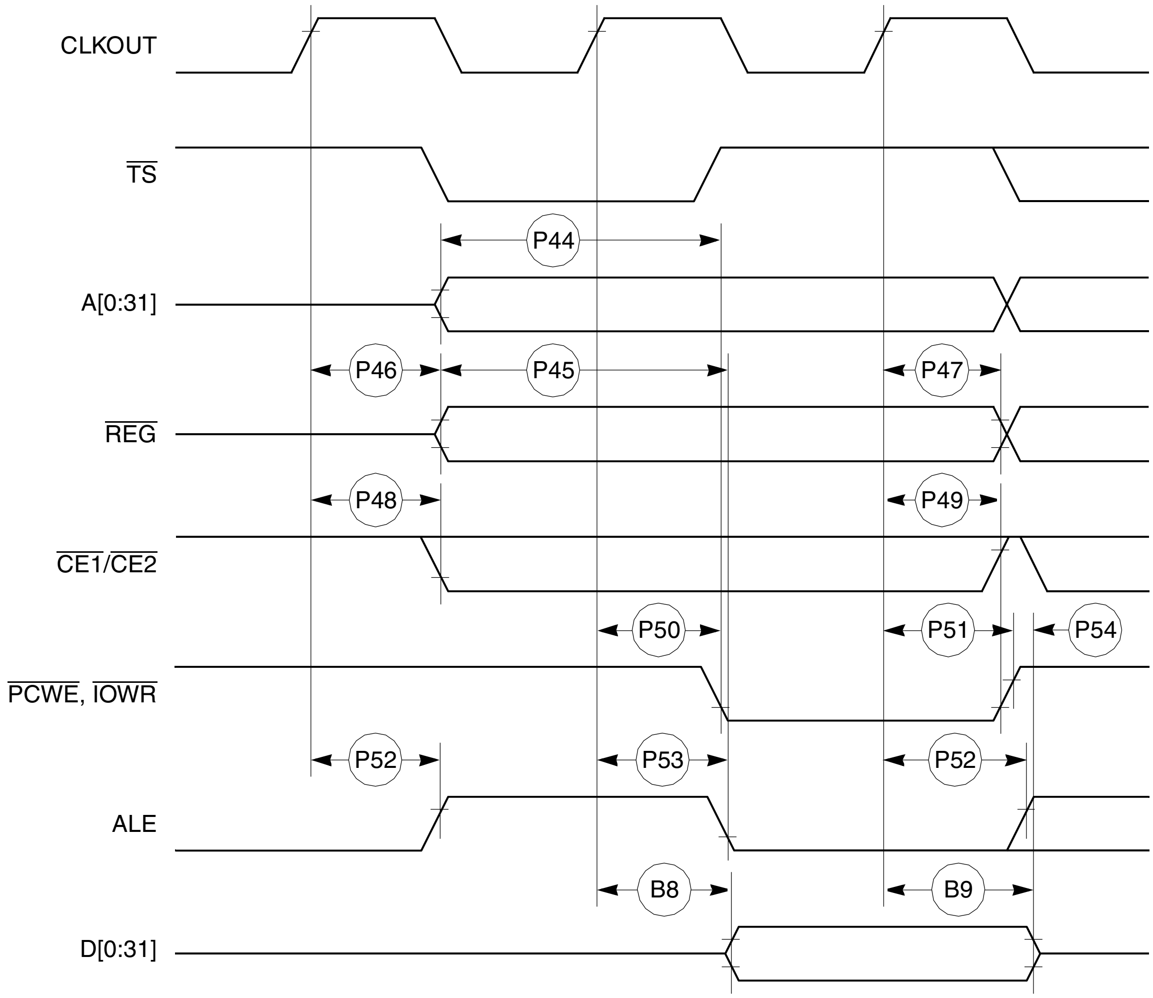


Figure 29. PCMCIA Access Cycles Timing External Bus Write

Figure 30 provides the PCMCIA $\overline{\text{WAIT}}$ signals detection timing.

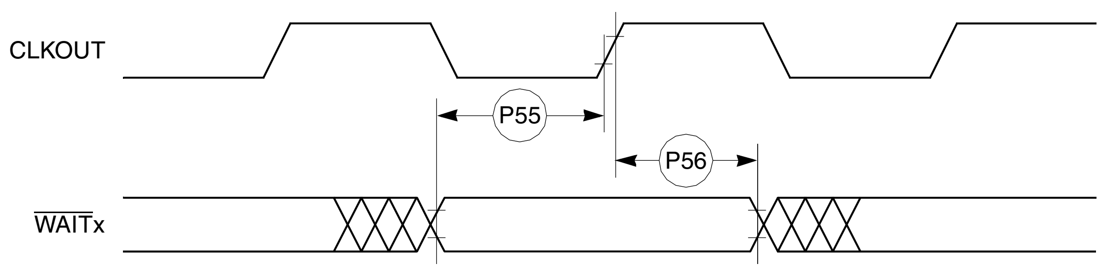


Figure 30. PCMCIA $\overline{\text{WAIT}}$ Signals Detection Timing

Table 14 shows the reset timing for the MPC885/MPC880.

Table 14. Reset Timing

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
R69	CLKOUT to $\overline{\text{HRESET}}$ high impedance (MAX = 0.00 × B1 + 20.00)	—	20.00	—	20.00	—	20.00	—	20.00	ns
R70	CLKOUT to $\overline{\text{SRESET}}$ high impedance (MAX = 0.00 × B1 + 20.00)	—	20.00	—	20.00	—	20.00	—	20.00	ns
R71	$\overline{\text{RSTCONF}}$ pulse width (MIN = 17.00 × B1)	515.20	—	425.00	—	257.60	—	212.50	—	ns
R72	—	—	—	—	—	—	—	—	—	—
R73	Configuration data to HRESET rising edge setup time (MIN = 15.00 × B1 + 50.00)	504.50	—	425.00	—	277.30	—	237.50	—	ns
R74	Configuration data to $\overline{\text{RSTCONF}}$ rising edge setup time (MIN = 0.00 × B1 + 350.00)	350.00	—	350.00	—	350.00	—	350.00	—	ns
R75	Configuration data hold time after $\overline{\text{RSTCONF}}$ negation (MIN = 0.00 × B1 + 0.00)	0.00	—	0.00	—	0.00	—	0.00	—	ns
R76	Configuration data hold time after $\overline{\text{HRESET}}$ negation (MIN = 0.00 × B1 + 0.00)	0.00	—	0.00	—	0.00	—	0.00	—	ns
R77	$\overline{\text{HRESET}}$ and $\overline{\text{RSTCONF}}$ asserted to data out drive (MAX = 0.00 × B1 + 25.00)	—	25.00	—	25.00	—	25.00	—	25.00	ns
R78	$\overline{\text{RSTCONF}}$ negated to data out high impedance (MAX = 0.00 × B1 + 25.00)	—	25.00	—	25.00	—	25.00	—	25.00	ns
R79	CLKOUT of last rising edge before chip three-states $\overline{\text{HRESET}}$ to data out high impedance (MAX = 0.00 × B1 + 25.00)	—	25.00	—	25.00	—	25.00	—	25.00	ns
R80	DSDI, DSCK setup (MIN = 3.00 × B1)	90.90	—	75.00	—	45.50	—	37.50	—	ns
R81	DSDI, DSCK hold time (MIN = 0.00 × B1 + 0.00)	0.00	—	0.00	—	0.00	—	0.00	—	ns
R82	$\overline{\text{SRESET}}$ negated to CLKOUT rising edge for DSDI and DSCK sample (MIN = 8.00 × B1)	242.40	—	200.00	—	121.20	—	100.00	—	ns

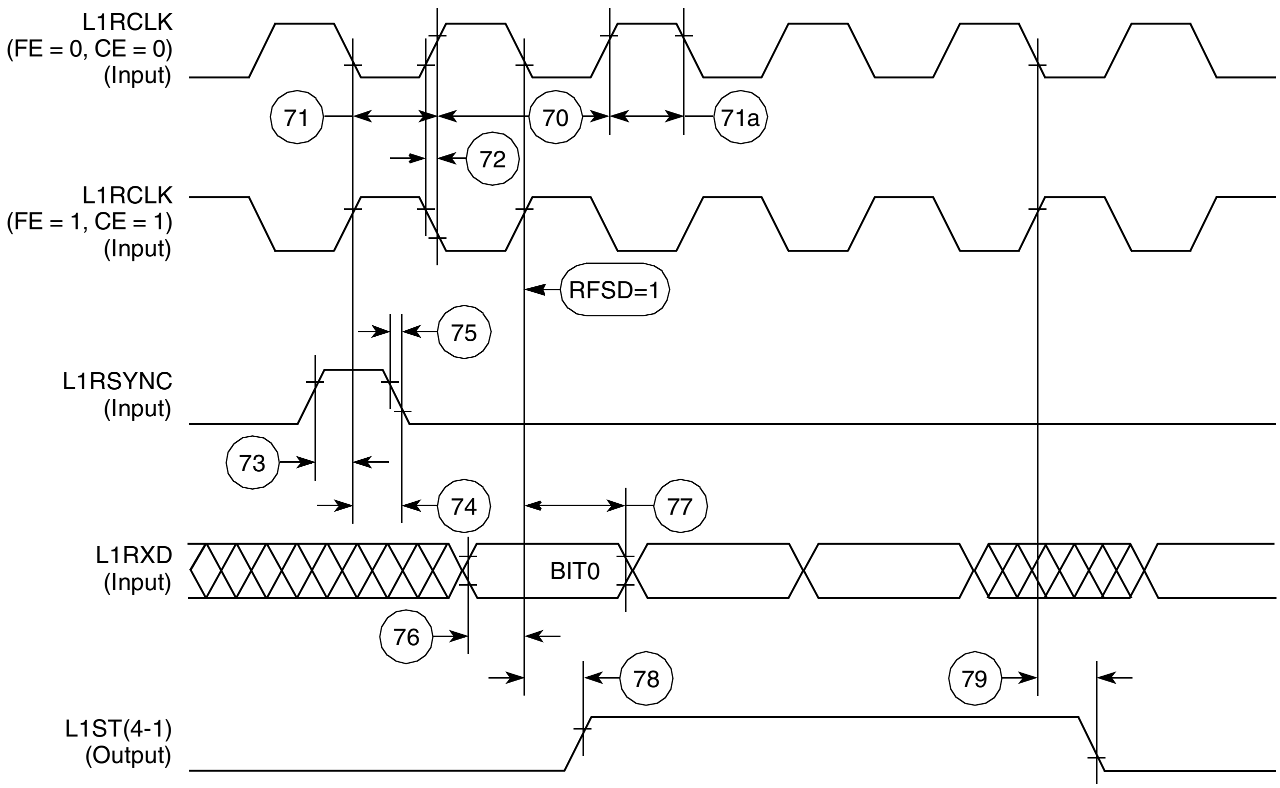


Figure 54. SI Receive Timing Diagram with Normal Clocking (DSC = 0)

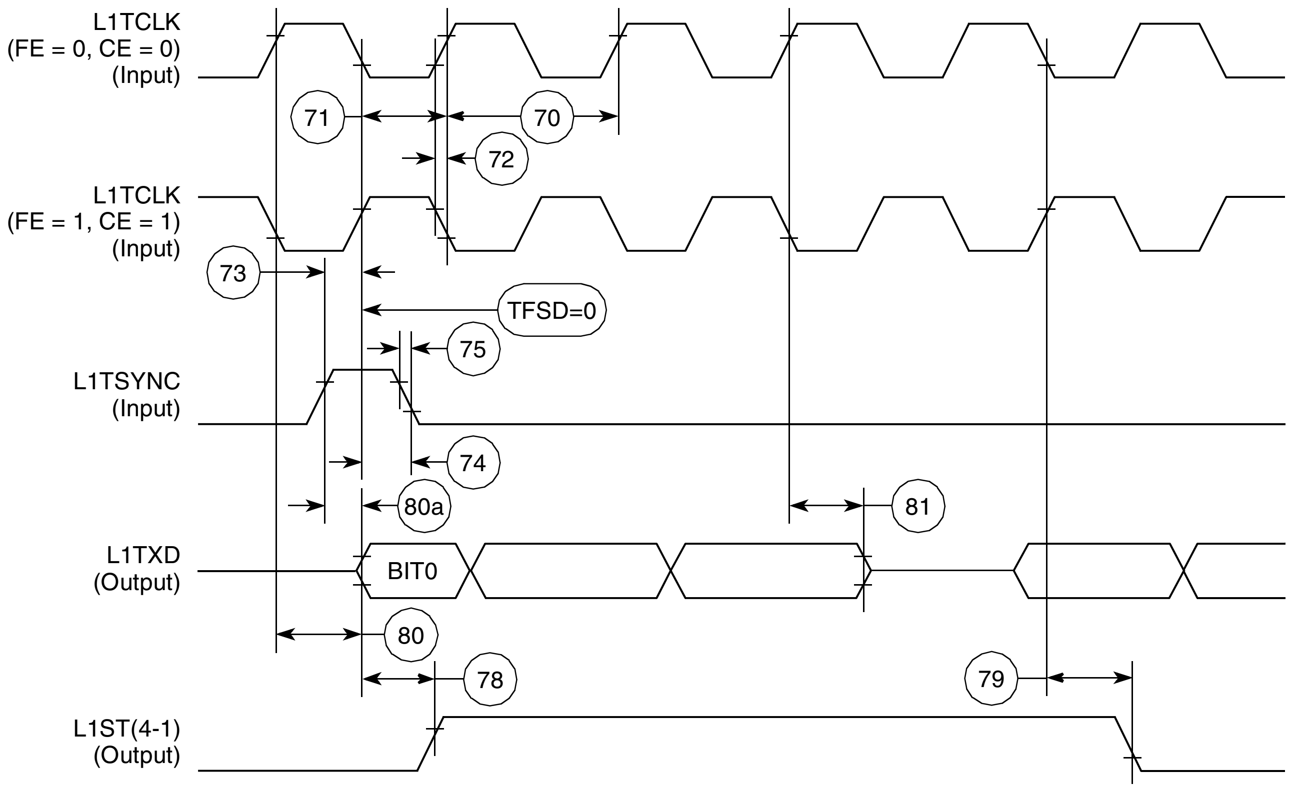


Figure 56. SI Transmit Timing Diagram (DSC = 0)

Figure 59 through Figure 61 show the NMSI timings.

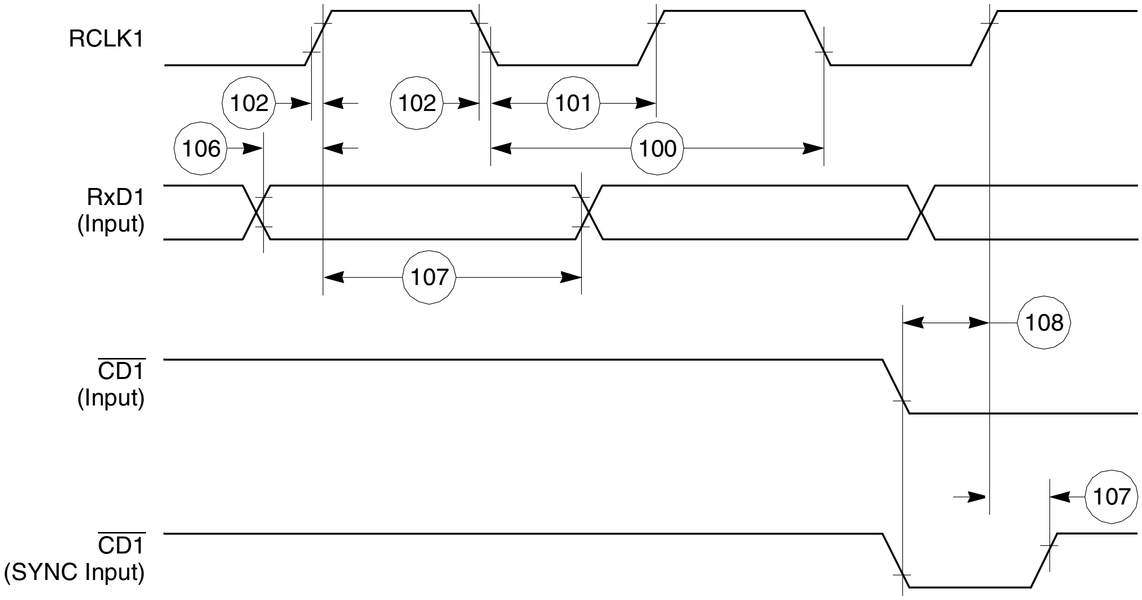


Figure 59. SCC NMSI Receive Timing Diagram

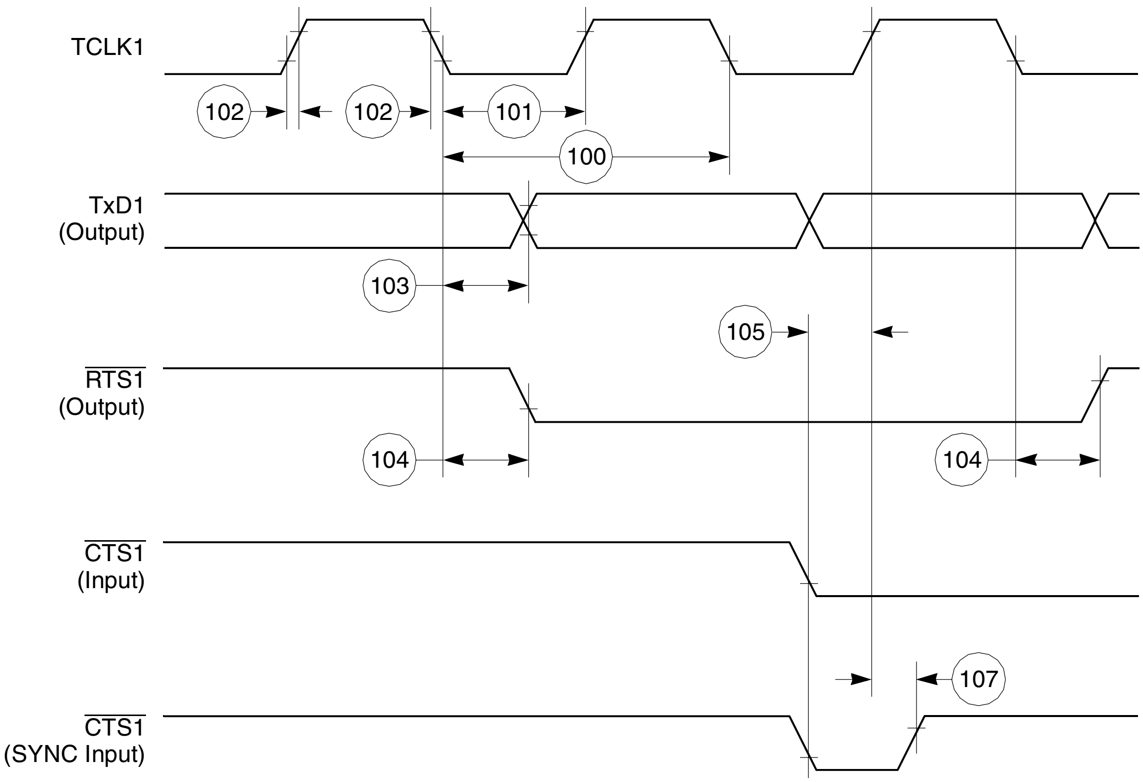
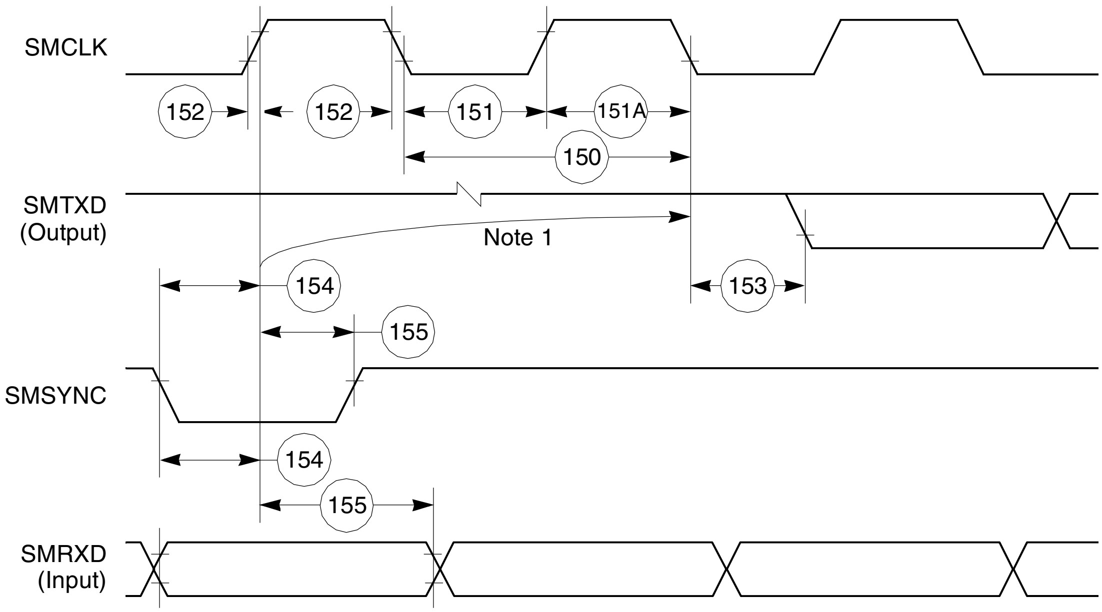


Figure 60. SCC NMSI Transmit Timing Diagram



Note:
1. This delay is equal to an integer number of character-length clocks.

Figure 65. SMC Transparent Timing Diagram

12.10 SPI Master AC Electrical Specifications

Table 26 provides the SPI master timings as shown in Figure 66 and Figure 67.

Table 26. SPI Master Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
160	MASTER cycle time	4	1024	t_{cyc}
161	MASTER clock (SCK) high or low time	2	512	t_{cyc}
162	MASTER data setup time (inputs)	15	—	ns
163	Master data hold time (inputs)	0	—	ns
164	Master data valid (after SCK edge)	—	10	ns
165	Master data hold time (outputs)	0	—	ns
166	Rise time output	—	15	ns
167	Fall time output	—	15	ns

Table 28. I²C Timing (SCL < 100 kHz) (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
210	SDL/SCL fall time	—	300	ns
211	Stop condition setup time	4.7	—	µs

[1] SCL frequency is given by SCL = BRGCLK_frequency/((BRG register + 3) × pre_scaler × 2).
The ratio SyncClk/(BRGCLK/pre_scaler) must be greater or equal to 4/1.

Table 29 provides the I²C (SCL > 100 kHz) timings.

Table 29. I²C Timing (SCL > 100 kHz)

Num	Characteristic	Expression	All Frequencies		Unit
			Min	Max	
200	SCL clock frequency (slave)	fSCL	0	BRGCLK/48	Hz
200	SCL clock frequency (master)[1]	fSCL	BRGCLK/16512	BRGCLK/48	Hz
202	Bus free time between transmissions	—	1/(2.2 × fSCL)	—	s
203	Low period of SCL	—	1/(2.2 × fSCL)	—	s
204	High period of SCL	—	1/(2.2 × fSCL)	—	s
205	Start condition setup time	—	1/(2.2 × fSCL)	—	s
206	Start condition hold time	—	1/(2.2 × fSCL)	—	s
207	Data hold time	—	0	—	s
208	Data setup time	—	1/(40 × fSCL)	—	s
209	SDL/SCL rise time	—	—	1/(10 × fSCL)	s
210	SDL/SCL fall time	—	—	1/(33 × fSCL)	s
211	Stop condition setup time	—	1/2(2.2 × fSCL)	—	s

[1] SCL frequency is given by SCL = BrgClk_frequency/((BRG register + 3) × pre_scaler × 2).
The ratio SyncClk/(Brg_Clk/pre_scaler) must be greater or equal to 4/1.

Figure 70 shows the I²C bus timing.

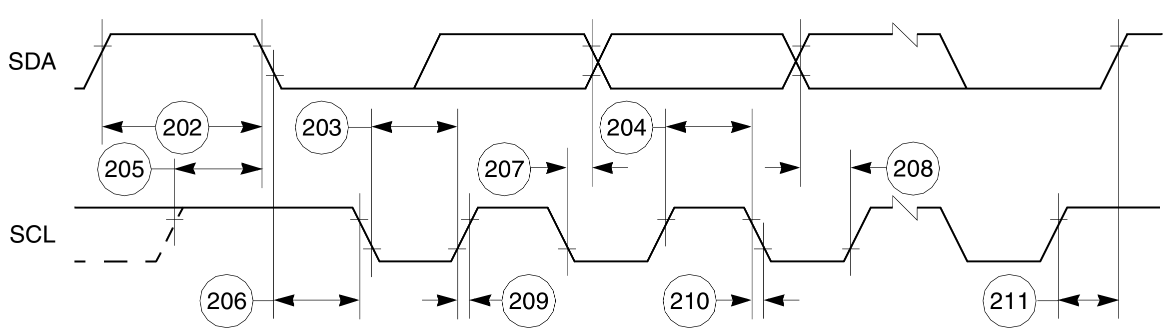


Figure 70. I²C Bus Timing Diagram

14 USB Electrical Characteristics

This section provides the AC timings for the USB interface.

14.1 USB Interface AC Timing Specifications

The USB Port uses the transmit clock on SCC1. Table 33 lists the USB interface timings.

Table 33. USB Interface AC Timing Specifications

Name	Characteristic	All Frequencies		Unit
		Min	Max	
US1	USBCLK frequency of operation[1] Low speed Full speed	 6 48		 MHz MHz
US4	USBCLK duty cycle (measured at 1.5 V)	45	55	%

[1] USBCLK accuracy should be ±500 ppm or better. USBCLK may be stopped to conserve power.

15 FEC Electrical Characteristics

This section provides the AC electrical specifications for the fast Ethernet controller (FEC). Note that the timing specifications for the MII signals are independent of system clock frequency (part speed designation). Also, MII signals use TTL signal levels compatible with devices operating at either 5.0 or 3.3 V.

15.1 MII and Reduced MII Receive Signal Timing

The receiver functions correctly up to a MII_RX_CLK maximum frequency of 25 MHz + 1%. The reduced MII (RMII) receiver functions correctly up to a RMII_REFCLK maximum frequency of 50 MHz + 1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_RX_CLK frequency – 1%.

Table 34 provides information on the MII and RMII receive signal timing.

Table 34. MII Receive Signal Timing

Num	Characteristic	Min	Max	Unit
M1	MII_RXD[3:0], MII_RX_DV, MII_RX_ERR to MII_RX_CLK setup	5	—	ns
M2	MII_RX_CLK to MII_RXD[3:0], MII_RX_DV, MII_RX_ER hold	5	—	ns
M3	MII_RX_CLK pulse width high	35%	65%	MII_RX_CLK period
M4	MII_RX_CLK pulse width low	35%	65%	MII_RX_CLK period
M1_RMII	RMII_RXD[1:0], RMII_CRS_DV, RMII_RX_ERR to RMII_REFCLK setup	4	—	ns
M2_RMII	RMII_REFCLK to RMII_RXD[1:0], RMII_CRS_DV, RMII_RX_ERR hold	2	—	ns

Table 39 contains a list of the MPC885 input and output signals and shows multiplexing and pin assignments.

Table 39. Pin Assignments

Name	Pin Number	Type
A[0:31]	M16, N18, N19, M19, M17, M18, L16, L19, L17, L18, K19, K18, K17, K16, J19, J17, J18, J16, E19, H18, H17, G19, F17, G17, H16, F19, D19, H19, E18, G18, F18, D18	Bidirectional Three-state
D[0:31]	P2, M1, L1, K2, N1, K4, H3, F2, P1, L4, L3, L2, N3, N2, K3, K1, J2, M4, J1, J3, H2, H1, J4, M3, G2, G1, G3, M2, H4, F1, E1, F3	Bidirectional Three-state
TSIZ0, $\overline{\text{REG}}$	G16	Bidirectional Three-state
TSIZ1	E17	Bidirectional Three-state
RD/$\overline{\text{WR}}$	D13	Bidirectional Three-state
$\overline{\text{BURST}}$	C10	Bidirectional Three-state
$\overline{\text{BDIP}}$, $\overline{\text{GPL\_B5}}$	A13	Output
$\overline{\text{TS}}$	A12	Bidirectional Active pull-up
$\overline{\text{TA}}$	C12	Bidirectional Active pull-up
$\overline{\text{TEA}}$	B12	Open-drain
$\overline{\text{BI}}$	D12	Bidirectional Active pull-up
$\overline{\text{IRQ2}}$, $\overline{\text{RSV}}$	B10	Bidirectional Three-state
$\overline{\text{IRQ4}}$, $\overline{\text{KR}}$, $\overline{\text{RETRY}}$, SPKROUT	C7	Bidirectional Three-state
$\overline{\text{CR}}$, $\overline{\text{IRQ3}}$	A11	Input
$\overline{\text{BR}}$	D11	Bidirectional
$\overline{\text{BG}}$	C11	Bidirectional
$\overline{\text{BB}}$	B11	Bidirectional Active pull-up
FRZ, $\overline{\text{IRQ6}}$	D10	Bidirectional
$\overline{\text{IRQ0}}$	N4	Input
$\overline{\text{IRQ1}}$	P3	Input
$\overline{\text{IRQ7}}$	P4	Input
$\overline{\text{CS}}$[0:5]	B14, C14, A15, D14, C16, A16	Output
$\overline{\text{CS6}}$, $\overline{\text{CE1\_B}}$	D15	Output
$\overline{\text{CS7}}$, $\overline{\text{CE2\_B}}$	B16	Output

Table 39. Pin Assignments (continued)

Name	Pin Number	Type
ALE_B, DSCK/AT1	D8	Bidirectional Three-state
IP_B[0:1], IWP[0:1], VFLS[0:1]	A9, D9	Bidirectional
IP_B2, $\overline{\text{IOIS16\_B}}$, AT2	C8	Bidirectional Three-state
IP_B3, IWP2, VF2	C9	Bidirectional
IP_B4, LWP0, VF0	B9	Bidirectional
IP_B5, LWP1, VF1	A10	Bidirectional
IP_B6, DSDI, AT0	A8	Bidirectional Three-state
IP_B7, $\overline{\text{PTR}}$, AT3	B8	Bidirectional Three-state
OP0, UtpClk_Split[1]	B6	Bidirectional
OP1	C6	Output
OP2, MODCK1, $\overline{\text{STS}}$	D6	Bidirectional
OP3, MODCK2, DSDO	A6	Bidirectional
BADDR30, $\overline{\text{REG}}$	A7	Output
BADDR[28:29]	C5, B5	Output
$\overline{\text{AS}}$	D7	Input
PA15, USBRXD	N16	Bidirectional
PA14, $\overline{\text{USBOE}}$	P17	Bidirectional (Optional: open-drain)
PA13, RXD2	W11	Bidirectional
PA12, TXD2	P16	Bidirectional (Optional: open-drain)
PA11, RXD4, MII1-TXD0, RMII1-TXD0	W9	Bidirectional (Optional: open-drain)
PA10, MII1-TXER, TIN4, CLK7	W17	Bidirectional (Optional: open-drain)
PA9, L1TXDA, RXD3	T15	Bidirectional (Optional: open-drain)
PA8, L1RXDA, TXD3	W15	Bidirectional (Optional: open-drain)
PA7, CLK1, L1RCLKA, BRGO1, TIN1	V14	Bidirectional
PA6, CLK2, $\overline{\text{TOUT1}}$	U13	Bidirectional
PA5, CLK3, L1TCLKA, BRGO2, TIN2	W13	Bidirectional

Table 39. Pin Assignments (continued)

Name	Pin Number	Type
PA4, $\overline{CTS4}$, MII1-TXD1, RMII1-TXD1	U4	Bidirectional
PA3, MII1-RXER, RMII1-RXER, BRGO3	W2	Bidirectional
PA2, MII1-RXDV, RMII1-CRS_DV, TXD4	T4	Bidirectional
PA1, MII1-RXD0, RMII1-RXD0, BRGO4	U1	Bidirectional
PA0, MII1-RXD1, RMII1-RXD1, $\overline{TOUT4}$	U3	Bidirectional
PB31, $\overline{SPISEL}$, MII1-TXCLK, RMII1-REFCLK	V3	Bidirectional (Optional: open-drain)
PB30, SPICLK	P18	Bidirectional (Optional: open-drain)
PB29, SPIMOSI	T19	Bidirectional (Optional: open-drain)
PB28, SPIMISO, BRGO4	V19	Bidirectional (Optional: open-drain)
PB27, I2CSDA, BRGO1	U19	Bidirectional (Optional: open-drain)
PB26, I2CSCL, BRGO2	R17	Bidirectional (Optional: open-drain)
PB25, RXADDR3[1], TXADDR3, SMTXD1	V17	Bidirectional (Optional: open-drain)
PB24, TXADDR3[1], RXADDR3, SMRXD1	U16	Bidirectional (Optional: open-drain)
PB23, TXADDR2[1], RXADDR2, $\overline{SDACK1}$, $\overline{SMSYN1}$	W16	Bidirectional (Optional: open-drain)
PB22, TXADDR4[1], RXADDR4, $\overline{SDACK2}$, $\overline{SMSYN2}$	V15	Bidirectional (Optional: open-drain)
PB21, SMTXD2, TXADDR1[1], BRG01, RXADDR1, PHSEL[1]	U14	Bidirectional (Optional: open-drain)
PB20, SMRXD2, L1CLKOA, TXADDR0[1], RXADDR0, PHSEL[0]	T13	Bidirectional (Optional: open-drain)
PB19, MII1-RXD3, $\overline{RTS4}$	V13	Bidirectional (Optional: open-drain)
PB18, RXADDR4[1], TXADDR4, $\overline{RTS2}$, L1ST2	T12	Bidirectional (Optional: open-drain)

Table 39. Pin Assignments (continued)

Name	Pin Number	Type
PD5, CLK8, L1TCLKB, UTPB6	V6	Bidirectional
PD4, CLK4, UTPB7	W4	Bidirectional
PD3, CLK7, TIN4, SOC	T9	Bidirectional
PE31, CLK8, L1TCLKB, MII1-RXCLK	U9	Bidirectional (Optional: open-drain)
PE30, L1RXDB, MII1-RXD2	W7	Bidirectional (Optional: open-drain)
PE29, MII2-CRS	T8	Bidirectional (Optional: open-drain)
PE28, $\overline{\text{TOUT3}}$, MII2-COL	V5	Bidirectional (Optional: open-drain)
PE27, $\overline{\text{RTS3}}$, L1RQB, MII2-RXER, RMII2-RXER	V4	Bidirectional (Optional: open-drain)
PE26, L1CLKOB, MII2-RXDV, RMII2-CRS_DV	T1	Bidirectional (Optional: open-drain)
PE25, RXD4, MII2-RXD3, L1ST2	T3	Bidirectional (Optional: open-drain)
PE24, SMRXD1, BRGO1, MII2-RXD2	V8	Bidirectional (Optional: open-drain)
PE23, $\overline{\text{SMSYN2}}$, TXD4, MII2-RXCLK, L1ST1	V2	Bidirectional (Optional: open-drain)
PE22, $\overline{\text{TOUT2}}$, MII2-RXD1, RMII2-RXD1, $\overline{\text{SDACK1}}$	V1	Bidirectional (Optional: open-drain)
PE21, SMRXD2, $\overline{\text{TOUT1}}$, MII2-RXD0, RMII2-RXD0, $\overline{\text{RTS3}}$	V9	Bidirectional (Optional: open-drain)
PE20, L1RSYNCA, SMTXD2, $\overline{\text{CTS3}}$, MII2-TXER	R4	Bidirectional (Optional: open-drain)
PE19, L1TXDB, MII2-TXEN, RMII2-TXEN	T6	Bidirectional (Optional: open-drain)
PE18, L1TSYNCA, SMTXD1, MII2-TXD3	R1	Bidirectional (Optional: open-drain)
PE17, TIN3, CLK5, BRGO3, $\overline{\text{SMSYN1}}$, MII2-TXD2	W8	Bidirectional (Optional: open-drain)
PE16, L1RCLKB, CLK6, TXD3, MII2-TXCLK, RMII2-REFCLK	T7	Bidirectional (Optional: open-drain)
PE15, $\overline{\text{TGATE1}}$, MII2-TXD1, RMII2-TXD1	W6	Bidirectional