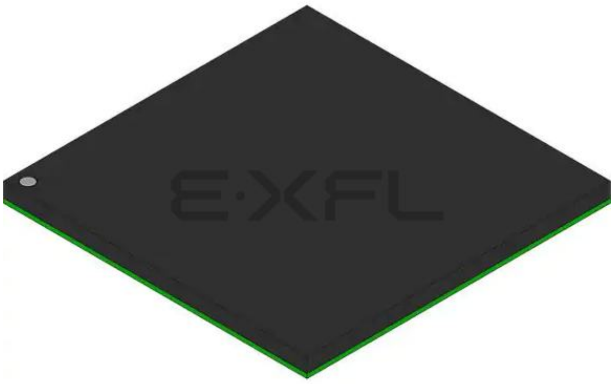

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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | MPC8xx |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 80MHz |
| Co-Processors/DSP | Communications; CPM |
| RAM Controllers | DRAM |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10Mbps (2), 10/100Mbps (2) |
| SATA | - |
| USB | USB 2.0 (1) |
| Voltage - I/O | 3.3V |
| Operating Temperature | 0°C ~ 95°C (TA) |
| Security Features | Cryptography |
| Package / Case | 357-BBGA |
| Supplier Device Package | 357-PBGA (25x25) |
| Purchase URL | https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc880zp80 |

# 1 Overview

The MPC885/MPC880 is a versatile single-chip integrated microprocessor and peripheral combination that can be used in a variety of controller applications and communications and networking systems. The MPC885/MPC880 provides enhanced ATM functionality, an additional fast Ethernet controller, a USB, and an encryption block.

Table 1 shows the functionality supported by MPC885/MPC880.

**Table 1. MPC885 Family**

| Part | Cache (Kbytes) | | Ethernet | | SCC | SMC | USB | ATM Support | Security Engine |
|---|---|---|---|---|---|---|---|---|---|
| | I Cache | D Cache | 10BaseT | 10/100 | | | | | |
| MPC885 | 8 | 8 | Up to 3 | 2 | 3 | 2 | 1 | Serial ATM and UTOPIA interface | Yes |
| MPC880 | 8 | 8 | Up to 2 | 2 | 2 | 2 | 1 | Serial ATM and UTOPIA interface | No |

# 2 Features

The MPC885/MPC880 is comprised of three modules that each use the 32-bit internal bus: a MPC8xx core, a system integration unit (SIU), and a communications processor module (CPM).

The following list summarizes the key MPC885/MPC880 features:

- Embedded MPC8xx core up to 133 MHz
- Maximum frequency operation of the external bus is 80 MHz (in 1:1 mode)
  - The 133-MHz core frequency supports 2:1 mode only.
  - The 66-/80-MHz core frequencies support both the 1:1 and 2:1 modes.
- Single-issue, 32-bit core (compatible with the Power Architecture definition) with thirty-two 32-bit general-purpose registers (GPRs)
  - The core performs branch prediction with conditional prefetch and without conditional execution.
  - 8-Kbyte data cache and 8-Kbyte instruction cache (see Table 1)
    - Instruction cache is two-way, set-associative with 256 sets in 2 blocks
    - Data cache is two-way, set-associative with 256 sets
    - Cache coherency for both instruction and data caches is maintained on 128-bit (4-word) cache blocks.
    - Caches are physically addressed, implement a least recently used (LRU) replacement algorithm, and are lockable on a cache block basis.
  - MMUs with 32-entry TLB, fully associative instruction and data TLBs
  - MMUs support multiple page sizes of 4, 16, and 512 Kbytes, and 8 Mbytes; 16 virtual address spaces and 16 protection groups
  - Advanced on-chip emulation debug mode

- Provides enhanced ATM functionality found on the MPC862 and MPC866 families and includes the following:
  - — Improved operation, administration and maintenance (OAM) support
  - — OAM performance monitoring (PM) support
  - — Multiple APC priority levels available to support a range of traffic pace requirements
  - — Port-to-port switching capability without the need for RAM-based microcode
  - — Simultaneous MII (100BaseT) and UTOPIA (half- or full -duplex) capability
  - — Optional statistical cell counters per PHY
  - — UTOPIA L2-compliant interface with added FIFO buffering to reduce the total cell transmission time and multi-PHY support. (The earlier UTOPIA L1 specification is also supported.)
  - — Parameter RAM for both SPI and $I^2C$ can be relocated without RAM-based microcode
  - — Supports full-duplex UTOPIA master (ATM side) and slave (PHY side) operations using a split bus
  - — AAL2/VBR functionality is ROM-resident
- Up to 32-bit data bus (dynamic bus sizing for 8, 16, and 32 bits)
- Thirty-two address lines
- Memory controller (eight banks)
  - — Contains complete dynamic RAM (DRAM) controller
  - — Each bank can be a chip select or $\overline{\text{RAS}}$ to support a DRAM bank
  - — Up to 30 wait states programmable per memory bank
  - — Glueless interface to DRAM, SIMMS, SRAM, EPROMs, Flash EPROMs, and other memory devices
  - — DRAM controller programmable to support most size and speed memory interfaces
  - — Four $\overline{\text{CAS}}$ lines, four $\overline{\text{WE}}$ lines, and one $\overline{\text{OE}}$ line
  - — Boot chip-select available at reset (options for 8-, 16-, or 32-bit memory)
  - — Variable block sizes (32 Kbytes–256 Mbytes)
  - — Selectable write protection
  - — On-chip bus arbitration logic
- General-purpose timers
  - — Four 16-bit timers or two 32-bit timers
  - — Gate mode can enable/disable counting.
  - — Interrupt can be masked on reference match and event capture
- Two fast Ethernet controllers (FEC)—Two 10/100 Mbps Ethernet/IEEE Std. 802.3™ CDMA/CS that interface through MII and/or RMII interfaces
- System integration unit (SIU)
  - — Bus monitor
  - — Software watchdog

- Periodic interrupt timer (PIT)
- Clock synthesizer
- Decrementer and time base
- Reset controller
- IEEE Std 1149.1™ test access port (JTAG)

- Security engine is optimized to handle all the algorithms associated with IPsec, SSL/TLS, SRTP, IEEE Std 802.11i™, and iSCSI processing. Available on the MPC885, the security engine contains a crypto-channel, a controller, and a set of crypto hardware accelerators (CHAs). The CHAs are:
  - Data encryption standard execution unit (DEU)
    - DES, 3DES
    - Two key (K1, K2, K1) or three key (K1, K2, K3)
    - ECB and CBC modes for both DES and 3DES
  - Advanced encryption standard unit (AESU)
    - Implements the Rijndael symmetric key cipher
    - ECB, CBC, and counter modes
    - 128-, 192-, and 256- bit key lengths
  - Message digest execution unit (MDEU)
    - SHA with 160- or 256-bit message digest
    - MD5 with 128-bit message digest
    - HMAC with either algorithm
  - Crypto-channel supporting multi-command descriptor chains
  - Integrated controller managing internal resources and bus mastering
  - Buffer size of 256 bytes for the DEU, AESU, and MDEU, with flow control for large data sizes
- Interrupts
  - Six external interrupt request (IRQ) lines
  - 12 port pins with interrupt capability
  - 23 internal interrupt sources
  - Programmable priority between SCCs
  - Programmable highest priority request
- Communications processor module (CPM)
  - RISC controller
  - Communication-specific commands (for example, GRACEFUL STOP TRANSMIT, ENTER HUNT MODE, and RESTART TRANSMIT)
  - Supports continuous mode transmission and reception on all serial channels
  - 8-Kbytes of dual-port RAM
  - Several serial DMA (SDMA) channels to support the CPM
  - Three parallel I/O registers with open-drain capability

# 5 Power Dissipation

Table 5 provides information on power dissipation. The modes are 1:1, where CPU and bus speeds are equal, and 2:1, where CPU frequency is twice bus speed.

**Table 5. Power Dissipation ($P_D$)**

| Die Revision | Bus Mode | CPU Frequency | Typical[1] | Maximum[2] | Unit |
|---|---|---|---|---|---|
| 0 | 1:1 | 66 MHz | 310 | 390 | mW |
| | | 80 MHz | 350 | 430 | mW |
| | 2:1 | 133 MHz | 430 | 495 | mW |

[1] Typical power dissipation at $V_{DDL}$ = $V_{DDSYN}$ = 1.8 V, and $V_{DDH}$ is at 3.3 V.
[2] Maximum power dissipation at $V_{DDL}$ = $V_{DDSYN}$ = 1.9 V, and $V_{DDH}$ is at 3.5 V.

**NOTE**

The values in Table 5 represent $V_{DDL}$-based power dissipation and do not include I/O power dissipation over $V_{DDH}$. I/O power dissipation varies widely by application due to buffer current, depending on external circuitry.

The $V_{DDSYN}$ power dissipation is negligible.

# 6 DC Characteristics

Table 6 provides the DC electrical characteristics for the MPC885/MPC880.

**Table 6. DC Electrical Specifications**

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Operating voltage | $V_{DDL}$ (core) | 1.7 | 1.9 | V |
| | $V_{DDH}$ (I/O) | 3.135 | 3.465 | V |
| | $V_{DDSYN}$[1] | 1.7 | 1.9 | V |
| | Difference between $V_{DDL}$ and $V_{DDSYN}$ | — | 100 | mV |
| Input high voltage (all inputs except EXTAL and EXTCLK)[2] | $V_{IH}$ | 2.0 | 3.465 | V |
| Input low voltage[3] | $V_{IL}$ | GND | 0.8 | V |
| EXTAL, EXTCLK input high voltage | $V_{IHC}$ | 0.7*($V_{DDH}$) | $V_{DDH}$ | V |
| Input leakage current, Vin = 5.5 V (except TMS, $\overline{TRST}$, DSCK and DSDI pins) for 5-V tolerant pins [2] | $I_{in}$ | — | 100 | µA |
| Input leakage current, $V_{in}$ = $V_{DDH}$ (except TMS, $\overline{TRST}$, DSCK, and DSDI) | $I_{In}$ | — | 10 | µA |
| Input leakage current, $V_{in}$ = 0 V (except TMS, $\overline{TRST}$, DSCK and DSDI pins) | $I_{In}$ | — | 10 | µA |
| Input capacitance[4] | $C_{in}$ | — | 20 | pF |

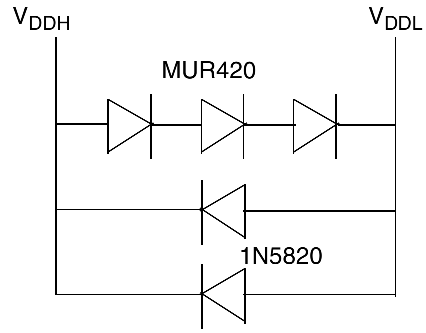


**Figure 5. Example Voltage Sequencing Circuit**

# 9 Layout Practices

Each $V_{DD}$ pin on the MPC885/MPC880 should be provided with a low-impedance path to the board's supply. Each GND pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The $V_{DD}$ power supply should be bypassed to ground using at least four 0.1 µF by-pass capacitors located as close as possible to the four sides of the package. Each board designed should be characterized and additional appropriate decoupling capacitors should be used if required. The capacitor leads and associated printed-circuit traces connecting to chip $V_{DD}$ and GND should be kept to less than half an inch per capacitor lead. At a minimum, a four-layer board employing two inner layers as $V_{DD}$ and GND planes should be used.

All output pins on the MPC885/MPC880 have fast rise and fall times. Printed-circuit (PC) trace interconnection length should be minimized in order to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the $V_{DD}$ and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins. For more information, please refer to the *MPC885 PowerQUICC™ Family Reference Manual*, Section 14.4.3, "Clock Synthesizer Power ($V_{DDSYN}$, $V_{SSSYN}$, $V_{SSSYN1}$)."

# 10 Bus Signal Timing

The maximum bus speed supported by the MPC885/MPC880 is 80 MHz. Higher-speed parts must be operated in half-speed bus mode (for example, an MPC885/MPC880 used at 133 MHz must be configured for a 66 MHz bus). Table 7 shows the frequency ranges for standard part frequencies in 1:1 bus mode, and Table 8 shows the frequency ranges for standard part frequencies in 2:1 bus mode.

**Table 9. Bus Operation Timings (continued)**

| Num | Characteristic | 33 MHz | | 40 MHz | | 66 MHz | | 80 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| B5 | CLKOUT fall time | — | 4.00 | — | 4.00 | — | 4.00 | — | 4.00 | ns |
| B7 | CLKOUT to A(0:31), BADDR(28:30), RD/$\overline{WR}$, $\overline{BURST}$, D(0:31) output hold (MIN = 0.25 × B1) | 7.60 | — | 6.30 | — | 3.80 | — | 3.13 | — | ns |
| B7a | CLKOUT to TSIZ(0:1), $\overline{REG}$, $\overline{RSV}$, $\overline{BDIP}$, PTR output hold (MIN = 0.25 × B1) | 7.60 | — | 6.30 | — | 3.80 | — | 3.13 | — | ns |
| B7b | CLKOUT to $\overline{BR}$, $\overline{BG}$, FRZ, VFLS(0:1), VF(0:2) IWP(0:2), LWP(0:1), $\overline{STS}$ output hold (MIN = 0.25 × B1) | 7.60 | — | 6.30 | — | 3.80 | — | 3.13 | — | ns |
| B8 | CLKOUT to A(0:31), BADDR(28:30) RD/$\overline{WR}$, $\overline{BURST}$, D(0:31) valid (MAX = 0.25 × B1 + 6.3) | — | 13.80 | — | 12.50 | — | 10.00 | — | 9.43 | ns |
| B8a | CLKOUT to TSIZ(0:1), $\overline{REG}$, $\overline{RSV}$, AT(0:3) $\overline{BDIP}$, PTR valid (MAX = 0.25 × B1 + 6.3) | — | 13.80 | — | 12.50 | — | 10.00 | — | 9.43 | ns |
| B8b | CLKOUT to $\overline{BR}$, $\overline{BG}$, VFLS(0:1), VF(0:2), IWP(0:2), FRZ, LWP(0:1), $\overline{STS}$ valid [4] (MAX = 0.25 × B1 + 6.3) | — | 13.80 | — | 12.50 | — | 10.00 | — | 9.43 | ns |
| B9 | CLKOUT to A(0:31), BADDR(28:30), RD/$\overline{WR}$, $\overline{BURST}$, D(0:31), TSIZ(0:1), $\overline{REG}$, $\overline{RSV}$, AT(0:3), PTR High-Z (MAX = 0.25 × B1 + 6.3) | 7.60 | 13.80 | 6.30 | 12.50 | 3.80 | 10.00 | 3.13 | 9.43 | ns |
| B11 | CLKOUT to $\overline{TS}$, $\overline{BB}$ assertion (MAX = 0.25 × B1 + 6.0) | 7.60 | 13.60 | 6.30 | 12.30 | 3.80 | 9.80 | 3.13 | 9.13 | ns |
| B11a | CLKOUT to $\overline{TA}$, $\overline{BI}$ assertion (when driven by the memory controller or PCMCIA interface) (MAX = 0.00 × B1 + 9.30[1]) | 2.50 | 9.30 | 2.50 | 9.30 | 2.50 | 9.30 | 2.50 | 9.30 | ns |
| B12 | CLKOUT to $\overline{TS}$, $\overline{BB}$ negation (MAX = 0.25 × B1 + 4.8) | 7.60 | 12.30 | 6.30 | 11.00 | 3.80 | 8.50 | 3.13 | 7.92 | ns |
| B12a | CLKOUT to $\overline{TA}$, $\overline{BI}$ negation (when driven by the memory controller or PCMCIA interface) (MAX = 0.00 × B1 + 9.00) | 2.50 | 9.00 | 2.50 | 9.00 | 2.50 | 9.00 | 2.5 | 9.00 | ns |
| B13 | CLKOUT to $\overline{TS}$, $\overline{BB}$ High-Z (MIN = 0.25 × B1) | 7.60 | 21.60 | 6.30 | 20.30 | 3.80 | 14.00 | 3.13 | 12.93 | ns |
| B13a | CLKOUT to $\overline{TA}$, $\overline{BI}$ High-Z (when driven by the memory controller or PCMCIA interface) (MIN = 0.00 × B1 + 2.5) | 2.50 | 15.00 | 2.50 | 15.00 | 2.50 | 15.00 | 2.5 | 15.00 | ns |
| B14 | CLKOUT to $\overline{TEA}$ assertion (MAX = 0.00 × B1 + 9.00) | 2.50 | 9.00 | 2.50 | 9.00 | 2.50 | 9.00 | 2.50 | 9.00 | ns |
| B15 | CLKOUT to $\overline{TEA}$ High-Z (MIN = 0.00 × B1 + 2.50) | 2.50 | 15.00 | 2.50 | 15.00 | 2.50 | 15.00 | 2.50 | 15.00 | ns |
| B16 | $\overline{TA}$, $\overline{BI}$ valid to CLKOUT (setup time) (MIN = 0.00 × B1 + 6.00) | 6.00 | — | 6.00 | — | 6.00 | — | 6 | — | ns |
| B16a | $\overline{TEA}$, $\overline{KR}$, $\overline{RETRY}$, $\overline{CR}$ valid to CLKOUT (setup time) (MIN = 0.00 × B1 + 4.5) | 4.50 | — | 4.50 | — | 4.50 | — | 4.50 | — | ns |

**Table 9. Bus Operation Timings (continued)**

| Num | Characteristic | 33 MHz | | 40 MHz | | 66 MHz | | 80 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| B36 | A(0:31), BADDR(28:30), and D(0:31) to $\overline{\text{GPL}}$ valid, as requested by control bit GxT4 in the corresponding word in the UPM (MIN = 0.25 × B1 – 2.00) | 5.60 | — | 4.30 | — | 1.80 | — | 1.13 | — | ns |
| B37 | UPWAIT valid to CLKOUT falling edge[9] (MIN = 0.00 × B1 + 6.00) | 6.00 | — | 6.00 | — | 6.00 | — | 6.00 | — | ns |
| B38 | CLKOUT falling edge to UPWAIT valid [9] (MIN = 0.00 × B1 + 1.00) | 1.00 | — | 1.00 | — | 1.00 | — | 1.00 | — | ns |
| B39 | $\overline{\text{AS}}$ valid to CLKOUT rising edge[10] (MIN = 0.00 × B1 + 7.00) | 7.00 | — | 7.00 | — | 7.00 | — | 7.00 | — | ns |
| B40 | A(0:31), TSIZ(0:1), RD/$\overline{\text{WR}}$, $\overline{\text{BURST}}$, valid to CLKOUT rising edge (MIN = 0.00 × B1 + 7.00) | 7.00 | — | 7.00 | — | 7.00 | — | 7.00 | — | ns |
| B41 | $\overline{\text{TS}}$ valid to CLKOUT rising edge (setup time) (MIN = 0.00 × B1 + 7.00) | 7.00 | — | 7.00 | — | 7.00 | — | 7.00 | — | ns |
| B42 | CLKOUT rising edge to $\overline{\text{TS}}$ valid (hold time) (MIN = 0.00 × B1 + 2.00) | 2.00 | — | 2.00 | — | 2.00 | — | 2.00 | — | ns |
| B43 | $\overline{\text{AS}}$ negation to memory controller signals negation (MAX = TBD) | — | TBD | — | TBD | — | TBD | — | TBD | ns |

1 For part speeds above 50 MHz, use 9.80 ns for B11a.
2 The timing required for $\overline{\text{BR}}$ input is relevant when the MPC885/MPC880 is selected to work with the internal bus arbiter. The timing for $\overline{\text{BG}}$ input is relevant when the MPC885/MPC880 is selected to work with the external bus arbiter.
3 For part speeds above 50 MHz, use 2 ns for B17.
4 The D(0:31) input timings B18 and B19 refer to the rising edge of the CLKOUT in which the $\overline{\text{TA}}$ input signal is asserted.
5 For part speeds above 50 MHz, use 2 ns for B19.
6 The D(0:31) input timings B20 and B21 refer to the falling edge of the CLKOUT. This timing is valid only for read accesses controlled by chip-selects under control of the user-programmable machine (UPM) in the memory controller, for data beats where DLT3 = 1 in the RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)
7 This formula applies to bus operation up to 50 MHz.
8 The timing B30 refers to $\overline{\text{CS}}$ when ACS = 00 and to $\overline{\text{CS}}$ and $\overline{\text{WE}}$(0:3) when CSNT = 0.
9 The signal UPWAIT is considered asynchronous to the CLKOUT and synchronized internally. The timings specified in B37 and B38 are specified to enable the freeze of the UPM output signals as described in Figure 21.
10 The $\overline{\text{AS}}$ signal is considered asynchronous to the CLKOUT. The timing B39 is specified in order to allow the behavior specified in Figure 24.

Figure 6 provides the control timing diagram.

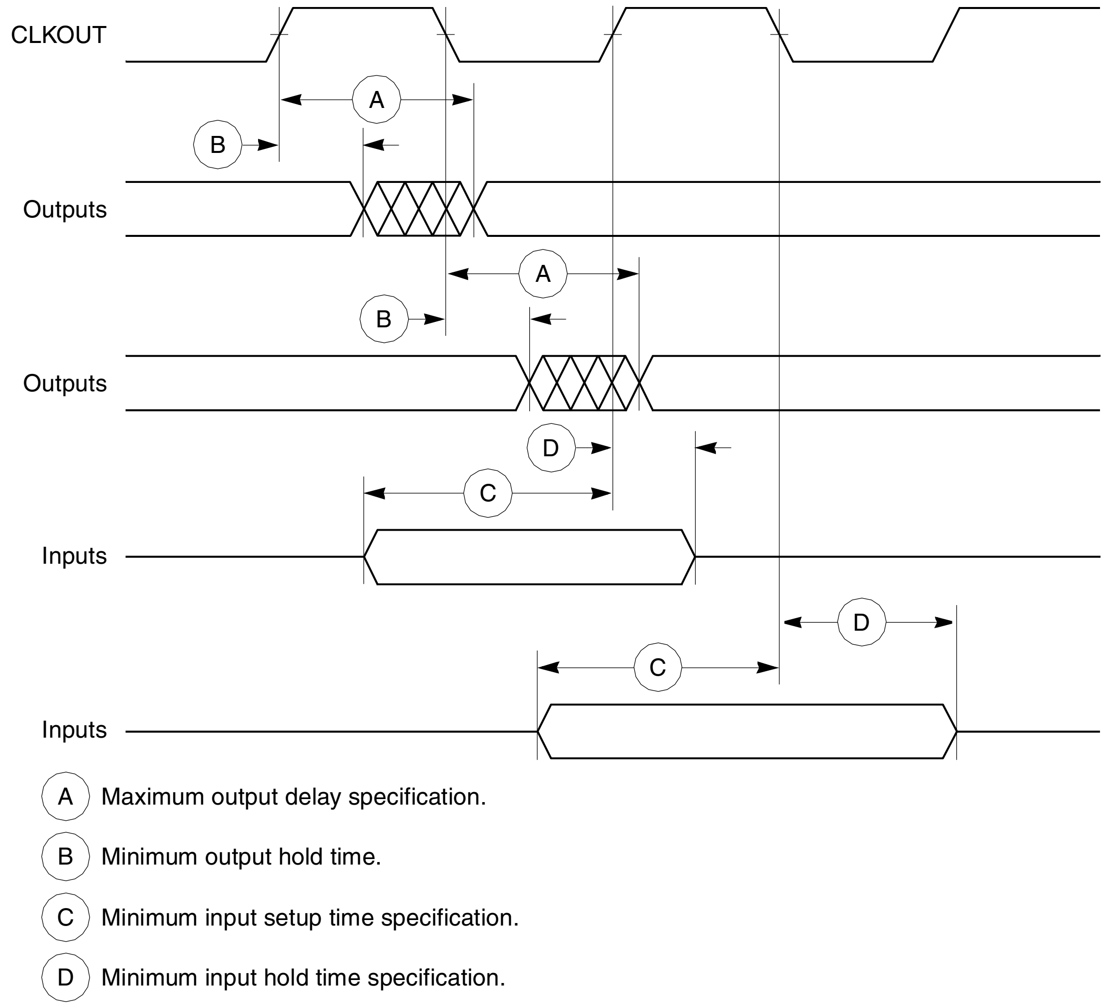


**Figure 6. Control Timing**

Figure 7 provides the timing for the external clock.

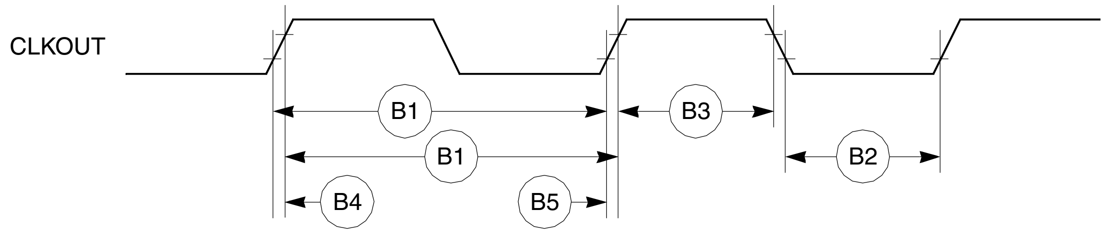


**Figure 7. External Clock Timing**

Table 13 shows the debug port timing for the MPC885/MPC880.

**Table 13. Debug Port Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| D61 | DSCK cycle time | $3 \times T_{CLOCKOUT}$ | — | — |
| D62 | DSCK clock pulse width | $1.25 \times T_{CLOCKOUT}$ | — | — |
| D63 | DSCK rise and fall times | 0.00 | 3.00 | ns |
| D64 | DSDI input data setup time | 8.00 | — | ns |
| D65 | DSDI data hold time | 5.00 | — | ns |
| D66 | DSCK low to DSDO data valid | 0.00 | 15.00 | ns |
| D67 | DSCK low to DSDO invalid | 0.00 | 2.00 | ns |

Figure 33 provides the input timing for the debug port clock.

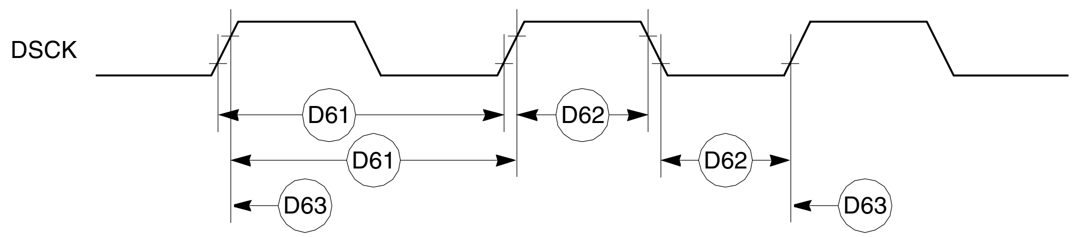


**Figure 33. Debug Port Clock Input Timing**

Figure 34 provides the timing for the debug port.

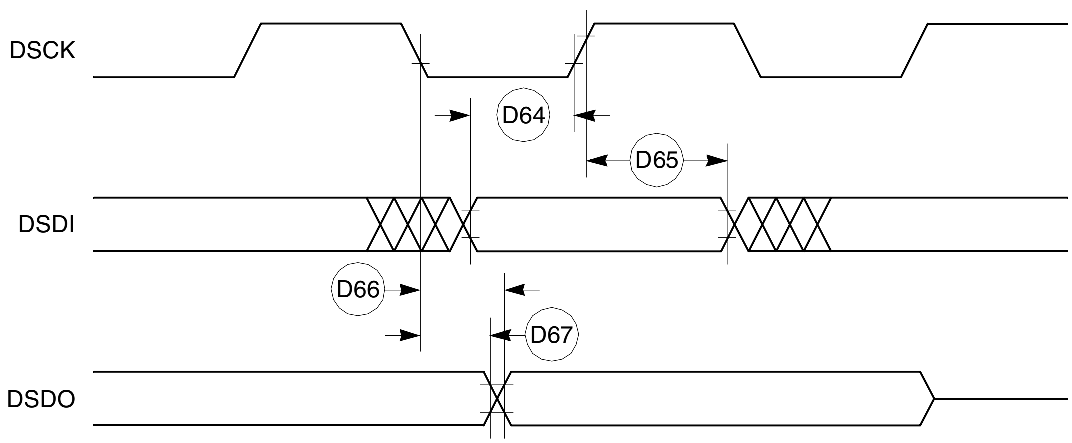


**Figure 34. Debug Port Timings**

# 11 IEEE 1149.1 Electrical Specifications

Table 15 provides the JTAG timings for the MPC885/MPC880 shown in Figure 38 through Figure 41.

**Table 15. JTAG Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| J82 | TCK cycle time | 100.00 | — | ns |
| J83 | TCK clock pulse width measured at 1.5 V | 40.00 | — | ns |
| J84 | TCK rise and fall times | 0.00 | 10.00 | ns |
| J85 | TMS, TDI data setup time | 5.00 | — | ns |
| J86 | TMS, TDI data hold time | 25.00 | — | ns |
| J87 | TCK low to TDO data valid | — | 27.00 | ns |
| J88 | TCK low to TDO data invalid | 0.00 | — | ns |
| J89 | TCK low to TDO high impedance | — | 20.00 | ns |
| J90 | $\overline{\text{TRST}}$ assert time | 100.00 | — | ns |
| J91 | $\overline{\text{TRST}}$ setup time to TCK low | 40.00 | — | ns |
| J92 | TCK falling edge to output valid | — | 50.00 | ns |
| J93 | TCK falling edge to output valid out of high impedance | — | 50.00 | ns |
| J94 | TCK falling edge to output high impedance | — | 50.00 | ns |
| J95 | Boundary scan input valid to TCK rising edge | 50.00 | — | ns |
| J96 | TCK rising edge to boundary scan input invalid | 50.00 | — | ns |

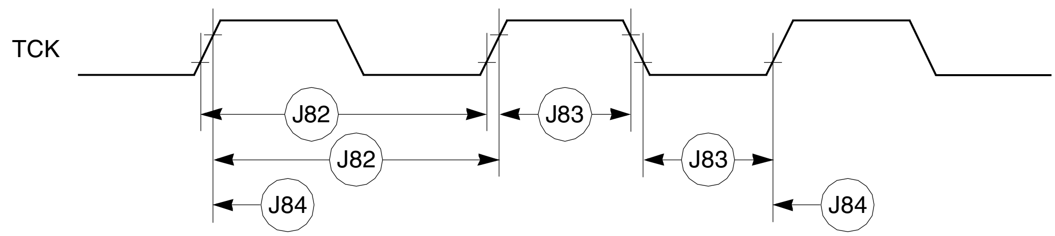


**Figure 38. JTAG Test Clock Input Timing**

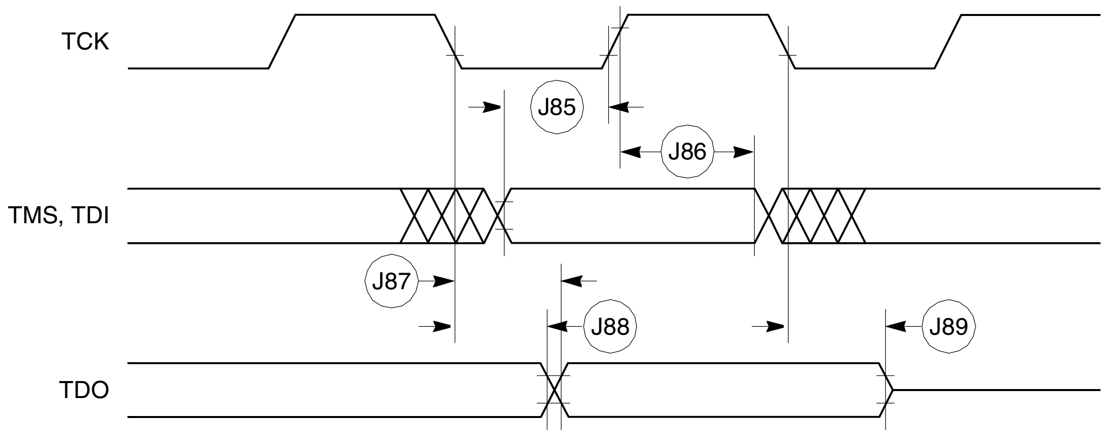


**Figure 39. JTAG Test Access Port Timing Diagram**

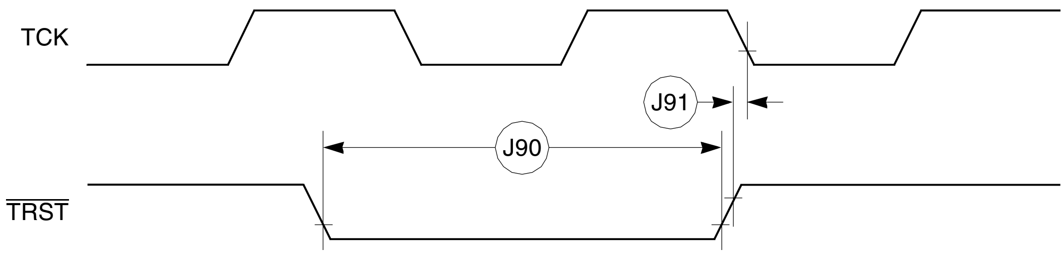


**Figure 40. JTAG $\overline{TRST}$ Timing Diagram**

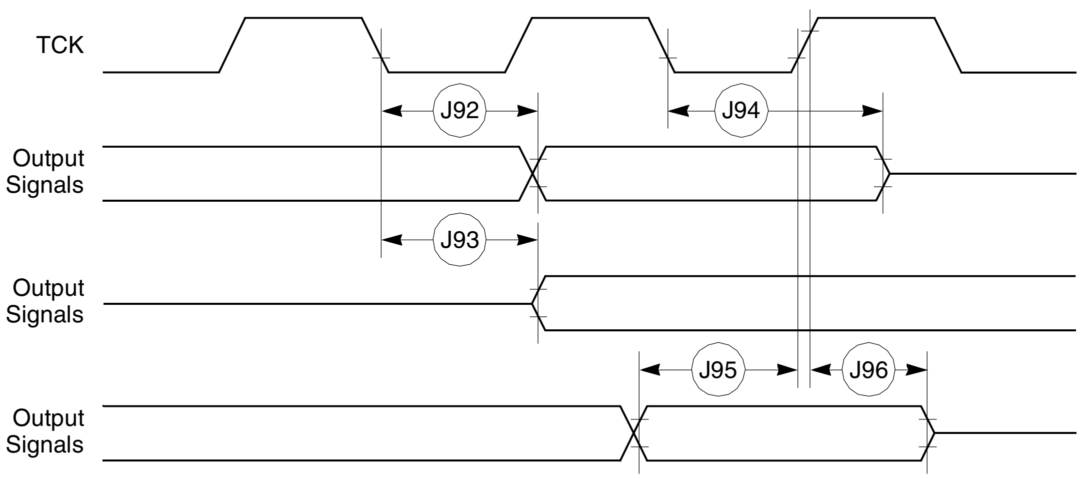


**Figure 41. Boundary Scan (JTAG) Timing Diagram**

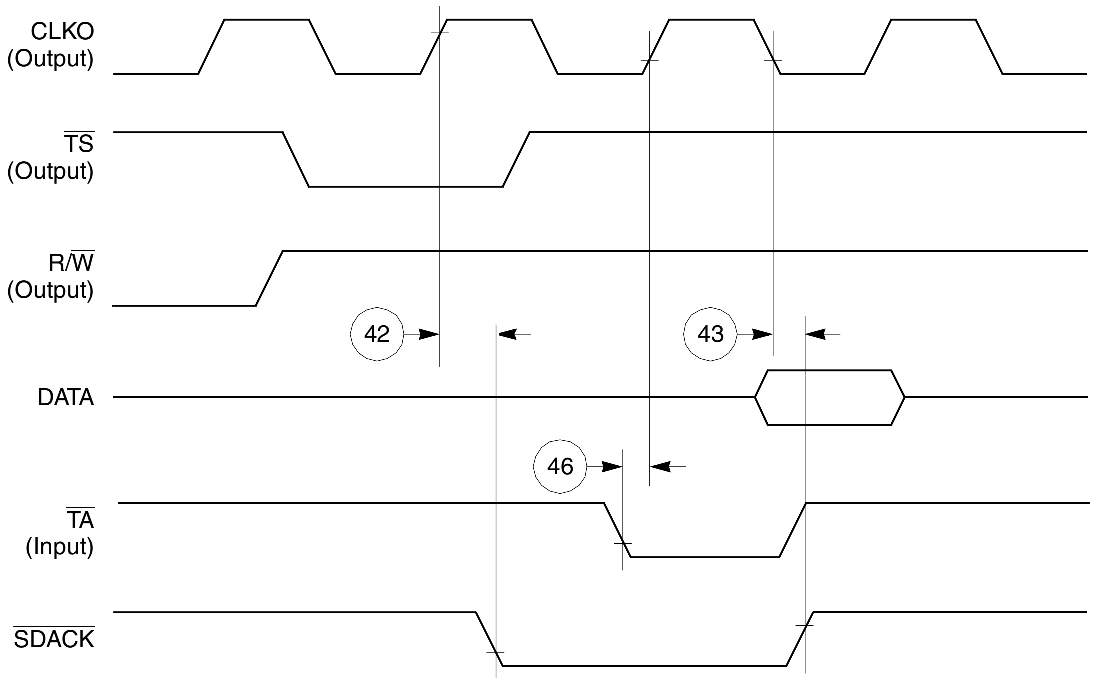


**Figure 49. SDACK Timing Diagram—Peripheral Write, Externally-Generated TA**

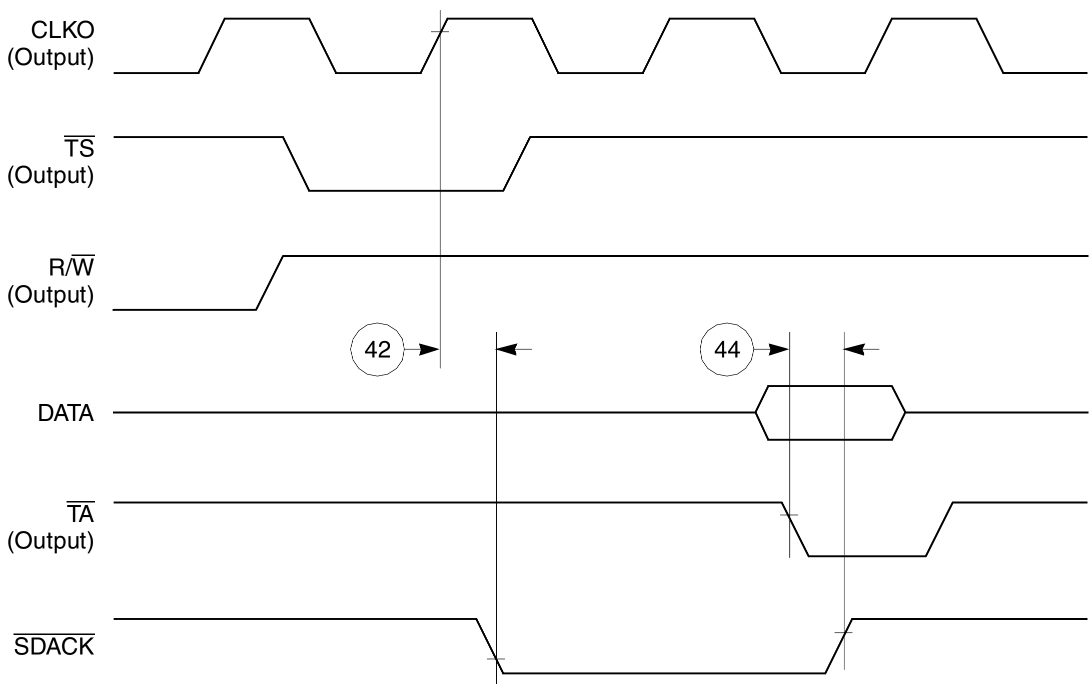


**Figure 50. SDACK Timing Diagram—Peripheral Write, Internally-Generated TA**

## 12.5 Timer AC Electrical Specifications

Table 20 provides the general-purpose timer timings as shown in Figure 53.

**Table 20. Timer Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 61 | TIN/$\overline{\text{TGATE}}$ rise and fall time | 10 | — | ns |
| 62 | TIN/$\overline{\text{TGATE}}$ low time | 1 | — | clk |
| 63 | TIN/$\overline{\text{TGATE}}$ high time | 2 | — | clk |
| 64 | TIN/$\overline{\text{TGATE}}$ cycle time | 3 | — | clk |
| 65 | CLKO low to $\overline{\text{TOUT}}$ valid | 3 | 25 | ns |

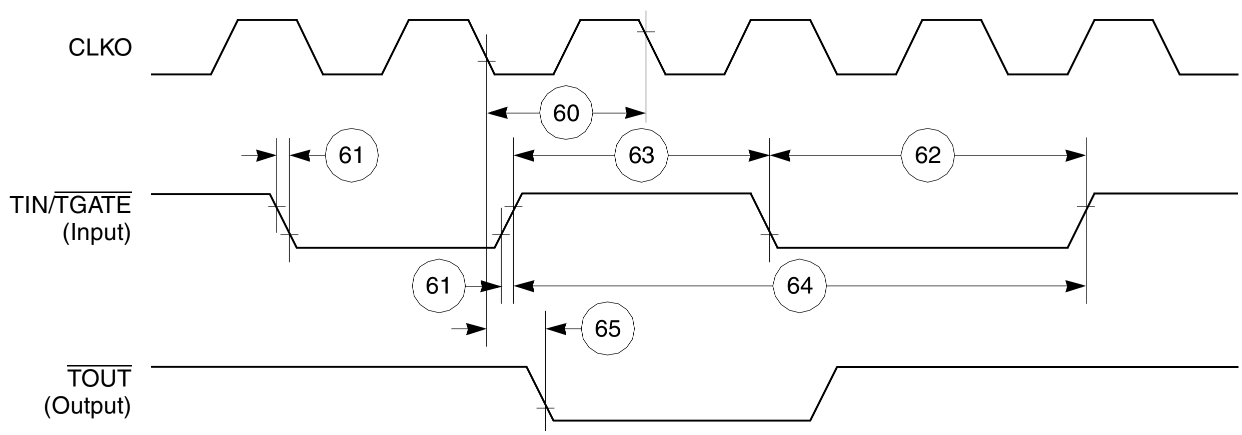


**Figure 53. CPM General-Purpose Timers Timing Diagram**

## 12.6 Serial Interface AC Electrical Specifications

Table 21 provides the serial interface timings as shown in Figure 54 through Figure 58.

**Table 21. SI Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 70 | L1RCLK, L1TCLK frequency (DSC = 0)[1, 2] | — | SYNCCLK/2.5 | MHz |
| 71 | L1RCLK, L1TCLK width low (DSC = 0)[2] | P + 10 | — | ns |
| 71a | L1RCLK, L1TCLK width high (DSC = 0)[3] | P + 10 | — | ns |
| 72 | L1TXD, L1ST(1–4), $\overline{\text{L1RQ}}$, L1CLKO rise/fall time | — | 15.00 | ns |
| 73 | L1RSYNC, L1TSYNC valid to L1CLK edge (SYNC setup time) | 20.00 | — | ns |
| 74 | L1CLK edge to L1RSYNC, L1TSYNC, invalid (SYNC hold time) | 35.00 | — | ns |
| 75 | L1RSYNC, L1TSYNC rise/fall time | — | 15.00 | ns |

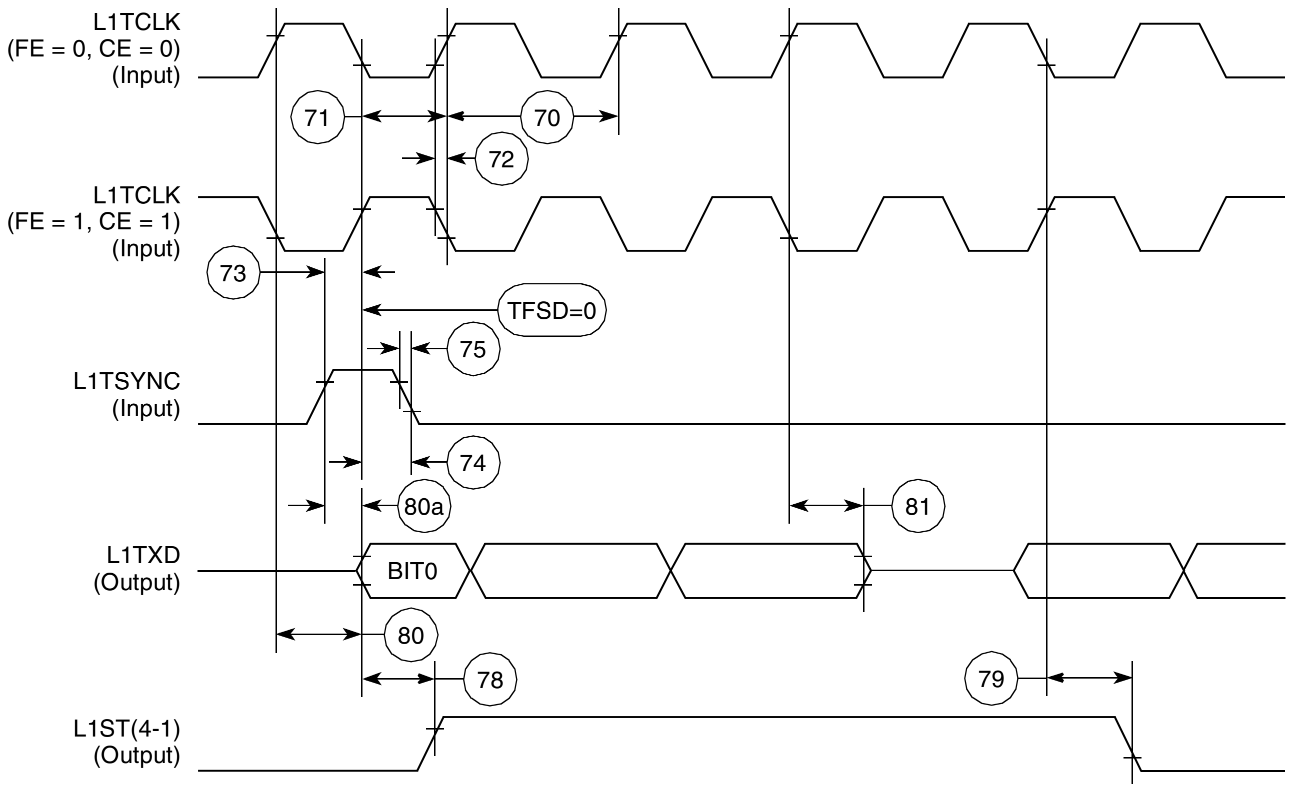


**Figure 56. SI Transmit Timing Diagram (DSC = 0)**

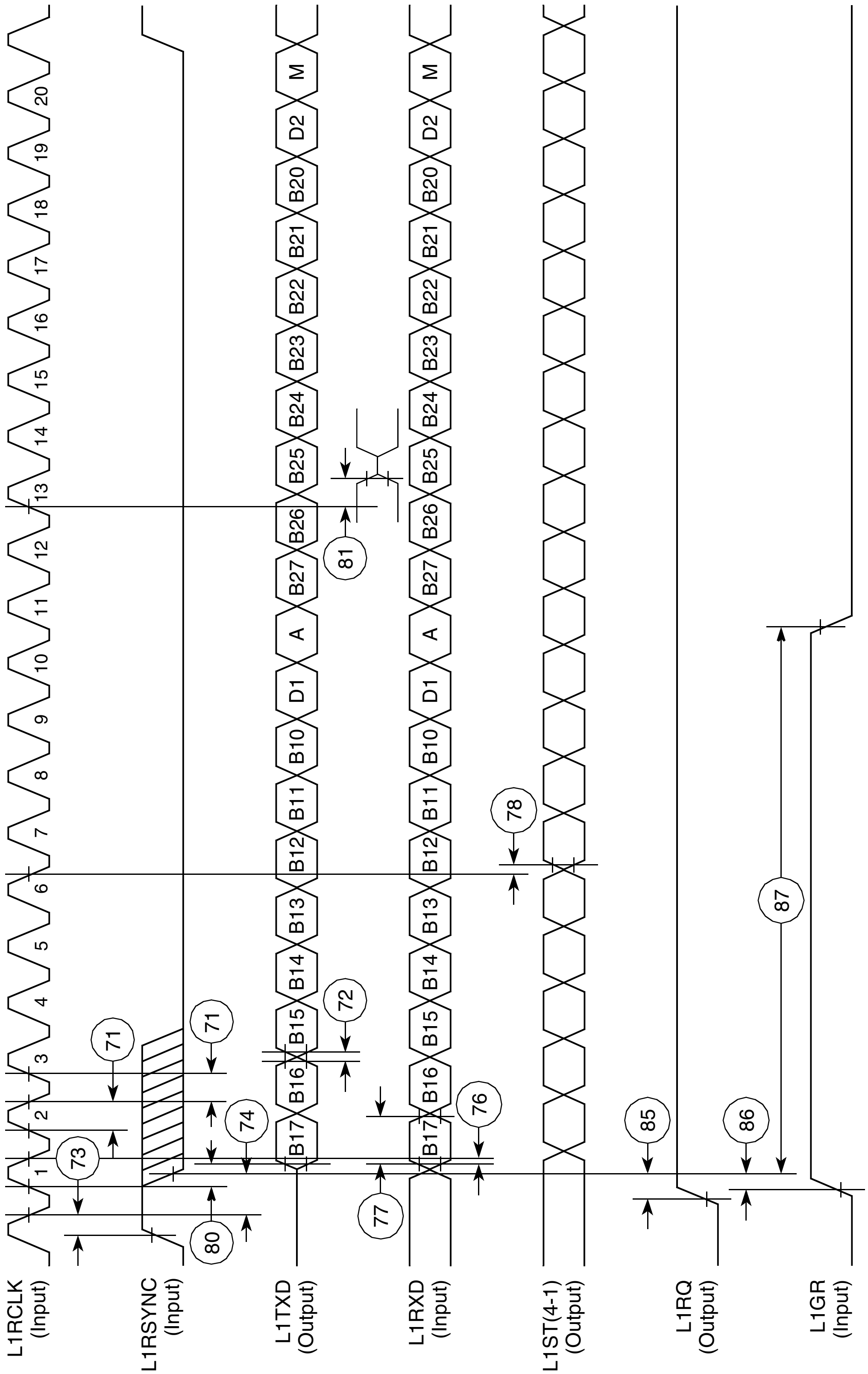


**Figure 58. IDL Timing**

## 12.7 SCC in NMSI Mode Electrical Specifications

Table 22 provides the NMSI external clock timing.

**Table 22. NMSI External Clock Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 100 | RCLK1 and TCLK1 width high[1] | 1/SYNCCLK | — | ns |
| 101 | RCLK1 and TCLK1 width low | 1/SYNCCLK + 5 | — | ns |
| 102 | RCLK1 and TCLK1 rise/fall time | — | 15.00 | ns |
| 103 | TXD1 active delay (from TCLK1 falling edge) | 0.00 | 50.00 | ns |
| 104 | $\overline{\text{RTS1}}$ active/inactive delay (from TCLK1 falling edge) | 0.00 | 50.00 | ns |
| 105 | $\overline{\text{CTS1}}$ setup time to TCLK1 rising edge | 5.00 | — | ns |
| 106 | RXD1 setup time to RCLK1 rising edge | 5.00 | — | ns |
| 107 | RXD1 hold time from RCLK1 rising edge[2] | 5.00 | — | ns |
| 108 | $\overline{\text{CD1}}$ setup time to RCLK1 rising edge | 5.00 | — | ns |

1 The ratios SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater than or equal to 2.25/1.
2 Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as external sync signals.

Table 23 provides the NMSI internal clock timing.

**Table 23. NMSI Internal Clock Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 100 | RCLK1 and TCLK1 frequency[1] | 0.00 | SYNCCLK/3 | MHz |
| 102 | RCLK1 and TCLK1 rise/fall time | — | — | ns |
| 103 | TXD1 active delay (from TCLK1 falling edge) | 0.00 | 30.00 | ns |
| 104 | $\overline{\text{RTS1}}$ active/inactive delay (from TCLK1 falling edge) | 0.00 | 30.00 | ns |
| 105 | $\overline{\text{CTS1}}$ setup time to TCLK1 rising edge | 40.00 | — | ns |
| 106 | RXD1 setup time to RCLK1 rising edge | 40.00 | — | ns |
| 107 | RXD1 hold time from RCLK1 rising edge[2] | 0.00 | — | ns |
| 108 | $\overline{\text{CD1}}$ setup time to RCLK1 rising edge | 40.00 | — | ns |

1 The ratios SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater than or equal to 3/1.
2 Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as external sync signals

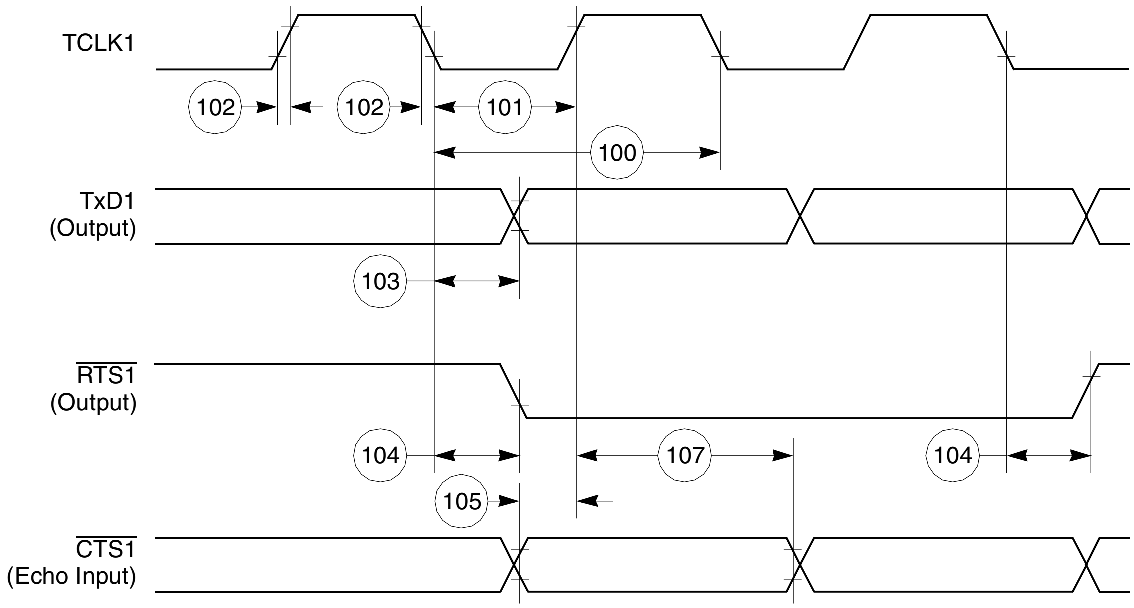


**Figure 61. HDLC Bus Timing Diagram**

## 12.8 Ethernet Electrical Specifications

Table 24 provides the Ethernet timings as shown in Figure 62 through Figure 64.

**Table 24. Ethernet Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 120 | CLSN width high | 40 | — | ns |
| 121 | RCLK1 rise/fall time | — | 15 | ns |
| 122 | RCLK1 width low | 40 | — | ns |
| 123 | RCLK1 clock period[1] | 80 | 120 | ns |
| 124 | RXD1 setup time | 20 | — | ns |
| 125 | RXD1 hold time | 5 | — | ns |
| 126 | RENA active delay (from RCLK1 rising edge of the last data bit) | 10 | — | ns |
| 127 | RENA width low | 100 | — | ns |
| 128 | TCLK1 rise/fall time | — | 15 | ns |
| 129 | TCLK1 width low | 40 | — | ns |
| 130 | TCLK1 clock period[1] | 99 | 101 | ns |
| 131 | TXD1 active delay (from TCLK1 rising edge) | — | 50 | ns |
| 132 | TXD1 inactive delay (from TCLK1 rising edge) | 6.5 | 50 | ns |
| 133 | TENA active delay (from TCLK1 rising edge) | 10 | 50 | ns |

**Table 28. I²C Timing (SCL < 100 kHz) (continued)**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 210 | SDL/SCL fall time | — | 300 | ns |
| 211 | Stop condition setup time | 4.7 | — | µs |

[1] SCL frequency is given by SCL = BRGCLK_frequency/((BRG register + 3) × pre_scaler × 2).
The ratio SyncClk/(BRGCLK/pre_scaler) must be greater or equal to 4/1.

Table 29 provides the I²C (SCL > 100 kHz) timings.

**Table 29. I²C Timing (SCL > 100 kHz)**

| Num | Characteristic | Expression | All Frequencies | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| 200 | SCL clock frequency (slave) | fSCL | 0 | BRGCLK/48 | Hz |
| 200 | SCL clock frequency (master)[1] | fSCL | BRGCLK/16512 | BRGCLK/48 | Hz |
| 202 | Bus free time between transmissions | — | 1/(2.2 × fSCL) | — | s |
| 203 | Low period of SCL | — | 1/(2.2 × fSCL) | — | s |
| 204 | High period of SCL | — | 1/(2.2 × fSCL) | — | s |
| 205 | Start condition setup time | — | 1/(2.2 × fSCL) | — | s |
| 206 | Start condition hold time | — | 1/(2.2 × fSCL) | — | s |
| 207 | Data hold time | — | 0 | — | s |
| 208 | Data setup time | — | 1/(40 × fSCL) | — | s |
| 209 | SDL/SCL rise time | — | — | 1/(10 × fSCL) | s |
| 210 | SDL/SCL fall time | — | — | 1/(33 × fSCL) | s |
| 211 | Stop condition setup time | — | 1/2(2.2 × fSCL) | — | s |

[1] SCL frequency is given by SCL = BrgClk_frequency/((BRG register + 3) × pre_scaler × 2).
The ratio SyncClk/(Brg_Clk/pre_scaler) must be greater or equal to 4/1.

Figure 70 shows the I²C bus timing.

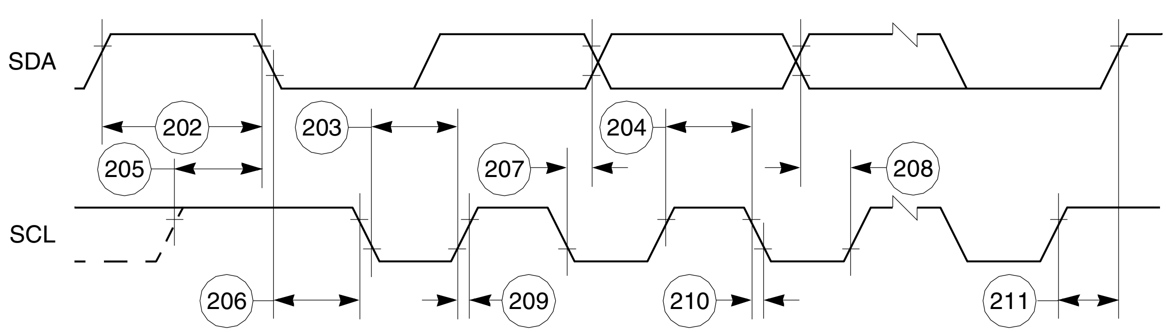


**Figure 70. I²C Bus Timing Diagram**

**Table 37. MII Serial Management Channel Timing (continued)**

| Num | Characteristic | Min | Max | Unit |
|---|---|---|---|---|
| M14 | MII_MDC pulse width high | 40% | 60% | MII_MDC period |
| M15 | MII_MDC pulse width low | 40% | 60% | MII_MDC period |

Figure 76 shows the MII serial management channel timing diagram.

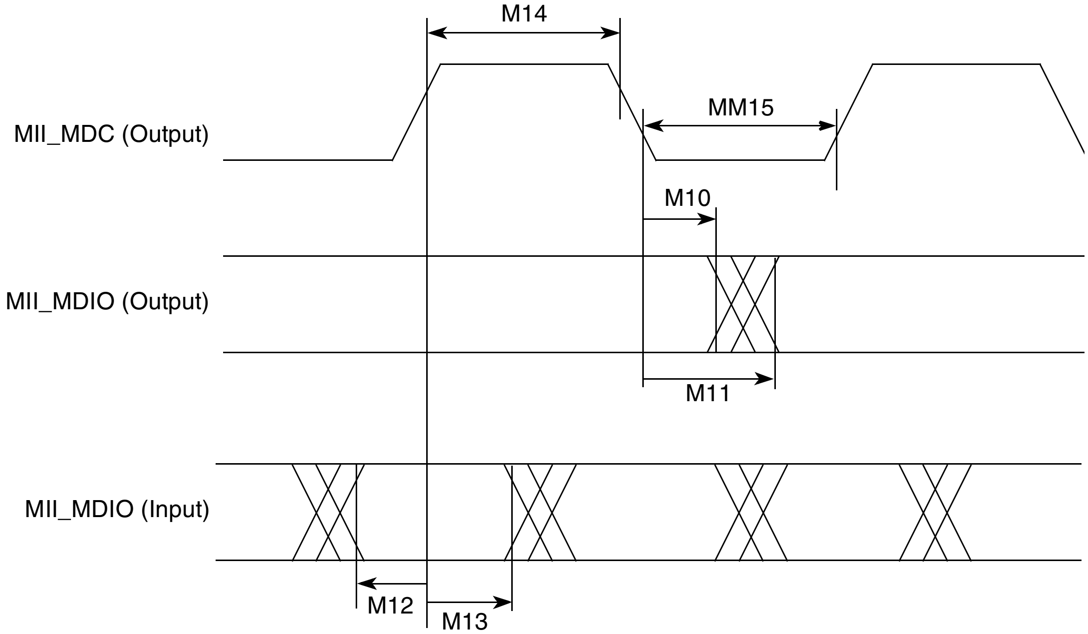


**Figure 76. MII Serial Management Channel Timing Diagram**

# 17 Document Revision History

Table 40 lists significant changes between revisions of this hardware specification.

**Table 40. Document Revision History**

| Revision Number | Date | Changes |
|---|---|---|
| 7 | 07/2010 | In Table 9, "Bus Operation Timings," changed the following:<br>• Updated TRLX condition value for B22a/b/c to "TRLX = [0 or 1]"<br>• Removed TRLX condition for B23<br>• Updated condition and equation for B30 to "Invalid GPCM read/write access (MIN = 0.25 × B1 – 2.00)"<br>• Updated note 8 to "The timing B30 refers to $\overline{CS}$ when ACS = 00 and to $\overline{CS}$ and $\overline{WE}$(0:3) when CSNT = 0." |
| 6 | 05/2010 | Added minimum load for CLKOUT in Section 10, "Bus Signal Timing." |
| 5 | 03/2009 | Updated formatting of Table 12 , "PCMCIA Port Timing," Table 13, "Debug Port Timing," Table 14, "Reset Timing," and Table 15, "JTAG Timing." |
| 4 | 08/2007 | • On page 1, updated first paragraph and added a second paragraph.<br>• After Table 2, inserted a new figure showing the undershoot/overshoot voltage (Figure 3) and renumbered the rest of the figures.<br>• In Table 9, for reset timings B29f and B29g added footnote indicating that the formula only applies to bus operation up to 50 MHz.<br>• In Figure 6, changed all reference voltage measurement points from 0.2 and 0.8 V to 50% level.<br>• In Table 18, changed num 46 description to read, "$\overline{TA}$ assertion to rising edge ..."<br>• In Figure 49, changed $\overline{TA}$ to reflect the rising edge of the clock. |
| 3.0 | 7/22/2004 | • Added sentence to Spec B1A about EXTCLK and CLKOUT being in Alignment for Integer Values<br>• Added a footnote to Spec 41 specifying that EDM = 1<br>• Added RMII1_EN under M1II_EN in Table 36 Pin Assignments<br>• Added a tablefootnote to Table 6 DC Electrical Specifications about meeting the VIL Max of the I2C Standard<br>• Put the new part numbers in the Ordering Information Section |
| 2.0 | 12/2003 | • Changed the maximum operating frequency to 133 MHz.<br>• Put in the orderable part numbers that are orderable.<br>• Put the timing in the 80 MHz column.<br>• Rounded the timings to hundredths in the 80 MHz column.<br>• Put the pin numbers in footnotes by the maximum currents in Table 6.<br>• Changed 22 and 41 in the Timing.<br>• Put in the Thermal numbers. |
| 1.0 | 9/2003 | • Added the DSP information in the Features list<br>• Fixed table formatting.<br>• Nontechnical edits.<br>• Released to the external web. |
| 0.9 | 8/2003 | Changed the USB description to full-/low-speed compatible. |
| 0.8 | 8/2003 | Added the Reference to USB 2.0 to the Features list and removed 1.1 from USB on the block diagrams. |
| 0.7 | 7/2003 | Added the RxClav and TxClav signals to PC15. |
| 0.6 | 6/2003 | Changed the pin descriptions per the June 22 spec. |
| 0.5 | 5/2003 | Changed some more typos, put in the phsel and phreq pins. Corrected the USB timing. |