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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	133MHz
Co-Processors/DSP	Communications; CPM, Security; SEC
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (3), 10/100Mbps (2)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 100°C (TA)
Security Features	Cryptography
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc885czp133

1 Overview

The MPC885/MPC880 is a versatile single-chip integrated microprocessor and peripheral combination that can be used in a variety of controller applications and communications and networking systems. The MPC885/MPC880 provides enhanced ATM functionality, an additional fast Ethernet controller, a USB, and an encryption block.

Table 1 shows the functionality supported by MPC885/MPC880.

Table 1. MPC885 Family

Part	Cache (Kbytes)		Ethernet		SCC	SMC	USB	ATM Support	Security Engine
	I Cache	D Cache	10BaseT	10/100					
MPC885	8	8	Up to 3	2	3	2	1	Serial ATM and UTOPIA interface	Yes
MPC880	8	8	Up to 2	2	2	2	1	Serial ATM and UTOPIA interface	No

2 Features

The MPC885/MPC880 is comprised of three modules that each use the 32-bit internal bus: a MPC8xx core, a system integration unit (SIU), and a communications processor module (CPM).

The following list summarizes the key MPC885/MPC880 features:

- Embedded MPC8xx core up to 133 MHz
- Maximum frequency operation of the external bus is 80 MHz (in 1:1 mode)
  - The 133-MHz core frequency supports 2:1 mode only.
  - The 66-/80-MHz core frequencies support both the 1:1 and 2:1 modes.
- Single-issue, 32-bit core (compatible with the Power Architecture definition) with thirty-two 32-bit general-purpose registers (GPRs)
  - The core performs branch prediction with conditional prefetch and without conditional execution.
  - 8-Kbyte data cache and 8-Kbyte instruction cache (see Table 1)
    - Instruction cache is two-way, set-associative with 256 sets in 2 blocks
    - Data cache is two-way, set-associative with 256 sets
    - Cache coherency for both instruction and data caches is maintained on 128-bit (4-word) cache blocks.
    - Caches are physically addressed, implement a least recently used (LRU) replacement algorithm, and are lockable on a cache block basis.
  - MMUs with 32-entry TLB, fully associative instruction and data TLBs
  - MMUs support multiple page sizes of 4, 16, and 512 Kbytes, and 8 Mbytes; 16 virtual address spaces and 16 protection groups
  - Advanced on-chip emulation debug mode

- On-chip 16 × 16 multiply accumulate controller (MAC)
  - One operation per clock (two-clock latency, one-clock blockage)
  - MAC operates concurrently with other instructions
  - FIR loop—Four clocks per four multiplies
- Four baud rate generators
  - Independent (can be connected to any SCC or SMC)
  - Allow changes during operation
  - Autobaud support option
- Up to three serial communication controllers (SCCs) supporting the following protocols:
  - Serial ATM capability on SCCs
  - Optional UTOPIA port on SCC4
  - Ethernet/IEEE Std 802.3™ optional on the SCC(s) supporting full 10-Mbps operation
  - HDLC/SDLC
  - HDLC bus (implements an HDLC-based local area network (LAN))
  - Asynchronous HDLC to support point-to-point protocol (PPP)
  - AppleTalk
  - Universal asynchronous receiver transmitter (UART)
  - Synchronous UART
  - Serial infrared (IrDA)
  - Binary synchronous communication (BISYNC)
  - Totally transparent (bit streams)
  - Totally transparent (frame based with optional cyclic redundancy check (CRC))
- Up to two serial management channels (SMCs) supporting the following protocols:
  - UART (low-speed operation)
  - Transparent
  - General circuit interface (GCI) controller
  - Provide management for BRI devices as GCI controller in time-division multiplexed (TDM) channels
- Universal serial bus (USB)—Supports operation as a USB function endpoint, a USB host controller, or both for testing purposes (loop-back diagnostics)
  - USB 2.0 full-/low-speed compatible
  - The USB function mode has the following features:
    - Four independent endpoints support control, bulk, interrupt, and isochronous data transfers.
    - CRC16 generation and checking
    - CRC5 checking
    - NRZI encoding/decoding with bit stuffing
    - 12- or 1.5-Mbps data rate

  - Flexible data buffers with multiple buffers per frame
  - Automatic retransmission upon transmit error
- The USB host controller has the following features:
  - Supports control, bulk, interrupt, and isochronous data transfers
  - CRC16 generation and checking
  - NRZI encoding/decoding with bit stuffing
  - Supports both 12- and 1.5-Mbps data rates (automatic generation of preamble token and data rate configuration). Note that low-speed operation requires an external hub.
  - Flexible data buffers with multiple buffers per frame
  - Supports local loop back mode for diagnostics (12 Mbps only)

- Serial peripheral interface (SPI)
  - Supports master and slave modes
  - Supports multiple-master operation on the same bus
- Inter-integrated circuit (I^2C) port
  - Supports master and slave modes
  - Supports a multiple-master environment
- Time-slot assigner (TSA)
  - Allows SCCs and SMCs to run in multiplexed and/or non-multiplexed operation
  - Supports T1, CEPT, PCM highway, ISDN basic rate, ISDN primary rate, user defined
  - 1- or 8-bit resolution
  - Allows independent transmit and receive routing, frame synchronization, and clocking
  - Allows dynamic changes
  - Can be internally connected to four serial channels (two SCCs and two SMCs)
- Parallel interface port (PIP)
  - Centronics interface support
  - Supports fast connection between compatible ports on MPC885/MPC880 and other MPC8xx devices
- PCMCIA interface
  - Master (socket) interface, release 2.1-compliant
  - Supports two independent PCMCIA sockets
  - 8 memory or I/O windows supported
- Debug interface
  - Eight comparators: four operate on instruction address, two operate on data address, and two operate on data
  - Supports conditions: = ≠ < >
  - Each watchpoint can generate a break point internally.
- Normal high and normal low power modes to conserve power

- 1.8-V core and 3.3-V I/O operation
- The MPC885/MPC880 comes in a 357-pin ball grid array (PBGA) package

The MPC885 block diagram is shown in Figure 1.

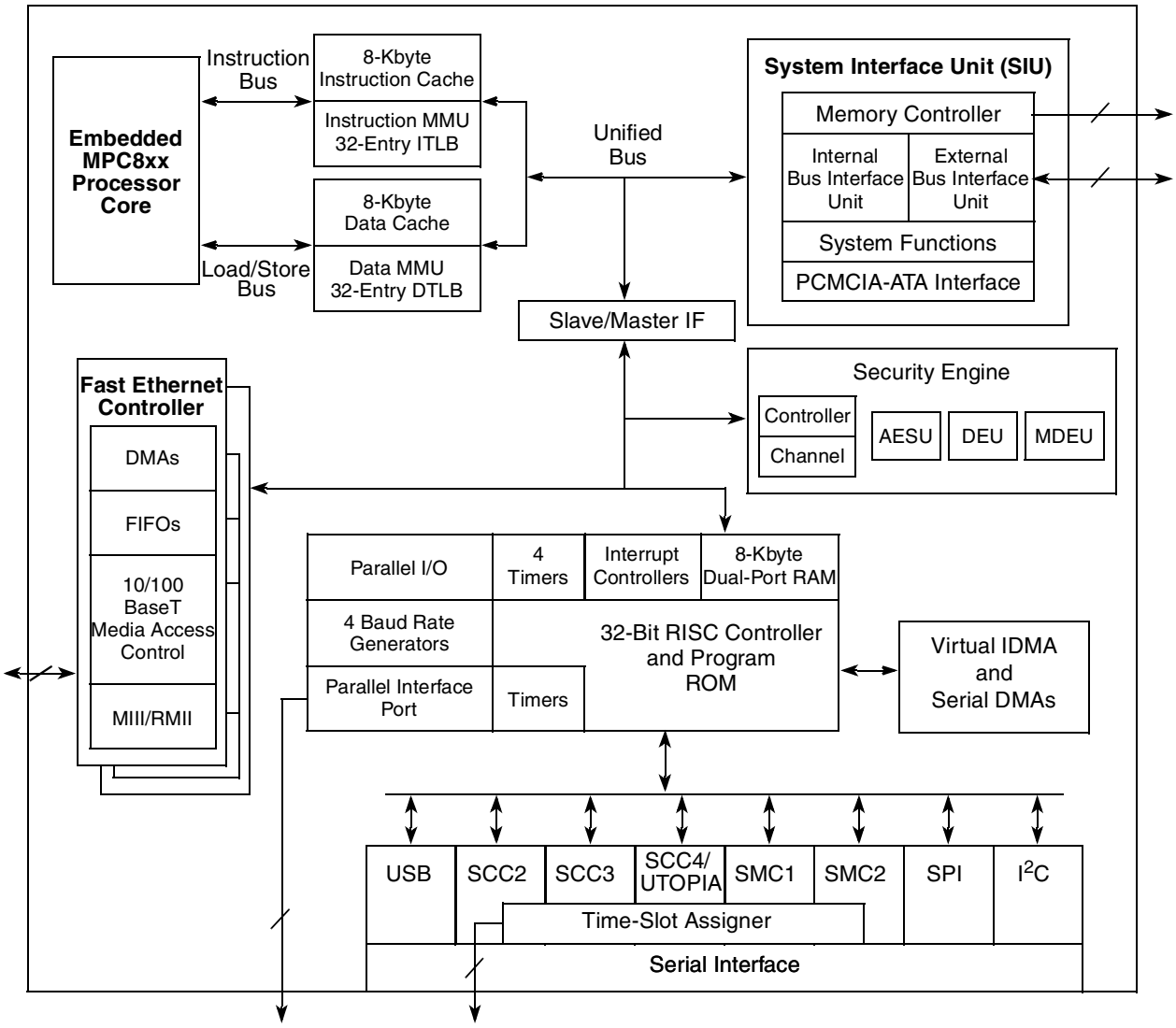


Figure 1. MPC885 Block Diagram

3 Maximum Tolerated Ratings

This section provides the maximum tolerated voltage and temperature ranges for the MPC885/MPC880. Table 2 displays the maximum tolerated ratings, and Table 3 displays the operating temperatures.

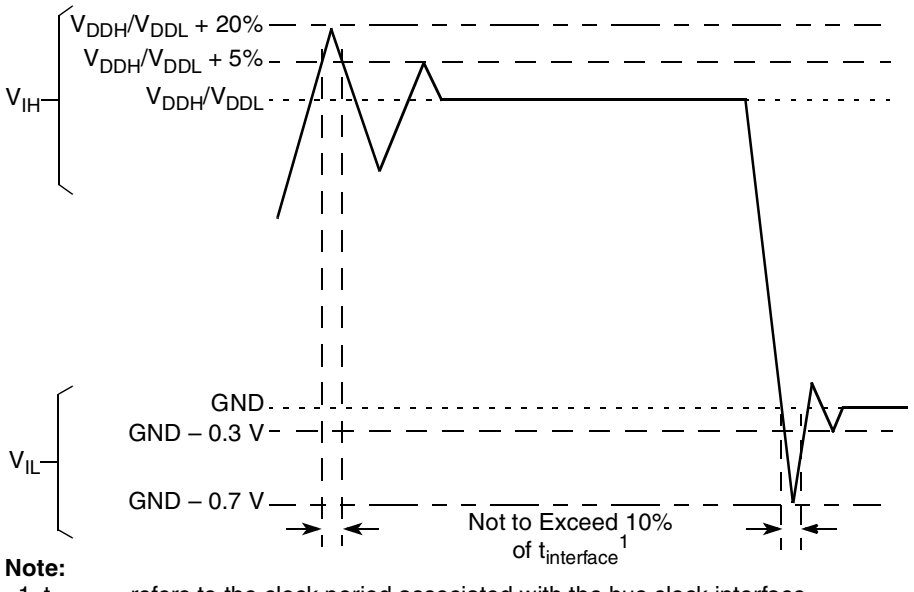
Table 2. Maximum Tolerated Ratings

Rating	Symbol	Value	Unit
Supply voltage[1]	V_{DDH}	–0.3 to 4.0	V
	V_{DDL}	–0.3 to 2.0	V
	VDDSYN	–0.3 to 2.0	V
	Difference between V_{DDL} and V_{DDSYN}	<100	mV
Input voltage[2]	V_{in}	GND – 0.3 to V_{DDH}	V
Storage temperature range	T_{stg}	–55 to +150	°C

1 The power supply of the device must start its ramp from 0.0 V.

2 Functional operating conditions are provided with the DC electrical specifications in Table 6. Absolute maximum ratings are stress ratings only; functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device. See Section 8, “Power Supply and Power Sequencing.”
Caution: All inputs that tolerate 5 V cannot be more than 2.5 V greater than V_{DDH}. This restriction applies to power up and normal operation (that is, if the MPC885/MPC880 is unpowered, a voltage greater than 2.5 V must not be applied to its inputs).

Figure 3 shows the undershoot and overshoot voltages at the interfaces of the MPC885/MPC880.



Note:
1. $t_{interface}$ refers to the clock period associated with the bus clock interface.

Figure 3. Undershoot/Overshoot Voltage for V_{DDH} and V_{DDL}

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B27a	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 1 (MIN = 1.50 × B1 – 2.00)	43.50	—	35.50	—	20.70	—	16.75	—	ns
B28	CLKOUT rising edge to $\overline{WE}$(0:3) negated GPCM write access CSNT = 0 (MAX = 0.00 × B1 + 9.00)	—	9.00	—	9.00	—	9.00	—	9.00	ns
B28a	CLKOUT falling edge to $\overline{WE}$(0:3) negated GPCM write access TRLX = 0, CSNT = 1, EBDF = 0 (MAX = 0.25 × B1 + 6.80)	7.60	14.30	6.30	13.00	3.80	10.50	3.13	9.93	ns
B28b	CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0, CSNT = 1 ACS = 10 or ACS = 11, EBDF = 0 (MAX = 0.25 × B1 + 6.80)	—	14.30	—	13.00	—	10.50	—	9.93	ns
B28c	CLKOUT falling edge to $\overline{WE}$(0:3) negated GPCM write access TRLX = 0, CSNT = 1 write access TRLX = 0, CSNT = 1, EBDF = 1 (MAX = 0.375 × B1 + 6.6)	10.90	18.00	10.90	18.00	5.20	12.30	4.69	11.29	ns
B28d	CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1 (MAX = 0.375 × B1 + 6.6)	—	18.00	—	18.00	—	12.30	—	11.30	ns
B29	$\overline{WE}$(0:3) negated to D(0:31) High-Z GPCM write access, CSNT = 0, EBDF = 0 (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	1.80	—	1.13	—	ns
B29a	$\overline{WE}$(0:3) negated to D(0:31) High-Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 0 (MIN = 0.50 × B1 – 2.00)	13.20	—	10.50	—	5.60	—	4.25	—	ns
B29b	$\overline{CS}$ negated to D(0:31) High-Z GPCM write access, ACS = 00, TRLX = 0 & CSNT = 0 (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	1.80	—	1.13	—	ns
B29c	$\overline{CS}$ negated to D(0:31) High-Z GPCM write access, TRLX = 0, CSNT = 1, ACS = 10, or ACS = 11 EBDF = 0 (MIN = 0.50 × B1 – 2.00)	13.20	—	10.50	—	5.60	—	4.25	—	ns
B29d	$\overline{WE}$(0:3) negated to D(0:31) High-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 0 (MIN = 1.50 × B1 – 2.00)	43.50	—	35.50	—	20.70	—	16.75	—	ns
B29e	$\overline{CS}$ negated to D(0:31) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11 EBDF = 0 (MIN = 1.50 × B1 – 2.00)	43.50	—	35.50	—	20.70	—	16.75	—	ns
B29f	$\overline{WE}$(0:3) negated to D(0:31) High-Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 1 (MIN = 0.375 × B1 – 6.30)[7]	5.00	—	3.00	—	0.00	—	0.00	—	ns
B29g	$\overline{CS}$ negated to D(0:31) High-Z GPCM write access, TRLX = 0, CSNT = 1 ACS = 10 or ACS = 11, EBDF = 1 (MIN = 0.375 × B1 – 6.30)[7]	5.00	—	3.00	—	0.00	—	0.00	—	ns

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B29h	$\overline{WE}$(0:3) negated to D(0:31) High-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 1 (MIN = 0.375 × B1 – 3.30)	38.40	—	31.10	—	17.50	—	13.85	—	ns
B29i	$\overline{CS}$ negated to D(0:31) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1 (MIN = 0.375 × B1 – 3.30)	38.40	—	31.10	—	17.50	—	13.85	—	ns
B30	$\overline{CS}$, $\overline{WE}$(0:3) negated to A(0:31), BADDR(28:30) Invalid GPCM read/write access[8] (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	1.80	—	1.13	—	ns
B30a	$\overline{WE}$(0:3) negated to A(0:31), BADDR(28:30) Invalid GPCM, write access, TRLX = 0, CSNT = 1, $\overline{CS}$ negated to A(0:31) invalid GPCM write access TRLX = 0, CSNT =1 ACS = 10, or ACS == 11, EBDF = 0 (MIN = 0.50 × B1 – 2.00)	13.20	—	10.50	—	5.60	—	4.25	—	ns
B30b	$\overline{WE}$(0:3) negated to A(0:31) invalid GPCM BADDR(28:30) invalid GPCM write access, TRLX = 1, CSNT = 1. $\overline{CS}$ negated to A(0:31) invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10, or ACS == 11 EBDF = 0 (MIN = 1.50 × B1 – 2.00)	43.50	—	35.50	—	20.70	—	16.75	—	ns
B30c	$\overline{WE}$(0:3) negated to A(0:31), BADDR(28:30) invalid GPCM write access, TRLX = 0, CSNT = 1. $\overline{CS}$ negated to A(0:31) invalid GPCM write access, TRLX = 0, CSNT = 1 ACS = 10, ACS == 11, EBDF = 1 (MIN = 0.375 × B1 – 3.00)	8.40	—	6.40	—	2.70	—	1.70	—	ns
B30d	$\overline{WE}$(0:3) negated to A(0:31), BADDR(28:30) invalid GPCM write access TRLX = 1, CSNT =1, $\overline{CS}$ negated to A(0:31) invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10 or 11, EBDF = 1	38.67	—	31.38	—	17.83	—	14.19	—	ns
B31	CLKOUT falling edge to $\overline{CS}$ valid, as requested by control bit CST4 in the corresponding word in the UPM (MAX = 0.00 × B1 + 6.00)	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B31a	CLKOUT falling edge to $\overline{CS}$ valid, as requested by control bit CST1 in the corresponding word in the UPM (MAX = 0.25 × B1 + 6.80)	7.60	14.30	6.30	13.00	3.80	10.50	3.13	10.00	ns
B31b	CLKOUT rising edge to $\overline{CS}$ valid, as requested by control bit CST2 in the corresponding word in the UPM (MAX = 0.00 × B1 + 8.00)	1.50	8.00	1.50	8.00	1.50	8.00	1.50	8.00	ns
B31c	CLKOUT rising edge to $\overline{CS}$ valid, as requested by control bit CST3 in the corresponding word in the UPM (MAX = 0.25 × B1 + 6.30)	7.60	13.80	6.30	12.50	3.80	10.00	3.13	9.40	ns
B31d	CLKOUT falling edge to $\overline{CS}$ valid, as requested by control bit CST1 in the corresponding word in the UPM EBDF = 1 (MAX = 0.375 × B1 + 6.6)	13.30	18.00	11.30	16.00	7.60	12.30	4.69	11.30	ns

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B36	A(0:31), BADDR(28:30), and D(0:31) to $\overline{\text{GPL}}$ valid, as requested by control bit GxT4 in the corresponding word in the UPM (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	1.80	—	1.13	—	ns
B37	UPWAIT valid to CLKOUT falling edge[9] (MIN = 0.00 × B1 + 6.00)	6.00	—	6.00	—	6.00	—	6.00	—	ns
B38	CLKOUT falling edge to UPWAIT valid [9] (MIN = 0.00 × B1 + 1.00)	1.00	—	1.00	—	1.00	—	1.00	—	ns
B39	$\overline{\text{AS}}$ valid to CLKOUT rising edge[10] (MIN = 0.00 × B1 + 7.00)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B40	A(0:31), TSIZ(0:1), RD/$\overline{\text{WR}}$, $\overline{\text{BURST}}$, valid to CLKOUT rising edge (MIN = 0.00 × B1 + 7.00)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B41	$\overline{\text{TS}}$ valid to CLKOUT rising edge (setup time) (MIN = 0.00 × B1 + 7.00)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B42	CLKOUT rising edge to $\overline{\text{TS}}$ valid (hold time) (MIN = 0.00 × B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B43	$\overline{\text{AS}}$ negation to memory controller signals negation (MAX = TBD)	—	TBD	—	TBD	—	TBD	—	TBD	ns

1 For part speeds above 50 MHz, use 9.80 ns for B11a.

2 The timing required for $\overline{\text{BR}}$ input is relevant when the MPC885/MPC880 is selected to work with the internal bus arbiter. The timing for $\overline{\text{BG}}$ input is relevant when the MPC885/MPC880 is selected to work with the external bus arbiter.

3 For part speeds above 50 MHz, use 2 ns for B17.

4 The D(0:31) input timings B18 and B19 refer to the rising edge of the CLKOUT in which the $\overline{\text{TA}}$ input signal is asserted.

5 For part speeds above 50 MHz, use 2 ns for B19.

6 The D(0:31) input timings B20 and B21 refer to the falling edge of the CLKOUT. This timing is valid only for read accesses controlled by chip-selects under control of the user-programmable machine (UPM) in the memory controller, for data beats where DLT3 = 1 in the RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

7 This formula applies to bus operation up to 50 MHz.

8 The timing B30 refers to $\overline{\text{CS}}$ when ACS = 00 and to $\overline{\text{CS}}$ and $\overline{\text{WE}}$(0:3) when CSNT = 0.

9 The signal UPWAIT is considered asynchronous to the CLKOUT and synchronized internally. The timings specified in B37 and B38 are specified to enable the freeze of the UPM output signals as described in Figure 21.

10 The $\overline{\text{AS}}$ signal is considered asynchronous to the CLKOUT. The timing B39 is specified in order to allow the behavior specified in Figure 24.

Figure 21 provides the timing for the asynchronous asserted UPWAIT signal controlled by the UPM.

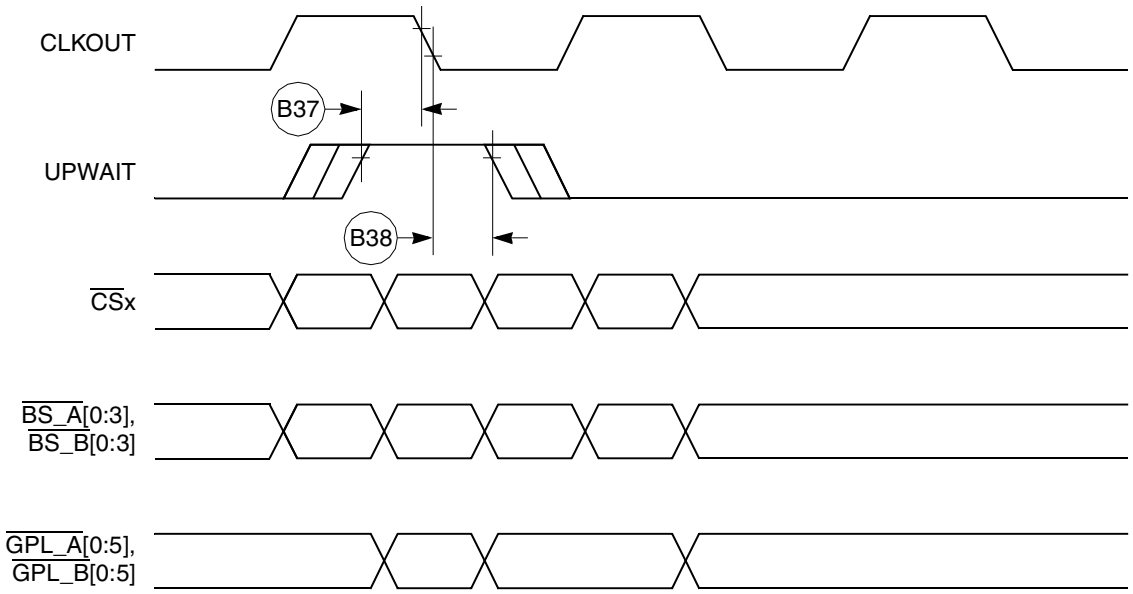


Figure 21. Asynchronous UPWAIT Asserted Detection in UPM-Handled Cycles Timing

Figure 22 provides the timing for the asynchronous negated UPWAIT signal controlled by the UPM.

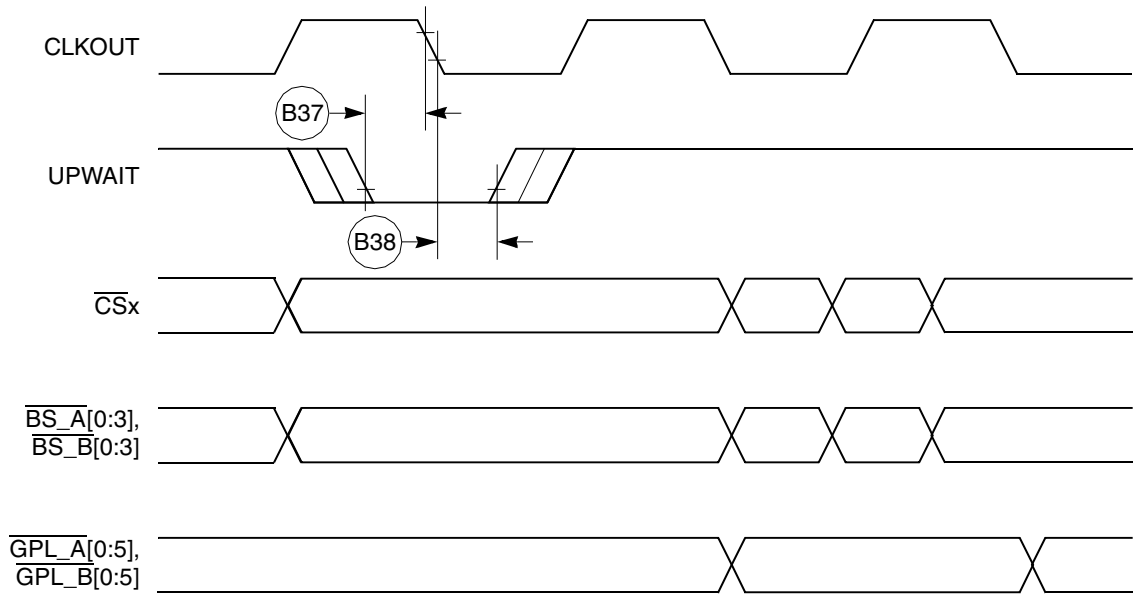


Figure 22. Asynchronous UPWAIT Negated Detection in UPM-Handled Cycles Timing

Table 11 shows the PCMCIA timing for the MPC885/MPC880.

Table 11. PCMCIA Timing

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
P44	A(0:31), $\overline{\text{REG}}$ valid to PCMCIA strobe asserted[1] (MIN = 0.75 × B1 – 2.00)	20.70	—	16.70	—	9.40	—	7.40	—	ns
P45	A(0:31), $\overline{\text{REG}}$ valid to ALE negation[1] (MIN = 1.00 × B1 – 2.00)	28.30	—	23.00	—	13.20	—	10.50	—	ns
P46	CLKOUT to $\overline{\text{REG}}$ valid (MAX = 0.25 × B1 + 8.00)	7.60	15.60	6.30	14.30	3.80	11.80	3.13	11.13	ns
P47	CLKOUT to $\overline{\text{REG}}$ invalid (MIN = 0.25 – B1 + 1.00)	8.60	—	7.30	—	4.80	—	4.13	—	ns
P48	CLKOUT to $\overline{\text{CE1}}$, $\overline{\text{CE2}}$ asserted (MAX = 0.25 × B1 + 8.00)	7.60	15.60	6.30	14.30	3.80	11.80	3.13	11.13	ns
P49	CLKOUT to $\overline{\text{CE1}}$, $\overline{\text{CE2}}$ negated (MAX = 0.25 × B1 + 8.00)	7.60	15.60	6.30	14.30	3.80	11.80	3.13	11.13	ns
P50	CLKOUT to $\overline{\text{PCOE}}$, $\overline{\text{IORD}}$, $\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ assert time (MAX = 0.00 × B1 + 11.00)	—	11.00	—	11.00	—	11.00	—	11.00	ns
P51	CLKOUT to $\overline{\text{PCOE}}$, $\overline{\text{IORD}}$, $\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ negate time (MAX = 0.00 × B1 + 11.00)	2.00	11.00	2.00	11.00	2.00	11.00	2.00	11.00	ns
P52	CLKOUT to ALE assert time (MAX = 0.25 × B1 + 6.30)	7.60	13.80	6.30	12.50	3.80	10.00	3.13	9.40	ns
P53	CLKOUT to ALE negate time (MAX = 0.25 × B1 + 8.00)	—	15.60	—	14.30	—	11.80	—	11.13	ns
P54	$\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ negated to D(0:31) invalid [1] (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	1.80	—	1.13	—	ns
P55	$\overline{\text{WAITA}}$ and $\overline{\text{WAITB}}$ valid to CLKOUT rising edge[1] (MIN = 0.00 × B1 + 8.00)	8.00	—	8.00	—	8.00	—	8.00	—	ns
P56	CLKOUT rising edge to $\overline{\text{WAITA}}$ and $\overline{\text{WAITB}}$ invalid[1] (MIN = 0.00 × B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns

[1] PSST = 1. Otherwise add PSST times cycle time.
PSHT = 0. Otherwise add PSHT times cycle time.

These synchronous timings define when the $\overline{\text{WAITx}}$ signals are detected in order to freeze (or relieve) the PCMCIA current cycle. The $\overline{\text{WAITx}}$ assertion will be effective only if it is detected 2 cycles before the PSL timer expiration. See Chapter 16, “PCMCIA Interface,” in the *MPC885 PowerQUICC™ Family Reference Manual*.

Table 12 shows the PCMCIA port timing for the MPC885/MPC880.

Table 12. PCMCIA Port Timing

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
P57	CLKOUT to OPx valid (MAX = 0.00 × B1 + 19.00)	—	19.00	—	19.00	—	19.00	—	19.00	ns
P58	$\overline{\text{HRESET}}$ negated to OPx drive[1] (MIN = 0.75 × B1 + 3.00)	25.70	—	21.70	—	14.40	—	12.40	—	ns
P59	IP_Xx valid to CLKOUT rising edge (MIN = 0.00 × B1 + 5.00)	5.00	—	5.00	—	5.00	—	5.00	—	ns
P60	CLKOUT rising edge to IP_Xx invalid (MIN = 0.00 × B1 + 1.00)	1.00	—	1.00	—	1.00	—	1.00	—	ns

1 OP2 and OP3 only.

Figure 31 provides the PCMCIA output port timing for the MPC885/MPC880.

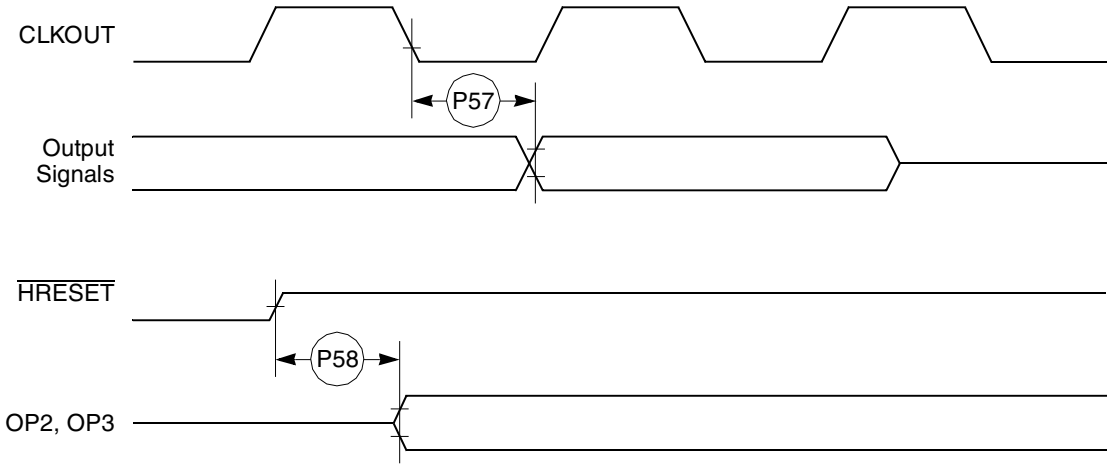


Figure 31. PCMCIA Output Port Timing

Figure 32 provides the PCMCIA input port timing for the MPC885/MPC880.

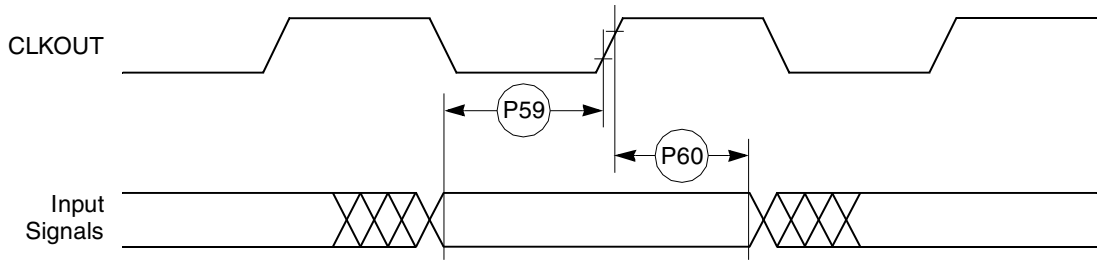


Figure 32. PCMCIA Input Port Timing

11 IEEE 1149.1 Electrical Specifications

Table 15 provides the JTAG timings for the MPC885/MPC880 shown in Figure 38 through Figure 41.

Table 15. JTAG Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
J82	TCK cycle time	100.00	—	ns
J83	TCK clock pulse width measured at 1.5 V	40.00	—	ns
J84	TCK rise and fall times	0.00	10.00	ns
J85	TMS, TDI data setup time	5.00	—	ns
J86	TMS, TDI data hold time	25.00	—	ns
J87	TCK low to TDO data valid	—	27.00	ns
J88	TCK low to TDO data invalid	0.00	—	ns
J89	TCK low to TDO high impedance	—	20.00	ns
J90	$\overline{\text{TRST}}$ assert time	100.00	—	ns
J91	$\overline{\text{TRST}}$ setup time to TCK low	40.00	—	ns
J92	TCK falling edge to output valid	—	50.00	ns
J93	TCK falling edge to output valid out of high impedance	—	50.00	ns
J94	TCK falling edge to output high impedance	—	50.00	ns
J95	Boundary scan input valid to TCK rising edge	50.00	—	ns
J96	TCK rising edge to boundary scan input invalid	50.00	—	ns

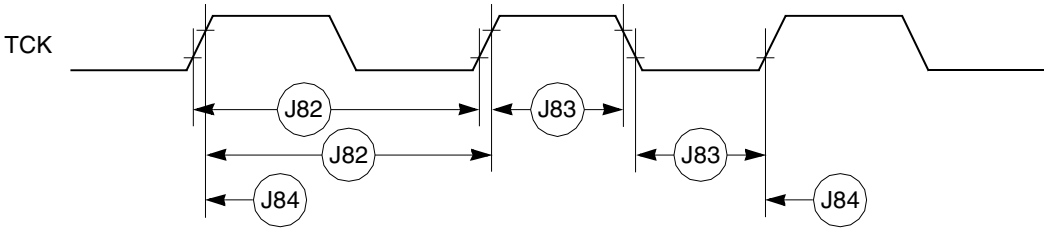


Figure 38. JTAG Test Clock Input Timing

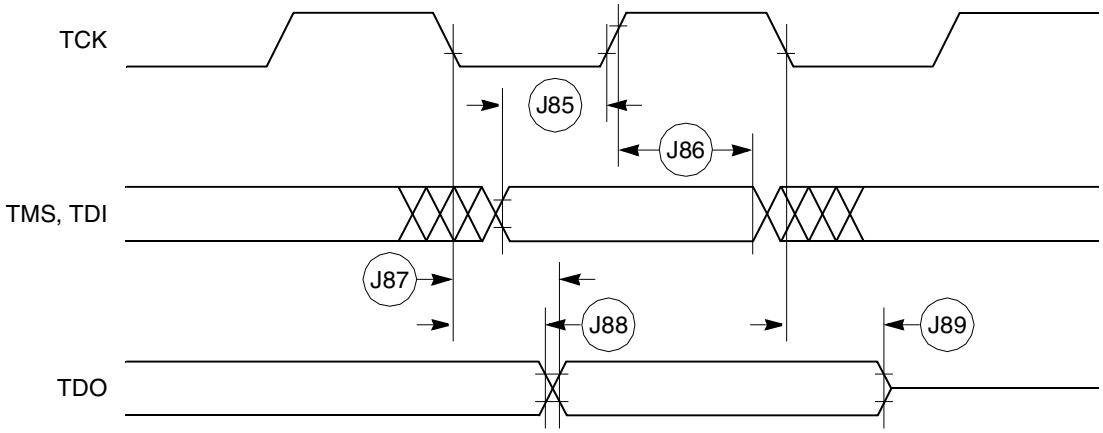


Figure 39. JTAG Test Access Port Timing Diagram

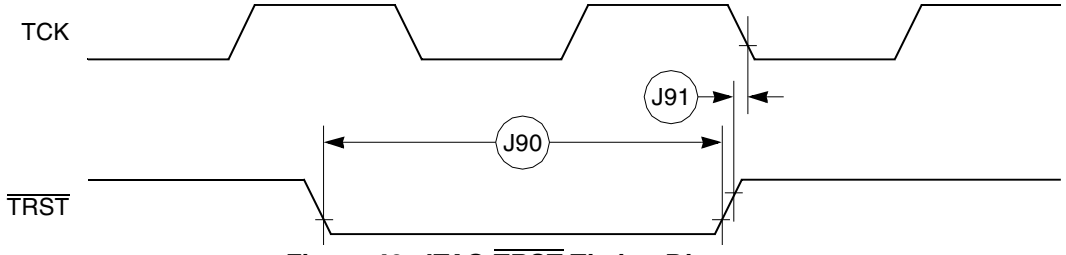


Figure 40. JTAG $\overline{\text{TRST}}$ Timing Diagram

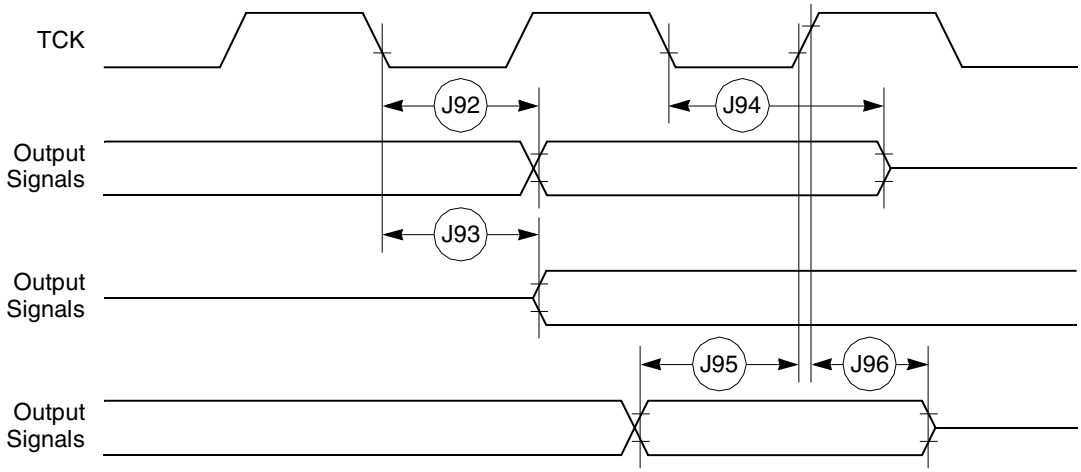


Figure 41. Boundary Scan (JTAG) Timing Diagram

12.3 IDMA Controller AC Electrical Specifications

Table 18 provides the IDMA controller timings as shown in Figure 48 tthrough Figure 51.

Table 18. IDMA Controller Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
40	$\overline{\text{DREQ}}$ setup time to clock high	7	—	ns
41	$\overline{\text{DREQ}}$ hold time from clock high [1]	TBD	—	ns
42	$\overline{\text{SDACK}}$ assertion delay from clock high	—	12	ns
43	$\overline{\text{SDACK}}$ negation delay from clock low	—	12	ns
44	$\overline{\text{SDACK}}$ negation delay from $\overline{\text{TA}}$ low	—	20	ns
45	$\overline{\text{SDACK}}$ negation delay from clock high	—	15	ns
46	$\overline{\text{TA}}$ assertion to rising edge of the clock setup time (applies to external $\overline{\text{TA}}$)	7	—	ns

[1] Applies to high-to-low mode (EDM = 1).

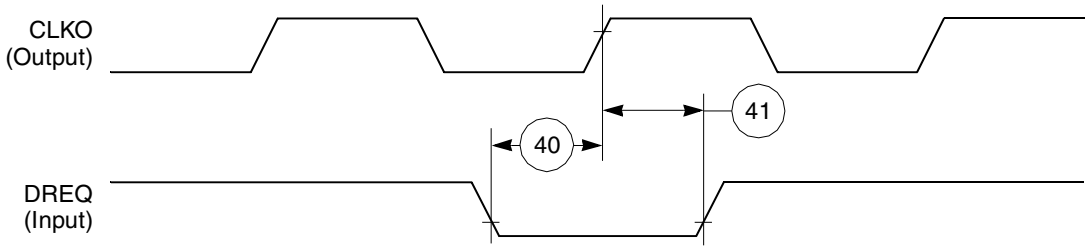


Figure 48. IDMA External Requests Timing Diagram

12.5 Timer AC Electrical Specifications

Table 20 provides the general-purpose timer timings as shown in Figure 53.

Table 20. Timer Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
61	TIN/$\overline{\text{TGATE}}$ rise and fall time	10	—	ns
62	TIN/$\overline{\text{TGATE}}$ low time	1	—	clk
63	TIN/$\overline{\text{TGATE}}$ high time	2	—	clk
64	TIN/$\overline{\text{TGATE}}$ cycle time	3	—	clk
65	CLKO low to $\overline{\text{TOUT}}$ valid	3	25	ns

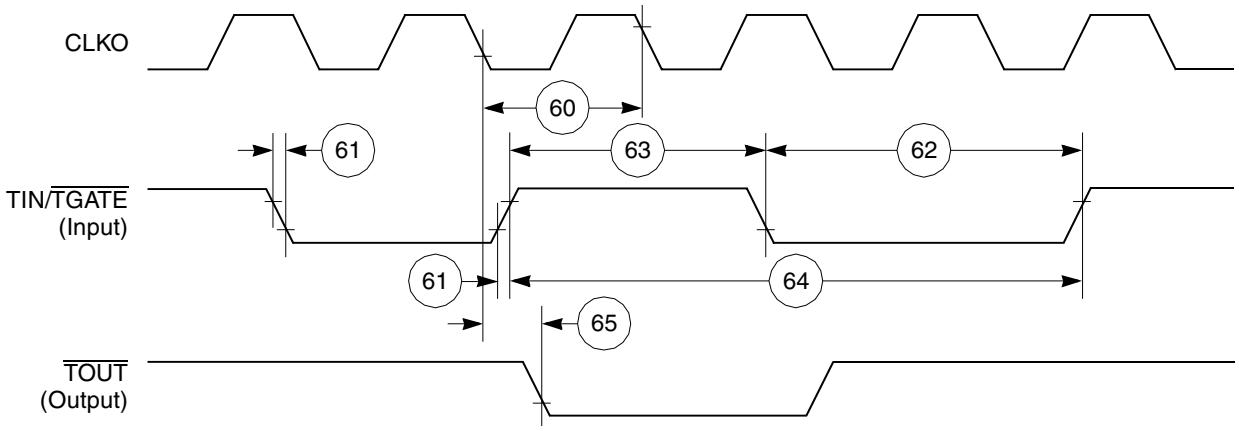


Figure 53. CPM General-Purpose Timers Timing Diagram

12.6 Serial Interface AC Electrical Specifications

Table 21 provides the serial interface timings as shown in Figure 54 through Figure 58.

Table 21. SI Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
70	L1RCLK, L1TCLK frequency (DSC = 0)[1, 2]	—	SYNCCLK/2.5	MHz
71	L1RCLK, L1TCLK width low (DSC = 0)[2]	P + 10	—	ns
71a	L1RCLK, L1TCLK width high (DSC = 0)[3]	P + 10	—	ns
72	L1TXD, L1ST(1–4), $\overline{\text{L1RQ}}$, L1CLKO rise/fall time	—	15.00	ns
73	L1RSYNC, L1TSYNC valid to L1CLK edge (SYNC setup time)	20.00	—	ns
74	L1CLK edge to L1RSYNC, L1TSYNC, invalid (SYNC hold time)	35.00	—	ns
75	L1RSYNC, L1TSYNC rise/fall time	—	15.00	ns

Figure 59 through Figure 61 show the NMSI timings.

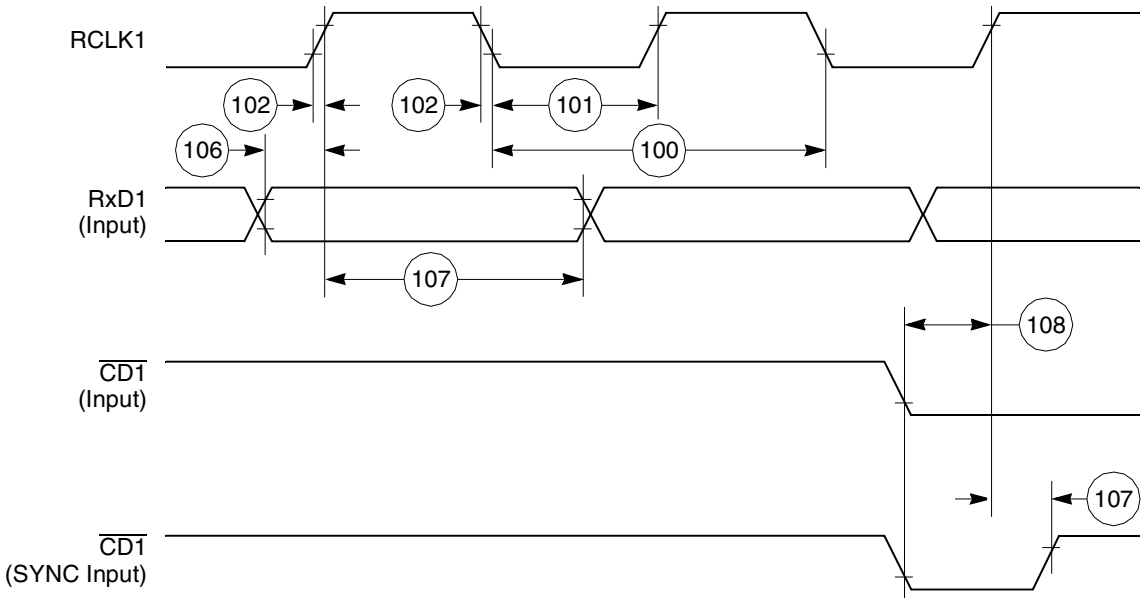


Figure 59. SCC NMSI Receive Timing Diagram

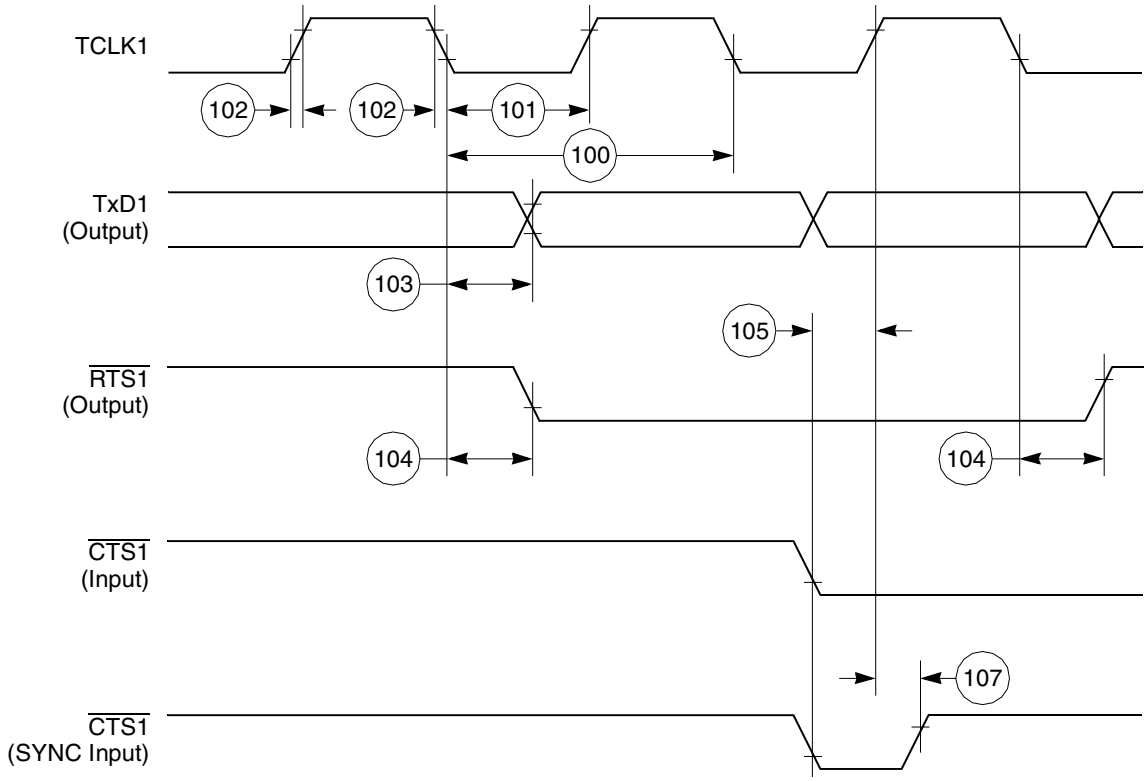


Figure 60. SCC NMSI Transmit Timing Diagram

Figure 74 shows the MII transmit signal timing diagram.

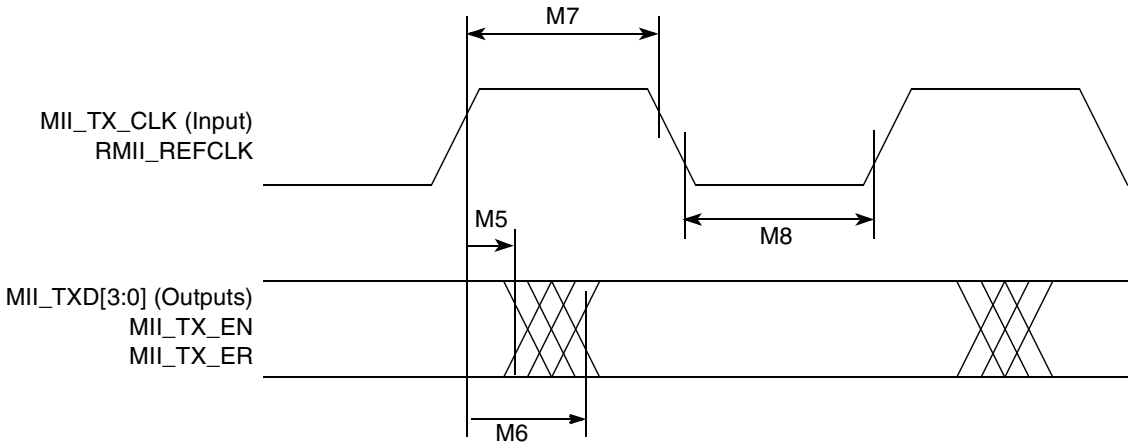


Figure 74. MII Transmit Signal Timing Diagram

15.3 MII Async Inputs Signal Timing (MII_CRS, MII_COL)

Table 36 provides information on the MII async inputs signal timing.

Table 36. MII Async Inputs Signal Timing

Num	Characteristic	Min	Max	Unit
M9	MII_CRS, MII_COL minimum pulse width	1.5	—	MII_TX_CLK period

Figure 75 shows the MII asynchronous inputs signal timing diagram.

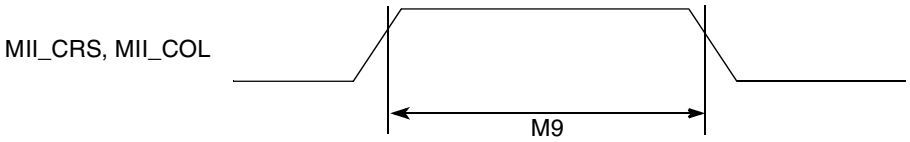


Figure 75. MII Async Inputs Timing Diagram

15.4 MII Serial Management Channel Timing (MII_MDIO, MII_MDC)

Table 37 provides information on the MII serial management channel signal timing. The FEC functions correctly with a maximum MDC frequency in excess of 2.5 MHz.

Table 37. MII Serial Management Channel Timing

Num	Characteristic	Min	Max	Unit
M10	MII_MDC falling edge to MII_MDIO output invalid (minimum propagation delay)	0	—	ns
M11	MII_MDC falling edge to MII_MDIO output valid (max prop delay)	—	25	ns
M12	MII_MDIO (input) to MII_MDC rising edge setup	10	—	ns
M13	MII_MDIO (input) to MII_MDC rising edge hold	0	—	ns

Table 39. Pin Assignments (continued)

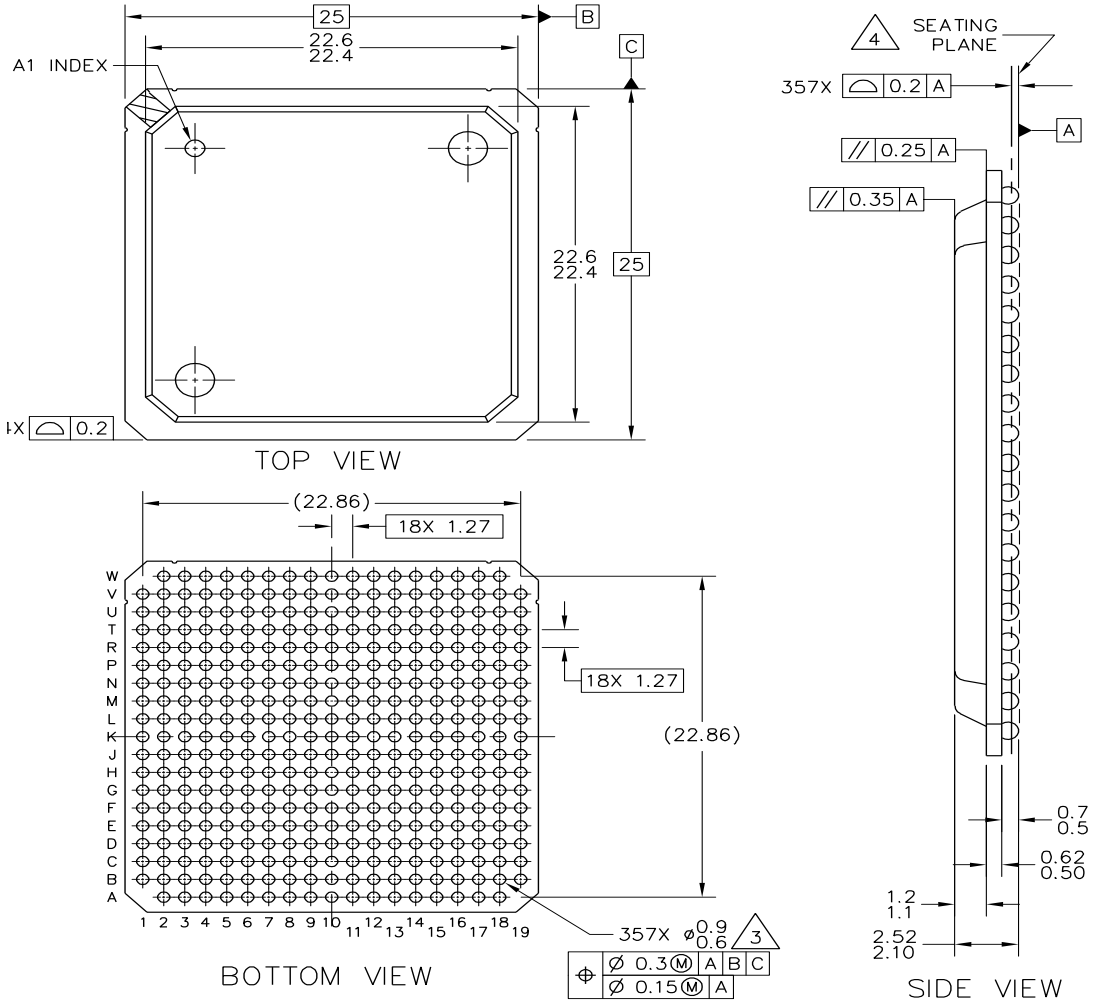
Name	Pin Number	Type
PA4, $\overline{\text{CTS4}}$, MII1-TXD1, RMII1-TXD1	U4	Bidirectional
PA3, MII1-RXER, RMII1-RXER, BRGO3	W2	Bidirectional
PA2, MII1-RXDV, RMII1-CRS_DV, TXD4	T4	Bidirectional
PA1, MII1-RXD0, RMII1-RXD0, BRGO4	U1	Bidirectional
PA0, MII1-RXD1, RMII1-RXD1, $\overline{\text{TOUT4}}$	U3	Bidirectional
PB31, $\overline{\text{SPISEL}}$, MII1-TXCLK, RMII1-REFCLK	V3	Bidirectional (Optional: open-drain)
PB30, SPICLK	P18	Bidirectional (Optional: open-drain)
PB29, SPIMOSI	T19	Bidirectional (Optional: open-drain)
PB28, SPIMISO, BRGO4	V19	Bidirectional (Optional: open-drain)
PB27, I2CSDA, BRGO1	U19	Bidirectional (Optional: open-drain)
PB26, I2CSCL, BRGO2	R17	Bidirectional (Optional: open-drain)
PB25, RXADDR3[1], TXADDR3, SMTXD1	V17	Bidirectional (Optional: open-drain)
PB24, TXADDR3[1], RXADDR3, SMRXD1	U16	Bidirectional (Optional: open-drain)
PB23, TXADDR2[1], RXADDR2, $\overline{\text{SDACK1}}$, $\overline{\text{SMSYN1}}$	W16	Bidirectional (Optional: open-drain)
PB22, TXADDR4[1], RXADDR4, $\overline{\text{SDACK2}}$, $\overline{\text{SMSYN2}}$	V15	Bidirectional (Optional: open-drain)
PB21, SMTXD2, TXADDR1[1], BRG01, RXADDR1, PHSEL[1]	U14	Bidirectional (Optional: open-drain)
PB20, SMRXD2, L1CLKOA, TXADDR0[1], RXADDR0, PHSEL[0]	T13	Bidirectional (Optional: open-drain)
PB19, MII1-RXD3, $\overline{\text{RTS4}}$	V13	Bidirectional (Optional: open-drain)
PB18, RXADDR4[1], TXADDR4, $\overline{\text{RTS2}}$, L1ST2	T12	Bidirectional (Optional: open-drain)

Table 39. Pin Assignments (continued)

Name	Pin Number	Type
PD5, CLK8, L1TCLKB, UTPB6	V6	Bidirectional
PD4, CLK4, UTPB7	W4	Bidirectional
PD3, CLK7, TIN4, SOC	T9	Bidirectional
PE31, CLK8, L1TCLKB, MII1-RXCLK	U9	Bidirectional (Optional: open-drain)
PE30, L1RXDB, MII1-RXD2	W7	Bidirectional (Optional: open-drain)
PE29, MII2-CRS	T8	Bidirectional (Optional: open-drain)
PE28, $\overline{\text{TOUT3}}$, MII2-COL	V5	Bidirectional (Optional: open-drain)
PE27, $\overline{\text{RTS3}}$, L1RQB, MII2-RXER, RMII2-RXER	V4	Bidirectional (Optional: open-drain)
PE26, L1CLKOB, MII2-RXDV, RMII2-CRS_DV	T1	Bidirectional (Optional: open-drain)
PE25, RXD4, MII2-RXD3, L1ST2	T3	Bidirectional (Optional: open-drain)
PE24, SMRXD1, BRGO1, MII2-RXD2	V8	Bidirectional (Optional: open-drain)
PE23, $\overline{\text{SMSYN2}}$, TXD4, MII2-RXCLK, L1ST1	V2	Bidirectional (Optional: open-drain)
PE22, $\overline{\text{TOUT2}}$, MII2-RXD1, RMII2-RXD1, $\overline{\text{SDACK1}}$	V1	Bidirectional (Optional: open-drain)
PE21, SMRXD2, $\overline{\text{TOUT1}}$, MII2-RXD0, RMII2-RXD0, $\overline{\text{RTS3}}$	V9	Bidirectional (Optional: open-drain)
PE20, L1RSYNCA, SMTXD2, $\overline{\text{CTS3}}$, MII2-TXER	R4	Bidirectional (Optional: open-drain)
PE19, L1TXDB, MII2-TXEN, RMII2-TXEN	T6	Bidirectional (Optional: open-drain)
PE18, L1TSYNCA, SMTXD1, MII2-TXD3	R1	Bidirectional (Optional: open-drain)
PE17, TIN3, CLK5, BRGO3, $\overline{\text{SMSYN1}}$, MII2-TXD2	W8	Bidirectional (Optional: open-drain)
PE16, L1RCLKB, CLK6, TXD3, MII2-TXCLK, RMII2-REFCLK	T7	Bidirectional (Optional: open-drain)
PE15, $\overline{\text{TGATE1}}$, MII2-TXD1, RMII2-TXD1	W6	Bidirectional

16.2 Mechanical Dimensions of the PBGA Package

Figure 78 shows the mechanical dimensions of the PBGA package.



NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M—1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

Figure 78. Mechanical Dimensions and Bottom Surface Nomenclature of the PBGA Package