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Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Active
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	66MHz
Co-Processors/DSP	Communications; CPM, Security; SEC
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (3), 10/100Mbps (2)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	Cryptography
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc885vr66

1 Overview

The MPC885/MPC880 is a versatile single-chip integrated microprocessor and peripheral combination that can be used in a variety of controller applications and communications and networking systems. The MPC885/MPC880 provides enhanced ATM functionality, an additional fast Ethernet controller, a USB, and an encryption block.

[Table 1](#) shows the functionality supported by MPC885/MPC880.

Table 1. MPC885 Family

Part	Cache (Kbytes)		Ethernet		SCC	SMC	USB	ATM Support	Security Engine
	I Cache	D Cache	10BaseT	10/100					
MPC885	8	8	Up to 3	2	3	2	1	Serial ATM and UTOPIA interface	Yes
MPC880	8	8	Up to 2	2	2	2	1	Serial ATM and UTOPIA interface	No

2 Features

The MPC885/MPC880 is comprised of three modules that each use the 32-bit internal bus: a MPC8xx core, a system integration unit (SIU), and a communications processor module (CPM).

The following list summarizes the key MPC885/MPC880 features:

- Embedded MPC8xx core up to 133 MHz
- Maximum frequency operation of the external bus is 80 MHz (in 1:1 mode)
 - The 133-MHz core frequency supports 2:1 mode only.
 - The 66-/80-MHz core frequencies support both the 1:1 and 2:1 modes.
- Single-issue, 32-bit core (compatible with the Power Architecture definition) with thirty-two 32-bit general-purpose registers (GPRs)
 - The core performs branch prediction with conditional prefetch and without conditional execution.
 - 8-Kbyte data cache and 8-Kbyte instruction cache (see [Table 1](#))
 - Instruction cache is two-way, set-associative with 256 sets in 2 blocks
 - Data cache is two-way, set-associative with 256 sets
 - Cache coherency for both instruction and data caches is maintained on 128-bit (4-word) cache blocks.
 - Caches are physically addressed, implement a least recently used (LRU) replacement algorithm, and are lockable on a cache block basis.
 - MMUs with 32-entry TLB, fully associative instruction and data TLBs
 - MMUs support multiple page sizes of 4, 16, and 512 Kbytes, and 8 Mbytes; 16 virtual address spaces and 16 protection groups
 - Advanced on-chip emulation debug mode

- Flexible data buffers with multiple buffers per frame
 - Automatic retransmission upon transmit error
- The USB host controller has the following features:
 - Supports control, bulk, interrupt, and isochronous data transfers
 - CRC16 generation and checking
 - NRZI encoding/decoding with bit stuffing
 - Supports both 12- and 1.5-Mbps data rates (automatic generation of preamble token and data rate configuration). Note that low-speed operation requires an external hub.
 - Flexible data buffers with multiple buffers per frame
 - Supports local loop back mode for diagnostics (12 Mbps only)
- Serial peripheral interface (SPI)
 - Supports master and slave modes
 - Supports multiple-master operation on the same bus
- Inter-integrated circuit (I²C) port
 - Supports master and slave modes
 - Supports a multiple-master environment
- Time-slot assigner (TSA)
 - Allows SCCs and SMCs to run in multiplexed and/or non-multiplexed operation
 - Supports T1, CEPT, PCM highway, ISDN basic rate, ISDN primary rate, user defined
 - 1- or 8-bit resolution
 - Allows independent transmit and receive routing, frame synchronization, and clocking
 - Allows dynamic changes
 - Can be internally connected to four serial channels (two SCCs and two SMCs)
- Parallel interface port (PIP)
 - Centronics interface support
 - Supports fast connection between compatible ports on MPC885/MPC880 and other MPC8xx devices
- PCMCIA interface
 - Master (socket) interface, release 2.1-compliant
 - Supports two independent PCMCIA sockets
 - 8 memory or I/O windows supported
- Debug interface
 - Eight comparators: four operate on instruction address, two operate on data address, and two operate on data
 - Supports conditions: = ≠ < >
 - Each watchpoint can generate a break point internally.
- Normal high and normal low power modes to conserve power

3 Maximum Tolerated Ratings

This section provides the maximum tolerated voltage and temperature ranges for the MPC885/MPC880. Table 2 displays the maximum tolerated ratings, and Table 3 displays the operating temperatures.

Table 2. Maximum Tolerated Ratings

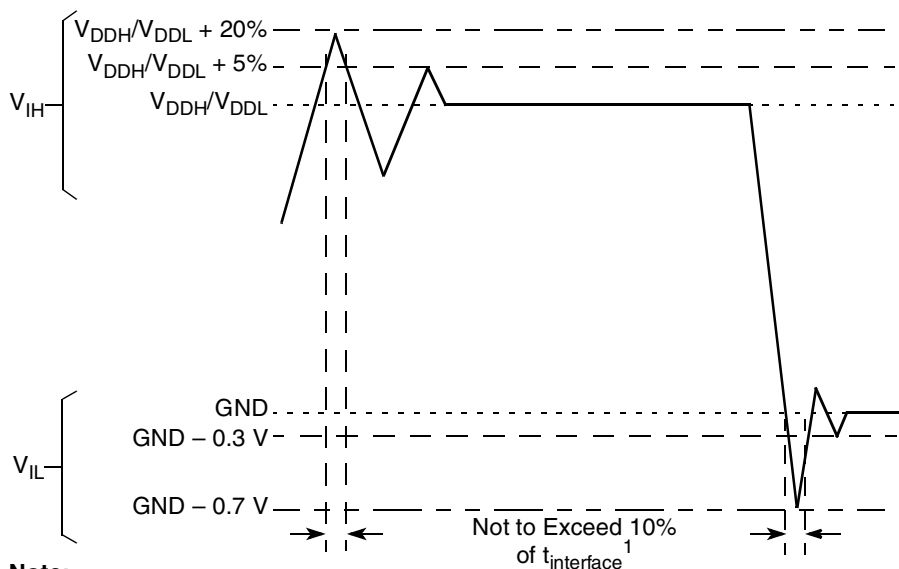
Rating	Symbol	Value	Unit
Supply voltage ¹	V_{DDH}	−0.3 to 4.0	V
	V_{DDL}	−0.3 to 2.0	V
	V_{DDSYN}	−0.3 to 2.0	V
	Difference between V_{DDL} and V_{DDSYN}	<100	mV
Input voltage ²	V_{in}	GND − 0.3 to V_{DDH}	V
Storage temperature range	T_{stg}	−55 to +150	°C

¹ The power supply of the device must start its ramp from 0.0 V.

² Functional operating conditions are provided with the DC electrical specifications in Table 6. Absolute maximum ratings are stress ratings only; functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device. See Section 8, “Power Supply and Power Sequencing.”

Caution: All inputs that tolerate 5 V cannot be more than 2.5 V greater than V_{DDH} . This restriction applies to power up and normal operation (that is, if the MPC885/MPC880 is unpowered, a voltage greater than 2.5 V must not be applied to its inputs).

Figure 3 shows the undershoot and overshoot voltages at the interfaces of the MPC885/MPC880.



Note:

1. $t_{interface}$ refers to the clock period associated with the bus clock interface.

Figure 3. Undershoot/Overshoot Voltage for V_{DDH} and V_{DDL}

7.6 References

Semiconductor Equipment and Materials International(415) 964-5111
805 East Middlefield Rd
Mountain View, CA 94043

MIL-SPEC and EIA/JESD (JEDEC) specifications800-854-7179 or
(Available from Global Engineering Documents)303-397-7956

JEDEC Specifications <http://www.jedec.org>

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
2. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

8 Power Supply and Power Sequencing

This section provides design considerations for the MPC885/MPC880 power supply. The MPC885/MPC880 has a core voltage (V_{DDL}) and PLL voltage (V_{DDSYN}), which both operate at a lower voltage than the I/O voltage V_{DDH} . The I/O section of the MPC885/MPC880 is supplied with 3.3 V across V_{DDH} and V_{SS} (GND).

The signals PA[0:15], PB[14:31], PC[4:15], PD[3:15], TDI, TDO, TCK, TRST_B, TMS, MII_TXEN, and MII_MDIO are 5 V tolerant. All inputs cannot be more than 2.5 V greater than V_{DDH} . In addition, 5-V tolerant pins cannot exceed 5.5 V and remaining input pins cannot exceed 3.465 V. This restriction applies to power up/down and normal operation.

One consequence of multiple power supplies is that when power is initially applied the voltage rails ramp up at different rates. The rates depend on the nature of the power supply, the type of load on each power supply, and the manner in which different voltages are derived. The following restrictions apply:

- V_{DDL} must not exceed V_{DDH} during power up and power down.
- V_{DDL} must not exceed 1.9 V, and V_{DDH} must not exceed 3.465 V.

These cautions are necessary for the long-term reliability of the part. If they are violated, the electrostatic discharge (ESD) protection diodes are forward-biased, and excessive current can flow through these diodes. If the system power supply design does not control the voltage sequencing, the circuit shown [Figure 5](#) can be added to meet these requirements. The MUR420 Schottky diodes control the maximum potential difference between the external bus and core power supplies on power up, and the 1N5820 diodes regulate the maximum potential difference on power down.

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B27a	A(0:31) and BADDR(28:30) to \overline{CS} asserted GPCM ACS = 11, TRLX = 1 (MIN = $1.50 \times B1 - 2.00$)	43.50	—	35.50	—	20.70	—	16.75	—	ns
B28	CLKOUT rising edge to $\overline{WE}(0:3)$ negated GPCM write access CSNT = 0 (MAX = $0.00 \times B1 + 9.00$)	—	9.00	—	9.00	—	9.00	—	9.00	ns
B28a	CLKOUT falling edge to $\overline{WE}(0:3)$ negated GPCM write access TRLX = 0, CSNT = 1, EBDF = 0 (MAX = $0.25 \times B1 + 6.80$)	7.60	14.30	6.30	13.00	3.80	10.50	3.13	9.93	ns
B28b	CLKOUT falling edge to \overline{CS} negated GPCM write access TRLX = 0, CSNT = 1 ACS = 10 or ACS = 11, EBDF = 0 (MAX = $0.25 \times B1 + 6.80$)	—	14.30	—	13.00	—	10.50	—	9.93	ns
B28c	CLKOUT falling edge to $\overline{WE}(0:3)$ negated GPCM write access TRLX = 0, CSNT = 1 write access TRLX = 0, CSNT = 1, EBDF = 1 (MAX = $0.375 \times B1 + 6.6$)	10.90	18.00	10.90	18.00	5.20	12.30	4.69	11.29	ns
B28d	CLKOUT falling edge to \overline{CS} negated GPCM write access TRLX = 0, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1 (MAX = $0.375 \times B1 + 6.6$)	—	18.00	—	18.00	—	12.30	—	11.30	ns
B29	$\overline{WE}(0:3)$ negated to D(0:31) High-Z GPCM write access, CSNT = 0, EBDF = 0 (MIN = $0.25 \times B1 - 2.00$)	5.60	—	4.30	—	1.80	—	1.13	—	ns
B29a	$\overline{WE}(0:3)$ negated to D(0:31) High-Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 0 (MIN = $0.50 \times B1 - 2.00$)	13.20	—	10.50	—	5.60	—	4.25	—	ns
B29b	\overline{CS} negated to D(0:31) High-Z GPCM write access, ACS = 00, TRLX = 0 & CSNT = 0 (MIN = $0.25 \times B1 - 2.00$)	5.60	—	4.30	—	1.80	—	1.13	—	ns
B29c	\overline{CS} negated to D(0:31) High-Z GPCM write access, TRLX = 0, CSNT = 1, ACS = 10, or ACS = 11 EBDF = 0 (MIN = $0.50 \times B1 - 2.00$)	13.20	—	10.50	—	5.60	—	4.25	—	ns
B29d	$\overline{WE}(0:3)$ negated to D(0:31) High-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 0 (MIN = $1.50 \times B1 - 2.00$)	43.50	—	35.50	—	20.70	—	16.75	—	ns
B29e	\overline{CS} negated to D(0:31) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11 EBDF = 0 (MIN = $1.50 \times B1 - 2.00$)	43.50	—	35.50	—	20.70	—	16.75	—	ns
B29f	$\overline{WE}(0:3)$ negated to D(0:31) High-Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 1 (MIN = $0.375 \times B1 - 6.30$) ⁷	5.00	—	3.00	—	0.00	—	0.00	—	ns
B29g	\overline{CS} negated to D(0:31) High-Z GPCM write access, TRLX = 0, CSNT = 1 ACS = 10 or ACS = 11, EBDF = 1 (MIN = $0.375 \times B1 - 6.30$) ⁷	5.00	—	3.00	—	0.00	—	0.00	—	ns

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B36	A(0:31), BADDR(28:30), and D(0:31) to \overline{GPL} valid, as requested by control bit GxT4 in the corresponding word in the UPM (MIN = $0.25 \times B1 - 2.00$)	5.60	—	4.30	—	1.80	—	1.13	—	ns
B37	UPWAIT valid to CLKOUT falling edge ⁹ (MIN = $0.00 \times B1 + 6.00$)	6.00	—	6.00	—	6.00	—	6.00	—	ns
B38	CLKOUT falling edge to UPWAIT valid ⁹ (MIN = $0.00 \times B1 + 1.00$)	1.00	—	1.00	—	1.00	—	1.00	—	ns
B39	\overline{AS} valid to CLKOUT rising edge ¹⁰ (MIN = $0.00 \times B1 + 7.00$)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B40	A(0:31), TSIZ(0:1), RD/ \overline{WR} , \overline{BURST} , valid to CLKOUT rising edge (MIN = $0.00 \times B1 + 7.00$)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B41	\overline{TS} valid to CLKOUT rising edge (setup time) (MIN = $0.00 \times B1 + 7.00$)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B42	CLKOUT rising edge to \overline{TS} valid (hold time) (MIN = $0.00 \times B1 + 2.00$)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B43	\overline{AS} negation to memory controller signals negation (MAX = TBD)	—	TBD	—	TBD	—	TBD	—	TBD	ns

¹ For part speeds above 50 MHz, use 9.80 ns for B11a.

² The timing required for \overline{BR} input is relevant when the MPC885/MPC880 is selected to work with the internal bus arbiter. The timing for \overline{BG} input is relevant when the MPC885/MPC880 is selected to work with the external bus arbiter.

³ For part speeds above 50 MHz, use 2 ns for B17.

⁴ The D(0:31) input timings B18 and B19 refer to the rising edge of the CLKOUT in which the \overline{TA} input signal is asserted.

⁵ For part speeds above 50 MHz, use 2 ns for B19.

⁶ The D(0:31) input timings B20 and B21 refer to the falling edge of the CLKOUT. This timing is valid only for read accesses controlled by chip-selects under control of the user-programmable machine (UPM) in the memory controller, for data beats where DLT3 = 1 in the RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

⁷ This formula applies to bus operation up to 50 MHz.

⁸ The timing B30 refers to \overline{CS} when ACS = 00 and to \overline{CS} and $\overline{WE}(0:3)$ when CSNT = 0.

⁹ The signal UPWAIT is considered asynchronous to the CLKOUT and synchronized internally. The timings specified in B37 and B38 are specified to enable the freeze of the UPM output signals as described in [Figure 21](#).

¹⁰ The \overline{AS} signal is considered asynchronous to the CLKOUT. The timing B39 is specified in order to allow the behavior specified in [Figure 24](#).

Figure 6 provides the control timing diagram.

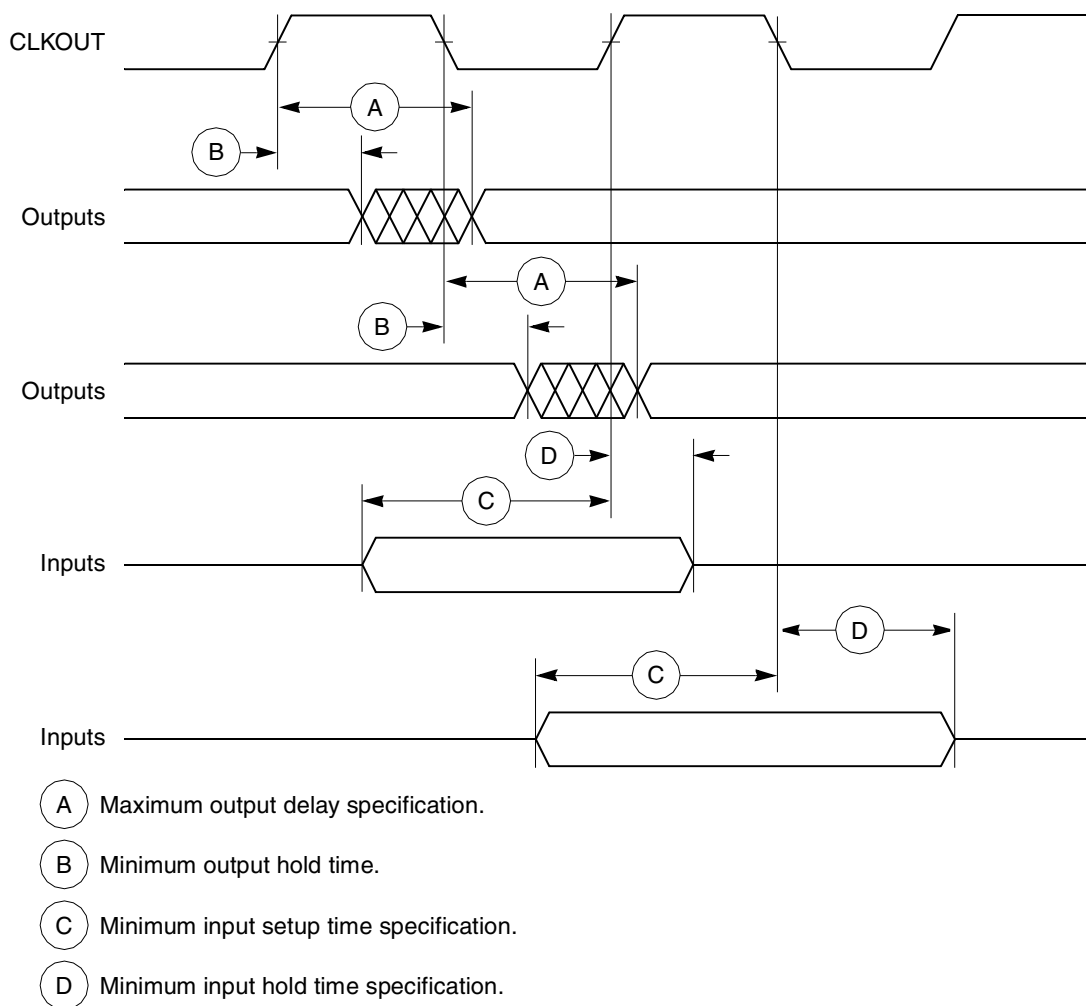


Figure 6. Control Timing

Figure 7 provides the timing for the external clock.

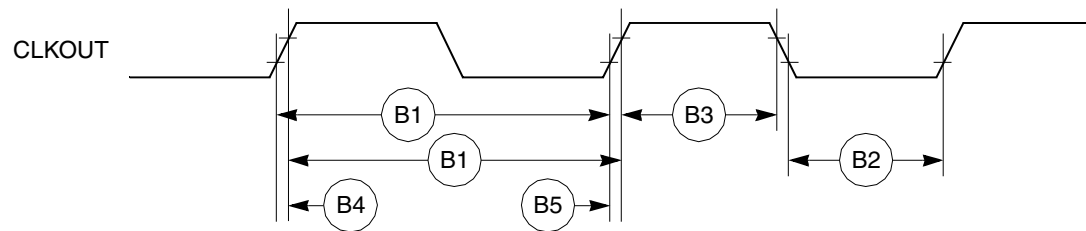


Figure 7. External Clock Timing

Figure 23 provides the timing for the synchronous external master access controlled by the GPCM.

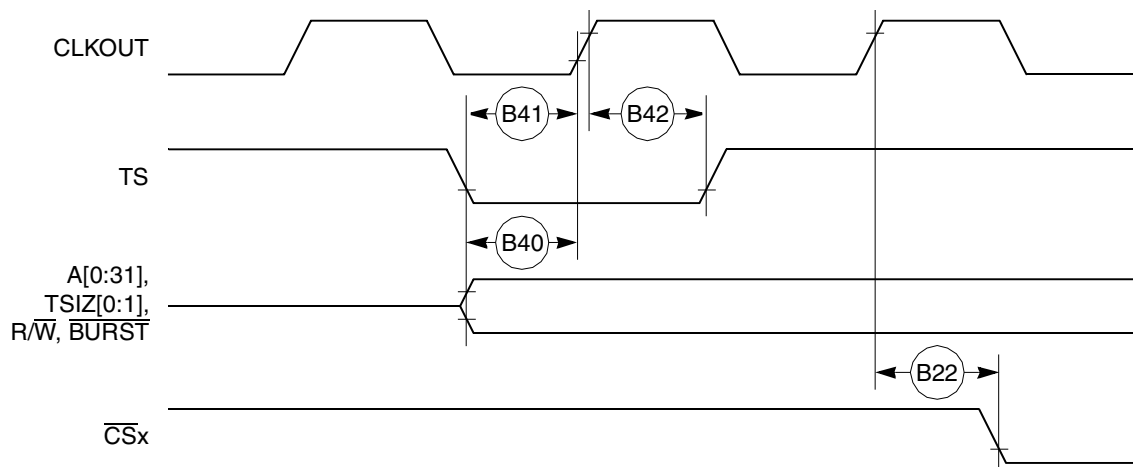


Figure 23. Synchronous External Master Access Timing (GPCM Handled—ACS = 00)

Figure 24 provides the timing for the asynchronous external master memory access controlled by the GPCM.

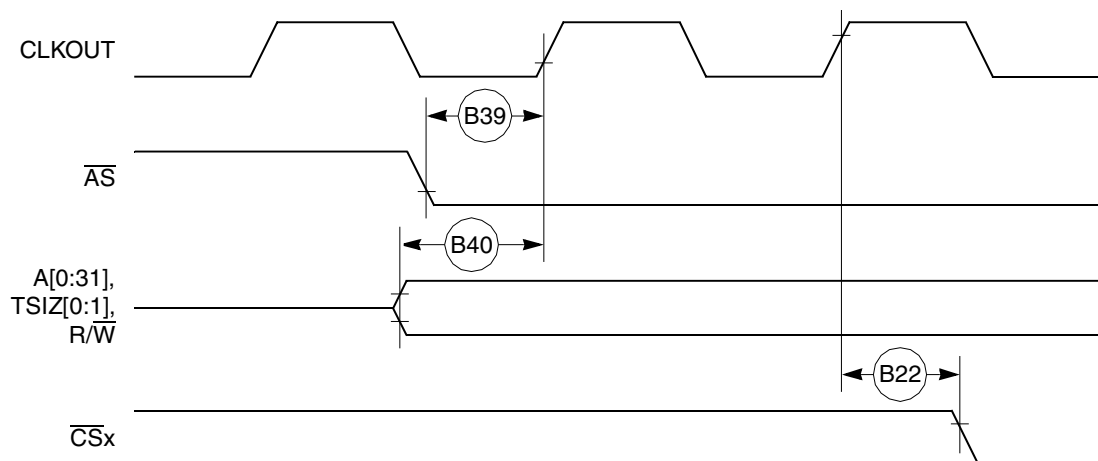


Figure 24. Asynchronous External Master Memory Access Timing (GPCM Controlled—ACS = 00)

Figure 25 provides the timing for the asynchronous external master control signals negation.

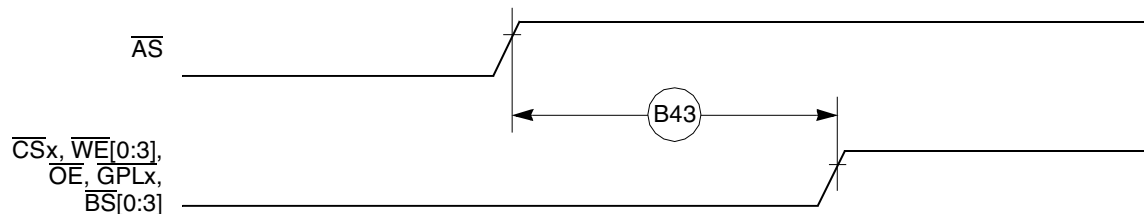


Figure 25. Asynchronous External Master—Control Signals Negation Timing

Table 12 shows the PCMCIA port timing for the MPC885/MPC880.

Table 12. PCMCIA Port Timing

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
P57	CLKOUT to OPx valid (MAX = $0.00 \times B1 + 19.00$)	—	19.00	—	19.00	—	19.00	—	19.00	ns
P58	HRESET negated to OPx drive ¹ (MIN = $0.75 \times B1 + 3.00$)	25.70	—	21.70	—	14.40	—	12.40	—	ns
P59	IP_Xx valid to CLKOUT rising edge (MIN = $0.00 \times B1 + 5.00$)	5.00	—	5.00	—	5.00	—	5.00	—	ns
P60	CLKOUT rising edge to IP_Xx invalid (MIN = $0.00 \times B1 + 1.00$)	1.00	—	1.00	—	1.00	—	1.00	—	ns

¹ OP2 and OP3 only.

Figure 31 provides the PCMCIA output port timing for the MPC885/MPC880.

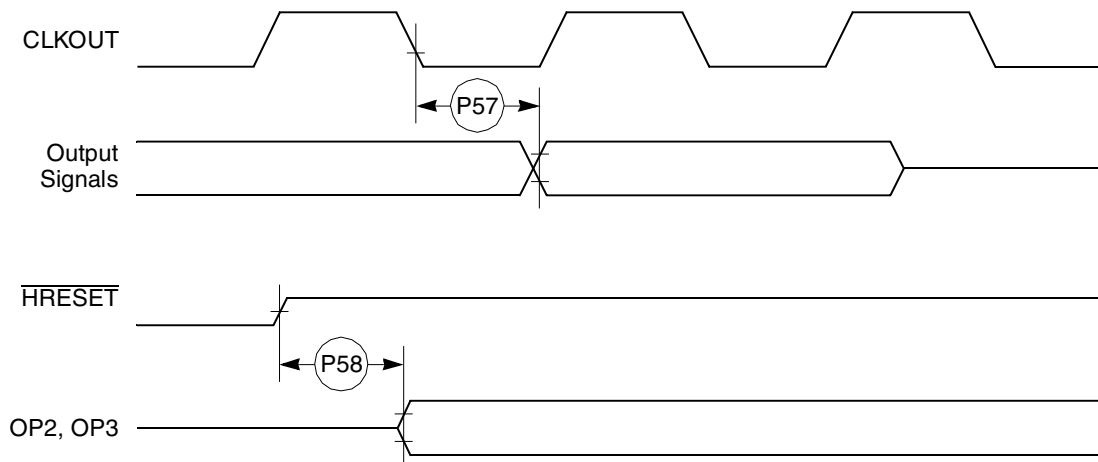


Figure 31. PCMCIA Output Port Timing

Figure 32 provides the PCMCIA input port timing for the MPC885/MPC880.

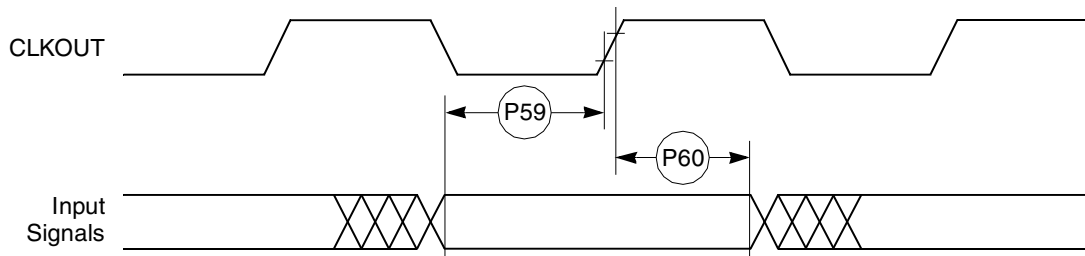


Figure 32. PCMCIA Input Port Timing

Table 14 shows the reset timing for the MPC885/MPC880.

Table 14. Reset Timing

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
R69	CLKOUT to $\overline{\text{HRESET}}$ high impedance (MAX = $0.00 \times B1 + 20.00$)	—	20.00	—	20.00	—	20.00	—	20.00	ns
R70	CLKOUT to $\overline{\text{SRESET}}$ high impedance (MAX = $0.00 \times B1 + 20.00$)	—	20.00	—	20.00	—	20.00	—	20.00	ns
R71	$\overline{\text{RSTCONF}}$ pulse width (MIN = $17.00 \times B1$)	515.20	—	425.00	—	257.60	—	212.50	—	ns
R72	—	—	—	—	—	—	—	—	—	—
R73	Configuration data to $\overline{\text{HRESET}}$ rising edge setup time (MIN = $15.00 \times B1 + 50.00$)	504.50	—	425.00	—	277.30	—	237.50	—	ns
R74	Configuration data to $\overline{\text{RSTCONF}}$ rising edge setup time (MIN = $0.00 \times B1 + 350.00$)	350.00	—	350.00	—	350.00	—	350.00	—	ns
R75	Configuration data hold time after $\overline{\text{RSTCONF}}$ negation (MIN = $0.00 \times B1 + 0.00$)	0.00	—	0.00	—	0.00	—	0.00	—	ns
R76	Configuration data hold time after $\overline{\text{HRESET}}$ negation (MIN = $0.00 \times B1 + 0.00$)	0.00	—	0.00	—	0.00	—	0.00	—	ns
R77	$\overline{\text{HRESET}}$ and $\overline{\text{RSTCONF}}$ asserted to data out drive (MAX = $0.00 \times B1 + 25.00$)	—	25.00	—	25.00	—	25.00	—	25.00	ns
R78	$\overline{\text{RSTCONF}}$ negated to data out high impedance (MAX = $0.00 \times B1 + 25.00$)	—	25.00	—	25.00	—	25.00	—	25.00	ns
R79	CLKOUT of last rising edge before chip three-states $\overline{\text{HRESET}}$ to data out high impedance (MAX = $0.00 \times B1 + 25.00$)	—	25.00	—	25.00	—	25.00	—	25.00	ns
R80	DSDI, DSCK setup (MIN = $3.00 \times B1$)	90.90	—	75.00	—	45.50	—	37.50	—	ns
R81	DSDI, DSCK hold time (MIN = $0.00 \times B1 + 0.00$)	0.00	—	0.00	—	0.00	—	0.00	—	ns
R82	$\overline{\text{SRESET}}$ negated to CLKOUT rising edge for DSDI and DSCK sample (MIN = $8.00 \times B1$)	242.40	—	200.00	—	121.20	—	100.00	—	ns

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Table 15 provides the JTAG timings for the MPC885/MPC880 shown in Figure 38 through Figure 41.

Table 15. JTAG Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
J82	TCK cycle time	100.00	—	ns
J83	TCK clock pulse width measured at 1.5 V	40.00	—	ns
J84	TCK rise and fall times	0.00	10.00	ns
J85	TMS, TDI data setup time	5.00	—	ns
J86	TMS, TDI data hold time	25.00	—	ns
J87	TCK low to TDO data valid	—	27.00	ns
J88	TCK low to TDO data invalid	0.00	—	ns
J89	TCK low to TDO high impedance	—	20.00	ns
J90	$\overline{\text{TRST}}$ assert time	100.00	—	ns
J91	$\overline{\text{TRST}}$ setup time to TCK low	40.00	—	ns
J92	TCK falling edge to output valid	—	50.00	ns
J93	TCK falling edge to output valid out of high impedance	—	50.00	ns
J94	TCK falling edge to output high impedance	—	50.00	ns
J95	Boundary scan input valid to TCK rising edge	50.00	—	ns
J96	TCK rising edge to boundary scan input invalid	50.00	—	ns

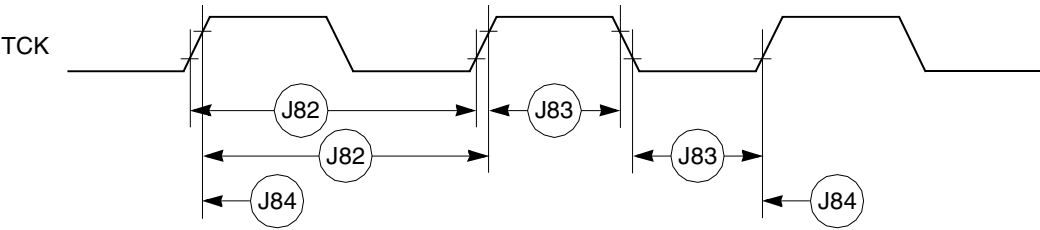


Figure 38. JTAG Test Clock Input Timing

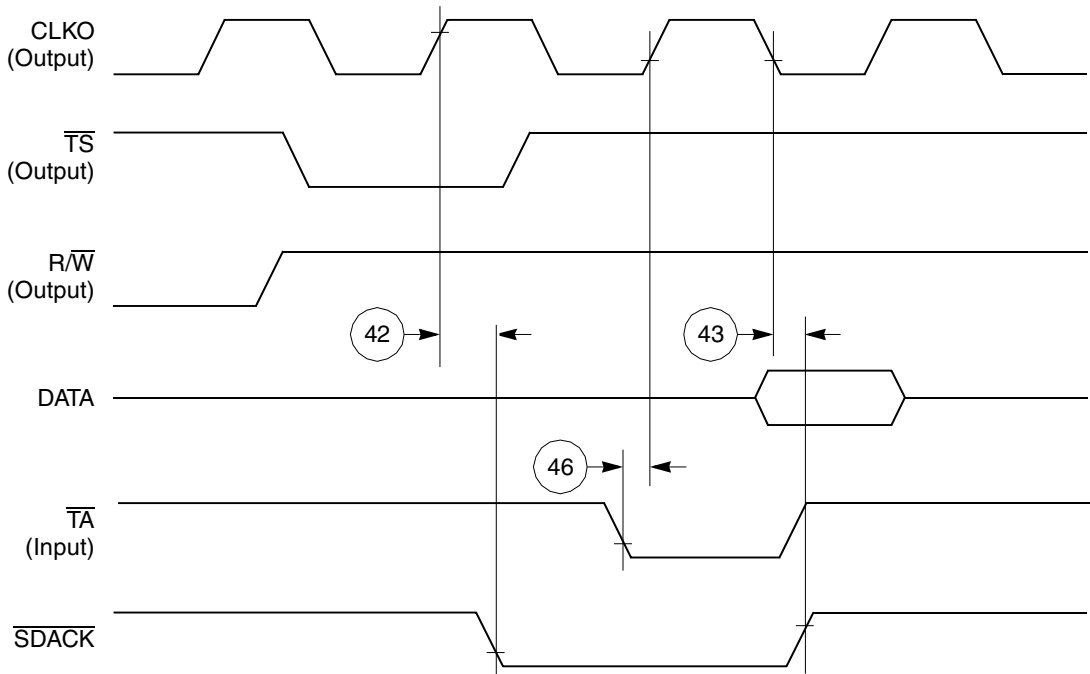


Figure 49. $\overline{\text{SDACK}}$ Timing Diagram—Peripheral Write, Externally-Generated $\overline{\text{TA}}$

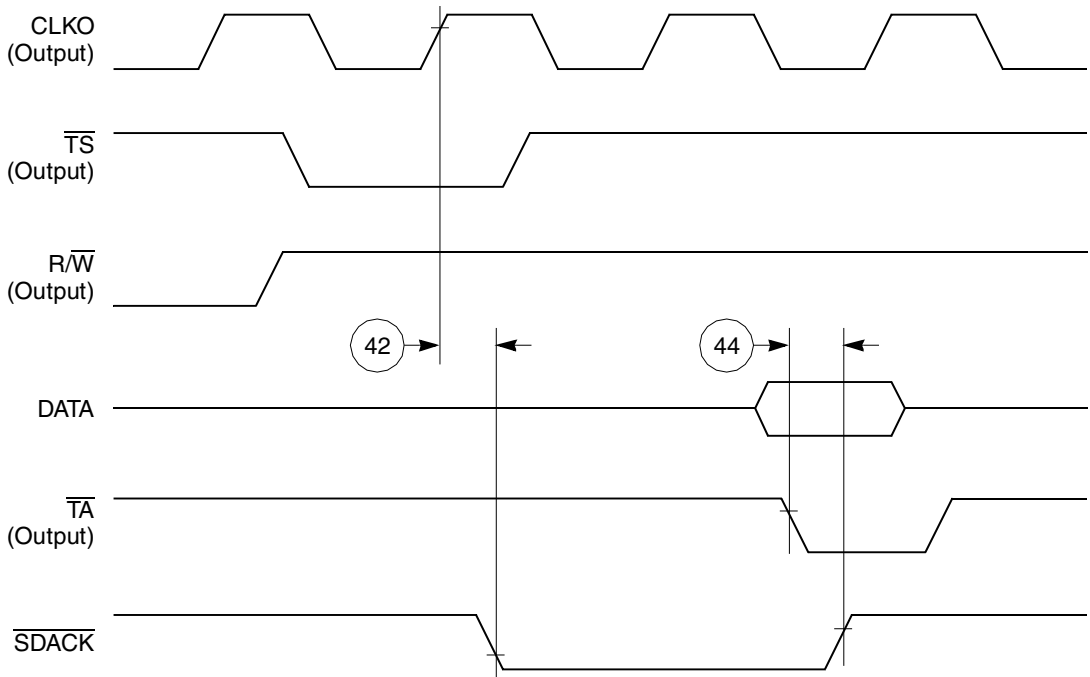


Figure 50. $\overline{\text{SDACK}}$ Timing Diagram—Peripheral Write, Internally-Generated $\overline{\text{TA}}$

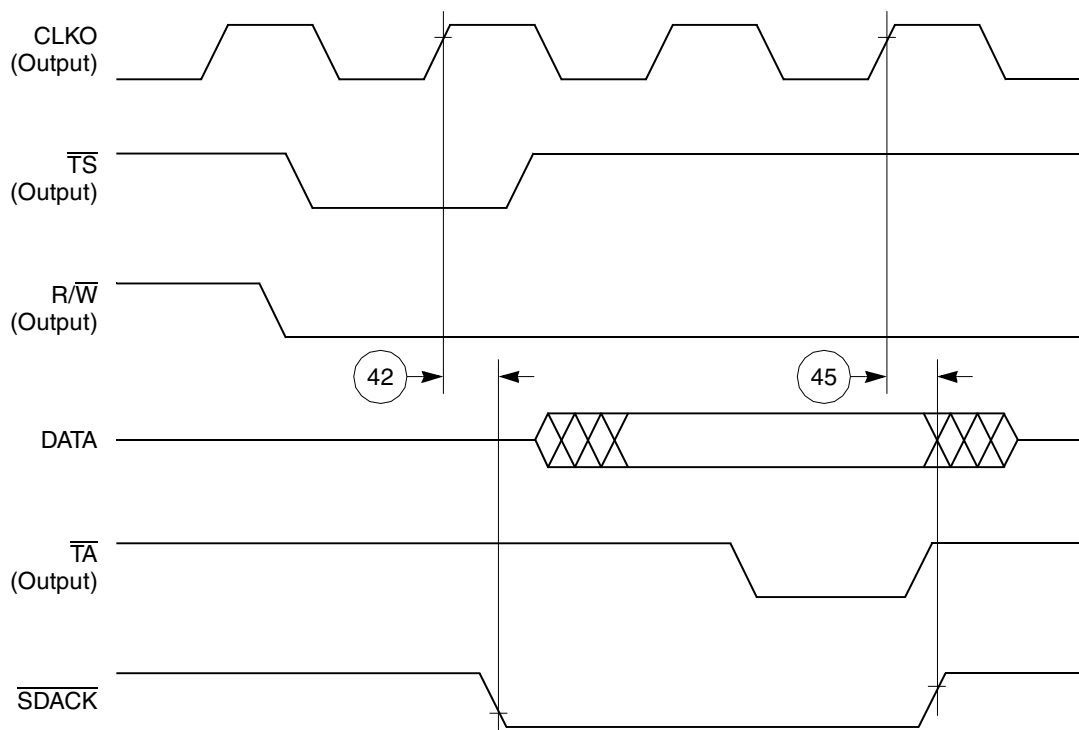


Figure 51. $\overline{\text{SDACK}}$ Timing Diagram—Peripheral Read, Internally-Generated $\overline{\text{TA}}$

12.4 Baud Rate Generator AC Electrical Specifications

Table 19 provides the baud rate generator timings as shown in Figure 52.

Table 19. Baud Rate Generator Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
50	BRGO rise and fall time	—	10	ns
51	BRGO duty cycle	40	60	%
52	BRGO cycle	40	—	ns

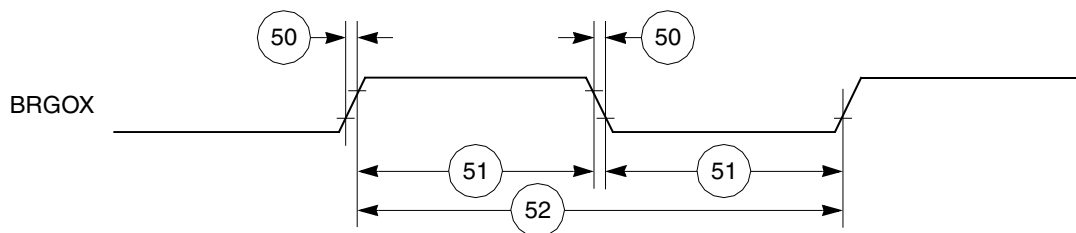


Figure 52. Baud Rate Generator Timing Diagram

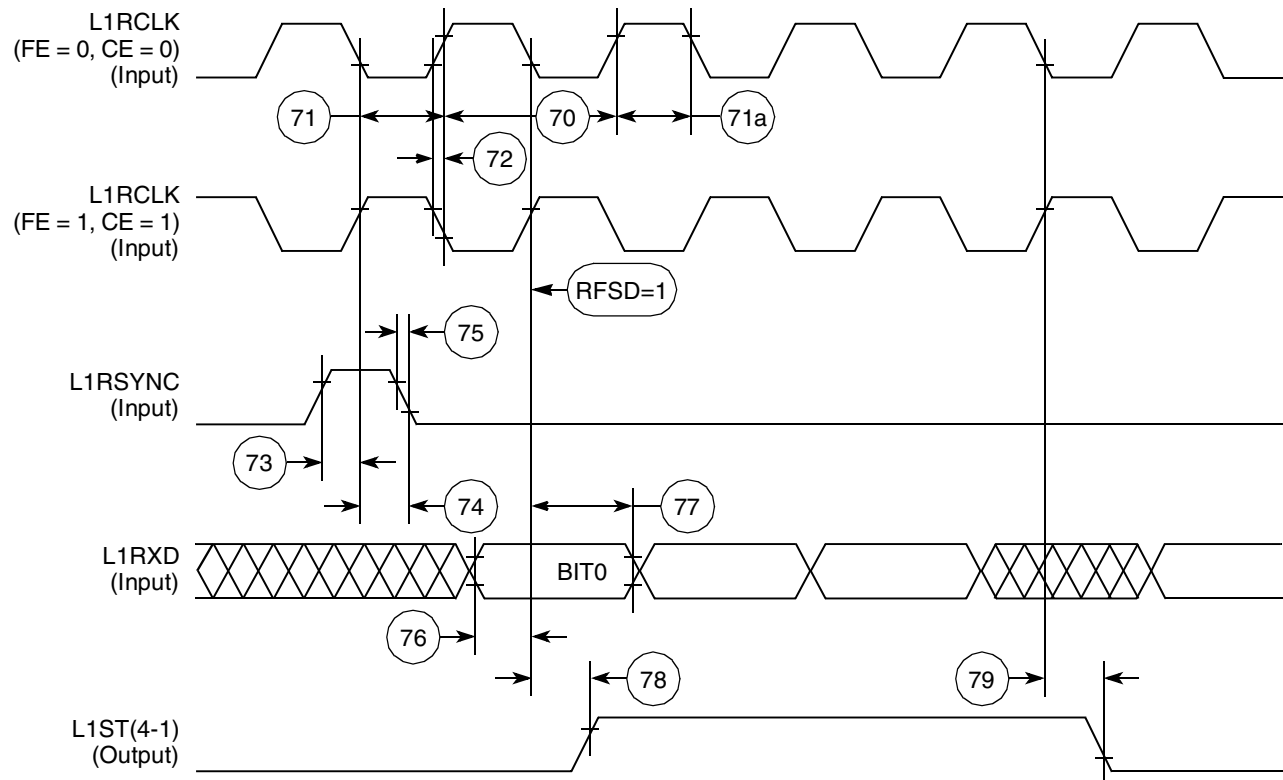


Figure 54. SI Receive Timing Diagram with Normal Clocking (DSC = 0)

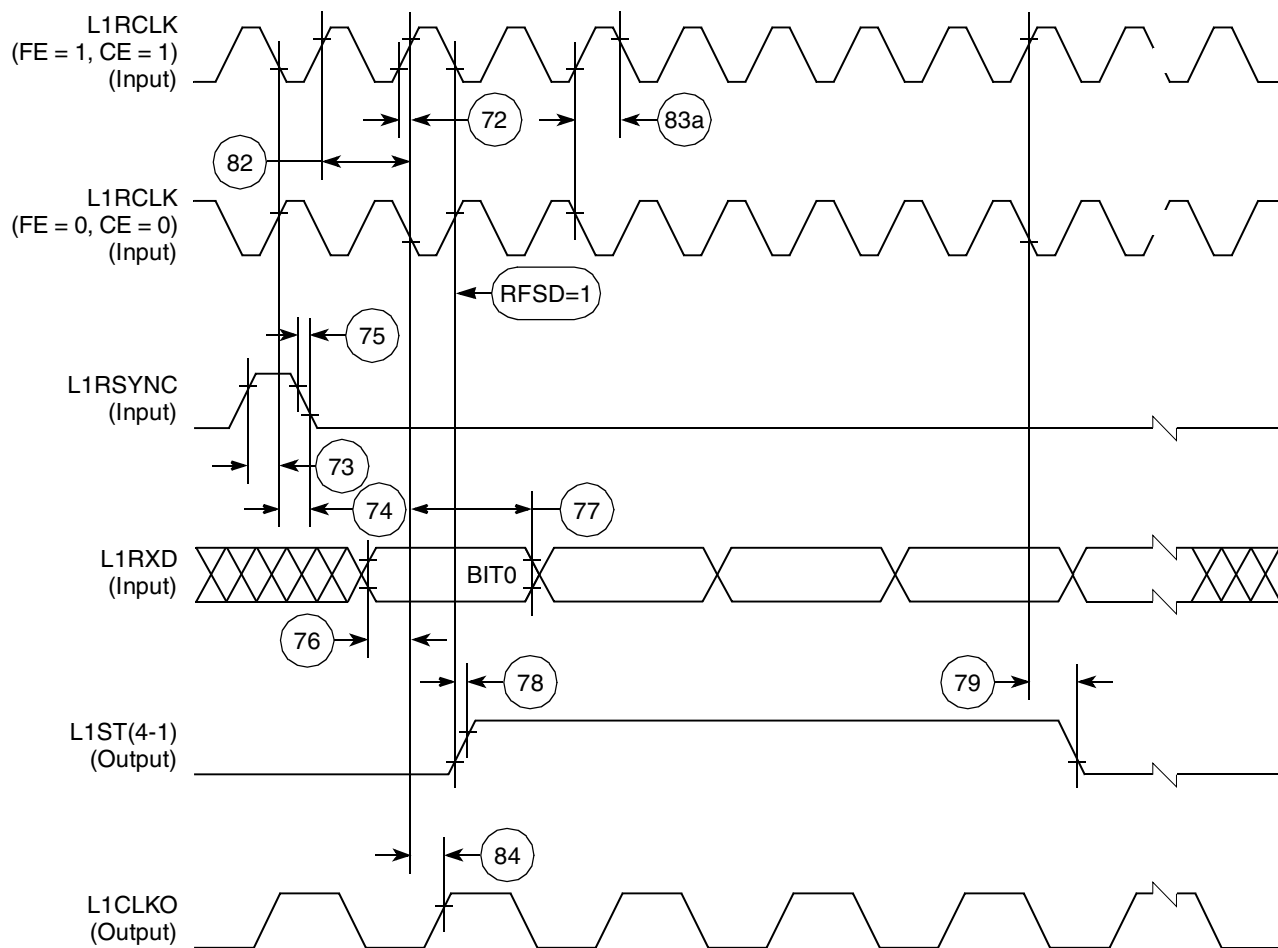


Figure 55. SI Receive Timing with Double-Speed Clocking (DSC = 1)

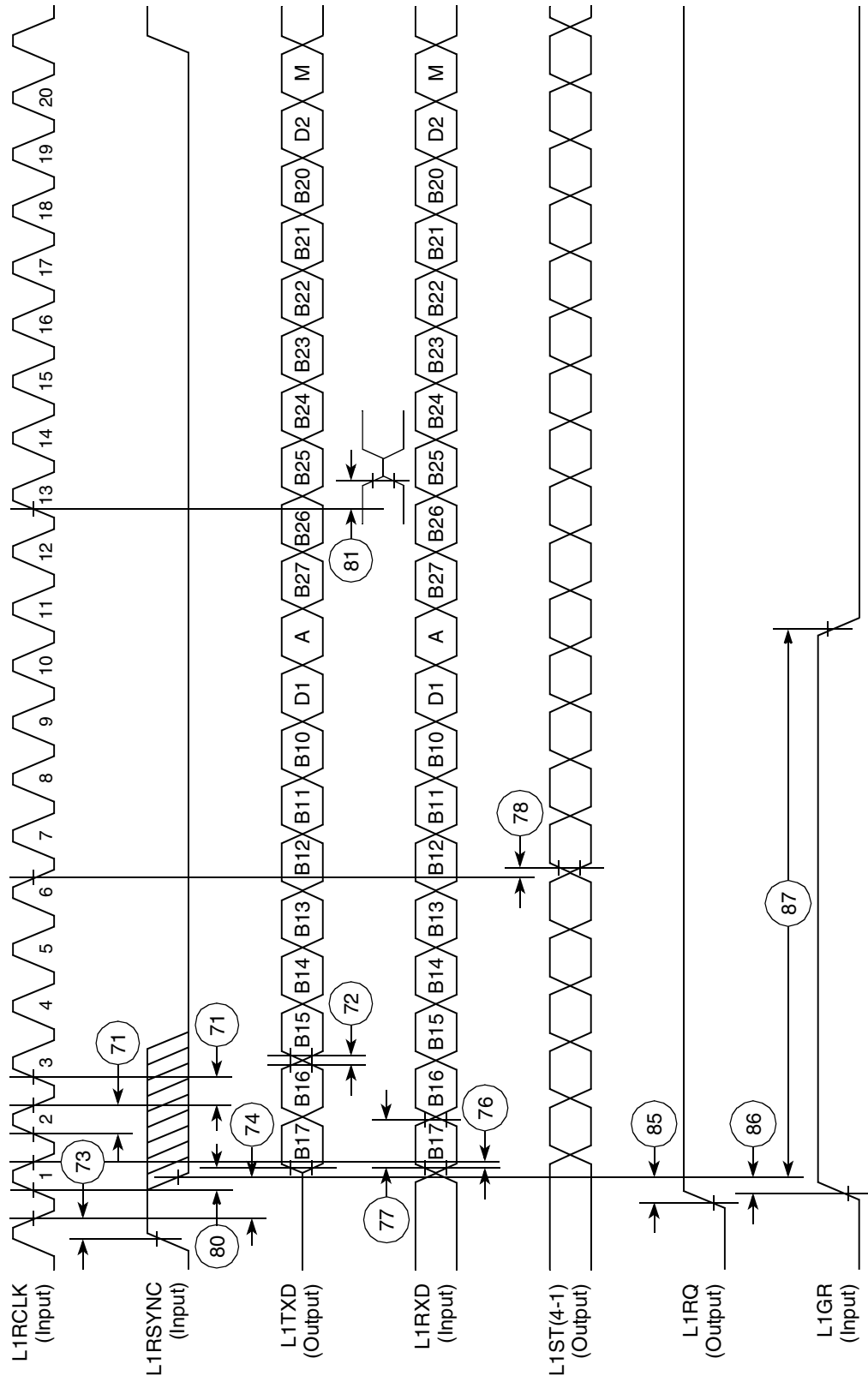
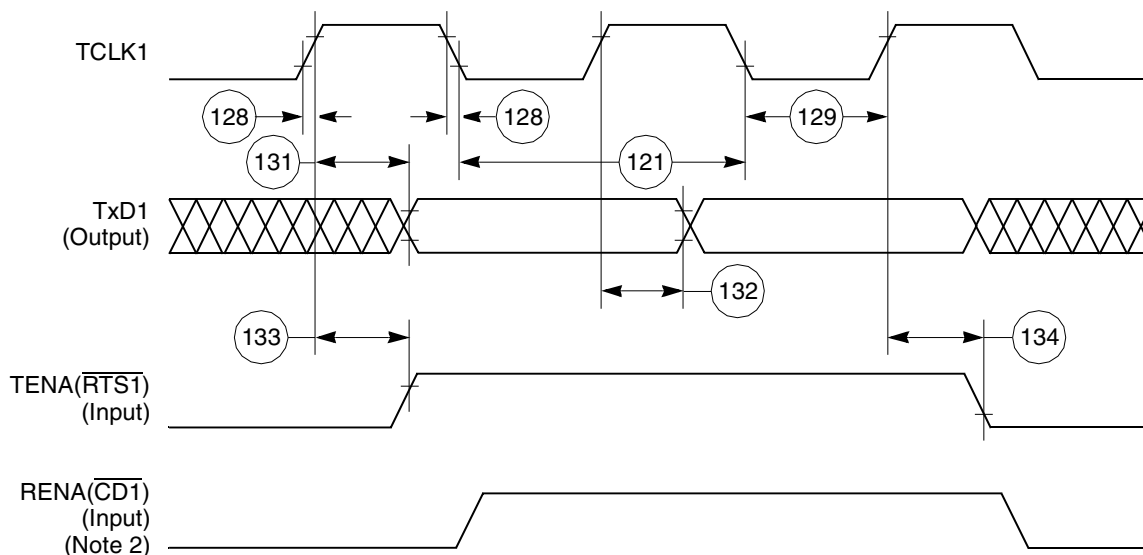


Figure 58. IDL Timing


Notes:

1. Transmit clock invert (TCI) bit in GSMR is set.
2. If RENA is negated before TENA or RENA is not asserted at all during transmit, then the CSL bit is set in the buffer descriptor at the end of the frame transmission.

Figure 64. Ethernet Transmit Timing Diagram

12.9 SMC Transparent AC Electrical Specifications

Table 25 provides the SMC transparent timings as shown in Figure 65.

Table 25. SMC Transparent Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
150	SMCLK clock period ¹	100	—	ns
151	SMCLK width low	50	—	ns
151A	SMCLK width high	50	—	ns
152	SMCLK rise/fall time	—	15	ns
153	SMTXD active delay (from SMCLK falling edge)	10	50	ns
154	SMRXD/SMSYNC setup time	20	—	ns
155	RXD1/SMSYNC hold time	5	—	ns

¹ SyncCLK must be at least twice as fast as SMCLK.

14 USB Electrical Characteristics

This section provides the AC timings for the USB interface.

14.1 USB Interface AC Timing Specifications

The USB Port uses the transmit clock on SCC1. [Table 33](#) lists the USB interface timings.

Table 33. USB Interface AC Timing Specifications

Name	Characteristic	All Frequencies		Unit
		Min	Max	
US1	USBCLK frequency of operation ¹			
	Low speed	6		MHz
	Full speed	48		MHz
US4	USBCLK duty cycle (measured at 1.5 V)	45	55	%

¹ USBCLK accuracy should be ± 500 ppm or better. USBCLK may be stopped to conserve power.

15 FEC Electrical Characteristics

This section provides the AC electrical specifications for the fast Ethernet controller (FEC). Note that the timing specifications for the MII signals are independent of system clock frequency (part speed designation). Also, MII signals use TTL signal levels compatible with devices operating at either 5.0 or 3.3 V.

15.1 MII and Reduced MII Receive Signal Timing

The receiver functions correctly up to a MII_RX_CLK maximum frequency of 25 MHz + 1%. The reduced MII (RMII) receiver functions correctly up to a RMII_REFCLK maximum frequency of 50 MHz + 1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_RX_CLK frequency – 1%.

[Table 34](#) provides information on the MII and RMII receive signal timing.

Table 34. MII Receive Signal Timing

Num	Characteristic	Min	Max	Unit
M1	MI1_RXD[3:0], MI1_RX_DV, MI1_RX_ERR to MI1_RX_CLK setup	5	—	ns
M2	MI1_RX_CLK to MI1_RXD[3:0], MI1_RX_DV, MI1_RX_ER hold	5	—	ns
M3	MI1_RX_CLK pulse width high	35%	65%	MI1_RX_CLK period
M4	MI1_RX_CLK pulse width low	35%	65%	MI1_RX_CLK period
M1_RMII	RMII_RXD[1:0], RMII_CRS_DV, RMII_RX_ERR to RMII_REFCLK setup	4	—	ns
M2_RMII	RMII_REFCLK to RMII_RXD[1:0], RMII_CRS_DV, RMII_RX_ERR hold	2	—	ns

Figure 74 shows the MII transmit signal timing diagram.

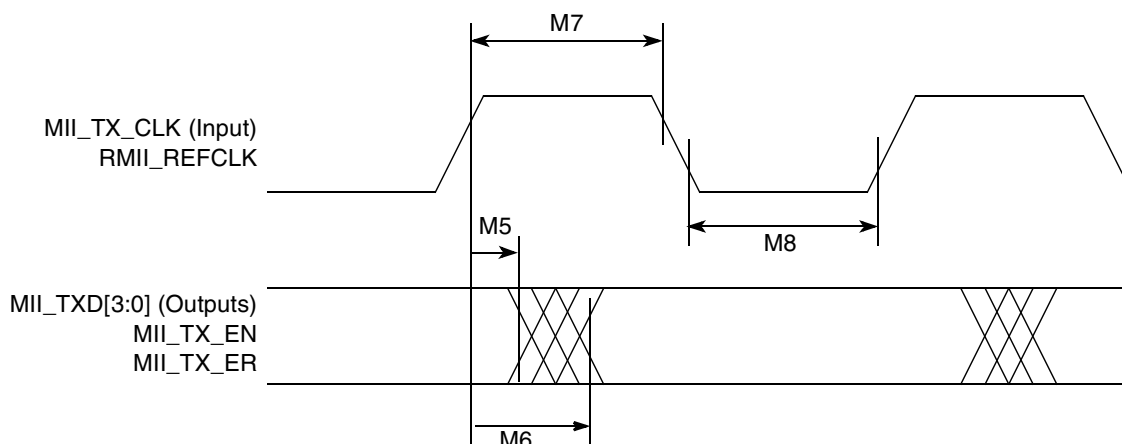


Figure 74. MII Transmit Signal Timing Diagram

15.3 MII Async Inputs Signal Timing (MII_CRSS, MII_COL)

Table 36 provides information on the MII async inputs signal timing.

Table 36. MII Async Inputs Signal Timing

Num	Characteristic	Min	Max	Unit
M9	MII_CRSS, MII_COL minimum pulse width	1.5	—	MII_TX_CLK period

Figure 75 shows the MII asynchronous inputs signal timing diagram.

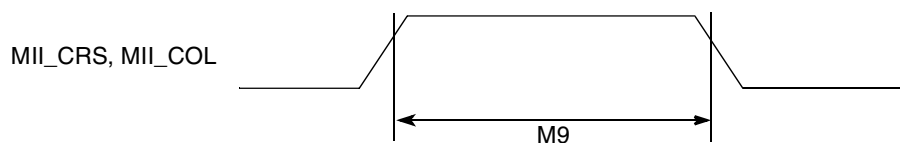


Figure 75. MII Async Inputs Timing Diagram

15.4 MII Serial Management Channel Timing (MII_MDIO, MII_MDC)

Table 37 provides information on the MII serial management channel signal timing. The FEC functions correctly with a maximum MDC frequency in excess of 2.5 MHz.

Table 37. MII Serial Management Channel Timing

Num	Characteristic	Min	Max	Unit
M10	MII_MDC falling edge to MII_MDIO output invalid (minimum propagation delay)	0	—	ns
M11	MII_MDC falling edge to MII_MDIO output valid (max prop delay)	—	25	ns
M12	MII_MDIO (input) to MII_MDC rising edge setup	10	—	ns
M13	MII_MDIO (input) to MII_MDC rising edge hold	0	—	ns

Table 39. Pin Assignments (continued)

Name	Pin Number	Type
PA4, $\overline{\text{CTS4}}$, MII1-TXD1, RMII1-TXD1	U4	Bidirectional
PA3, MII1-RXER, RMII1-RXER, BRGO3	W2	Bidirectional
PA2, MII1-RXDV, RMII1-CRS_DV, TXD4	T4	Bidirectional
PA1, MII1-RXD0, RMII1-RXD0, BRGO4	U1	Bidirectional
PA0, MII1-RXD1, RMII1-RXD1, $\overline{\text{TOUT4}}$	U3	Bidirectional
PB31, $\overline{\text{SPISEL}}$, MII1-TXCLK, RMII1-REFCLK	V3	Bidirectional (Optional: open-drain)
PB30, SPICLK	P18	Bidirectional (Optional: open-drain)
PB29, SPIMOSI	T19	Bidirectional (Optional: open-drain)
PB28, SPIMISO, BRGO4	V19	Bidirectional (Optional: open-drain)
PB27, I2CSDA, BRGO1	U19	Bidirectional (Optional: open-drain)
PB26, I2CSCL, BRGO2	R17	Bidirectional (Optional: open-drain)
PB25, RXADDR3 ¹ , TXADDR3, SMTXD1	V17	Bidirectional (Optional: open-drain)
PB24, TXADDR3 ¹ , RXADDR3, SMRXD1	U16	Bidirectional (Optional: open-drain)
PB23, TXADDR2 ¹ , RXADDR2, $\overline{\text{SDACK1}}$, SMSYN1	W16	Bidirectional (Optional: open-drain)
PB22, TXADDR4 ¹ , RXADDR4, $\overline{\text{SDACK2}}$, SMSYN2	V15	Bidirectional (Optional: open-drain)
PB21, SMTXD2, TXADDR1 ¹ , BRG01, RXADDR1, PHSEL[1]	U14	Bidirectional (Optional: open-drain)
PB20, SMRXD2, L1CLKOA, TXADDR0 ¹ , RXADDR0, PHSEL[0]	T13	Bidirectional (Optional: open-drain)
PB19, MII1-RXD3, $\overline{\text{RTS4}}$	V13	Bidirectional (Optional: open-drain)
PB18, RXADDR4 ¹ , TXADDR4, $\overline{\text{RTS2}}$, L1ST2	T12	Bidirectional (Optional: open-drain)