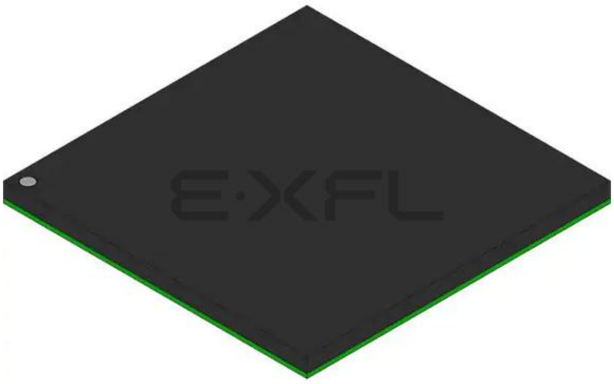

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	66MHz
Co-Processors/DSP	Communications; CPM, Security; SEC
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (3), 10/100Mbps (2)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	Cryptography
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc885zp66

The MPC880 block diagram is shown in Figure 2.

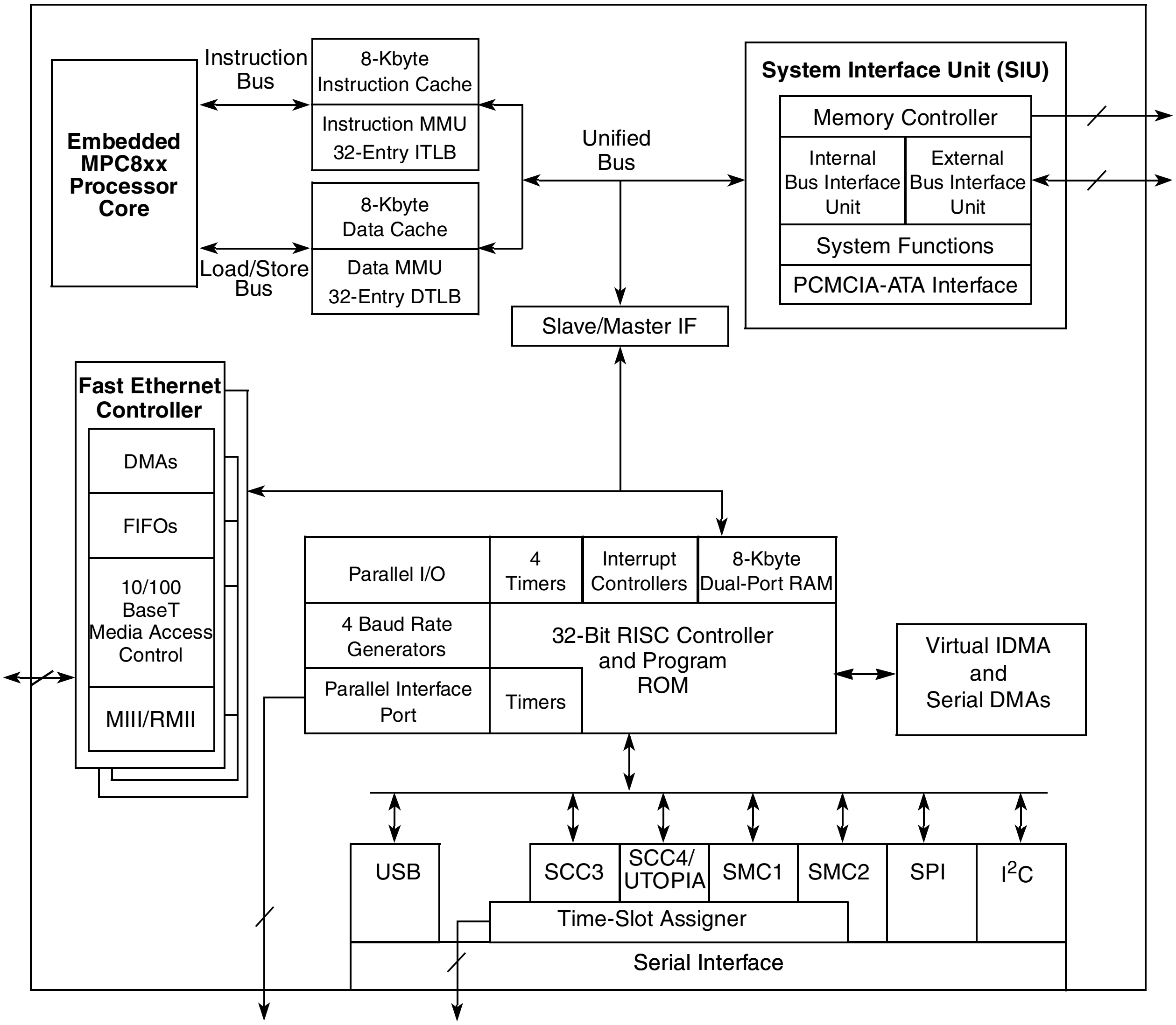

Figure 2. MPC880 Block Diagram

Table 6. DC Electrical Specifications (continued)

Characteristic	Symbol	Min	Max	Unit
Output high voltage, I_{OH} = –2.0 mA, except XTAL and open-drain pins	V_{OH}	2.4	—	V
Output low voltage I_{OL} = 2.0 mA (CLKOUT) I_{OL} = 3.2 mA[5] I_{OL} = 5.3 mA[6] I_{OL} = 7.0 mA (TXD1/PA14, TXD2/PA12) I_{OL} = 8.9 mA ($\overline{\text{TS}}$, $\overline{\text{TA}}$, $\overline{\text{TEA}}$, $\overline{\text{BI}}$, $\overline{\text{BB}}$, $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$)	V_{OL}	—	0.5	V

1 The difference between V_{DDL} and V_{DDSYN} cannot be more than 100 mV.

2 The signals PA[0:15], PB[14:31], PC[4:15], PD[3:15], PE(14:31), TDI, TDO, TCK, $\overline{\text{TRST}}$, TMS, MII1_TXEN, MII_MDIO are 5-V tolerant. The minimum voltage is still 2.0 V.

3 V_{IL}(max) for the I^2C interface is 0.8 V rather than the 1.5 V as specified in the I^2C standard.

4 Input capacitance is periodically sampled.

5 A(0:31), TSIZ0/$\overline{\text{REG}}$, TSIZ1, D(0:31), $\overline{\text{IRQ}}$(2:4), $\overline{\text{IRQ6}}$, RD/$\overline{\text{WR}}$, $\overline{\text{BURST}}$, IP_B(3:7), PA(0:11), PA13, PA15, PB(14:31), PC(4:15), PD(3:15), PE(14:31), MII1_CRS, MII_MDIO, MII1_TXEN, and MII1_COL.

6 $\overline{\text{BDIP}}$/$\overline{\text{GPL\_B}}$(5), $\overline{\text{BR}}$, $\overline{\text{BG}}$, FRZ/$\overline{\text{IRQ6}}$, $\overline{\text{CS}}$(0:7), $\overline{\text{WE}}$(0:3), $\overline{\text{BS\_A}}$(0:3), $\overline{\text{GPL\_A0}}$/$\overline{\text{GPL\_B0}}$, $\overline{\text{OE}}$/$\overline{\text{GPL\_A1}}$/$\overline{\text{GPL\_B1}}$, $\overline{\text{GPL\_A}}$(2:3)/$\overline{\text{GPL\_B}}$(2:3)/$\overline{\text{CS}}$(2:3), UPWAITA/$\overline{\text{GPL\_A4}}$, UPWAITB/$\overline{\text{GPL\_B4}}$, $\overline{\text{GPL\_A5}}$, ALE_A, $\overline{\text{CE1}}$_A, $\overline{\text{CE2}}$_A, OP(0:3), and BADDR(28:30).

7 Thermal Calculation and Measurement

For the following discussions, $P_D = (V_{DDL} \times I_{DDL})$ + PI/O, where PI/O is the power dissipation of the I/O drivers.

NOTE

The V_{DDSYN} power dissipation is negligible.

7.1 Estimation with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, in °C can be obtained from the following equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_A = ambient temperature (ºC)

$R_{\theta JA}$ = package junction-to-ambient thermal resistance (ºC/W)

P_D = power dissipation in package

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. However, the answer is only an estimate; test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

Table 7. Frequency Ranges for Standard Part Frequencies (1:1 Bus Mode)

Part Frequency	66 MHz		80 MHz	
	Min	Max	Min	Max
Core frequency	40	66.67	40	80
Bus frequency	40	66.67	40	80

Table 8. Frequency Ranges for Standard Part Frequencies (2:1 Bus Mode)

Part Frequency	66 MHz		80 MHz		133 MHz	
	Min	Max	Min	Max	Min	Max
Core frequency	40	66.67	40	80	40	133
Bus frequency	20	33.33	20	40	20	66

Table 9 provides the timings for the MPC885/MPC880 at 33-, 40-, 66-, and 80-MHz bus operation.

The timing for the MPC885/MPC880 bus shown assumes a 50-pF load for maximum delays and a 0-pF load for minimum delays. CLKOUT assumes a 100-pF load for maximum delays and a 50-pF load for minimum delays.

Table 9. Bus Operation Timings

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B1	Bus period (CLKOUT), see Table 7	—	—	—	—	—	—	—	—	ns
B1a	EXTCLK to CLKOUT phase skew - If CLKOUT is an integer multiple of EXTCLK, then the rising edge of EXTCLK is aligned with the rising edge of CLKOUT. For a non-integer multiple of EXTCLK, this synchronization is lost, and the rising edges of EXTCLK and CLKOUT have a continuously varying phase skew.	–2	+2	–2	+2	–2	+2	–2	+2	ns
B1b	CLKOUT frequency jitter peak-to-peak	—	1	—	1	—	1	—	1	ns
B1c	Frequency jitter on EXTCLK	—	0.50	—	0.50	—	0.50	—	0.50	%
B1d	CLKOUT phase jitter peak-to-peak for OSCLK ≥ 15 MHz	—	4	—	4	—	4	—	4	ns
	CLKOUT phase jitter peak-to-peak for OSCLK < 15 MHz	—	5	—	5	—	5	—	5	ns
B2	CLKOUT pulse width low (MIN = 0.4 × B1, MAX = 0.6 × B1)	12.1	18.2	10.0	15.0	6.1	9.1	5.0	7.5	ns
B3	CLKOUT pulse width high (MIN = 0.4 × B1, MAX = 0.6 × B1)	12.1	18.2	10.0	15.0	6.1	9.1	5.0	7.5	ns
B4	CLKOUT rise time	—	4.00	—	4.00	—	4.00	—	4.00	ns

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B5	CLKOUT fall time	—	4.00	—	4.00	—	4.00	—	4.00	ns
B7	CLKOUT to A(0:31), BADDR(28:30), RD/WR, BURST, D(0:31) output hold (MIN = 0.25 × B1)	7.60	—	6.30	—	3.80	—	3.13	—	ns
B7a	CLKOUT to TSIZ(0:1), REG, RSV, BDIP, PTR output hold (MIN = 0.25 × B1)	7.60	—	6.30	—	3.80	—	3.13	—	ns
B7b	CLKOUT to BR, BG, FRZ, VFLS(0:1), VF(0:2) IWP(0:2), LWP(0:1), STS output hold (MIN = 0.25 × B1)	7.60	—	6.30	—	3.80	—	3.13	—	ns
B8	CLKOUT to A(0:31), BADDR(28:30) RD/WR, BURST, D(0:31) valid (MAX = 0.25 × B1 + 6.3)	—	13.80	—	12.50	—	10.00	—	9.43	ns
B8a	CLKOUT to TSIZ(0:1), REG, RSV, AT(0:3) BDIP, PTR valid (MAX = 0.25 × B1 + 6.3)	—	13.80	—	12.50	—	10.00	—	9.43	ns
B8b	CLKOUT to BR, BG, VFLS(0:1), VF(0:2), IWP(0:2), FRZ, LWP(0:1), STS valid [4] (MAX = 0.25 × B1 + 6.3)	—	13.80	—	12.50	—	10.00	—	9.43	ns
B9	CLKOUT to A(0:31), BADDR(28:30), RD/WR, BURST, D(0:31), TSIZ(0:1), REG, RSV, AT(0:3), PTR High-Z (MAX = 0.25 × B1 + 6.3)	7.60	13.80	6.30	12.50	3.80	10.00	3.13	9.43	ns
B11	CLKOUT to TS, BB assertion (MAX = 0.25 × B1 + 6.0)	7.60	13.60	6.30	12.30	3.80	9.80	3.13	9.13	ns
B11a	CLKOUT to TA, BI assertion (when driven by the memory controller or PCMCIA interface) (MAX = 0.00 × B1 + 9.30[1])	2.50	9.30	2.50	9.30	2.50	9.30	2.50	9.30	ns
B12	CLKOUT to TS, BB negation (MAX = 0.25 × B1 + 4.8)	7.60	12.30	6.30	11.00	3.80	8.50	3.13	7.92	ns
B12a	CLKOUT to TA, BI negation (when driven by the memory controller or PCMCIA interface) (MAX = 0.00 × B1 + 9.00)	2.50	9.00	2.50	9.00	2.50	9.00	2.5	9.00	ns
B13	CLKOUT to TS, BB High-Z (MIN = 0.25 × B1)	7.60	21.60	6.30	20.30	3.80	14.00	3.13	12.93	ns
B13a	CLKOUT to TA, BI High-Z (when driven by the memory controller or PCMCIA interface) (MIN = 0.00 × B1 + 2.5)	2.50	15.00	2.50	15.00	2.50	15.00	2.5	15.00	ns
B14	CLKOUT to TEA assertion (MAX = 0.00 × B1 + 9.00)	2.50	9.00	2.50	9.00	2.50	9.00	2.50	9.00	ns
B15	CLKOUT to TEA High-Z (MIN = 0.00 × B1 + 2.50)	2.50	15.00	2.50	15.00	2.50	15.00	2.50	15.00	ns
B16	TA, BI valid to CLKOUT (setup time) (MIN = 0.00 × B1 + 6.00)	6.00	—	6.00	—	6.00	—	6	—	ns
B16a	TEA, KR, RETRY, CR valid to CLKOUT (setup time) (MIN = 0.00 × B1 + 4.5)	4.50	—	4.50	—	4.50	—	4.50	—	ns

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B16b	$\overline{\text{BB}}$, $\overline{\text{BG}}$, $\overline{\text{BR}}$, valid to CLKOUT (setup time)[2] (4MIN = 0.00 × B1 + 0.00)	4.00	—	4.00	—	4.00	—	4.00	—	ns
B17	CLKOUT to $\overline{\text{TA}}$, $\overline{\text{TEA}}$, $\overline{\text{BI}}$, $\overline{\text{BB}}$, $\overline{\text{BG}}$, $\overline{\text{BR}}$ valid (hold time) (MIN = 0.00 × B1 + 1.00[3])	1.00	—	1.00	—	2.00	—	2.00	—	ns
B17a	CLKOUT to $\overline{\text{KR}}$, $\overline{\text{RETRY}}$, $\overline{\text{CR}}$ valid (hold time) (MIN = 0.00 × B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B18	D(0:31) valid to CLKOUT rising edge (setup time)[4] (MIN = 0.00 × B1 + 6.00)	6.00	—	6.00	—	6.00	—	6.00	—	ns
B19	CLKOUT rising edge to D(0:31) valid (hold time)[4] (MIN = 0.00 × B1 + 1.00[5])	1.00	—	1.00	—	2.00	—	2.00	—	ns
B20	D(0:31) valid to CLKOUT falling edge (setup time)[6] (MIN = 0.00 × B1 + 4.00)	4.00	—	4.00	—	4.00	—	4.00	—	ns
B21	CLKOUT falling edge to D(0:31) valid (hold time)[6] (MIN = 0.00 × B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B22	CLKOUT rising edge to $\overline{\text{CS}}$ asserted GPCM ACS = 00 (MAX = 0.25 × B1 + 6.3)	7.60	13.80	6.30	12.50	3.80	10.00	3.13	9.43	ns
B22a	CLKOUT falling edge to $\overline{\text{CS}}$ asserted GPCM ACS = 10, TRLX = [0 or 1] (MAX = 0.00 × B1 + 8.00)	—	8.00	—	8.00	—	8.00	—	8.00	ns
B22b	CLKOUT falling edge to $\overline{\text{CS}}$ asserted GPCM ACS = 11, TRLX = [0 or 1], EBDF = 0 (MAX = 0.25 × B1 + 6.3)	7.60	13.80	6.30	12.50	3.80	10.00	3.13	9.43	ns
B22c	CLKOUT falling edge to $\overline{\text{CS}}$ asserted GPCM ACS = 11, TRLX = [0 or 1], EBDF = 1 (MAX = 0.375 × B1 + 6.6)	10.90	18.00	10.90	16.00	5.20	12.30	4.69	10.93	ns
B23	CLKOUT rising edge to $\overline{\text{CS}}$ negated GPCM read access, GPCM write access ACS = 00 and CSNT = 0 (MAX = 0.00 × B1 + 8.00)	2.00	8.00	2.00	8.00	2.00	8.00	2.00	8.00	ns
B24	A(0:31) and BADDR(28:30) to $\overline{\text{CS}}$ asserted GPCM ACS = 10, TRLX = 0 (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	1.80	—	1.13	—	ns
B24a	A(0:31) and BADDR(28:30) to $\overline{\text{CS}}$ asserted GPCM ACS = 11 TRLX = 0 (MIN = 0.50 × B1 – 2.00)	13.20	—	10.50	—	5.60	—	4.25	—	ns
B25	CLKOUT rising edge to $\overline{\text{OE}}$, $\overline{\text{WE}}$(0:3) asserted (MAX = 0.00 × B1 + 9.00)	—	9.00	—	9.00	—	9.00	—	9.00	ns
B26	CLKOUT rising edge to $\overline{\text{OE}}$ negated (MAX = 0.00 × B1 + 9.00)	2.00	9.00	2.00	9.00	2.00	9.00	2.00	9.00	ns
B27	A(0:31) and BADDR(28:30) to $\overline{\text{CS}}$ asserted GPCM ACS = 10, TRLX = 1 (MIN = 1.25 × B1 – 2.00)	35.90	—	29.30	—	16.90	—	13.60	—	ns

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B27a	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 1 (MIN = 1.50 × B1 – 2.00)	43.50	—	35.50	—	20.70	—	16.75	—	ns
B28	CLKOUT rising edge to $\overline{WE}$(0:3) negated GPCM write access CSNT = 0 (MAX = 0.00 × B1 + 9.00)	—	9.00	—	9.00	—	9.00	—	9.00	ns
B28a	CLKOUT falling edge to $\overline{WE}$(0:3) negated GPCM write access TRLX = 0, CSNT = 1, EBDF = 0 (MAX = 0.25 × B1 + 6.80)	7.60	14.30	6.30	13.00	3.80	10.50	3.13	9.93	ns
B28b	CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0, CSNT = 1 ACS = 10 or ACS = 11, EBDF = 0 (MAX = 0.25 × B1 + 6.80)	—	14.30	—	13.00	—	10.50	—	9.93	ns
B28c	CLKOUT falling edge to $\overline{WE}$(0:3) negated GPCM write access TRLX = 0, CSNT = 1 write access TRLX = 0, CSNT = 1, EBDF = 1 (MAX = 0.375 × B1 + 6.6)	10.90	18.00	10.90	18.00	5.20	12.30	4.69	11.29	ns
B28d	CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1 (MAX = 0.375 × B1 + 6.6)	—	18.00	—	18.00	—	12.30	—	11.30	ns
B29	$\overline{WE}$(0:3) negated to D(0:31) High-Z GPCM write access, CSNT = 0, EBDF = 0 (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	1.80	—	1.13	—	ns
B29a	$\overline{WE}$(0:3) negated to D(0:31) High-Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 0 (MIN = 0.50 × B1 – 2.00)	13.20	—	10.50	—	5.60	—	4.25	—	ns
B29b	$\overline{CS}$ negated to D(0:31) High-Z GPCM write access, ACS = 00, TRLX = 0 & CSNT = 0 (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	1.80	—	1.13	—	ns
B29c	$\overline{CS}$ negated to D(0:31) High-Z GPCM write access, TRLX = 0, CSNT = 1, ACS = 10, or ACS = 11 EBDF = 0 (MIN = 0.50 × B1 – 2.00)	13.20	—	10.50	—	5.60	—	4.25	—	ns
B29d	$\overline{WE}$(0:3) negated to D(0:31) High-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 0 (MIN = 1.50 × B1 – 2.00)	43.50	—	35.50	—	20.70	—	16.75	—	ns
B29e	$\overline{CS}$ negated to D(0:31) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11 EBDF = 0 (MIN = 1.50 × B1 – 2.00)	43.50	—	35.50	—	20.70	—	16.75	—	ns
B29f	$\overline{WE}$(0:3) negated to D(0:31) High-Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 1 (MIN = 0.375 × B1 – 6.30)[7]	5.00	—	3.00	—	0.00	—	0.00	—	ns
B29g	$\overline{CS}$ negated to D(0:31) High-Z GPCM write access, TRLX = 0, CSNT = 1 ACS = 10 or ACS = 11, EBDF = 1 (MIN = 0.375 × B1 – 6.30)[7]	5.00	—	3.00	—	0.00	—	0.00	—	ns

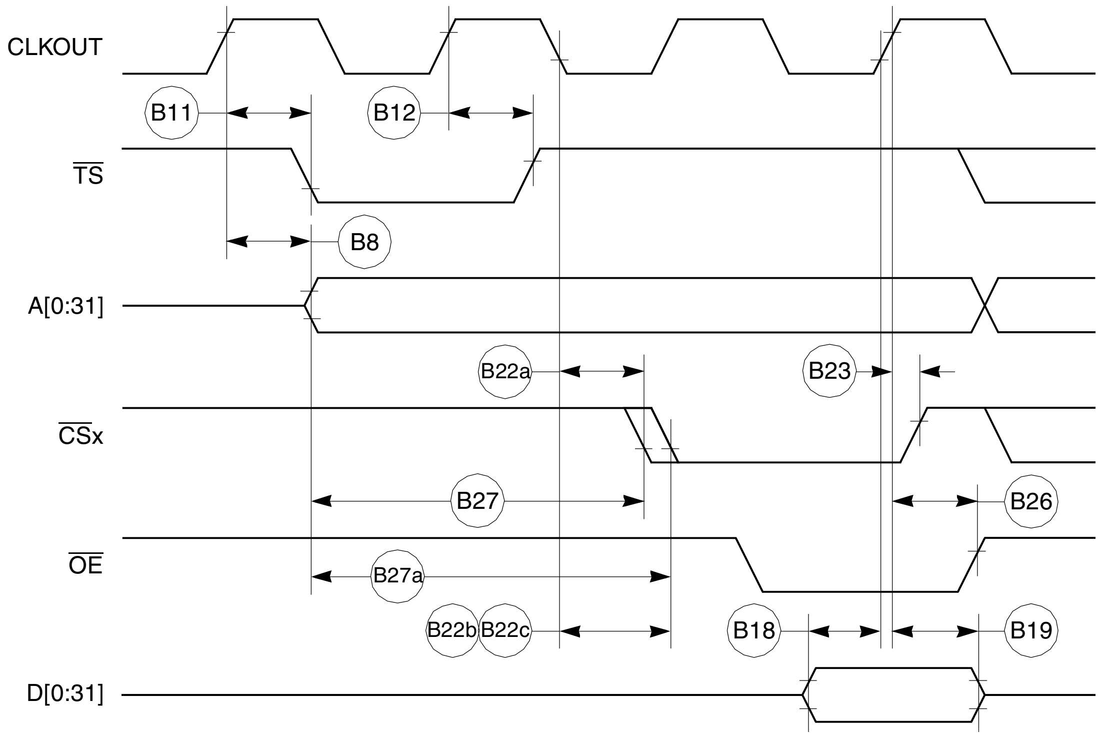

Figure 16. External Bus Read Timing (GPCM Controlled—TRLX = 1, ACS = 10, ACS = 11)

Table 12 shows the PCMCIA port timing for the MPC885/MPC880.

Table 12. PCMCIA Port Timing

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
P57	CLKOUT to OPx valid (MAX = 0.00 × B1 + 19.00)	—	19.00	—	19.00	—	19.00	—	19.00	ns
P58	$\overline{\text{HRESET}}$ negated to OPx drive[1] (MIN = 0.75 × B1 + 3.00)	25.70	—	21.70	—	14.40	—	12.40	—	ns
P59	IP_Xx valid to CLKOUT rising edge (MIN = 0.00 × B1 + 5.00)	5.00	—	5.00	—	5.00	—	5.00	—	ns
P60	CLKOUT rising edge to IP_Xx invalid (MIN = 0.00 × B1 + 1.00)	1.00	—	1.00	—	1.00	—	1.00	—	ns

[1] OP2 and OP3 only.

Figure 31 provides the PCMCIA output port timing for the MPC885/MPC880.

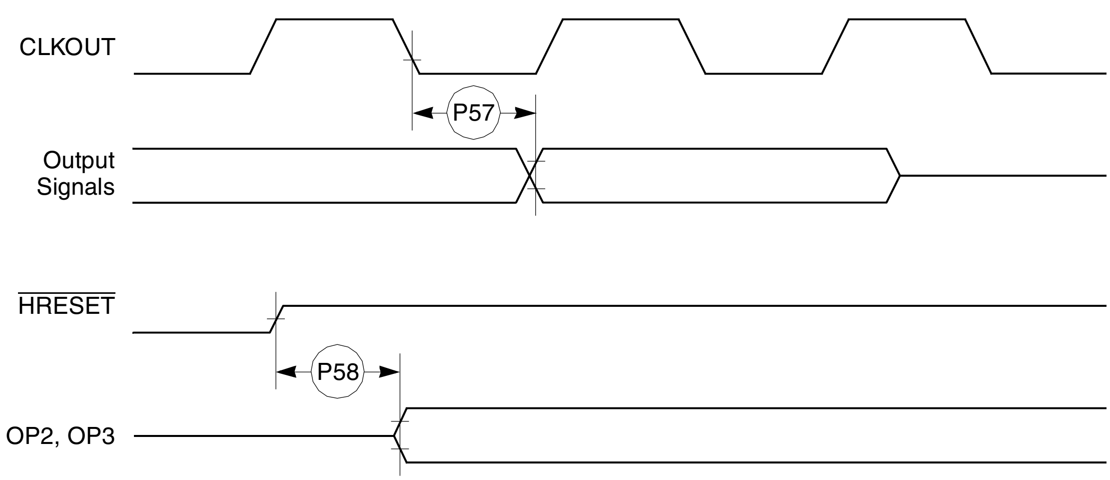

Figure 31. PCMCIA Output Port Timing

Figure 32 provides the PCMCIA input port timing for the MPC885/MPC880.

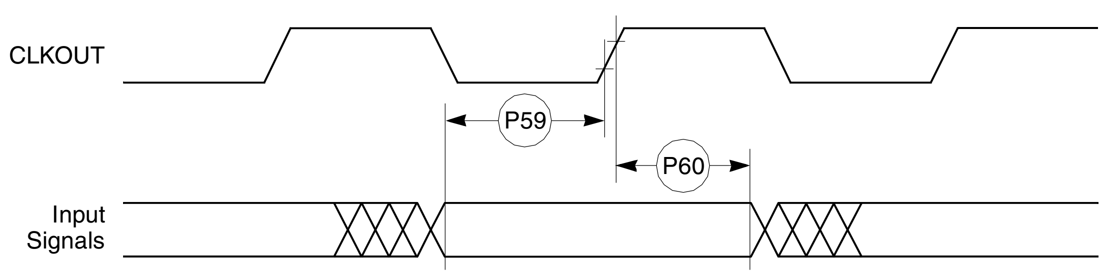

Figure 32. PCMCIA Input Port Timing

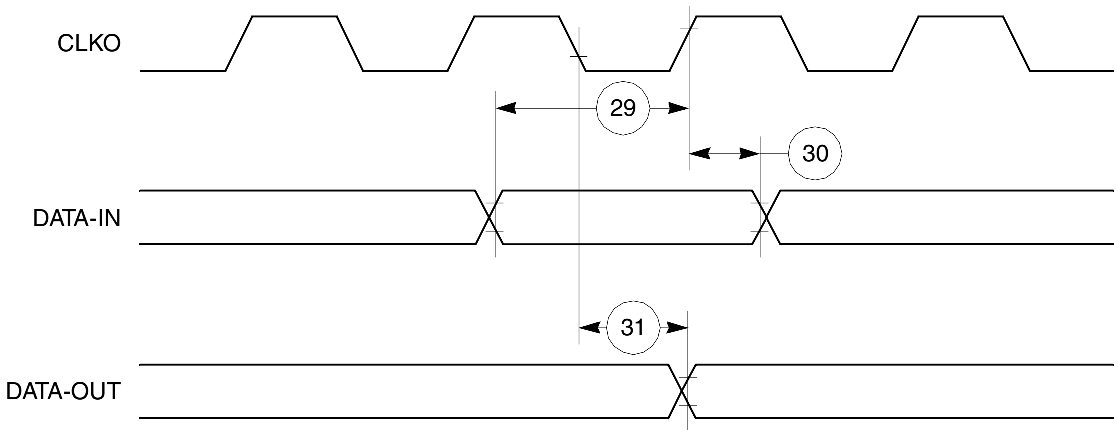

Figure 46. Parallel I/O Data-In/Data-Out Timing Diagram

12.2 Port C Interrupt AC Electrical Specifications

Table 17 provides the timings for port C interrupts.

Table 17. Port C Interrupt Timing

Num	Characteristic	33.34 MHz		Unit
		Min	Max	
35	Port C interrupt pulse width low (edge-triggered mode)	55	—	ns
36	Port C interrupt minimum time between active edges	55	—	ns

Figure 47 shows the port C interrupt detection timing.

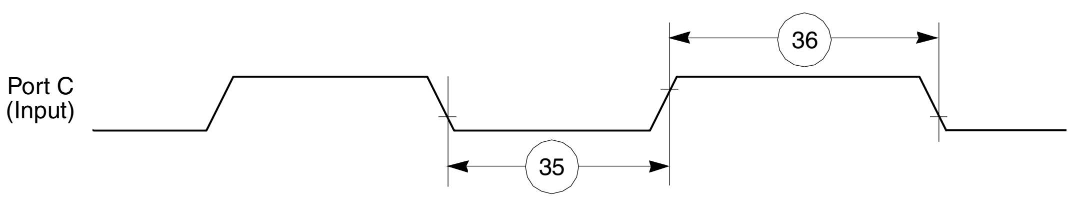

Figure 47. Port C Interrupt Detection Timing

12.3 IDMA Controller AC Electrical Specifications

Table 18 provides the IDMA controller timings as shown in Figure 48 tthrough Figure 51.

Table 18. IDMA Controller Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
40	$\overline{\text{DREQ}}$ setup time to clock high	7	—	ns
41	$\overline{\text{DREQ}}$ hold time from clock high [1]	TBD	—	ns
42	$\overline{\text{SDACK}}$ assertion delay from clock high	—	12	ns
43	$\overline{\text{SDACK}}$ negation delay from clock low	—	12	ns
44	$\overline{\text{SDACK}}$ negation delay from $\overline{\text{TA}}$ low	—	20	ns
45	$\overline{\text{SDACK}}$ negation delay from clock high	—	15	ns
46	$\overline{\text{TA}}$ assertion to rising edge of the clock setup time (applies to external $\overline{\text{TA}}$)	7	—	ns

[1] Applies to high-to-low mode (EDM = 1).

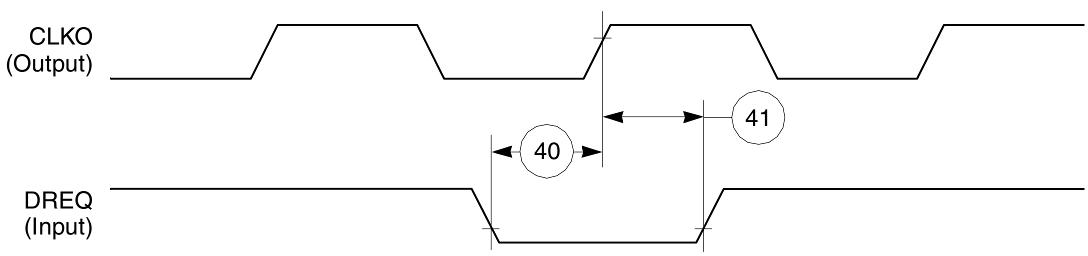

Figure 48. IDMA External Requests Timing Diagram

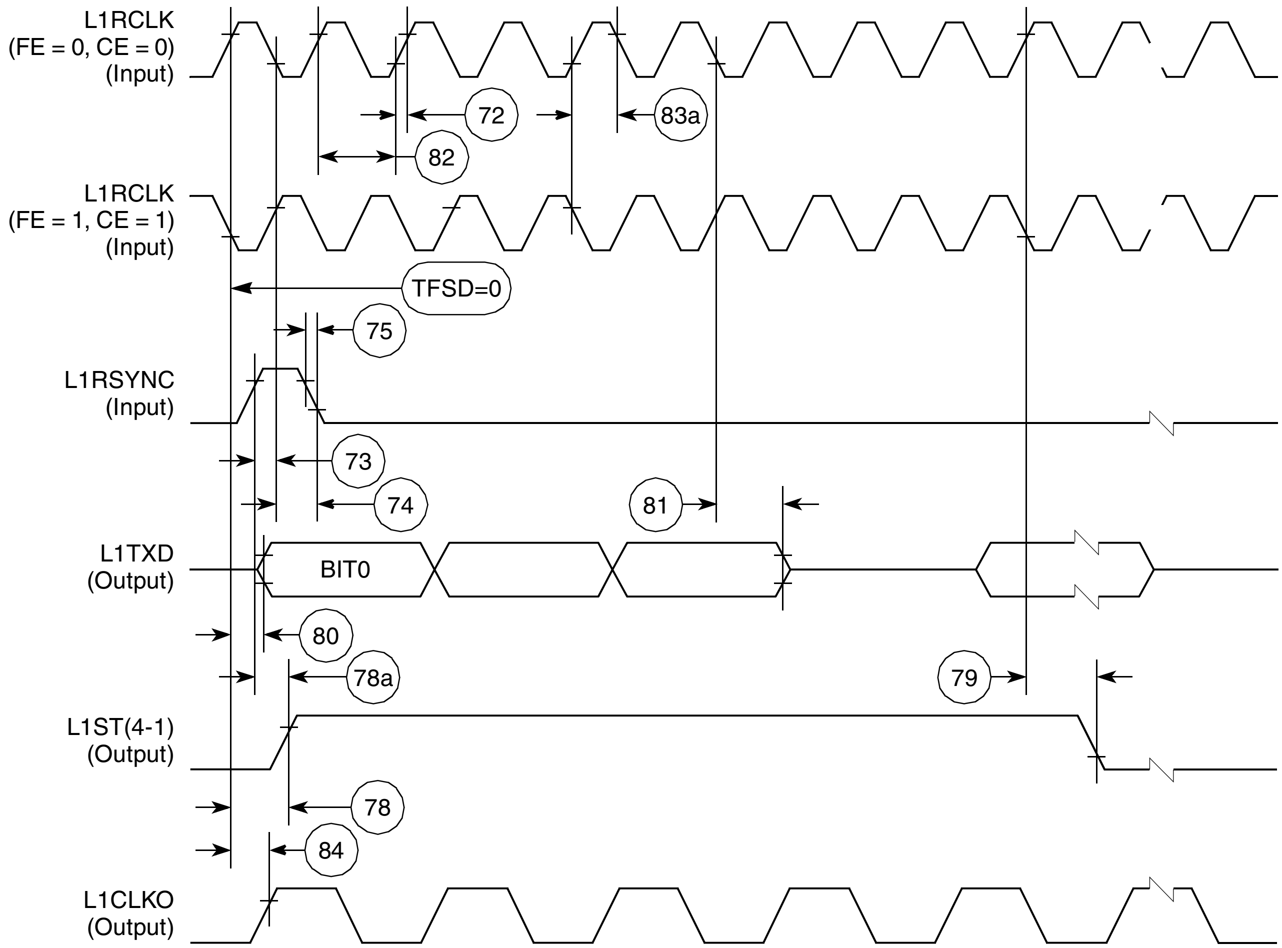

Figure 57. SI Transmit Timing with Double Speed Clocking (DSC = 1)

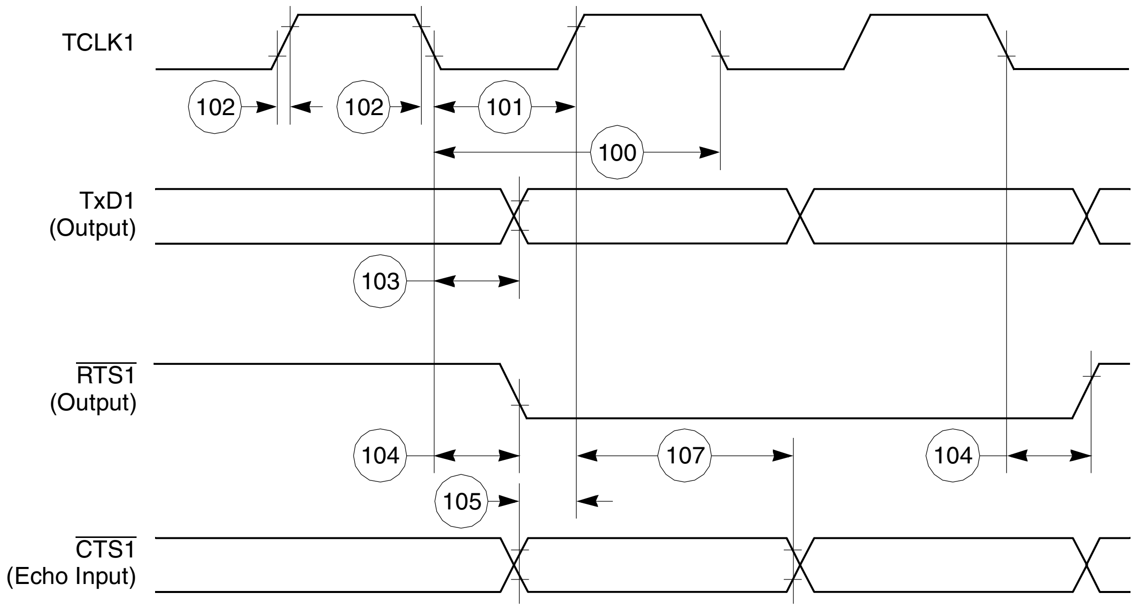

Figure 61. HDLC Bus Timing Diagram

12.8 Ethernet Electrical Specifications

Table 24 provides the Ethernet timings as shown in Figure 62 through Figure 64.

Table 24. Ethernet Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
120	CLSN width high	40	—	ns
121	RCLK1 rise/fall time	—	15	ns
122	RCLK1 width low	40	—	ns
123	RCLK1 clock period[1]	80	120	ns
124	RXD1 setup time	20	—	ns
125	RXD1 hold time	5	—	ns
126	RENA active delay (from RCLK1 rising edge of the last data bit)	10	—	ns
127	RENA width low	100	—	ns
128	TCLK1 rise/fall time	—	15	ns
129	TCLK1 width low	40	—	ns
130	TCLK1 clock period[1]	99	101	ns
131	TXD1 active delay (from TCLK1 rising edge)	—	50	ns
132	TXD1 inactive delay (from TCLK1 rising edge)	6.5	50	ns
133	TENA active delay (from TCLK1 rising edge)	10	50	ns

Table 24. Ethernet Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
134	TENA inactive delay (from TCLK1 rising edge)	10	50	ns
138	CLKO1 low to $\overline{\text{SDACK}}$ asserted[2]	—	20	ns
139	CLKO1 low to $\overline{\text{SDACK}}$ negated [2]	—	20	ns

[1] The ratios SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater than or equal to 2/1.

[2] $\overline{\text{SDACK}}$ is asserted whenever the SDMA writes the incoming frame DA into memory.

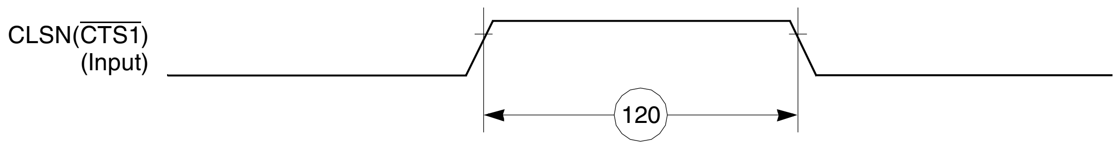

Figure 62. Ethernet Collision Timing Diagram

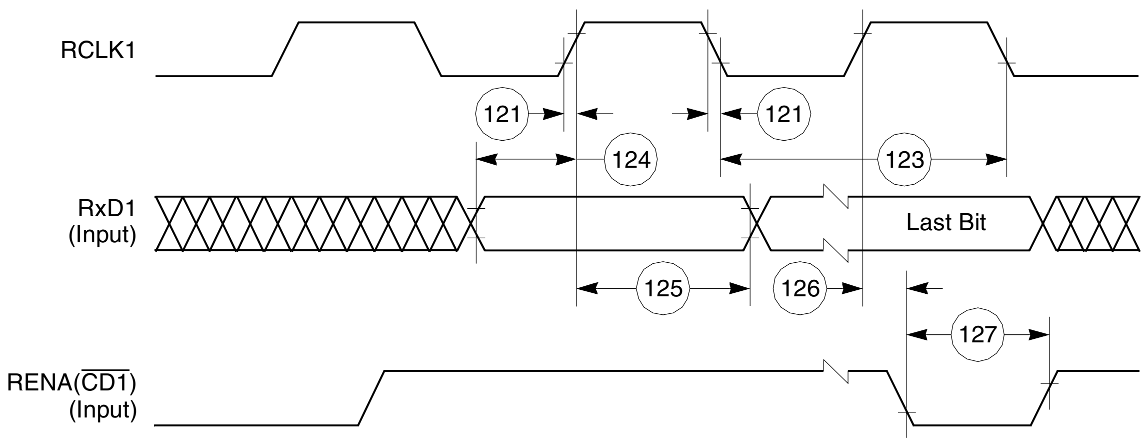

Figure 63. Ethernet Receive Timing Diagram

Table 28. I²C Timing (SCL < 100 kHz) (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
210	SDL/SCL fall time	—	300	ns
211	Stop condition setup time	4.7	—	µs

1 SCL frequency is given by SCL = BRGCLK_frequency/((BRG register + 3) × pre_scaler × 2).
The ratio SyncClk/(BRGCLK/pre_scaler) must be greater or equal to 4/1.

Table 29 provides the I²C (SCL > 100 kHz) timings.

Table 29. I²C Timing (SCL > 100 kHz)

Num	Characteristic	Expression	All Frequencies		Unit
			Min	Max	
200	SCL clock frequency (slave)	fSCL	0	BRGCLK/48	Hz
200	SCL clock frequency (master)[1]	fSCL	BRGCLK/16512	BRGCLK/48	Hz
202	Bus free time between transmissions	—	1/(2.2 × fSCL)	—	s
203	Low period of SCL	—	1/(2.2 × fSCL)	—	s
204	High period of SCL	—	1/(2.2 × fSCL)	—	s
205	Start condition setup time	—	1/(2.2 × fSCL)	—	s
206	Start condition hold time	—	1/(2.2 × fSCL)	—	s
207	Data hold time	—	0	—	s
208	Data setup time	—	1/(40 × fSCL)	—	s
209	SDL/SCL rise time	—	—	1/(10 × fSCL)	s
210	SDL/SCL fall time	—	—	1/(33 × fSCL)	s
211	Stop condition setup time	—	1/2(2.2 × fSCL)	—	s

1 SCL frequency is given by SCL = BrgClk_frequency/((BRG register + 3) × pre_scaler × 2).
The ratio SyncClk/(Brg_Clk/pre_scaler) must be greater or equal to 4/1.

Figure 70 shows the I²C bus timing.

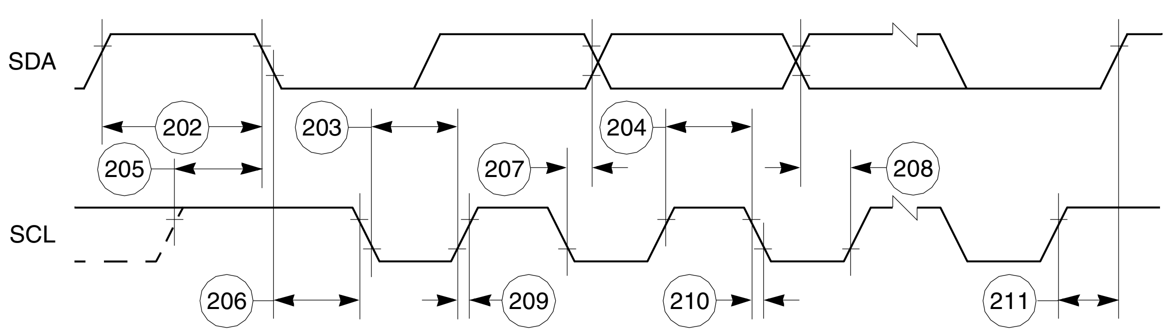

Figure 70. I²C Bus Timing Diagram

Figure 73 shows MII receive signal timing.

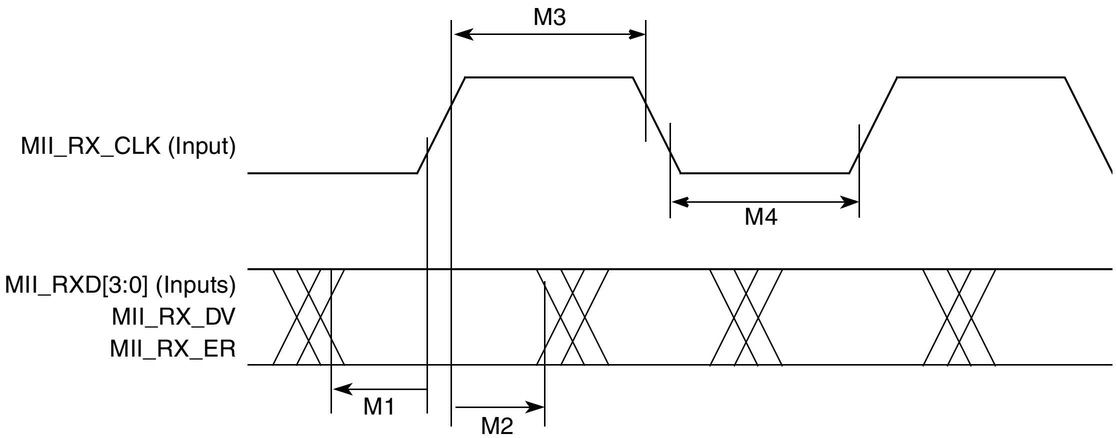

Figure 73. MII Receive Signal Timing Diagram

15.2 MII and Reduced MII Transmit Signal Timing

The transmitter functions correctly up to a MII_TX_CLK maximum frequency of 25 MHz + 1%. The RMII transmitter functions correctly up to a RMII_REFCLK maximum frequency of 50 MHz + 1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_TX_CLK frequency – 1%.

Table 35 provides information on the MII and RMII transmit signal timing.

Table 35. MII Transmit Signal Timing

Num	Characteristic	Min	Max	Unit
M5	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER invalid	5	—	ns
M6	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER valid	—	25	ns
M20_RMII	RMII_TXD[1:0], RMII_TX_EN to RMII_REFCLK setup	4	—	ns
M21_RMII	RMII_TXD[1:0], RMII_TX_EN data hold from RMII_REFCLK rising edge	2	—	ns
M7	MII_TX_CLK and RMII_REFCLK pulse width high	35%	65%	MII_TX_CLK or RMII_REFCLK period
M8	MII_TX_CLK and RMII_REFCLK pulse width low	35%	65%	MII_TX_CLK or RMII_REFCLK period

Figure 74 shows the MII transmit signal timing diagram.

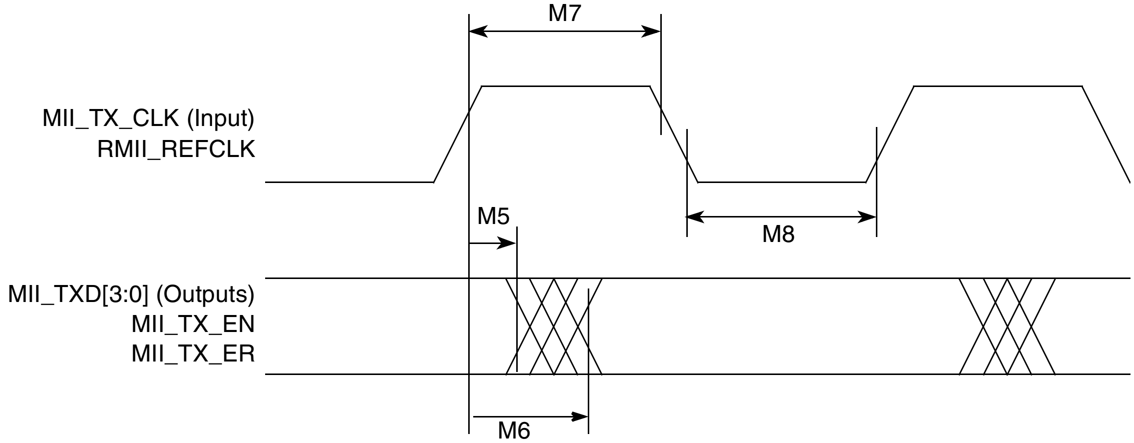

Figure 74. MII Transmit Signal Timing Diagram

15.3 MII Async Inputs Signal Timing (MII_CRS, MII_COL)

Table 36 provides information on the MII async inputs signal timing.

Table 36. MII Async Inputs Signal Timing

Num	Characteristic	Min	Max	Unit
M9	MII_CRS, MII_COL minimum pulse width	1.5	—	MII_TX_CLK period

Figure 75 shows the MII asynchronous inputs signal timing diagram.

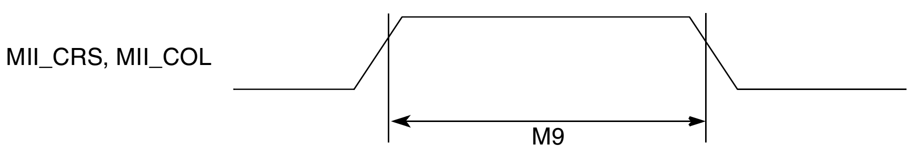

Figure 75. MII Async Inputs Timing Diagram

15.4 MII Serial Management Channel Timing (MII_MDIO, MII_MDC)

Table 37 provides information on the MII serial management channel signal timing. The FEC functions correctly with a maximum MDC frequency in excess of 2.5 MHz.

Table 37. MII Serial Management Channel Timing

Num	Characteristic	Min	Max	Unit
M10	MII_MDC falling edge to MII_MDIO output invalid (minimum propagation delay)	0	—	ns
M11	MII_MDC falling edge to MII_MDIO output valid (max prop delay)	—	25	ns
M12	MII_MDIO (input) to MII_MDC rising edge setup	10	—	ns
M13	MII_MDIO (input) to MII_MDC rising edge hold	0	—	ns

16.1 Pin Assignments

Figure 77 shows the top-view pinout of the PBGA package. For additional information, see the *MPC885 PowerQUICC™ Family Reference Manual*.

NOTE: This is the top view of the device.

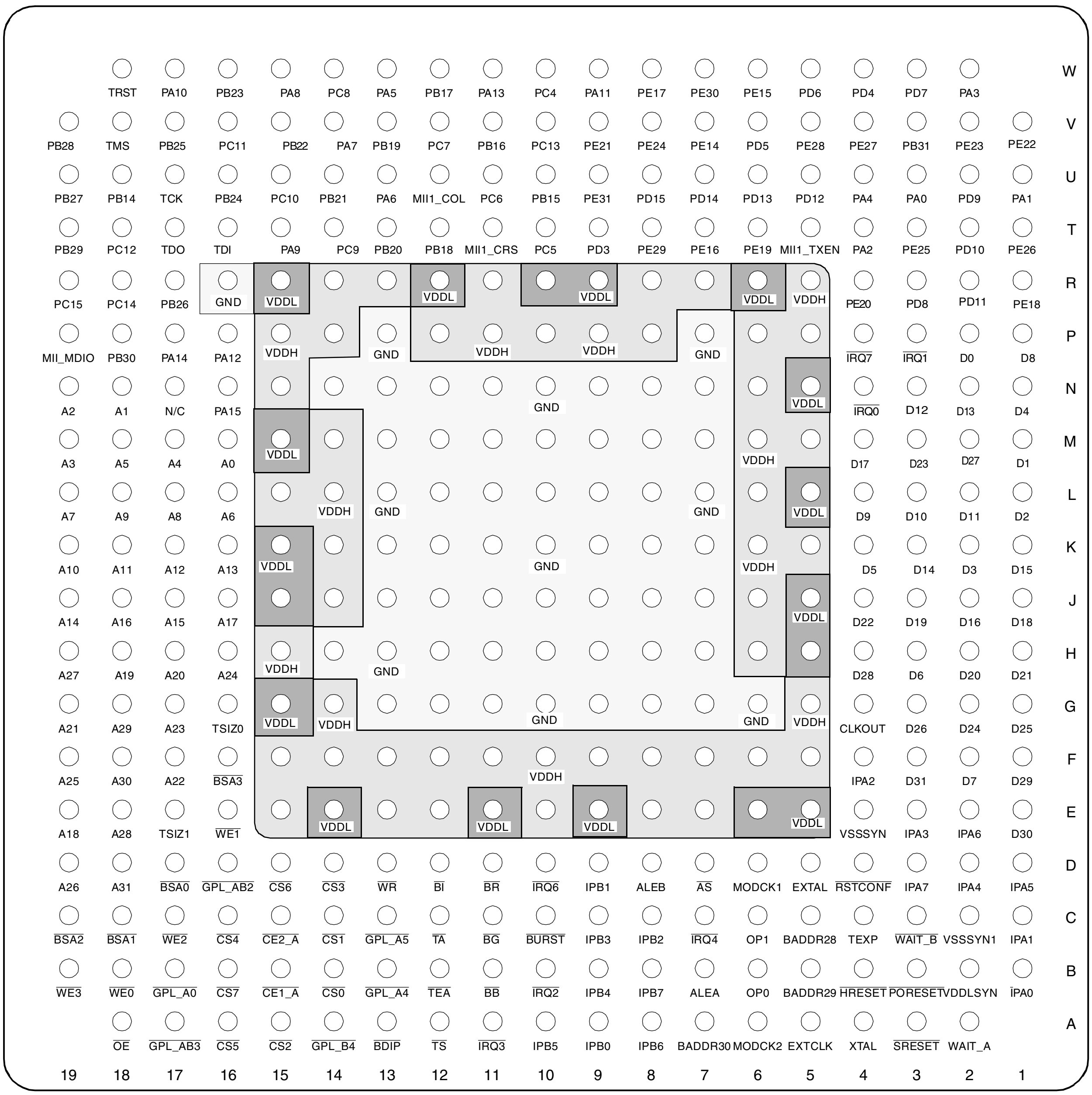

Figure 77. Pinout of the PBGA Package

Table 39 contains a list of the MPC885 input and output signals and shows multiplexing and pin assignments.

Table 39. Pin Assignments

Name	Pin Number	Type
A[0:31]	M16, N18, N19, M19, M17, M18, L16, L19, L17, L18, K19, K18, K17, K16, J19, J17, J18, J16, E19, H18, H17, G19, F17, G17, H16, F19, D19, H19, E18, G18, F18, D18	Bidirectional Three-state
D[0:31]	P2, M1, L1, K2, N1, K4, H3, F2, P1, L4, L3, L2, N3, N2, K3, K1, J2, M4, J1, J3, H2, H1, J4, M3, G2, G1, G3, M2, H4, F1, E1, F3	Bidirectional Three-state
TSIZ0, $\overline{\text{REG}}$	G16	Bidirectional Three-state
TSIZ1	E17	Bidirectional Three-state
RD/$\overline{\text{WR}}$	D13	Bidirectional Three-state
$\overline{\text{BURST}}$	C10	Bidirectional Three-state
$\overline{\text{BDIP}}$, $\overline{\text{GPL\_B5}}$	A13	Output
$\overline{\text{TS}}$	A12	Bidirectional Active pull-up
$\overline{\text{TA}}$	C12	Bidirectional Active pull-up
$\overline{\text{TEA}}$	B12	Open-drain
$\overline{\text{BI}}$	D12	Bidirectional Active pull-up
$\overline{\text{IRQ2}}$, $\overline{\text{RSV}}$	B10	Bidirectional Three-state
$\overline{\text{IRQ4}}$, $\overline{\text{KR}}$, $\overline{\text{RETRY}}$, SPKROUT	C7	Bidirectional Three-state
$\overline{\text{CR}}$, $\overline{\text{IRQ3}}$	A11	Input
$\overline{\text{BR}}$	D11	Bidirectional
$\overline{\text{BG}}$	C11	Bidirectional
$\overline{\text{BB}}$	B11	Bidirectional Active pull-up
FRZ, $\overline{\text{IRQ6}}$	D10	Bidirectional
$\overline{\text{IRQ0}}$	N4	Input
$\overline{\text{IRQ1}}$	P3	Input
$\overline{\text{IRQ7}}$	P4	Input
$\overline{\text{CS}}$[0:5]	B14, C14, A15, D14, C16, A16	Output
$\overline{\text{CS6}}$, $\overline{\text{CE1\_B}}$	D15	Output
$\overline{\text{CS7}}$, $\overline{\text{CE2\_B}}$	B16	Output

Table 39. Pin Assignments (continued)

Name	Pin Number	Type
PA4, $\overline{CTS4}$, MII1-TXD1, RMII1-TXD1	U4	Bidirectional
PA3, MII1-RXER, RMII1-RXER, BRGO3	W2	Bidirectional
PA2, MII1-RXDV, RMII1-CRS_DV, TXD4	T4	Bidirectional
PA1, MII1-RXD0, RMII1-RXD0, BRGO4	U1	Bidirectional
PA0, MII1-RXD1, RMII1-RXD1, $\overline{TOUT4}$	U3	Bidirectional
PB31, $\overline{SPISEL}$, MII1-TXCLK, RMII1-REFCLK	V3	Bidirectional (Optional: open-drain)
PB30, SPICLK	P18	Bidirectional (Optional: open-drain)
PB29, SPIMOSI	T19	Bidirectional (Optional: open-drain)
PB28, SPIMISO, BRGO4	V19	Bidirectional (Optional: open-drain)
PB27, I2CSDA, BRGO1	U19	Bidirectional (Optional: open-drain)
PB26, I2CSCL, BRGO2	R17	Bidirectional (Optional: open-drain)
PB25, RXADDR3[1], TXADDR3, SMTXD1	V17	Bidirectional (Optional: open-drain)
PB24, TXADDR3[1], RXADDR3, SMRXD1	U16	Bidirectional (Optional: open-drain)
PB23, TXADDR2[1], RXADDR2, $\overline{SDACK1}$, $\overline{SMSYN1}$	W16	Bidirectional (Optional: open-drain)
PB22, TXADDR4[1], RXADDR4, $\overline{SDACK2}$, $\overline{SMSYN2}$	V15	Bidirectional (Optional: open-drain)
PB21, SMTXD2, TXADDR1[1], BRG01, RXADDR1, PHSEL[1]	U14	Bidirectional (Optional: open-drain)
PB20, SMRXD2, L1CLKOA, TXADDR0[1], RXADDR0, PHSEL[0]	T13	Bidirectional (Optional: open-drain)
PB19, MII1-RXD3, $\overline{RTS4}$	V13	Bidirectional (Optional: open-drain)
PB18, RXADDR4[1], TXADDR4, $\overline{RTS2}$, L1ST2	T12	Bidirectional (Optional: open-drain)

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