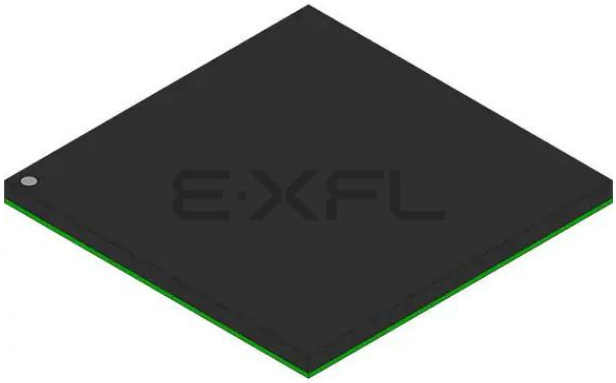

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	80MHz
Co-Processors/DSP	Communications; CPM, Security; SEC
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (3), 10/100Mbps (2)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	Cryptography
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc885zp80

3 Maximum Tolerated Ratings

This section provides the maximum tolerated voltage and temperature ranges for the MPC885/MPC880. Table 2 displays the maximum tolerated ratings, and Table 3 displays the operating temperatures.

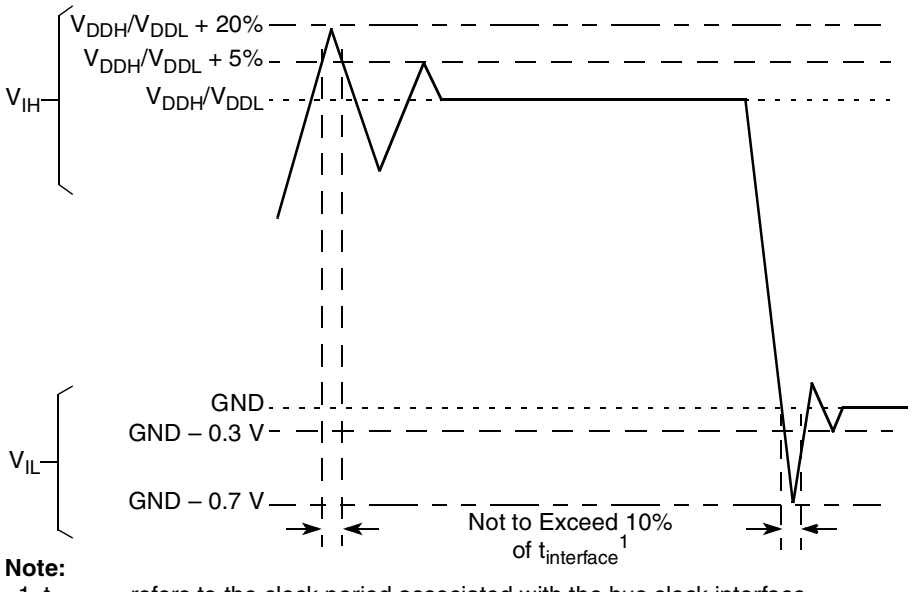
Table 2. Maximum Tolerated Ratings

Rating	Symbol	Value	Unit
Supply voltage[1]	V_{DDH}	–0.3 to 4.0	V
	V_{DDL}	–0.3 to 2.0	V
	VDDSYN	–0.3 to 2.0	V
	Difference between V_{DDL} and V_{DDSYN}	<100	mV
Input voltage[2]	V_{in}	GND – 0.3 to V_{DDH}	V
Storage temperature range	T_{stg}	–55 to +150	°C

1 The power supply of the device must start its ramp from 0.0 V.

2 Functional operating conditions are provided with the DC electrical specifications in Table 6. Absolute maximum ratings are stress ratings only; functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device. See Section 8, “Power Supply and Power Sequencing.”
Caution: All inputs that tolerate 5 V cannot be more than 2.5 V greater than V_{DDH}. This restriction applies to power up and normal operation (that is, if the MPC885/MPC880 is unpowered, a voltage greater than 2.5 V must not be applied to its inputs).

Figure 3 shows the undershoot and overshoot voltages at the interfaces of the MPC885/MPC880.



Note:
1. $t_{interface}$ refers to the clock period associated with the bus clock interface.

Figure 3. Undershoot/Overshoot Voltage for V_{DDH} and V_{DDL}

Table 6. DC Electrical Specifications (continued)

Characteristic	Symbol	Min	Max	Unit
Output high voltage, I_{OH} = –2.0 mA, except XTAL and open-drain pins	V_{OH}	2.4	—	V
Output low voltage I_{OL} = 2.0 mA (CLKOUT) I_{OL} = 3.2 mA[5] I_{OL} = 5.3 mA[6] I_{OL} = 7.0 mA (TXD1/PA14, TXD2/PA12) I_{OL} = 8.9 mA ($\overline{TS}$, $\overline{TA}$, $\overline{TEA}$, $\overline{BI}$, $\overline{BB}$, $\overline{HRESET}$, $\overline{SRESET}$)	V_{OL}	—	0.5	V

1 The difference between V_{DDL} and V_{DDSYN} cannot be more than 100 mV.

2 The signals PA[0:15], PB[14:31], PC[4:15], PD[3:15], PE(14:31), TDI, TDO, TCK, $\overline{TRST}$, TMS, MII1_TXEN, MII_MDIO are 5-V tolerant. The minimum voltage is still 2.0 V.

3 V_{IL}(max) for the I^2C interface is 0.8 V rather than the 1.5 V as specified in the I^2C standard.

4 Input capacitance is periodically sampled.

5 A(0:31), TSIZ0/$\overline{REG}$, TSIZ1, D(0:31), $\overline{IRQ}$(2:4), $\overline{IRQ6}$, RD/$\overline{WR}$, $\overline{BURST}$, IP_B(3:7), PA(0:11), PA13, PA15, PB(14:31), PC(4:15), PD(3:15), PE(14:31), MII1_CRS, MII_MDIO, MII1_TXEN, and MII1_COL.

6 $\overline{BDIP}$/$\overline{GPL\_B}$(5), $\overline{BR}$, $\overline{BG}$, FRZ/$\overline{IRQ6}$, $\overline{CS}$(0:7), $\overline{WE}$(0:3), $\overline{BS}$_A(0:3), $\overline{GPL\_A0}$/$\overline{GPL\_B0}$, $\overline{OE}$/$\overline{GPL\_A1}$/$\overline{GPL\_B1}$, $\overline{GPL\_A}$(2:3)/$\overline{GPL\_B}$(2:3)/$\overline{CS}$(2:3), UPWAITA/$\overline{GPL\_A4}$, UPWAITB/$\overline{GPL\_B4}$, $\overline{GPL\_A5}$, ALE_A, $\overline{CE}$1_A, $\overline{CE}$2_A, OP(0:3), and BADDR(28:30).

7 Thermal Calculation and Measurement

For the following discussions, $P_D = (V_{DDL} \times I_{DDL}) + PI/O$, where PI/O is the power dissipation of the I/O drivers.

NOTE

The V_{DDSYN} power dissipation is negligible.

7.1 Estimation with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, in °C can be obtained from the following equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_A = ambient temperature (ºC)

$R_{\theta JA}$ = package junction-to-ambient thermal resistance (ºC/W)

P_D = power dissipation in package

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. However, the answer is only an estimate; test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

7.6 References

Semiconductor Equipment and Materials International(415) 964-5111
805 East Middlefield Rd
Mountain View, CA 94043

MIL-SPEC and EIA/JESD (JEDEC) specifications800-854-7179 or
(Available from Global Engineering Documents)303-397-7956

JEDEC Specifications http://www.jedec.org

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
2. 2. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

8 Power Supply and Power Sequencing

This section provides design considerations for the MPC885/MPC880 power supply. The MPC885/MPC880 has a core voltage (V_{DDL}) and PLL voltage (V_{DDSYN}), which both operate at a lower voltage than the I/O voltage V_{DDH}. The I/O section of the MPC885/MPC880 is supplied with 3.3 V across V_{DDH} and V_{SS} (GND).

The signals PA[0:15], PB[14:31], PC[4:15], PD[3:15], TDI, TDO, TCK, TRST_B, TMS, MII_TXEN, and MII_MDIO are 5 V tolerant. All inputs cannot be more than 2.5 V greater than V_{DDH}. In addition, 5-V tolerant pins cannot exceed 5.5 V and remaining input pins cannot exceed 3.465 V. This restriction applies to power up/down and normal operation.

One consequence of multiple power supplies is that when power is initially applied the voltage rails ramp up at different rates. The rates depend on the nature of the power supply, the type of load on each power supply, and the manner in which different voltages are derived. The following restrictions apply:

- V_{DDL} must not exceed V_{DDH} during power up and power down.
- V_{DDL} must not exceed 1.9 V, and V_{DDH} must not exceed 3.465 V.

These cautions are necessary for the long-term reliability of the part. If they are violated, the electrostatic discharge (ESD) protection diodes are forward-biased, and excessive current can flow through these diodes. If the system power supply design does not control the voltage sequencing, the circuit shown Figure 5 can be added to meet these requirements. The MUR420 Schottky diodes control the maximum potential difference between the external bus and core power supplies on power up, and the 1N5820 diodes regulate the maximum potential difference on power down.

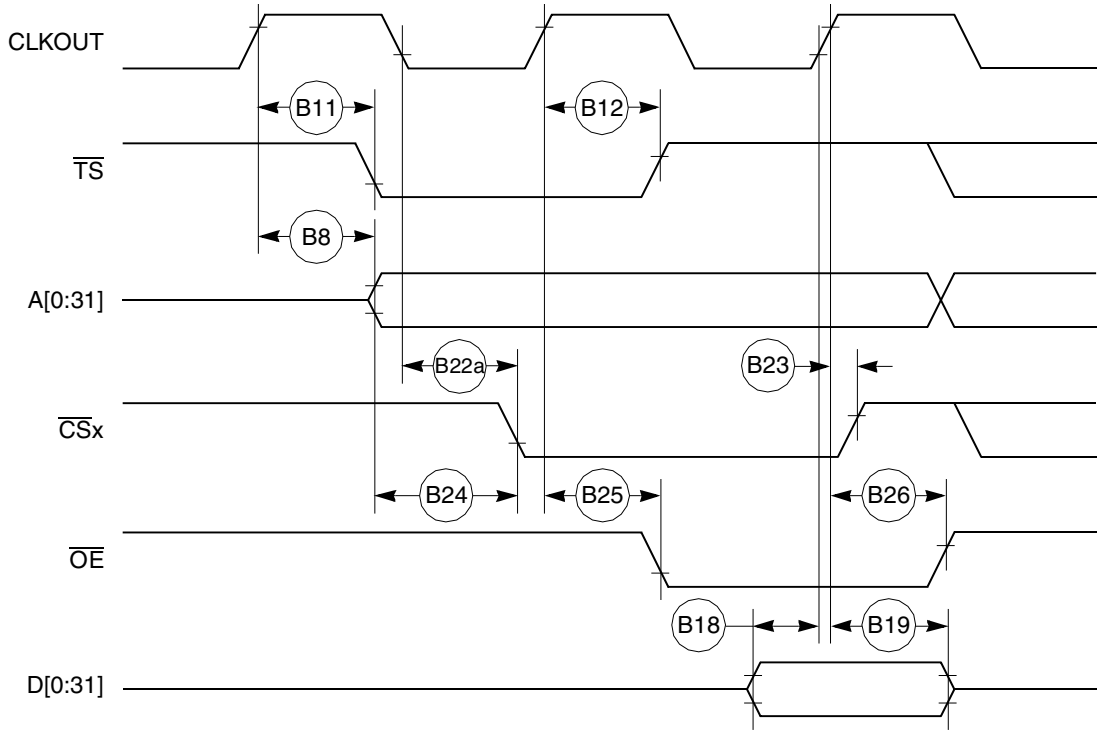


Figure 14. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 10)

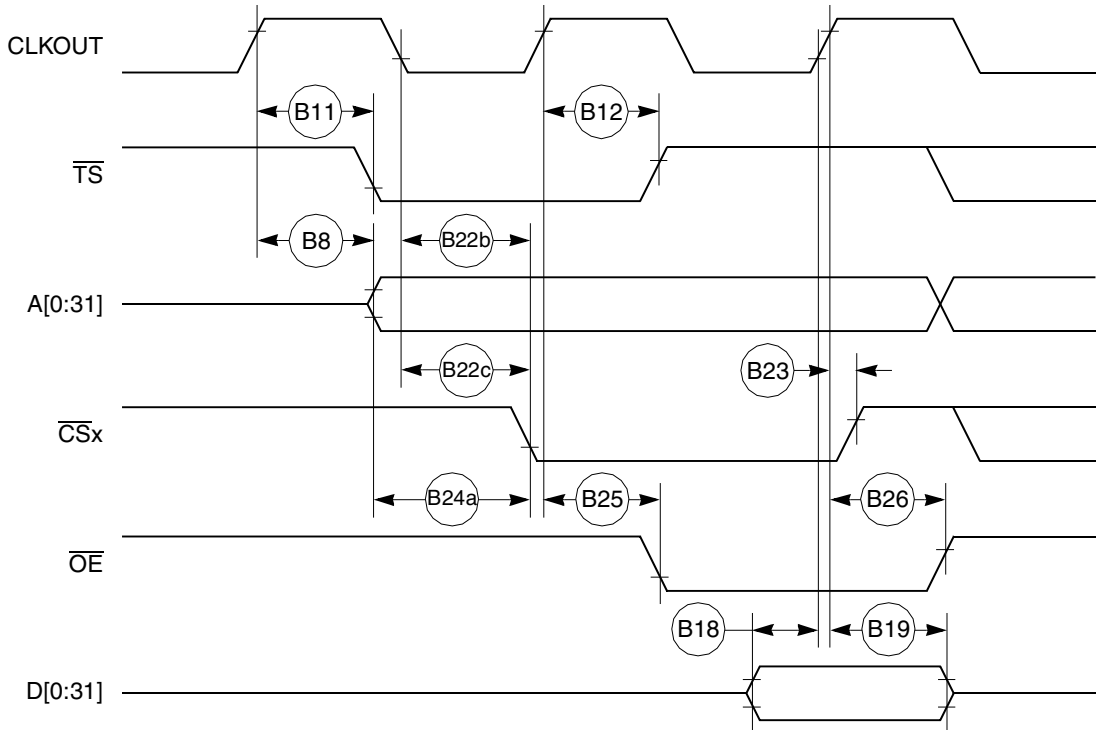


Figure 15. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 11)

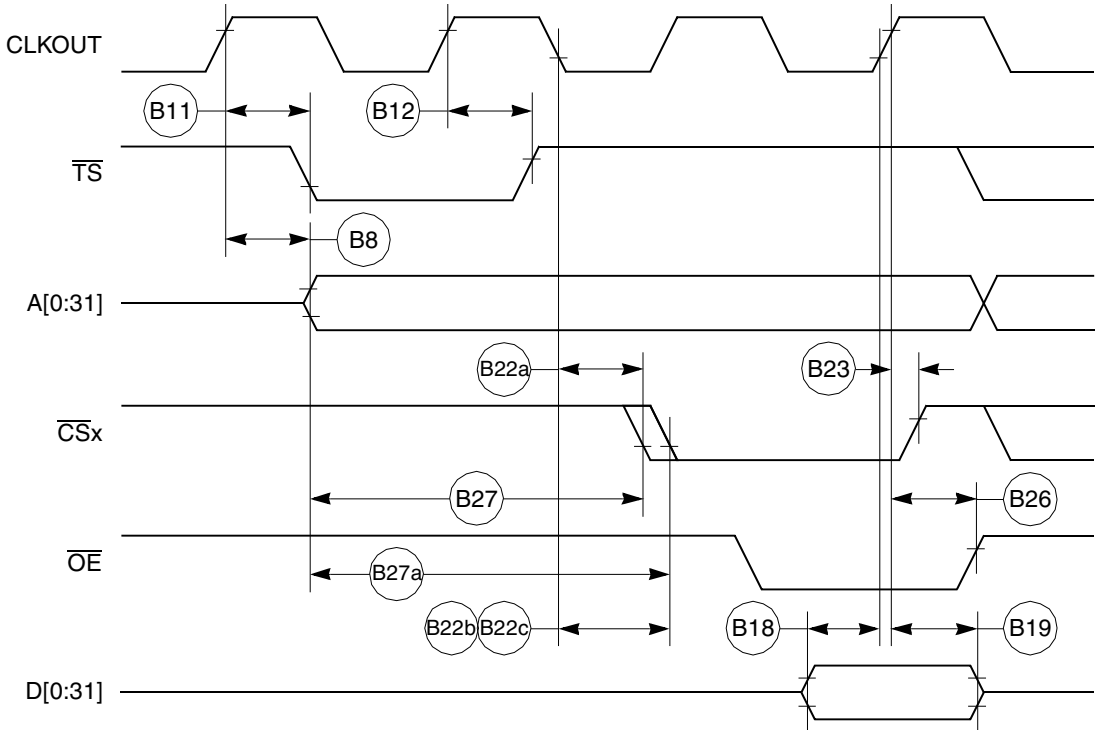


Figure 16. External Bus Read Timing (GPCM Controlled—TRLX = 1, ACS = 10, ACS = 11)

Figure 20 provides the timing for the external bus controlled by the UPM.

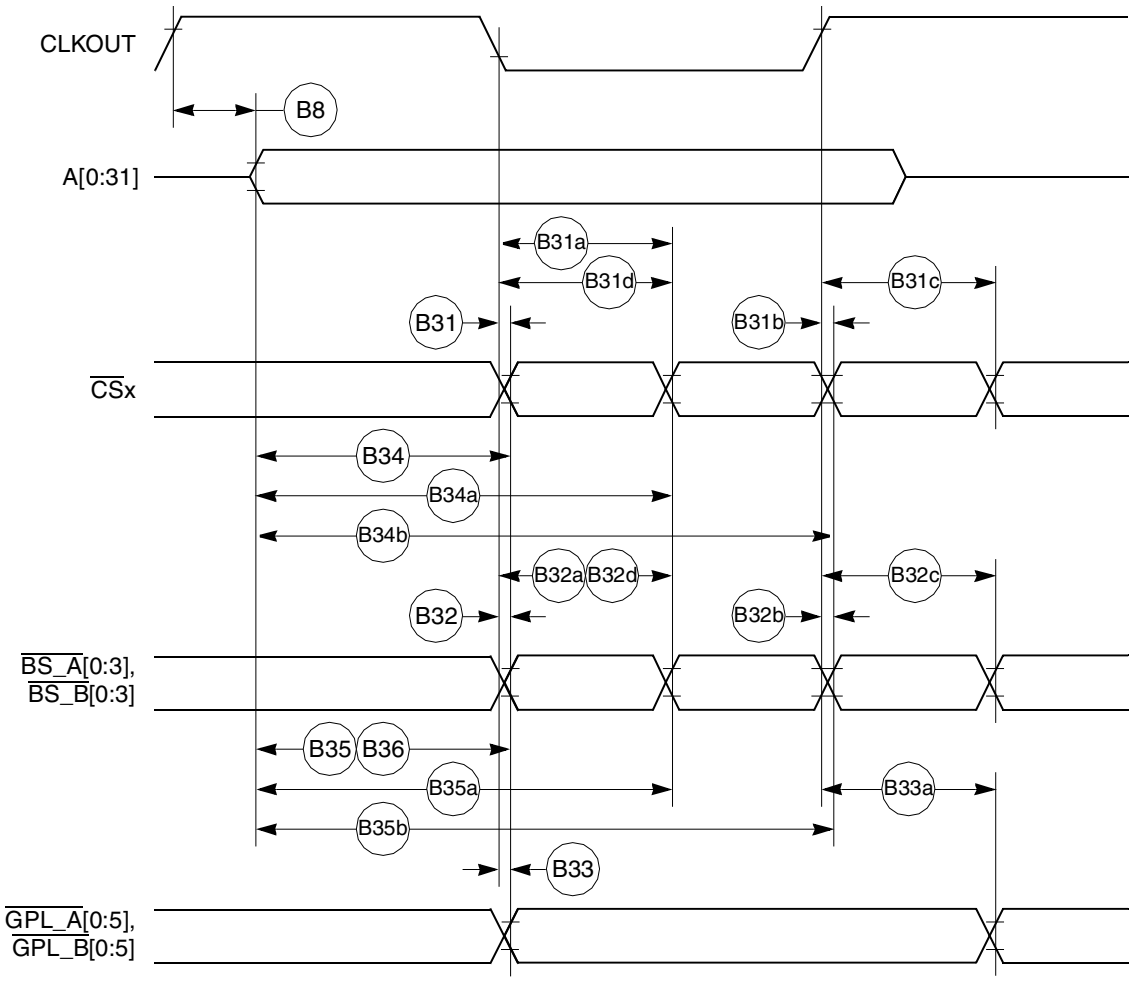


Figure 20. External Bus Timing (UPM-Controlled Signals)

Figure 21 provides the timing for the asynchronous asserted UPWAIT signal controlled by the UPM.

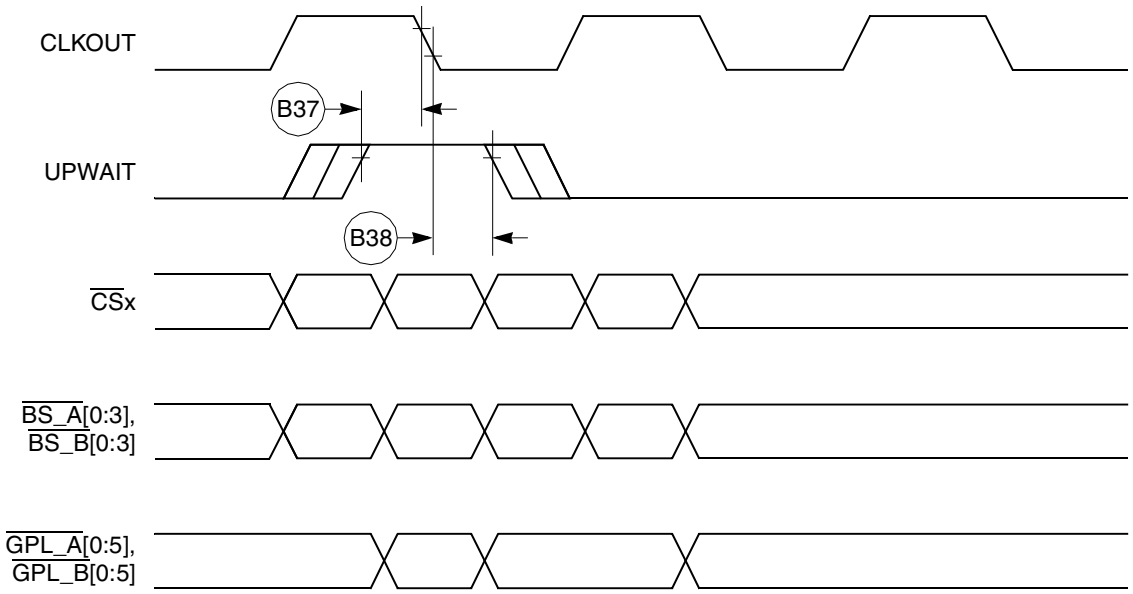


Figure 21. Asynchronous UPWAIT Asserted Detection in UPM-Handled Cycles Timing

Figure 22 provides the timing for the asynchronous negated UPWAIT signal controlled by the UPM.

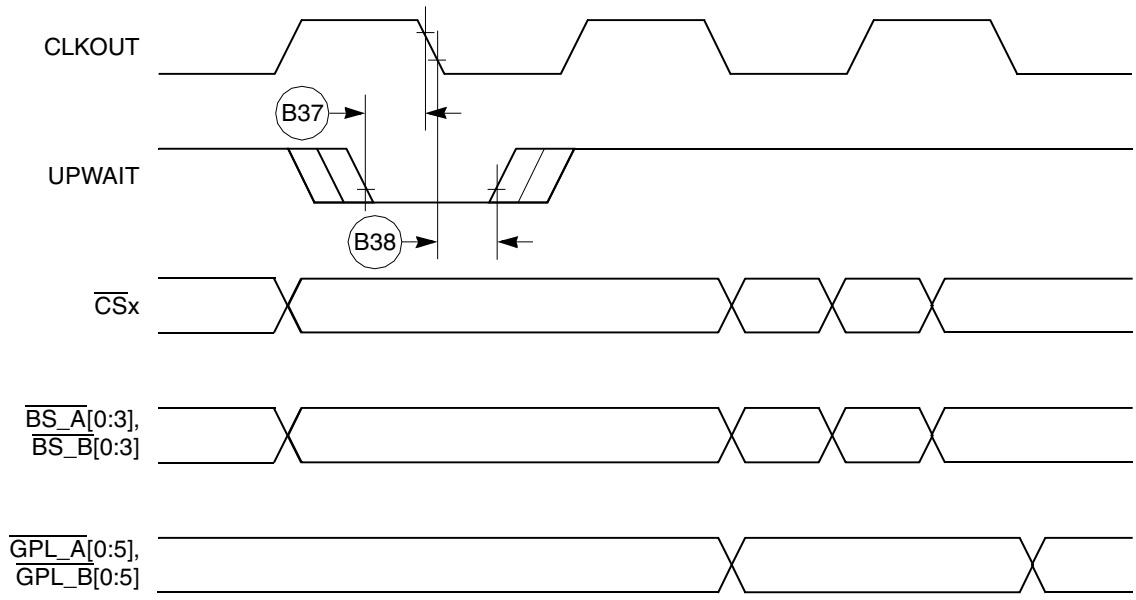


Figure 22. Asynchronous UPWAIT Negated Detection in UPM-Handled Cycles Timing

Table 11 shows the PCMCIA timing for the MPC885/MPC880.

Table 11. PCMCIA Timing

Num	Characteristic	33 MHz		40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
P44	A(0:31), $\overline{\text{REG}}$ valid to PCMCIA strobe asserted[1] (MIN = 0.75 × B1 – 2.00)	20.70	—	16.70	—	9.40	—	7.40	—	ns
P45	A(0:31), $\overline{\text{REG}}$ valid to ALE negation[1] (MIN = 1.00 × B1 – 2.00)	28.30	—	23.00	—	13.20	—	10.50	—	ns
P46	CLKOUT to $\overline{\text{REG}}$ valid (MAX = 0.25 × B1 + 8.00)	7.60	15.60	6.30	14.30	3.80	11.80	3.13	11.13	ns
P47	CLKOUT to $\overline{\text{REG}}$ invalid (MIN = 0.25 – B1 + 1.00)	8.60	—	7.30	—	4.80	—	4.13	—	ns
P48	CLKOUT to $\overline{\text{CE1}}$, $\overline{\text{CE2}}$ asserted (MAX = 0.25 × B1 + 8.00)	7.60	15.60	6.30	14.30	3.80	11.80	3.13	11.13	ns
P49	CLKOUT to $\overline{\text{CE1}}$, $\overline{\text{CE2}}$ negated (MAX = 0.25 × B1 + 8.00)	7.60	15.60	6.30	14.30	3.80	11.80	3.13	11.13	ns
P50	CLKOUT to $\overline{\text{PCOE}}$, $\overline{\text{IORD}}$, $\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ assert time (MAX = 0.00 × B1 + 11.00)	—	11.00	—	11.00	—	11.00	—	11.00	ns
P51	CLKOUT to $\overline{\text{PCOE}}$, $\overline{\text{IORD}}$, $\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ negate time (MAX = 0.00 × B1 + 11.00)	2.00	11.00	2.00	11.00	2.00	11.00	2.00	11.00	ns
P52	CLKOUT to ALE assert time (MAX = 0.25 × B1 + 6.30)	7.60	13.80	6.30	12.50	3.80	10.00	3.13	9.40	ns
P53	CLKOUT to ALE negate time (MAX = 0.25 × B1 + 8.00)	—	15.60	—	14.30	—	11.80	—	11.13	ns
P54	$\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ negated to D(0:31) invalid [1] (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	1.80	—	1.13	—	ns
P55	$\overline{\text{WAITA}}$ and $\overline{\text{WAITB}}$ valid to CLKOUT rising edge[1] (MIN = 0.00 × B1 + 8.00)	8.00	—	8.00	—	8.00	—	8.00	—	ns
P56	CLKOUT rising edge to $\overline{\text{WAITA}}$ and $\overline{\text{WAITB}}$ invalid[1] (MIN = 0.00 × B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns

[1] PSST = 1. Otherwise add PSST times cycle time.
PSHT = 0. Otherwise add PSHT times cycle time.

These synchronous timings define when the $\overline{\text{WAITx}}$ signals are detected in order to freeze (or relieve) the PCMCIA current cycle. The $\overline{\text{WAITx}}$ assertion will be effective only if it is detected 2 cycles before the PSL timer expiration. See Chapter 16, “PCMCIA Interface,” in the *MPC885 PowerQUICC™ Family Reference Manual*.

Figure 28 provides the PCMCIA access cycle timing for the external bus read.

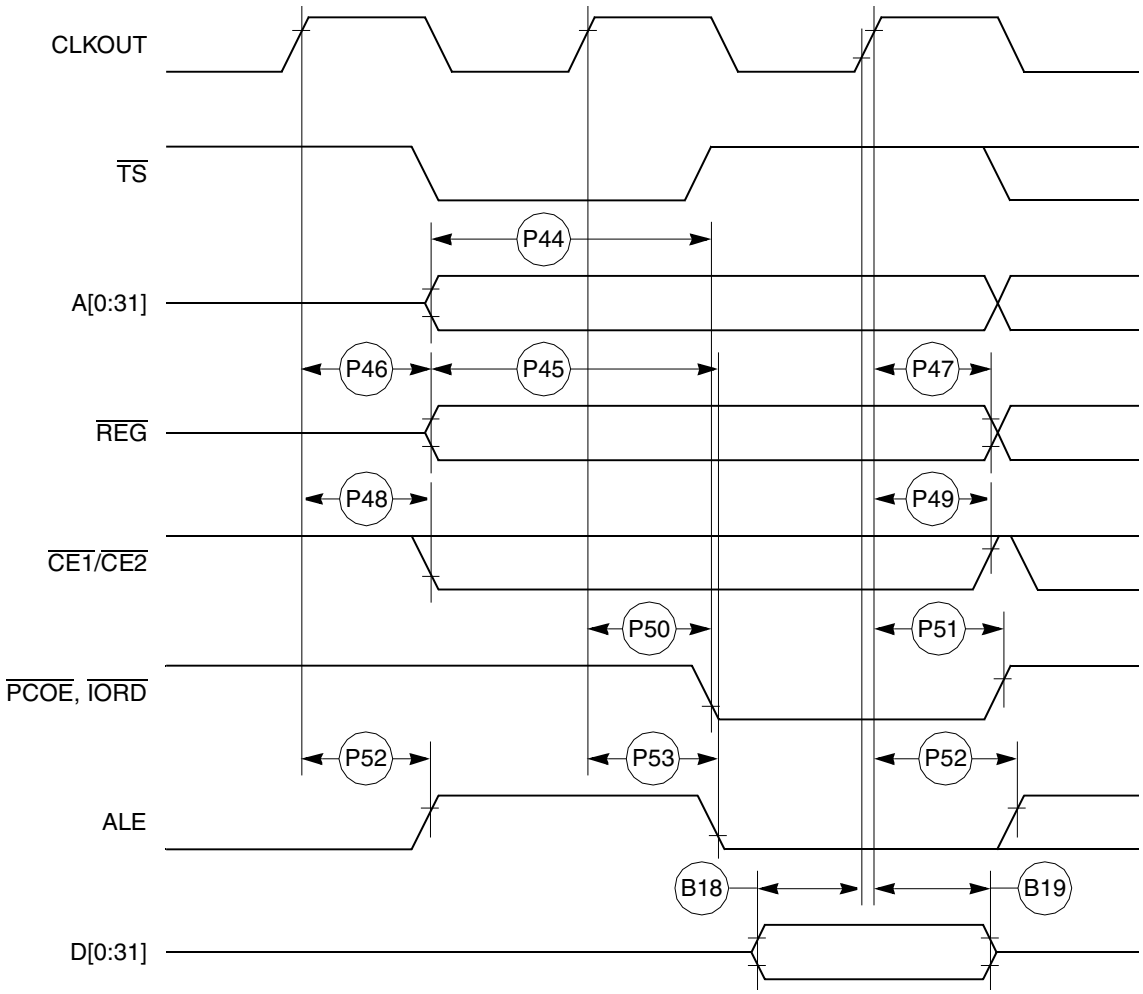


Figure 28. PCMCIA Access Cycles Timing External Bus Read

Figure 29 provides the PCMCIA access cycle timing for the external bus write.

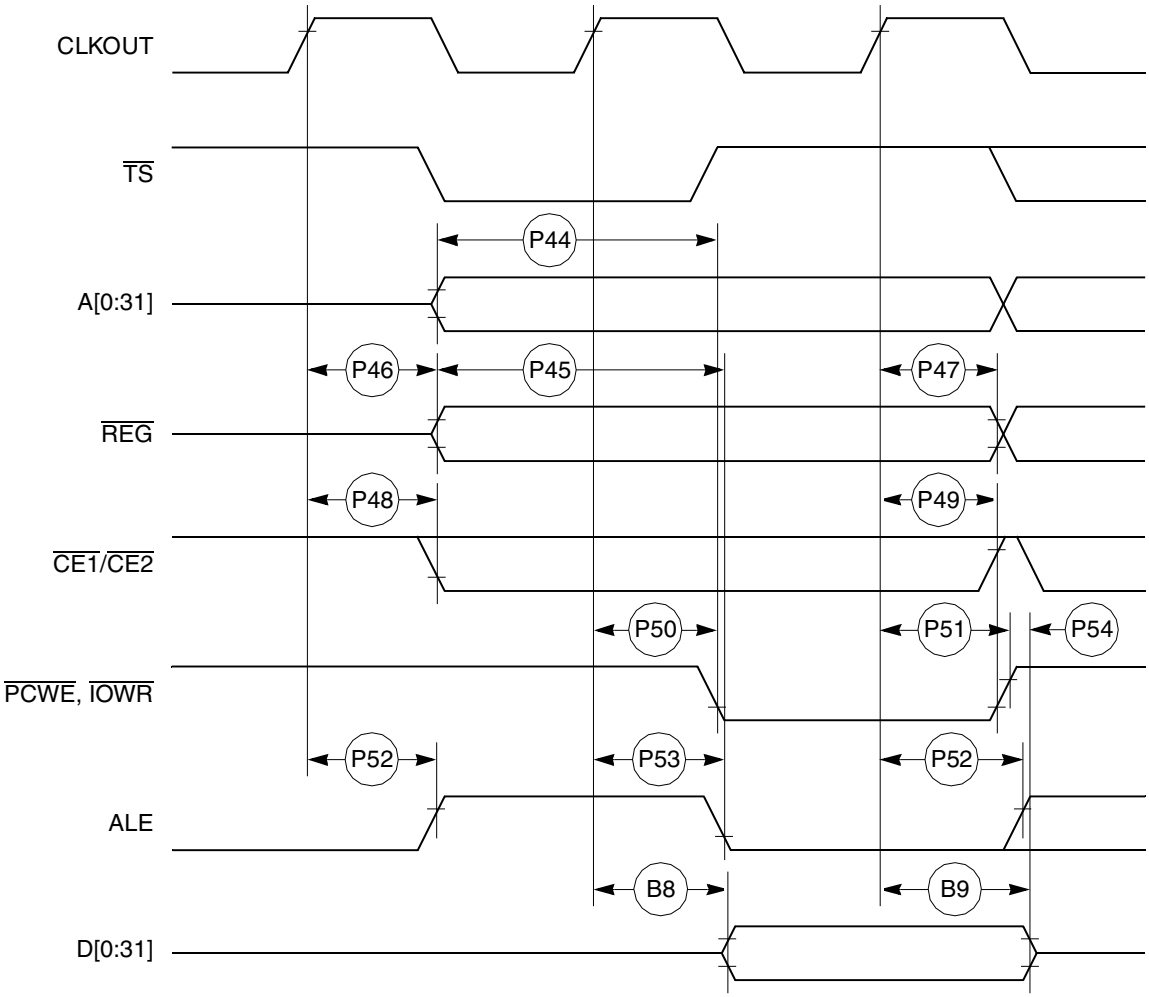


Figure 29. PCMCIA Access Cycles Timing External Bus Write

Figure 30 provides the PCMCIA WAIT signals detection timing.

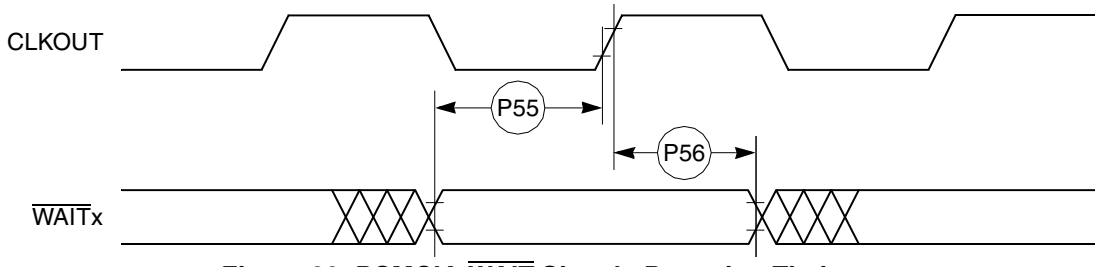


Figure 30. PCMCIA WAIT Signals Detection Timing

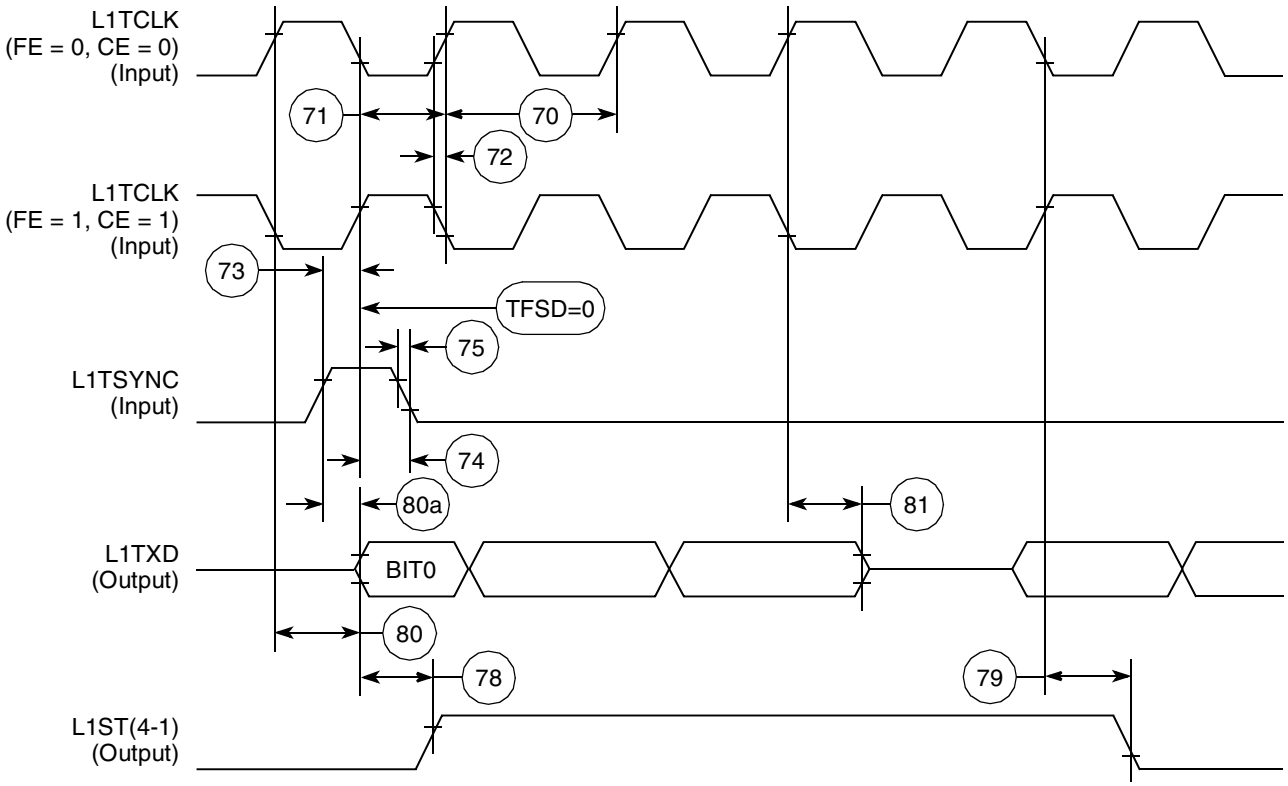
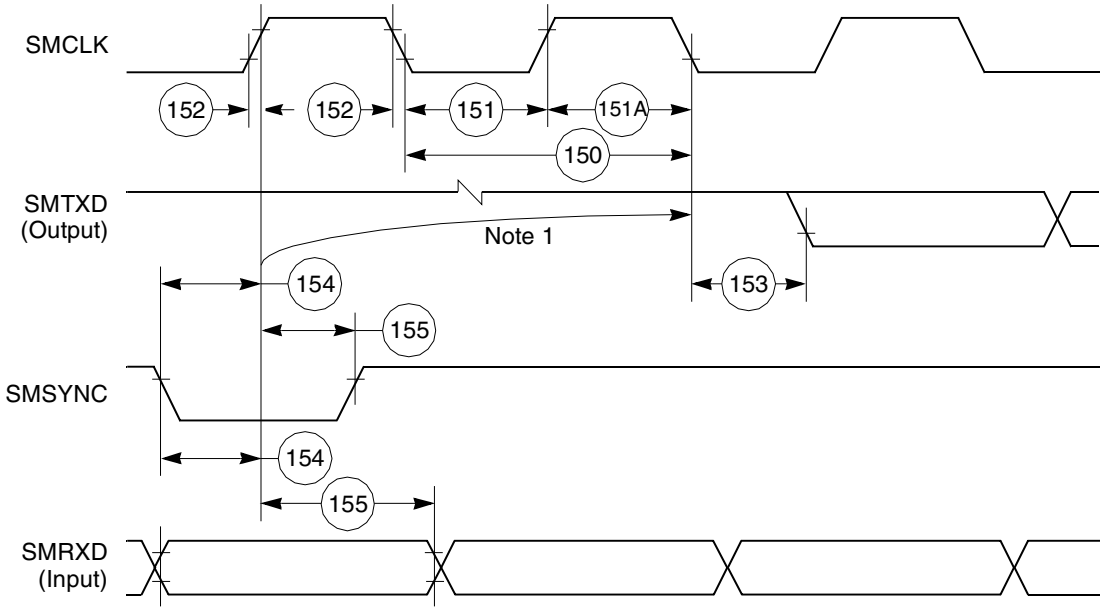


Figure 56. SI Transmit Timing Diagram (DSC = 0)



Note:
1. This delay is equal to an integer number of character-length clocks.

Figure 65. SMC Transparent Timing Diagram

12.10 SPI Master AC Electrical Specifications

Table 26 provides the SPI master timings as shown in Figure 66 and Figure 67.

Table 26. SPI Master Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
160	MASTER cycle time	4	1024	t_{cyc}
161	MASTER clock (SCK) high or low time	2	512	t_{cyc}
162	MASTER data setup time (inputs)	15	—	ns
163	Master data hold time (inputs)	0	—	ns
164	Master data valid (after SCK edge)	—	10	ns
165	Master data hold time (outputs)	0	—	ns
166	Rise time output	—	15	ns
167	Fall time output	—	15	ns

Figure 71 shows signal timings during UTOPIA receive operations.

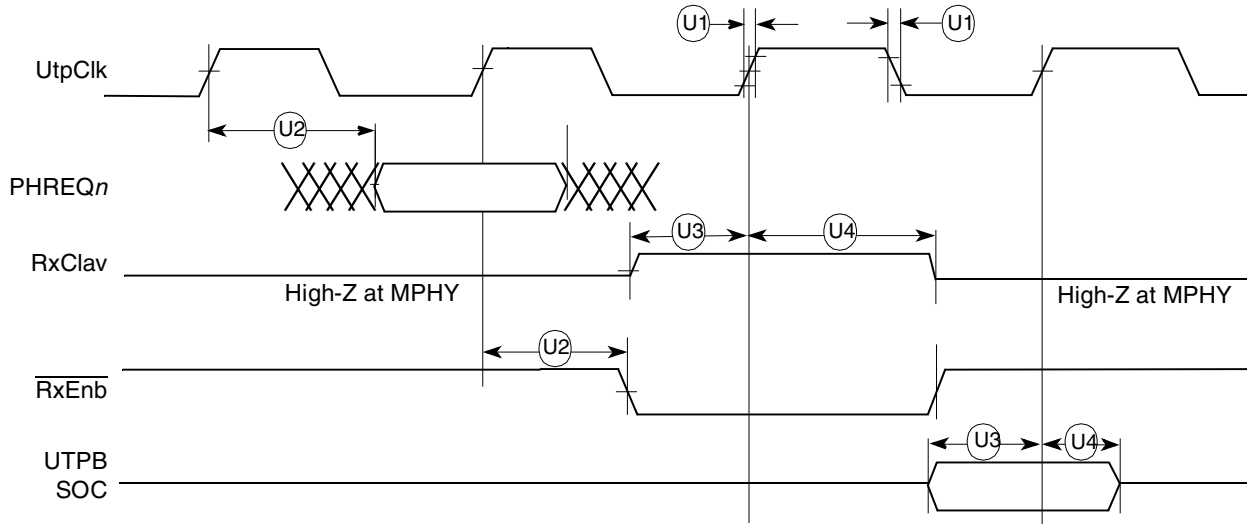


Figure 71. UTOPIA Receive Timing

Figure 72 shows signal timings during UTOPIA transmit operations.

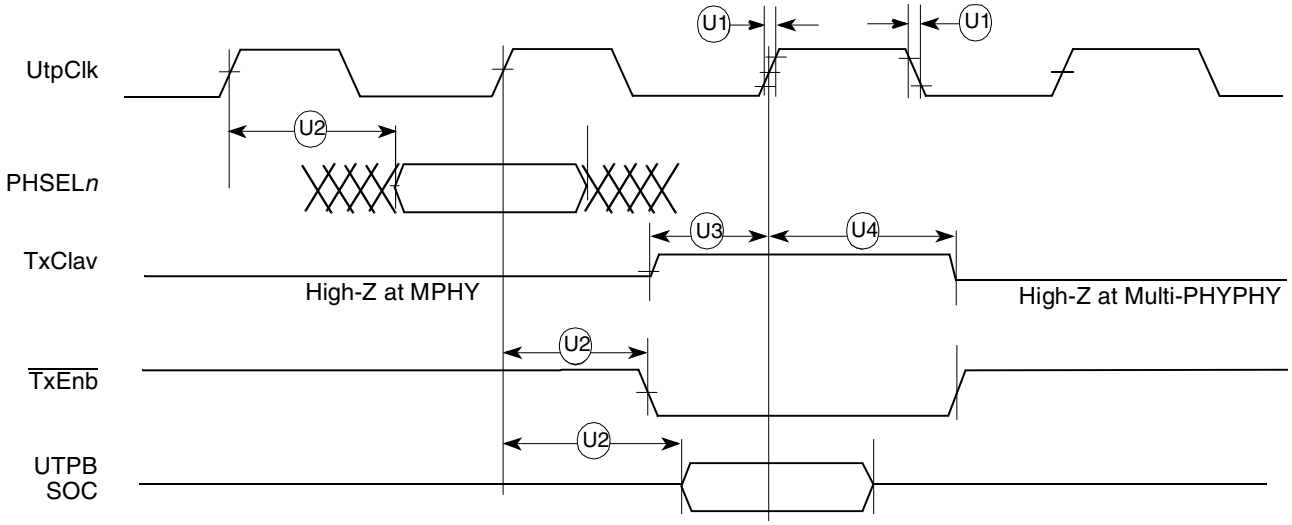


Figure 72. UTOPIA Transmit Timing

14 USB Electrical Characteristics

This section provides the AC timings for the USB interface.

14.1 USB Interface AC Timing Specifications

The USB Port uses the transmit clock on SCC1. Table 33 lists the USB interface timings.

Table 33. USB Interface AC Timing Specifications

Name	Characteristic	All Frequencies		Unit
		Min	Max	
US1	USBCLK frequency of operation[1] Low speed Full speed	 6 48		 MHz MHz
US4	USBCLK duty cycle (measured at 1.5 V)	45	55	%

[1] USBCLK accuracy should be ±500 ppm or better. USBCLK may be stopped to conserve power.

15 FEC Electrical Characteristics

This section provides the AC electrical specifications for the fast Ethernet controller (FEC). Note that the timing specifications for the MII signals are independent of system clock frequency (part speed designation). Also, MII signals use TTL signal levels compatible with devices operating at either 5.0 or 3.3 V.

15.1 MII and Reduced MII Receive Signal Timing

The receiver functions correctly up to a MII_RX_CLK maximum frequency of 25 MHz + 1%. The reduced MII (RMII) receiver functions correctly up to a RMII_REFCLK maximum frequency of 50 MHz + 1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_RX_CLK frequency – 1%.

Table 34 provides information on the MII and RMII receive signal timing.

Table 34. MII Receive Signal Timing

Num	Characteristic	Min	Max	Unit
M1	MII_RXD[3:0], MII_RX_DV, MII_RX_ERR to MII_RX_CLK setup	5	—	ns
M2	MII_RX_CLK to MII_RXD[3:0], MII_RX_DV, MII_RX_ER hold	5	—	ns
M3	MII_RX_CLK pulse width high	35%	65%	MII_RX_CLK period
M4	MII_RX_CLK pulse width low	35%	65%	MII_RX_CLK period
M1_RMII	RMII_RXD[1:0], RMII_CRS_DV, RMII_RX_ERR to RMII_REFCLK setup	4	—	ns
M2_RMII	RMII_REFCLK to RMII_RXD[1:0], RMII_CRS_DV, RMII_RX_ERR hold	2	—	ns

Figure 74 shows the MII transmit signal timing diagram.

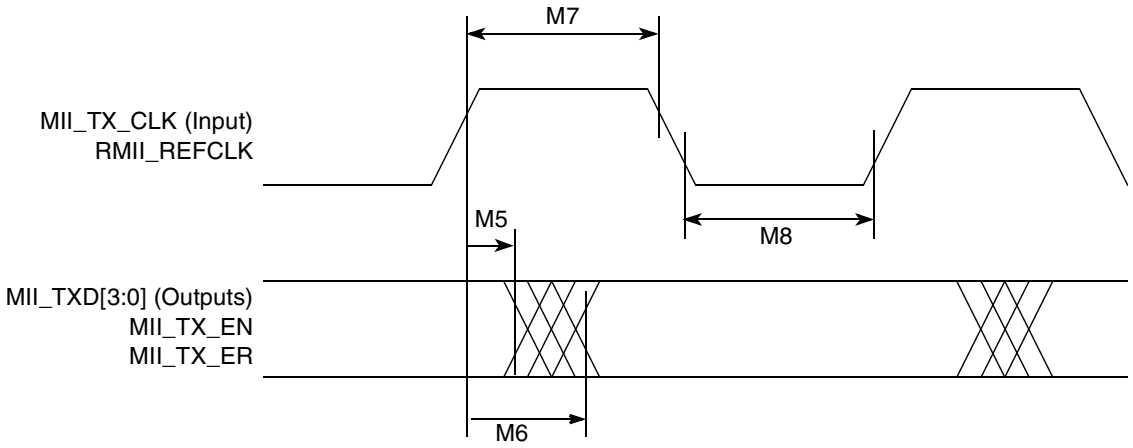


Figure 74. MII Transmit Signal Timing Diagram

15.3 MII Async Inputs Signal Timing (MII_CRS, MII_COL)

Table 36 provides information on the MII async inputs signal timing.

Table 36. MII Async Inputs Signal Timing

Num	Characteristic	Min	Max	Unit
M9	MII_CRS, MII_COL minimum pulse width	1.5	—	MII_TX_CLK period

Figure 75 shows the MII asynchronous inputs signal timing diagram.

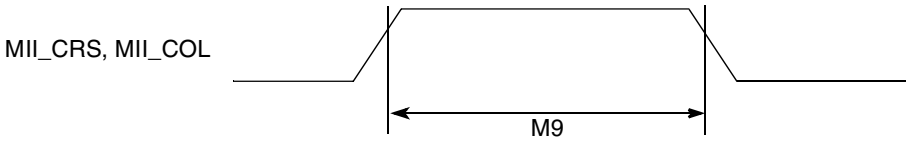


Figure 75. MII Async Inputs Timing Diagram

15.4 MII Serial Management Channel Timing (MII_MDIO, MII_MDC)

Table 37 provides information on the MII serial management channel signal timing. The FEC functions correctly with a maximum MDC frequency in excess of 2.5 MHz.

Table 37. MII Serial Management Channel Timing

Num	Characteristic	Min	Max	Unit
M10	MII_MDC falling edge to MII_MDIO output invalid (minimum propagation delay)	0	—	ns
M11	MII_MDC falling edge to MII_MDIO output valid (max prop delay)	—	25	ns
M12	MII_MDIO (input) to MII_MDC rising edge setup	10	—	ns
M13	MII_MDIO (input) to MII_MDC rising edge hold	0	—	ns

16.1 Pin Assignments

Figure 77 shows the top-view pinout of the PBGA package. For additional information, see the *MPC885 PowerQUICC™ Family Reference Manual*.

NOTE: This is the top view of the device.

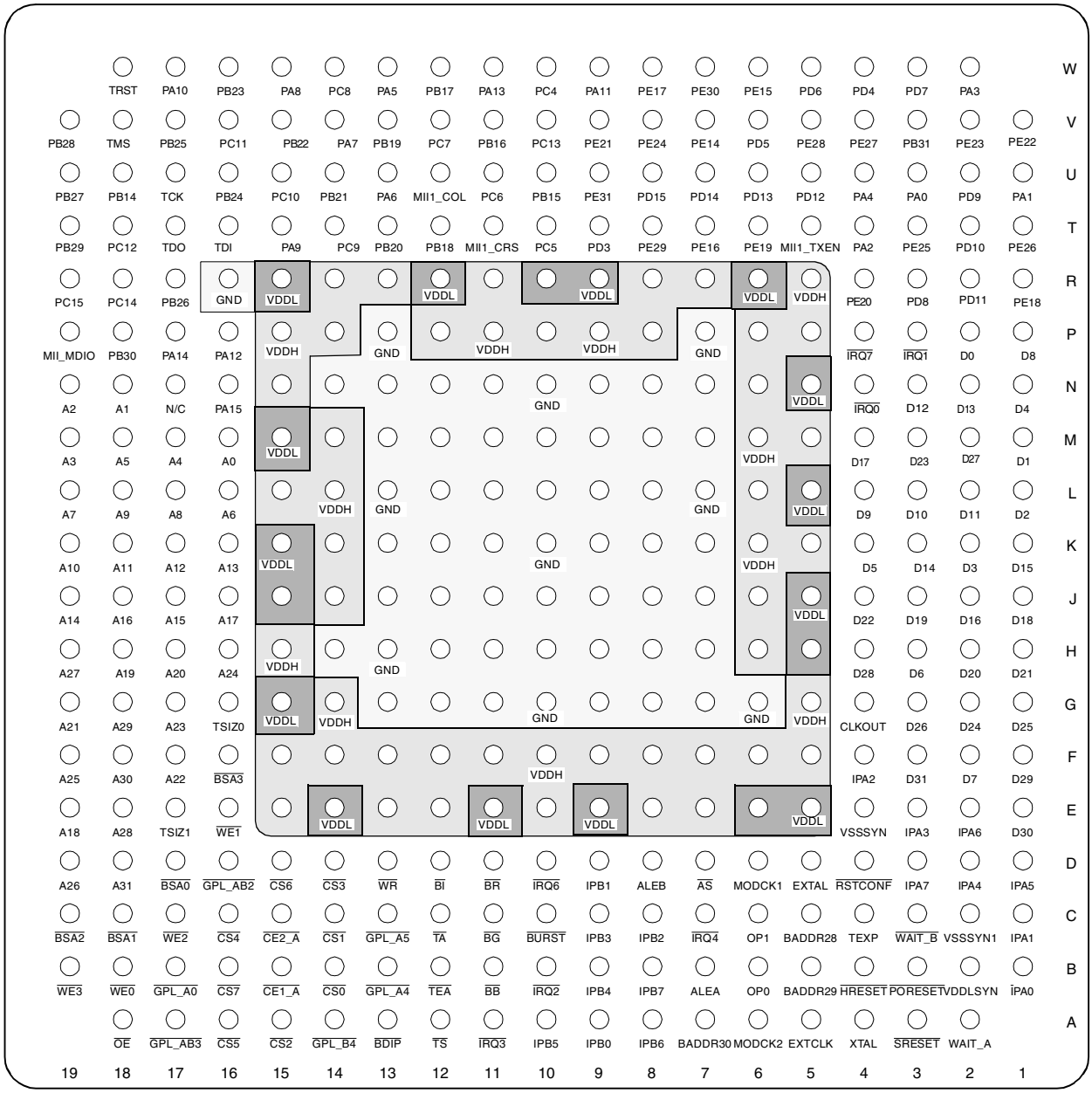


Figure 77. Pinout of the PBGA Package

Table 39. Pin Assignments (continued)

Name	Pin Number	Type
WE0, BS_B0, IORD	B18	Output
WE1, BS_B1, IOWR	E16	Output
WE2, BS_B2, PCOE	C17	Output
WE3, BS_B3, PCWE	B19	Output
BS_A[0:3]	D17, C18, C19, F16	Output
GPL_A0, GPL_B0	B17	Output
OE, GPL_A1, GPL_B1	A18	Output
GPL_A[2:3], GPL_B[2:3], CS[2:3]	D16, A17	Output
UPWAITA, GPL_A4	B13	Bidirectional
UPWAITB, GPL_B4	A14	Bidirectional
GPL_A5	C13	Output
PORESET	B3	Input
RSTCONF	D4	Input
HRESET	B4	Open-drain
SRESET	A3	Open-drain
XTAL	A4	Analog output
EXTAL	D5	Analog input (3.3 V only)
CLKOUT	G4	Output
EXTCLK	A5	Input (3.3 V only)
TEXP	C4	Output
ALE_A	B7	Output
CE1_A	B15	Output
CE2_A	C15	Output
WAIT_A, SOC_Split[1]	A2	Input
WAIT_B	C3	Input
IP_A0, UTPB_Split0[1]	B1	Input
IP_A1, UTPB_Split1[1]	C1	Input
IP_A2, IOIS16_A, UTPB_Split2[1]	F4	Input
IP_A3, UTPB_Split3[1]	E3	Input
IP_A4, UTPB_Split4[1]	D2	Input
IP_A5, UTPB_Split5[1]	D1	Input
IP_A6, UTPB_Split6[1]	E2	Input
IP_A7, UTPB_Split7[1]	D3	Input

Table 39. Pin Assignments (continued)

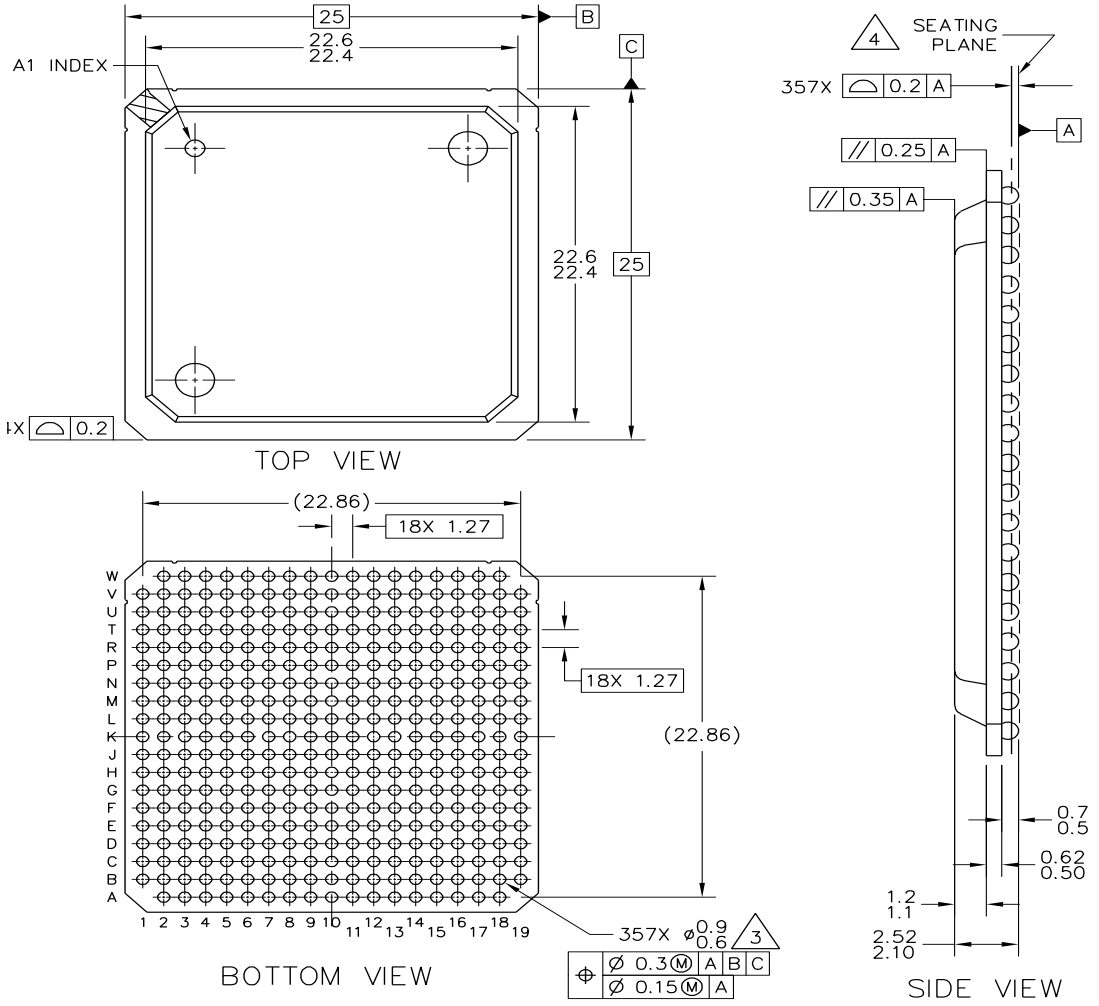
Name	Pin Number	Type
ALE_B, DSCK/AT1	D8	Bidirectional Three-state
IP_B[0:1], IWP[0:1], VFLS[0:1]	A9, D9	Bidirectional
IP_B2, $\overline{\text{IOIS16\_B}}$, AT2	C8	Bidirectional Three-state
IP_B3, IWP2, VF2	C9	Bidirectional
IP_B4, LWP0, VF0	B9	Bidirectional
IP_B5, LWP1, VF1	A10	Bidirectional
IP_B6, DSDI, AT0	A8	Bidirectional Three-state
IP_B7, $\overline{\text{PTR}}$, AT3	B8	Bidirectional Three-state
OP0, UtpClk_Split[1]	B6	Bidirectional
OP1	C6	Output
OP2, MODCK1, $\overline{\text{STS}}$	D6	Bidirectional
OP3, MODCK2, DSDO	A6	Bidirectional
BADDR30, $\overline{\text{REG}}$	A7	Output
BADDR[28:29]	C5, B5	Output
$\overline{\text{AS}}$	D7	Input
PA15, USBRXD	N16	Bidirectional
PA14, $\overline{\text{USBOE}}$	P17	Bidirectional (Optional: open-drain)
PA13, RXD2	W11	Bidirectional
PA12, TXD2	P16	Bidirectional (Optional: open-drain)
PA11, RXD4, MII1-TXD0, RMII1-TXD0	W9	Bidirectional (Optional: open-drain)
PA10, MII1-TXER, TIN4, CLK7	W17	Bidirectional (Optional: open-drain)
PA9, L1TXDA, RXD3	T15	Bidirectional (Optional: open-drain)
PA8, L1RXDA, TXD3	W15	Bidirectional (Optional: open-drain)
PA7, CLK1, L1RCLKA, BRGO1, TIN1	V14	Bidirectional
PA6, CLK2, $\overline{\text{TOUT1}}$	U13	Bidirectional
PA5, CLK3, L1TCLKA, BRGO2, TIN2	W13	Bidirectional

Table 39. Pin Assignments (continued)

Name	Pin Number	Type
PD5, CLK8, L1TCLKB, UTPB6	V6	Bidirectional
PD4, CLK4, UTPB7	W4	Bidirectional
PD3, CLK7, TIN4, SOC	T9	Bidirectional
PE31, CLK8, L1TCLKB, MII1-RXCLK	U9	Bidirectional (Optional: open-drain)
PE30, L1RXDB, MII1-RXD2	W7	Bidirectional (Optional: open-drain)
PE29, MII2-CRS	T8	Bidirectional (Optional: open-drain)
PE28, $\overline{\text{TOUT3}}$, MII2-COL	V5	Bidirectional (Optional: open-drain)
PE27, $\overline{\text{RTS3}}$, L1RQB, MII2-RXER, RMII2-RXER	V4	Bidirectional (Optional: open-drain)
PE26, L1CLKOB, MII2-RXDV, RMII2-CRS_DV	T1	Bidirectional (Optional: open-drain)
PE25, RXD4, MII2-RXD3, L1ST2	T3	Bidirectional (Optional: open-drain)
PE24, SMRXD1, BRGO1, MII2-RXD2	V8	Bidirectional (Optional: open-drain)
PE23, $\overline{\text{SMSYN2}}$, TXD4, MII2-RXCLK, L1ST1	V2	Bidirectional (Optional: open-drain)
PE22, $\overline{\text{TOUT2}}$, MII2-RXD1, RMII2-RXD1, $\overline{\text{SDACK1}}$	V1	Bidirectional (Optional: open-drain)
PE21, SMRXD2, $\overline{\text{TOUT1}}$, MII2-RXD0, RMII2-RXD0, $\overline{\text{RTS3}}$	V9	Bidirectional (Optional: open-drain)
PE20, L1RSYNCA, SMTXD2, $\overline{\text{CTS3}}$, MII2-TXER	R4	Bidirectional (Optional: open-drain)
PE19, L1TXDB, MII2-TXEN, RMII2-TXEN	T6	Bidirectional (Optional: open-drain)
PE18, L1TSYNCA, SMTXD1, MII2-TXD3	R1	Bidirectional (Optional: open-drain)
PE17, TIN3, CLK5, BRGO3, $\overline{\text{SMSYN1}}$, MII2-TXD2	W8	Bidirectional (Optional: open-drain)
PE16, L1RCLKB, CLK6, TXD3, MII2-TXCLK, RMII2-REFCLK	T7	Bidirectional (Optional: open-drain)
PE15, $\overline{\text{TGATE1}}$, MII2-TXD1, RMII2-TXD1	W6	Bidirectional

16.2 Mechanical Dimensions of the PBGA Package

Figure 78 shows the mechanical dimensions of the PBGA package.



NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M—1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

Figure 78. Mechanical Dimensions and Bottom Surface Nomenclature of the PBGA Package