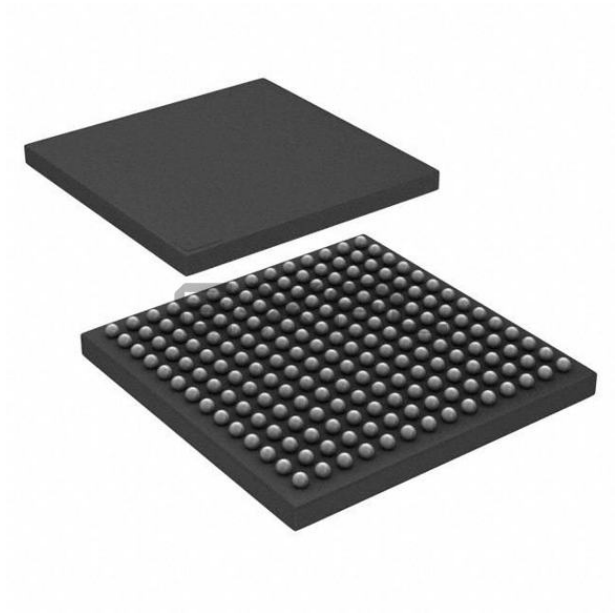

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	528MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SAI, SPDIF, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	127
Program Memory Size	-
Program Memory Type	External Program Memory
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 20x12b
Oscillator Type	External, Internal
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	196-LFBGA
Supplier Device Package	196-LFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mimxrt1052cvl5b

The i.MX RT1050 is specifically useful for applications such as:

- Industrial Human Machine Interfaces (HMI)
- Motor Control
- Home Appliance

1.1 Features

The i.MX RT1050 processors are based on Arm Cortex-M7 MPCore™ Platform, which has the following features:

- Supports single Arm Cortex-M7 MPCore with:
  - 32 KB L1 Instruction Cache
  - 32 KB L1 Data Cache
  - Full featured Floating Point Unit (FPU) with support of the VFPv5 architecture
  - Support the Armv7-M Thumb instruction set
- Integrated MPU, up to 16 individual protection regions
- Up to 512 KB I-TCM and D-TCM in total
- Frequency of 528 MHz
- Cortex M7 CoreSight™ components integration for debug
- Frequency of the core, as per Table 9, "Operating ranges," on page 19.

The SoC-level memory system consists of the following additional components:

  - Boot ROM (96 KB)
  - On-chip RAM (512 KB)
    - Configurable RAM size up to 512 KB shared with M7 TCM
- External memory interfaces:
  - 8/16-bit SDRAM, up to SDRAM-166
  - 8/16-bit SLC NAND FLASH, with ECC handled in software
  - SD/eMMC
  - SPI NOR FLASH
  - Parallel NOR FLASH with XIP support
  - Single/Dual channel Quad SPI FLASH with XIP support
- Timers and PWMs:
  - Two General Programmable Timers (GPT)
    - 4-channel generic 32-bit resolution timer
    - Each support standard capture and compare operation
  - Four Periodical Interrupt Timer (PIT)
    - Generic 16-bit resolution timer
    - Periodical interrupt generation
  - Four Quad Timers (QTimer)

3 Modules list

The i.MX RT1050 processors contain a variety of digital and analog modules. Table 2 describes these modules in alphabetical order.

Table 2. i.MX RT1050 modules list

Block Mnemonic	Block Name	Subsystem	Brief Description
ACMP1 ACMP2 ACMP3 ACMP4	Analog Comparator	Analog	The comparator (CMP) provides a circuit for comparing two analog input voltages. The comparator circuit is designed to operate across the full range of the supply voltage (rail-to-rail operation).
ADC1 ADC2	Analog to Digital Converter	Analog	The ADC is a 12-bit general purpose analog to digital converter.
AOI	And-Or-Inverter	Cross Trigger	The AOI provides a universal boolean function generator using a four team sum of products expression with each product term containing true or complement values of the four selected inputs (A, B, C, D).
Arm	Arm Platform	Arm	The Arm Core Platform includes one Cortex-M7 core. It includes associated sub-blocks, such as Nested Vectored Interrupt Controller (NVIC), Floating-Point Unit (FPU), Memory Protection Unit (MPU), and CoreSight debug modules.
BEE	Bus Encryption Engine	Security	On-The-Fly FlexSPI Flash Decryption
CCM GPC SRC	Clock Control Module, General Power Controller, System Reset Controller	Clocks, Resets, and Power Control	These modules are responsible for clock and reset distribution in the system, and also for the system power management.
CSI	Parallel CSI	Multimedia Peripherals	The CSI IP provides parallel CSI standard camera interface port. The CSI parallel data ports are up to 24 bits. It is designed to support 24-bit RGB888/YUV444, CCIR656 video interface, 8-bit YCbCr, YUV or RGB, and 8-bit/10-bit/16-bit Bayer data input.
CSU	Central Security Unit	Security	The Central Security Unit (CSU) is responsible for setting comprehensive security policy within the i.MX RT1050 platform.
DAP	Debug Access Port	System Control Peripherals	The DAP provides real-time access for the debugger without halting the core to: • System memory and peripheral registers • All debug configuration registers The DAP also provides debugger access to JTAG scan chains. The DAP module is internal to the Cortex-M7 Core Platform.

3.1 Special signal considerations

Table 3 lists special signal considerations for the i.MX RT1050 processors. The signal names are listed in alphabetical order.

The package contact assignments can be found in Section 6, "Package information and contact assignments." Signal descriptions are provided in the *i.MX RT1050 Reference Manual* (IMXRT1050_RM).

Table 3. Special signal considerations

Signal Name	Remarks
CCM_CLK1_P/ CCM_CLK1_N	One general purpose differential high speed clock Input/output (LVDS I/O) is provided. It can be used: • To feed external reference clock to the PLLs and further to the modules inside SoC. • To output internal SoC clock to be used outside the SoC as either reference clock or as a functional clock for peripherals. See the *i.MX RT1050 Reference Manual* (IMX6ULRM) for details on the respective clock trees. Alternatively one may use single ended signal to drive CLK1_P input. In this case corresponding CLK1_N input should be tied to the constant voltage level equal 1/2 of the input signal swing. Termination should be provided in case of high frequency signals. After initialization, the CLK1 input/output can be disabled (if not used). If unused either or both of the CLK1_N/P pairs may remain unconnected.
DCDC_PSWITCH	PAD is in DCDC_IN domain and connected the ground to bypass DCDC. To enable DCDC function, assert to DCDC_IN with at least 1ms delay for DCDC_IN rising edge.
RTC_XTALI/RTC_XTALO	If the user wishes to configure RTC_XTALI and RTC_XTALO as an RTC oscillator, a 32.768 kHz crystal, (≤100 kΩ ESR, 10 pF load) should be connected between RTC_XTALI and RTC_XTALO. Keep in mind the capacitors implemented on either side of the crystal are about twice the crystal load capacitor. To hit the exact oscillation frequency, the board capacitors need to be reduced to account for board and chip parasitics. The integrated oscillation amplifier is self biasing, but relatively weak. Care must be taken to limit parasitic leakage from RTC_XTALI and RTC_XTALO to either power or ground (>100 MΩ). This will debias the amplifier and cause a reduction of startup margin. Typically RTC_XTALI and RTC_XTALO should bias to approximately 0.5 V. If it is desired to feed an external low frequency clock into RTC_XTALI the RTC_XTALO pin must remain unconnected or driven with a complimentary signal. The logic level of this forcing clock should not exceed VDD_SNVS_CAP level and the frequency should be <100 kHz under typical conditions. In case when high accuracy real time clock are not required system may use internal low frequency ring oscillator. It is recommended to connect RTC_XTALI to GND and keep RTC_XTALO unconnected.
XTALI/XTALO	A 24.0 MHz crystal should be connected between XTALI and XTALO. The crystal must be rated for a maximum drive level of 250 μW. An ESR (equivalent series resistance) of typical 80 Ω is recommended. NXP SDK software requires 24 MHz on XTALI/XTALO. The crystal can be eliminated if an external 24 MHz oscillator is available in the system. In this case, XTALO must be directly driven by the external oscillator and XTALI mounted with 18 pF capacitor. The logic level of this forcing clock cannot exceed NVCC_PLL level. If this clock is used as a reference for USB, then there are strict frequency tolerance and jitter requirements. See OSC24M chapter and relevant interface specifications chapters for details.
GPANAIO	This signal is reserved for NXP manufacturing use only. This output must remain unconnected.

  - No external component required
  - Starts up quicker than 32 kHz crystal oscillator
- External crystal oscillator with on-chip support circuit:
  - At power up, ring oscillator is utilized. After crystal oscillator is stable, the clock circuit switches over to the crystal oscillator automatically.
  - Higher accuracy than ring oscillator
  - If no external crystal is present, then the ring oscillator is utilized

The decision of choosing a clock source should be taken based on real-time clock use and precision time-out.

4.1.5 Maximum supply currents

The data shown in Table 11 represent a use case designed specifically to show the maximum current consumption possible. All cores are running at the defined maximum frequency and are limited to L1 cache accesses only to ensure no pipeline stalls. Although a valid condition, it would have a very limited practical use case, if at all, and be limited to an extremely low duty cycle unless the intention were to specifically show the worst case power consumption.

See the i.MX RT1050 Power Consumption Measurement Application Note for more details on typical power consumption under various use case definitions.

Table 11. Maximum supply currents

Power Rail	Conditions	Max Current	Unit
DCDC_IN	Max power for FF chip at 105 ^{o}C	100	mA
VDD_HIGH_IN	Include internal loading in analog	50	mA
VDD_SNVS_IN	—	250	μA
USB_OTG1_VBUS USB_OTG2_VBUS	25 mA for each active USB interface	50	mA
VDDA_ADC_3P3	3.3 V power supply for 12-bit ADC, 600 μA typical, 750 μA max, for each ADC. 100 Ohm max loading for touch panel, cause 33 mA current.	40	mA
NVCC_GPIO NVCC_SD0 NVCC_SD1 NVCC_EMC	Imax = N x C x V x (0.5 x F) Where: N—Number of IO pins supplied by the power line C—Equivalent external capacitive load V—IO voltage (0.5 x F)—Data change rate. Up to 0.5 of the clock rate (F) In this equation, Imax is in Amps, C in Farads, V in Volts, and F in Hertz.		

4.1.6 Low power mode supply currents

Table 12 shows the current core consumption (not including I/O) of i.MX RT1050 processors in selected low power modes.

Table 12. Low power mode current and power consumption

Mode	Test Conditions	Supply	Typical[1]	Units
SYSTEM IDLE	• LDO_2P5 set to 2.5 V, LDO_1P1 set to 1.1 V • CPU in WFI, CPU clock gated • 24 MHz XTAL is ON • 528 PLL is active, other PLLs are power down • Peripheral clock gated, but remain powered	DCDC_IN (3.0 V for A0 and 3.3 V for A1)	4.0	mA
		VDD_HIGH_IN (3.3 V)	4.7	
		VDD_SNVS_IN (3.3 V)	0.036	
		Total	27.63	mW
LOW POWER IDLE	• LDO_2P5 and LDO_1P1 are set to Weak mode • WFI, half FlexRAM power down in power gate mode • All PLLs are power down • 24 MHz XTAL is off, 24 MHz RCOSC used as clock source • Peripheral clock gated, but remain powered	DCDC_IN (3.0 V for A0 and 3.3 V for A1)	2.2	mA
		VDD_HIGH_IN (3.3 V)	0.3	
		VDD_SNVS_IN (3.3 V)	0.042	
		Total	7.73	mW
SUSPEND (DSM)	• LDO_2P5 and LDO_1P1 are shut off • CPU in Power Gate mode • All PLLs are power down • 24 MHz XTAL is off, 24 MHz RCOSC is off • All clocks are shut off, except 32 kHz RTC • Peripheral clock gated, but remain powered	DCDC_IN (3.0 V for A0 and 3.3 V for A1)	0.2[2]	mA
		VDD_HIGH_IN (3.3 V)	0.037	
		VDD_SNVS_IN (3.3 V)	0.02	
		Total	0.788	mW
SNVS (RTC)	• All SOC digital logic, analog module are shut off • 32 kHz RTC is alive	DCDC_IN (0 V)	0	mA
		VDD_HIGH_IN (0 V)	0	
		VDD_SNVS_IN (3.3 V)	0.02	
		Total	0.066	mW

1 Typical process material in fab

2 Average current

4.1.7 USB PHY current consumption

4.1.7.1 Power down mode

In power down mode, everything is powered down, including the USB VBUS valid detectors in typical condition. Table 13 shows the USB interface current consumption in power down mode.

Table 13. USB PHY current consumption in power down mode

	VDD_USB_CAP (3.0 V)	VDD_HIGH_CAP (2.5 V)	NVCC_PLL (1.1 V)
Current	5.1 μA	1.7 μA	< 0.5 μA

NOTE

The currents on the VDD_HIGH_CAP and VDD_USB_CAP were identified to be the voltage divider circuits in the USB-specific level shifters.

4.2 System power and clocks

This section provide the information about the system power and clocks.

4.2.1 Power supplies requirements and restrictions

The system design must comply with power-up sequence, power-down sequence, and steady state guidelines as described in this section to guarantee the reliable operation of the device. Any deviation from these sequences may result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting
- Irreversible damage to the processor (worst-case scenario)

4.2.1.1 Power-up sequence

The below restrictions must be followed:

- VDD_SNVS_IN supply must be turned on before any other power supply or be connected (shorted) with VDD_HIGH_IN supply.
- If a coin cell is used to power VDD_SNVS_IN, then ensure that it is connected before any other supply is switched on.
- When internal DCDC is enabled, external delay circuit is required to delay the “DCDC_PSWITCH” signal 1 ms after DCDC_IN is stable.
- POR_B should be held low during the entire power up sequence.

NOTE

The POR_B input (if used) must be immediately asserted at power-up and remain asserted until after the last power rail reaches its working voltage. In the absence of an external reset feeding the POR_B input, the internal POR module takes control. See the *i.MX RT1050 Reference Manual* (IMXRT1050_RM) for further details and to ensure that all necessary requirements are being met.

NOTE

Need to ensure that there is no back voltage (leakage) from any supply on the board towards the 3.3 V supply (for example, from the external components that use both the 1.8 V and 3.3 V supplies).

NOTE

USB_OTG1_VBUS, USB_OTG2_VBUS, and VDDA_ADC_3P3 are not part of the power supply sequence and may be powered at any time.

4.2.1.2 Power-down sequence

The following restrictions must be followed:

- VDD_SNVS_IN supply must be turned off after any other power supply or be connected (shorted) with VDD_HIGH_IN supply.
- If a coin cell is used to power VDD_SNVS_IN, then ensure that it is removed after any other supply is switched off.

4.2.1.3 Power supplies usage

All I/O pins should not be externally driven while the I/O power supply for the pin (NVCC_xxx) is OFF. This can cause internal latch-up and malfunctions due to reverse current flows. For information about I/O power supply of each pin, see "Power Rail" columns in pin list tables of Section 6, "Package information and contact assignments."

4.2.2 Integrated LDO voltage regulator parameters

Various internal supplies can be powered ON from internal LDO voltage regulators. All the supply pins named *_CAP must be connected to external capacitors. The onboard LDOs are intended for internal use only and should not be used to power any external circuitry. See the *i.MX RT1050 Reference Manual* (IMXRT1050_RM) for details on the power tree scheme.

NOTE

The *_CAP signals should not be powered externally. These signals are intended for internal LDO operation only.

4.2.2.1 Digital regulators (LDO_SNVS)

There are one digital LDO regulator ("Digital", because of the logic loads that they drive, not because of their construction). The advantages of the regulator is to reduce the input supply variation because of its input supply ripple rejection and its on-die trimming. This translates into more stable voltage for the on-chip logics.

The regulator has two basic modes:

- Power Gate. The regulation FET is switched fully off limiting the current draw from the supply. The analog part of the regulator is powered down here limiting the power consumption.
- Analog regulation mode. The regulation FET is controlled such that the output voltage of the regulator equals the target voltage.

For additional information, see the *i.MX RT1050 Reference Manual* (IMXRT1050_RM).

4.2.2.2 Regulators for analog modules

4.2.2.2.1 LDO_1P1

The LDO_1P1 regulator implements a programmable linear-regulator function from VDD_HIGH_IN (see Table 9 for minimum and maximum input requirements). Typical Programming Operating Range is 1.0 V

4.3.3.1 Single voltage GPIO output buffer impedance

Table 25 shows the GPIO output buffer impedance (NVCC_XXXX 1.8 V).

Table 25. GPIO output buffer average impedance (NVCC_XXXX 1.8 V)

Parameter	Symbol	Drive Strength (DSE)	Typ Value	Unit
Output Driver Impedance	Rdrv	001 010 011 100 101 110 111	260 130 88 65 52 43 37	Ω

Table 26 shows the GPIO output buffer impedance (NVCC_XXXX 3.3 V).

Table 26. GPIO output buffer average impedance (NVCC_XXXX 3.3 V)

Parameter	Symbol	Drive Strength (DSE)	Typ Value	Unit
Output Driver Impedance	Rdrv	001 010 011 100 101 110 111	157 78 53 39 32 26 23	Ω

4.4 System modules

This section contains the timing and electrical parameters for the modules in the i.MX RT1050 processor.

4.4.1 Reset timings parameters

Figure 7 shows the reset timing and Table 27 lists the timing parameters.

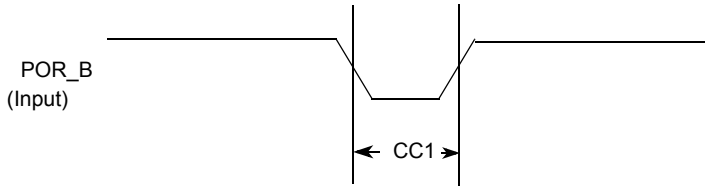


Figure 7. Reset timing diagram

Table 27. Reset timing parameters

ID	Parameter	Min	Max	Unit
CC1	Duration of POR_B to be qualified as valid.	1	—	RTC_XTALI cycle

Table 29. JTAG timing (continued)

ID	Parameter[1,2]	All Frequencies		Unit
		Min	Max	
SJ9	JTAG_TMS, JTAG_TDI data hold time	25	—	ns
SJ10	JTAG_TCK low to JTAG_TDO data valid	—	44	ns
SJ11	JTAG_TCK low to JTAG_TDO high impedance	—	44	ns
SJ12	JTAG_TRST_B assert time	100	—	ns
SJ13	JTAG_TRST_B set-up time to JTAG_TCK low	40	—	ns

1 T_{DC} = target frequency of SJC
2 V_M = mid-point voltage

4.5 External memory interface

The following sections provide information about external memory interfaces.

4.5.1 SEMC specifications

The following sections provide information on SEMC interface.

Measurements are with a load of 15 pf and an input slew rate of 1 V/ns.

4.5.1.1 SEMC output timing

There are ASYNC and SYNC mode for SEMC output timing.

4.5.1.1.1 SEMC output timing in ASYNC mode

Table 30 shows SEMC output timing in ASYNC mode.

Table 30. SEMC output timing in ASYNC mode

Symbol	Parameter	Min.	Max.	Unit	Comment
	Frequency of operation	—	166	MHz	
T_{CK}	Internal clock period	6	—	ns	
T_{AVO}	Address output valid time	—	2	ns	These timing parameters apply to Address and ADV# for NOR/PSRAM in ASYNC mode.
T_{AHO}	Address output hold time	(TCK - 2) [1]	—	ns	
T_{ADVL}	ADV# low time	(TCK - 1) [2]			
T_{DVO}	Data output valid time	—	2	ns	These timing parameters apply to Data/CLE/ALE and WE# for NAND, apply to Data/DM/CRE for NOR/PSRAM, apply to Data/DCX and WRX for DBI interface.
T_{DHO}	Data output hold time	(TCK - 2) [3]	—	ns	
T_{WEL}	WE# low time	(TCK - 1) [4]		ns	

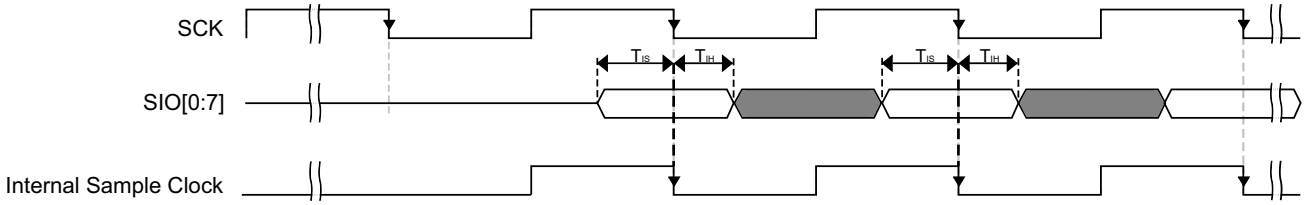


Figure 17. FlexSPI input timing in SDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0X0, 0X1

NOTE

Timing shown is based on the memory generating read data on the SCK falling edge, and FlexSPI controller sampling read data on the falling edge.

4.5.2.1.2 SDR mode with FlexSPI*n*_MCR0[RXCLKSRC] = 0x3

There are two cases when the memory provides both read data and the read strobe in SDR mode:

- A1 - Memory generates both read data and read strobe on SCK rising edge (or falling edge)
- A2 - Memory generates read data on SCK falling edge and generates read strobe on SCK rising edgeSCK rising edge

Table 37. FlexSPI input timing in SDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x3 (case A1)

Symbol	Parameter	Value		Unit
		Min	Max	
	Frequency of operation	—	166	MHz
T_{SCKD}	Time from SCK to data valid	—	—	ns
T_{SCKDQS}	Time from SCK to DQS	—	—	ns
T_{SCKD} - T_{SCKDQS}	Time delta between T_{SCKD} and T_{SCKDQS}	-2	2	ns

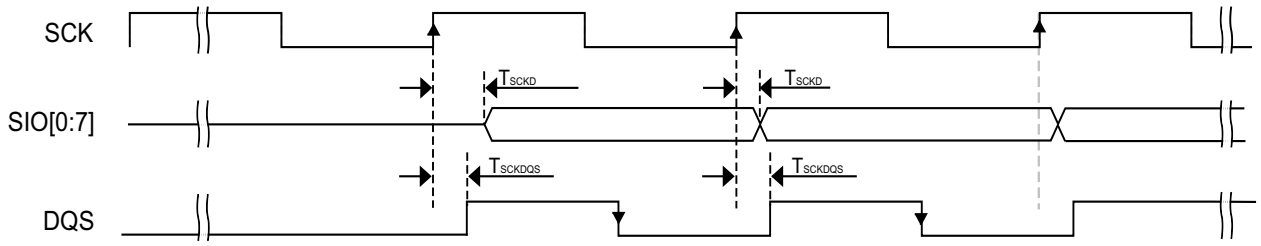


Figure 18. FlexSPI input timing in SDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0X3 (case A1)

4.6.2 LCD Controller (LCDIF) timing parameters

Figure 28 shows the LCDIF timing and Table 47 lists the timing parameters.

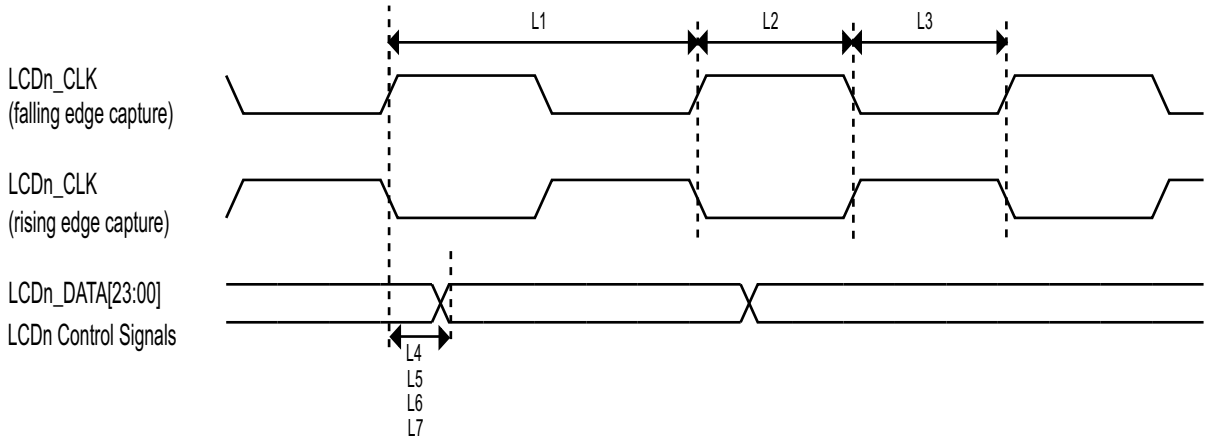


Figure 28. LCD timing

Table 47. LCD timing parameters

ID	Parameter	Symbol	Min	Max	Unit
L1	LCD pixel clock frequency	tCLK(LCD)	—	75	MHz
L2	LCD pixel clock high (falling edge capture)	tCLKH(LCD)	3	—	ns
L3	LCD pixel clock low (rising edge capture)	tCLKL(LCD)	3	—	ns
L4	LCD pixel clock high to data valid (falling edge capture)	td(CLKH-DV)	-1	1	ns
L5	LCD pixel clock low to data valid (rising edge capture)	td(CLKL-DV)	-1	1	ns
L6	LCD pixel clock high to control signal valid (falling edge capture)	td(CLKH-CTRLV)	-1	1	ns
L7	LCD pixel clock low to control signal valid (rising edge capture)	td(CLKL-CTRLV)	-1	1	ns

4.7 Audio

This section provide information about SAI/I2S and SPDIF.

4.7.1 SAI/I2S switching specifications

This section provides the AC timings for the SAI in master (clocks driven) and slave (clocks input) modes. All timings are given for non-inverted serial clock polarity (SAI_TCR[TSCKP] = 0, SAI_RCR[RSCKP] = 0) and non-inverted frame sync (SAI_TCR[TFSI] = 0, SAI_RCR[RFSI] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (SAI_BCLK) and/or the frame sync (SAI_FS) shown in the figures below.

Table 51. DCDC electrical specifications (continued)

Mode	Buck mode, one output	Notes
Loading in low power modes	200 μA ~ 30 mA	—
Efficiency	90% max	@150 mA
Low power mode	Open loop mode	Ripple is about 15 mV in Run mode
Run mode	• Always continuous mode • Support discontinuous mode	Configurable by register
Inductor	4.7 μH	—
Capacitor	33 μF	—
Over voltage protection	1.55 V	Detect VDDSOC, when the voltage is higher than 1.6 V, shutdown DCDC.
Over Current protection	1 A	Detect the peak current • Run mode: when the current is larger than 1 A, shutdown DCDC.
Low DCDC_IN detection	2.6 V	Detect the DCDC_IN, when battery is lower than 2.6 V, shutdown DCDC.

4.8.2 A/D converter

This section introduces information about A/D converter.

4.8.2.1 12-bit ADC electrical characteristics

The section provide information about 12-bit ADC electrical characteristics.

4.8.2.1.1 12-bit ADC operating conditions

Table 52. 12-bit ADC operating conditions

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
Supply voltage	Absolute	V_{DDA}	3.0	-	3.6	V	—
	Delta to VDD (VDD-VDDA)[2]	ΔV_{DDA}	-100	0	100	mV	—
Ground voltage	Delta to VSS (VSS-VSSAD)	ΔV_{SSAD}	-100	0	100	mV	—
Ref Voltage High	—	V_{DDA}	1.13	V_{DDA}	V_{DDA}	V	—
Ref Voltage Low	—	V_{SS}	V_{SSAD}	V_{SSAD}	V_{SSAD}	V	—
Input Voltage	—	V_{ADIN}	V_{REFL}	—	V_{REFH}	V	—
Input Capacitance	8/10/12 bit modes	C_{ADIN}	—	1.5	2	pF	—

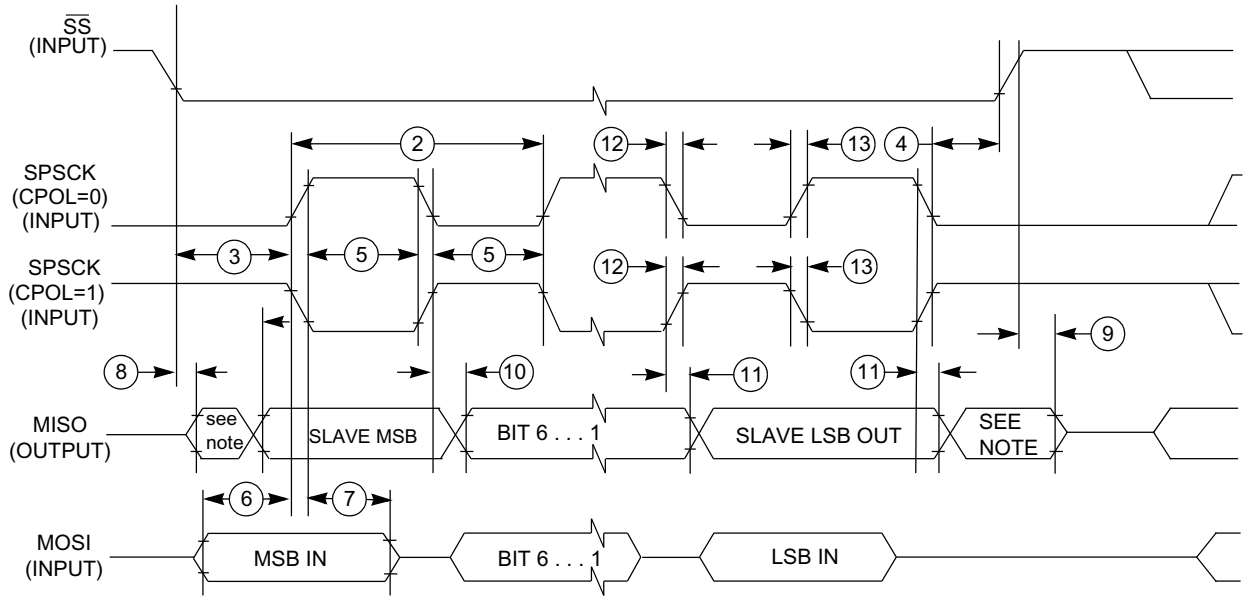


Figure 36. LPSPI Slave mode timing (CPHA = 0)

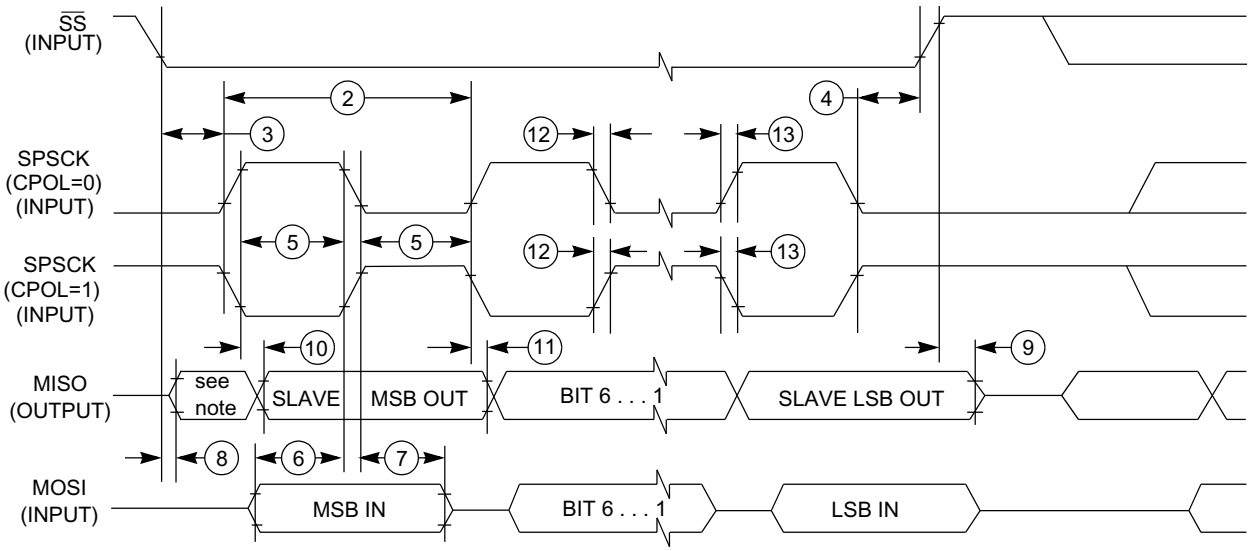


Figure 37. LPSPI Slave mode timing (CPHA = 1)

4.9.4.1 ENET MII mode timing

This subsection describes MII receive, transmit, asynchronous inputs, and serial management signal timings.

4.9.4.1.1 MII receive signal timing (ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER, and ENET_RX_CLK)

The receiver functions correctly up to an ENET_RX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the ENET_RX_CLK frequency.

Figure 42 shows MII receive signal timings. Table 62 describes the timing parameters (M1–M4) shown in the figure.

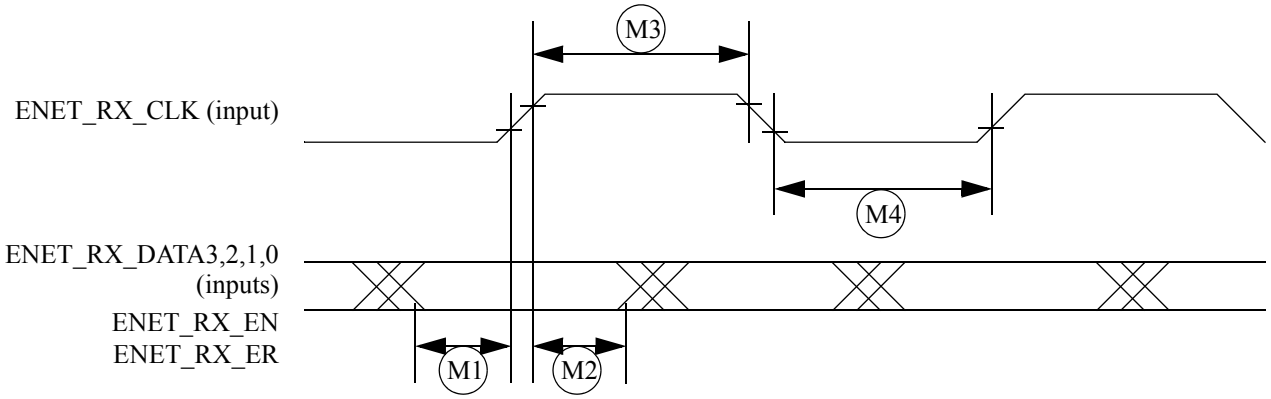


Figure 42. MII receive signal timing diagram

Table 62. MII receive signal timing

ID	Characteristic[1]	Min.	Max.	Unit
M1	ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER to ENET_RX_CLK setup	5	—	ns
M2	ENET_RX_CLK to ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER hold	5	—	ns
M3	ENET_RX_CLK pulse width high	35%	65%	ENET_RX_CLK period
M4	ENET_RX_CLK pulse width low	35%	65%	ENET_RX_CLK period

[1] ENET_RX_EN, ENET_RX_CLK, and ENET0_RXD0 have the same timing in 10 Mbps 7-wire interface mode.

4.9.4.1.2 MII transmit signal timing (ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER, and ENET_TX_CLK)

The transmitter functions correctly up to an ENET_TX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the ENET_TX_CLK frequency.

Figure 46 shows RMII mode timings. Table 66 describes the timing parameters (M16–M21) shown in the figure.

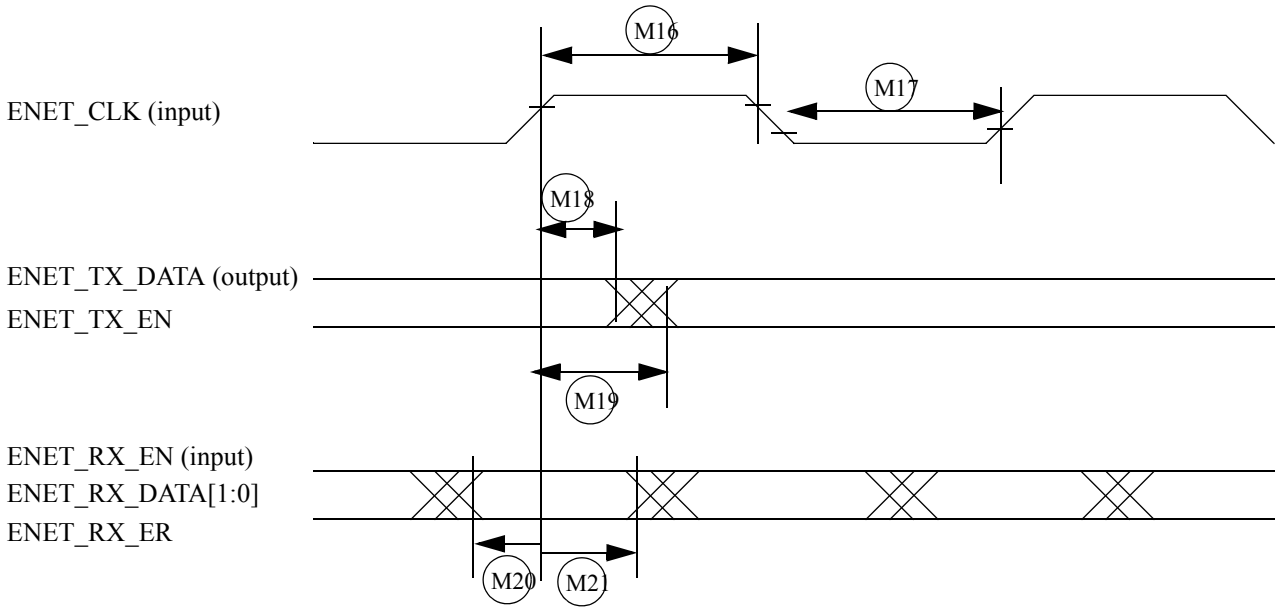


Figure 46. RMII mode signal timing diagram

Table 66. RMII signal timing

ID	Characteristic	Min.	Max.	Unit
M16	ENET_CLK pulse width high	35%	65%	ENET_CLK period
M17	ENET_CLK pulse width low	35%	65%	ENET_CLK period
M18	ENET_CLK to ENET0_TXD[1:0], ENET_TX_DATA invalid	4	—	ns
M19	ENET_CLK to ENET0_TXD[1:0], ENET_TX_DATA valid	—	13	ns
M20	ENET_RX_DATAD[1:0], ENET_RX_EN(ENET_RX_EN), ENET_RX_ER to ENET_CLK setup	2	—	ns
M21	ENET_CLK to ENET_RX_DATAD[1:0], ENET_RX_EN, ENET_RX_ER hold	2	—	ns

4.9.5 Flexible Controller Area Network (FLEXCAN) AC electrical specifications

Please refer to Section 4.3.2.1, “General purpose I/O AC parameters.

4.9.6 LPUART electrical specifications

Please refer to Section 4.3.2.1, “General purpose I/O AC parameters.

Table 71. Boot trough NOR

GPIO_EMC_34	semc.DATA[12]	ALT 0	—
GPIO_EMC_35	semc.DATA[13]	ALT 0	—
GPIO_EMC_36	semc.DATA[14]	ALT 0	—
GPIO_EMC_37	semc.DATA[15]	ALT 0	—
GPIO_EMC_09	semc.ADDR[0]	ALT 0	—
GPIO_EMC_10	semc.ADDR[1]	ALT 0	—
GPIO_EMC_11	semc.ADDR[2]	ALT 0	—
GPIO_EMC_12	semc.ADDR[3]	ALT 0	—
GPIO_EMC_13	semc.ADDR[4]	ALT 0	—
GPIO_EMC_14	semc.ADDR[5]	ALT 0	—
GPIO_EMC_15	semc.ADDR[6]	ALT 0	—
GPIO_EMC_16	semc.ADDR[7]	ALT 0	—
GPIO_EMC_19	semc.ADDR[11]	ALT 0	—
GPIO_EMC_20	semc.ADDR[12]	ALT 0	—
GPIO_EMC_21	semc.BA0	ALT 0	—
GPIO_EMC_22	semc.BA1	ALT 0	—
GPIO_EMC_41	semc.CSX[0]	ALT 0	—

Table 72. Boot through FlexSPI

PAD Name	IO Function	Mux Mode	Comments
GPIO_SD_B1_00	flexspi.B_DATA[3]	ALT 1	—
GPIO_SD_B1_01	flexspi.B_DATA[2]	ALT 1	—
GPIO_SD_B1_02	flexspi.B_DATA[1]	ALT 1	—
GPIO_SD_B1_03	flexspi.B_DATA[0]	ALT 1	—
GPIO_SD_B1_04	flexspi.B_SCLK	ALT 1	—
GPIO_SD_B0_05	flexspi.B_DQS	ALT 4	—
GPIO_SD_B0_04	flexspi.B_SS0_B	ALT 4	—
GPIO_SD_B0_01	flexspi.B_SS1_B	ALT 6	—
GPIO_SD_B1_05	flexspi.A_DQS	ALT 1	—
GPIO_SD_B1_06	flexspi.A_SS0_B	ALT 1	—
GPIO_SD_B0_00	flexspi.A_SS1_B	ALT 6	—
GPIO_SD_B1_07	flexspi.A_SCLK	ALT 1	—
GPIO_SD_B1_08	flexspi.A_DATA[0]	ALT 1	—
GPIO_SD_B1_09	flexspi.A_DATA[1]	ALT 1	—

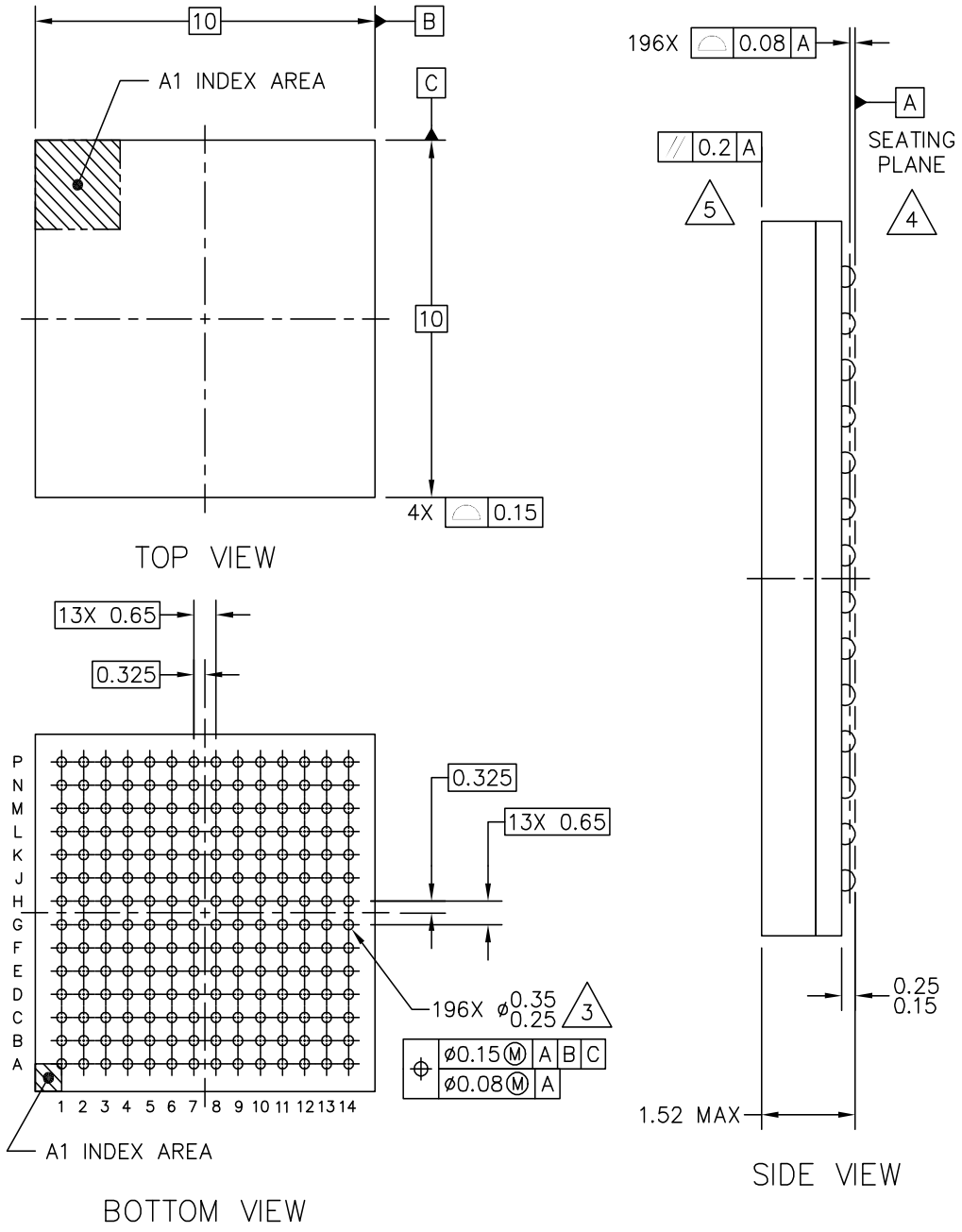
6 Package information and contact assignments

This section includes the contact assignment information and mechanical package drawing.

6.1 10 x 10 mm package information

6.1.1 10 x 10 mm, 0.65 mm pitch, ball matrix

Figure 48 shows the top, bottom, and side views of the 10 x 10 mm MAPBGA package.



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TITLE: PBGA, LOW PROFILE, FINE PITCH, 196 I/O, 10 X 10 PKG, 0.65 MM PITCH (MAP)	DOCUMENT NO: 98ASA00030D	REV: A
	STANDARD: NON-JEDEC	
	SOT1546-1	05 JAN 2016

Figure 48. 10 x 10 mm BGA, case x package top, bottom, and side Views

Table 82. 10 x 10 mm functional contact assignments (continued)

PMIC_STBY_REQ	L7	VDD_SNVS_IN	Digital GPIO	ALT0	CCM.PMIC_VSTBY_REQ	Output	100 K PU (PKE disabled)
POR_B	M7	VDD_SNVS_IN	Digital GPIO	ALT0	SRC.POR_B	Input	100 K PU
RTC_XTALI	N9	—	—	—	—	—	—
RTC_XTALO	P9	—	—	—	—	—	—
TEST_MODE	K6	VDD_SNVS_IN	Digital GPIO	ALT0	TCU.TEST_MODE	Input	100 K PU
USB_OTG1_CHD_B	N12	—	—	—	—	—	—
USB_OTG1_DN	M8	—	—	—	—	—	—
USB_OTG1_DP	L8	—	—	—	—	—	—
USB_OTG1_VBUS	N6	—	—	—	—	—	—
USB_OTG2_DN	N7	—	—	—	—	—	—
USB_OTG2_DP	P7	—	—	—	—	—	—
USB_OTG2_VBUS	P6	—	—	—	—	—	—
XTALI	P11	—	—	—	—	—	—
XTALO	N11	—	—	—	—	—	—
WAKEUP	L6	VDD_SNVS_IN	Digital GPIO	ALT5	GPIO5.IO[0]	Input	100 K PU

6.1.3 10 x 10 mm, 0.65 mm pitch, ball map

Table 83 shows the 10 x 10 mm, 0.65 mm pitch ball map for the i.MX RT1050.

Table 83. 10 x 10 mm, 0.65 mm pitch, ball map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	VSS	GPIO_EMC_27	GPIO_EMC_20	GPIO_EMC_17	GPIO_EMC_16	GPIO_EMC_13	GPIO_EMC_40	GPIO_B0_06	GPIO_B0_07	GPIO_B0_11	GPIO_B1_00	GPIO_B1_08	GPIO_B1_09	VSS	A
B	GPIO_EMC_15	GPIO_EMC_18	GPIO_EMC_26	GPIO_EMC_19	VSS	GPIO_EMC_14	GPIO_EMC_39	GPIO_B0_05	GPIO_B0_08	VSS	GPIO_B1_01	GPIO_B1_07	GPIO_B1_10	GPIO_B1_15	B
C	GPIO_EMC_21	GPIO_EMC_09	GPIO_EMC_36	GPIO_EMC_33	GPIO_EMC_31	GPIO_EMC_30	GPIO_EMC_41	GPIO_B0_04	GPIO_B0_09	GPIO_B0_12	GPIO_B1_02	GPIO_B1_06	GPIO_B1_11	GPIO_B1_14	C
D	GPIO_EMC_28	GPIO_EMC_25	GPIO_EMC_24	GPIO_EMC_34	GPIO_EMC_32	GPIO_EMC_38	GPIO_B0_00	GPIO_B0_03	GPIO_B0_10	GPIO_B0_13	GPIO_B1_03	GPIO_B1_05	GPIO_B1_12	GPIO_B1_13	D
E	GPIO_EMC_29	VSS	GPIO_EMC_00	GPIO_EMC_37	GPIO_EMC_35	NVCC_EMC	GPIO_B0_01	GPIO_B0_02	NVCC_GPIO	GPIO_B0_14	GPIO_B0_15	GPIO_B1_04	VSS	GPIO_AD_B0_06	E
F	GPIO_EMC_22	GPIO_EMC_04	GPIO_EMC_01	GPIO_EMC_02	NVCC_EMC	VDD_SOC_IN	VDD_SOC_IN	VDD_SOC_IN	VDD_SOC_IN	NVCC_GPIO	GPIO_AD_B0_04	GPIO_AD_B0_07	GPIO_AD_B0_08	GPIO_AD_B0_09	F
G	GPIO_EMC_10	GPIO_EMC_23	GPIO_EMC_11	GPIO_EMC_03	GPIO_EMC_05	VDD_SOC_IN	VSS	VSS	VDD_SOC_IN	GPIO_AD_B0_11	GPIO_AD_B0_03	GPIO_AD_B1_14	GPIO_AD_B0_10	GPIO_AD_B0_05	G