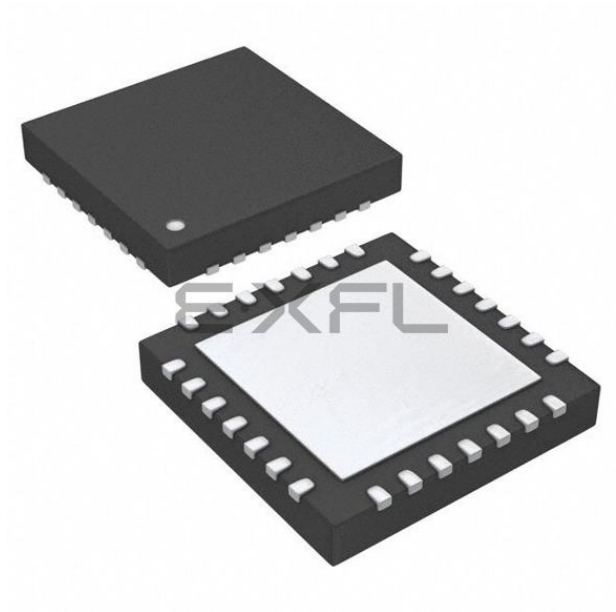

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 64MHz |
| Connectivity | I²C, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, LVD, POR, PWM, WDT |
| Number of I/O | 25 |
| Program Memory Size | 64KB (32K x 16) |
| Program Memory Type | FLASH |
| EEPROM Size | 1K x 8 |
| RAM Size | 3.6K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.3V ~ 5.5V |
| Data Converters | A/D 24x10b; D/A 1x5b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-VQFN Exposed Pad |
| Supplier Device Package | 28-QFN (6x6) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic18f26k40-i-ml |

## PIC18(L)F2x/4xK40 Family Types

| Device | Data Sheet Index | Program Memory Flash (bytes) | Data SRAM (bytes) | Data EEPROM (bytes) | I/O Pins | 16-bit Timers | Comparators | 10-bit ADC$^2$ with Computation (ch) | 5-bit DAC | Zero-Cross Detect | CCP/10-bit PWM | CWG | 8-bit TMR with HLT | Windowed Watchdog Timer | CRC with Memory Scan | EUSART | I$^2$C/SPI | PPS | Peripheral Module Disable | Temperature Indicator | Debug(1) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PIC18(L)F24K40 | **(1)** | 16k | 1024 | 256 | 25 | 4 | 2 | 24 | 1 | 1 | 2/2 | 1 | 3 | Y | Y | 1 | 1 | Y | Y | Y | I |
| PIC18(L)F25K40 | **(1)** | 32k | 2048 | 256 | 25 | 4 | 2 | 24 | 1 | 1 | 2/2 | 1 | 3 | Y | Y | 1 | 1 | Y | Y | Y | I |
| PIC18(L)F26K40 | **(2)** | 64k | 3728 | 1024 | 25 | 4 | 2 | 24 | 1 | 1 | 2/2 | 1 | 3 | Y | Y | 2 | 2 | Y | Y | Y | I |
| PIC18(L)F27K40 | **(3)** | 128k | 3728 | 1024 | 25 | 4 | 2 | 24 | 1 | 1 | 2/2 | 1 | 3 | Y | Y | 2 | 2 | Y | Y | Y | I |
| PIC18(L)F45K40 | **(2)** | 32k | 2048 | 256 | 36 | 4 | 2 | 35 | 1 | 1 | 2/2 | 1 | 3 | Y | Y | 2 | 2 | Y | Y | Y | I |
| PIC18(L)F46K40 | **(2)** | 64k | 3728 | 1024 | 36 | 4 | 2 | 35 | 1 | 1 | 2/2 | 1 | 3 | Y | Y | 2 | 2 | Y | Y | Y | I |
| PIC18(L)F47K40 | **(3)** | 128k | 3728 | 1024 | 36 | 4 | 2 | 35 | 1 | 1 | 2/2 | 1 | 3 | Y | Y | 2 | 2 | Y | Y | Y | I |

**Note 1:** Debugging Methods: (I) – Integrated on Chip.

**Data Sheet Index:** (Unshaded devices are described in this document.)

1. DS40001843 PIC18(L)F24/25K40 Data Sheet, 28-Pin, 8-bit Flash Microcontrollers
2. DS40001816 PIC18(L)F26/45/46K40 Data Sheet, 28/40/44-Pin, 8-bit Flash Microcontrollers
3. DS40001844 PIC18(L)F27/47K40 Data Sheet, 28/40/44-Pin, 8-bit Flash Microcontrollers

**Note:** For other small form-factor package availability and marking information, please visit **http://www.microchip.com/packaging** or contact your local sales office.

## Pin Allocation Tables

### TABLE 1: 28-PIN ALLOCATION TABLE (PIC18(L)F26K40)

| I/O(2) | 28-Pin SPDIP, SOIC, SSOP | 28-Pin (U)QFN | A/D | Reference | Comparator | Timers | CCP | CWG | ZCD | Interrupt | EUSART | DSM | MSSP | Pull-up | Basic |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RA0 | 2 | 27 | ANA0 | — | C1IN0-<br>C2IN0- | — | — | — | — | IOCA0 | — | — | — | Y | — |
| RA1 | 3 | 28 | ANA1 | — | C1IN1-<br>C2IN1- | — | — | — | — | IOCA1 | — | — | — | Y | — |
| RA2 | 4 | 1 | ANA2 | DAC1OUT1<br>VREF- (DAC)<br>VREF- (ADC) | C1IN0+<br>C2IN0+ | — | — | — | — | IOCA2 | — | — | — | Y | — |
| RA3 | 5 | 2 | ANA3 | VREF+ (DAC)<br>VREF+ (ADC) | C1IN1+ | — | — | — | — | IOCA3 | — | MDCIN1(1) | — | Y | — |
| RA4 | 6 | 3 | ANA4 | — | — | T0CKI(1) | — | — | — | IOCA4 | — | MDCIN2(1) | — | Y | — |
| RA5 | 7 | 4 | ANA5 | — | — | — | — | — | — | IOCA5 | — | MDMIN(1) | $\overline{SS1}$(1) | Y | — |
| RA6 | 10 | 7 | ANA6 | — | — | — | — | — | — | IOCA6 | — | — | — | Y | CLKOUT<br>OSC2 |
| RA7 | 9 | 6 | ANA7 | — | — | — | — | — | — | IOCA7 | — | — | — | Y | OSC1<br>CLKIN |
| RB0 | 21 | 18 | ANB0 | — | C2IN1+ | — | — | CWG1(1) | ZCDIN | IOCB0<br>INT0(1) | — | — | $\overline{SS2}$(1) | Y | — |
| RB1 | 22 | 19 | ANB1 | — | C1IN3-<br>C2IN3- | — | — | — | — | IOCB1<br>INT1(1) | — | — | SCK2(1)<br>SCL2(3,4) | Y | — |
| RB2 | 23 | 20 | ANB2 | — | — | — | — | — | — | IOCB2<br>INT2(1) | — | — | SDI2(1)<br>SDA2(3,4) | Y | — |
| RB3 | 24 | 21 | ANB3 | — | C1IN2-<br>C2IN2- | — | — | — | — | IOCB3 | — | — | — | Y | — |
| RB4 | 25 | 22 | ANB4 | — | — | T5G(1) | — | — | — | IOCB4 | — | — | — | Y | — |
| RB5 | 26 | 23 | ANB5 | — | — | T1G(1) | — | — | — | IOCB5 | — | — | — | Y | — |
| RB6 | 27 | 24 | ANB6 | — | — | — | — | — | — | IOCB6 | CK2(1) | — | — | Y | ICSPCLK |
| RB7 | 28 | 25 | ANB7 | DAC1OUT2 | — | T6AIN(1) | — | — | — | IOCB7 | RX2/DT2(1) | — | — | Y | ICSPDAT |

**Note 1:** Default peripheral input. Input can be moved to any other pin with the PPS input selection registers (Register 17-1).

**2:** All pin outputs default to PORT latch data. Any pin can be selected as a peripheral digital output with the PPS output selection registers.

**3:** These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

**4:** These pins are configured for $I^2C$ logic levels; The SCLx/SDAx signals may be assigned to any of these pins. PPS assignments to the other pins (e.g., RB1) will operate, but input logic levels will be standard TTL/ST as selected by the INLVL register, instead of the $I^2C$ specific or SMBus input buffer thresholds.

**TABLE 2: 40/44-PIN ALLOCATION TABLE (PIC18(L)F45/46K40)**

| I/O(2) | 40-Pin PDIP | 40-Pin UQFN | 44-Pin QFN | 44-Pin TQFP | A/D | Reference | Comparator | Timers | CCP | CWG | ZCD | Interrupt | EUSART | DSM | MSSP | Pull-up | Basic |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RA0 | 2 | 17 | 19 | 19 | ANA0 | — | C1INO-<br>C2IN0- | — | — | — | — | IOCA0 | — | — | — | Y | — |
| RA1 | 3 | 18 | 20 | 20 | ANA1 | — | C1IN1-<br>C2IN1- | — | — | — | — | IOCA1 | — | — | — | Y | — |
| RA2 | 4 | 19 | 21 | 21 | ANA2 | DAC1OUT1<br>VREF- (DAC5)<br>VREF- (ADC) | C1IN0+<br>C2IN0+ | — | — | — | — | IOCA2 | — | — | — | Y | — |
| RA3 | 5 | 20 | 22 | 22 | ANA3 | VREF+ (DAC5)<br>VREF+ (ADC) | C1IN1+ | — | — | — | — | IOCA3 | — | MDCIN1(1) | — | Y | — |
| RA4 | 6 | 21 | 23 | 23 | ANA4 | — | — | T0CKI(1) | — | — | — | IOCA4 | — | MDCIN2(1) | — | Y | — |
| RA5 | 7 | 22 | 24 | 24 | ANA5 | — | — | — | — | — | — | IOCA5 | — | MDMIN(1) | $\overline{SS1}$(1) | Y | — |
| RA6 | 14 | 29 | 33 | 31 | ANA6 | — | — | — | — | — | — | IOCA6 | — | — | — | Y | CLKOUT<br>OSC2 |
| RA7 | 13 | 28 | 32 | 30 | ANA7 | — | — | — | — | — | — | IOCA7 | — | — | — | Y | OSC1<br>CLKIN |
| RB0 | 33 | 8 | 9 | 8 | ANB0 | — | C2IN1+ | — | — | CWG1(1) | ZCDIN | IOCB0<br>INT0(1) | — | — | $\overline{SS2}$(1) | Y | — |
| RB1 | 34 | 9 | 10 | 9 | ANB1 | — | C1IN3-<br>C2IN3- | — | — | — | — | IOCB1<br>INT1(1) | — | — | SCK2(1)<br>SCL2(3,4) | Y | — |
| RB2 | 35 | 10 | 11 | 10 | ANB2 | — | — | — | — | — | — | IOCB2<br>INT2(1) | — | — | SDI2(1)<br>SDA2(3,4) | Y | — |
| RB3 | 36 | 11 | 12 | 11 | ANB3 | — | C1IN2-<br>C2IN2- | — | — | — | — | IOCB3 | — | — | — | Y | — |
| RB4 | 37 | 12 | 14 | 14 | ANB4 | — | — | T5G(1) | — | — | — | IOCB4 | — | — | — | Y | — |
| RB5 | 38 | 13 | 15 | 15 | ANB5 | — | — | T1G(1) | — | — | — | IOCB5 | — | — | — | Y | — |
| RB6 | 39 | 14 | 16 | 16 | ANB6 | — | — | — | — | — | — | IOCB6 | CK2(1) | — | — | Y | ICSPCLK |
| RB7 | 40 | 15 | 17 | 17 | ANB7 | DAC1OUT2 | — | T6AIN(1) | — | — | — | IOCB7 | RX2/DT2(1) | — | — | Y | ICSPDAT |
| RC0 | 15 | 30 | 34 | 32 | ANC0 | — | — | T1CKI(1)<br>T3CKI(1)<br>T3G(1) | — | — | — | IOCC0 | — | — | — | Y | SOSCO |
| RC1 | 16 | 31 | 35 | 35 | ANC1 | — | — | — | CCP2(1) | — | — | IOCC1 | — | — | — | Y | SOSCIN<br>SOSCI |

**Note 1:** Default peripheral input. Input can be moved to any other pin with the PPS input selection registers (Register 17-1).

**2:** All pin outputs default to PORT latch data. Any pin can be selected as a peripheral digital output with the PPS output selection registers.

**3:** These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

**4:** These pins are configured for I2C logic levels; The SCLx/SDAx signals may be assigned to any of these pins. PPS assignments to the other pins (e.g., RB1) will operate, but input logic levels will be standard TTL/ST as selected by the INLVL register, instead of the I2C specific or SMBus input buffer thresholds.

# 4.0 OSCILLATOR MODULE (WITH FAIL-SAFE CLOCK MONITOR)

## 4.1 Overview

The oscillator module has multiple clock sources and selection features that allow it to be used in a wide range of applications while maximizing performance and minimizing power consumption. Figure 4-1 illustrates a block diagram of the oscillator module.

Clock sources can be supplied from external oscillators, quartz-crystal resonators and ceramic resonators. In addition, the system clock source can be supplied from one of two internal oscillators and PLL circuits, with a choice of speeds selectable via software. Additional clock features include:

- Selectable system clock source between external or internal sources via software.
- Fail-Safe Clock Monitor (FSCM) designed to detect a failure of the external clock source (LP, XT, HS, ECH, ECM, ECL) and switch automatically to the internal oscillator.
- Oscillator Start-up Timer (OST) ensures stability of crystal oscillator sources.

The RSTOSC bits of Configuration Word 1 (Register 3-1) determine the type of oscillator that will be used when the device runs after Reset, including when it is first powered up.

If an external clock source is selected, the FEXTOSC bits of Configuration Word 1 must be used in conjunction with the RSTOSC bits to select the External Clock mode.

The external oscillator module can be configured in one of the following clock modes, by setting the FEXTOSC<2:0> bits of Configuration Word 1:

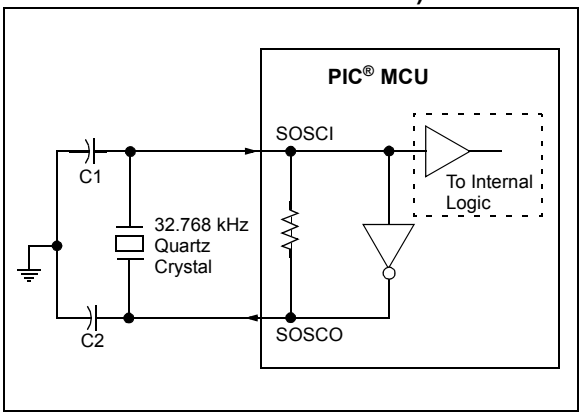
1. ECL – External Clock Low-Power mode (below 100 kHz)
2. ECM – External Clock Medium Power mode (100 kHz to 8 MHz)
3. ECH – External Clock High-Power mode (above 8 MHz)
4. LP – 32 kHz Low-Power Crystal mode.
5. XT – Medium Gain Crystal or Ceramic Resonator Oscillator mode (between 100 kHz and 8 MHz)
6. HS – High Gain Crystal or Ceramic Resonator mode (above 4 MHz)

The ECH, ECM, and ECL Clock modes rely on an external logic level signal as the device clock source. The LP, XT, and HS Clock modes require an external crystal or resonator to be connected to the device. Each mode is optimized for a different frequency range. The internal oscillator block produces low and high-frequency clock sources, designated LFINTOSC and HFINTOSC. (see Internal Oscillator Block, Figure 4-1). Multiple device clock frequencies may be derived from these clock sources.

#### 4.3.1.5 Secondary Oscillator

The secondary oscillator is a separate oscillator block that can be used as an alternate system clock source. The secondary oscillator is optimized for 32.768 kHz, and can be used with an external crystal oscillator connected to the SOSCI and SOSCO device pins, or an external clock source connected to the SOSCIN pin. The secondary oscillator can be selected during run-time using clock switching. Refer to **Section 4.4 "Clock Switching"** for more information.

**FIGURE 4-5: QUARTZ CRYSTAL OPERATION (SECONDARY OSCILLATOR)**




**Note 1:** Quartz crystal characteristics vary according to type, package and manufacturer. The user should consult the manufacturer data sheets for specifications and recommended application.

**2:** Always verify oscillator performance over the $V_{DD}$ and temperature range that is expected for the application.

**3:** For oscillator design assistance, reference the following Microchip Application Notes:

- AN826, "*Crystal Oscillator Basics and Crystal Selection for PIC® and PIC® Devices*" (DS00826)
- AN849, "*Basic PIC® Oscillator Design*" (DS00849)
- AN943, "*Practical PIC® Oscillator Analysis and Design*" (DS00943)
- AN949, "*Making Your Oscillator Work*" (DS00949)
- TB097, "*Interfacing a Micro Crystal MS1V-T1K 32.768 kHz Tuning Fork Crystal to a PIC16F690/SS*" (DS91097)
- AN1288, "*Design Practices for Low-Power External Oscillators*" (DS01288)

### 4.3.2 INTERNAL CLOCK SOURCES

The device may be configured to use the internal oscillator block as the system clock by performing one of the following actions:

- Program the RSTOSC<2:0> bits in Configuration Words to select the INTOSC clock source, which will be used as the default system clock upon a device Reset.
- Write the NOSC<2:0> bits in the OSCCON1 register to switch the system clock source to the internal oscillator during run-time. See **Section 4.4 "Clock Switching"** for more information.

In INTOSC mode, OSC1/CLKIN is available for general purpose I/O. OSC2/CLKOUT is available for general purpose I/O or CLKOUT.

The function of the OSC2/CLKOUT pin is determined by the $\overline{\text{CLKOUTEN}}$ bit in Configuration Words.

The internal oscillator block has two independent oscillators that can produce two internal system clock sources.

1. The **HFINTOSC** (High-Frequency Internal Oscillator) is factory-calibrated and operates from 1 to 64 MHz. The frequency of HFINTOSC can be selected through the OSCFRQ Frequency Selection register, and fine-tuning can be done via the OSCTUNE register.
2. The **LFINTOSC** (Low-Frequency Internal Oscillator) is factory-calibrated and operates at 31 kHz.

**FIGURE 5-2: CLOCK REFERENCE TIMING**

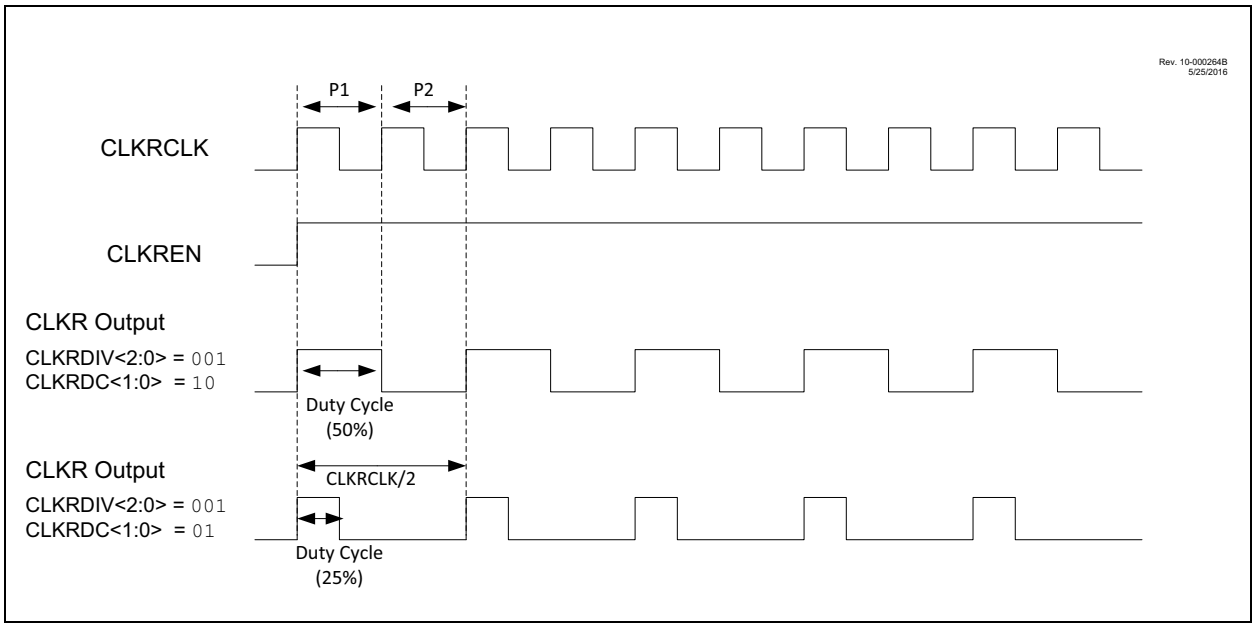
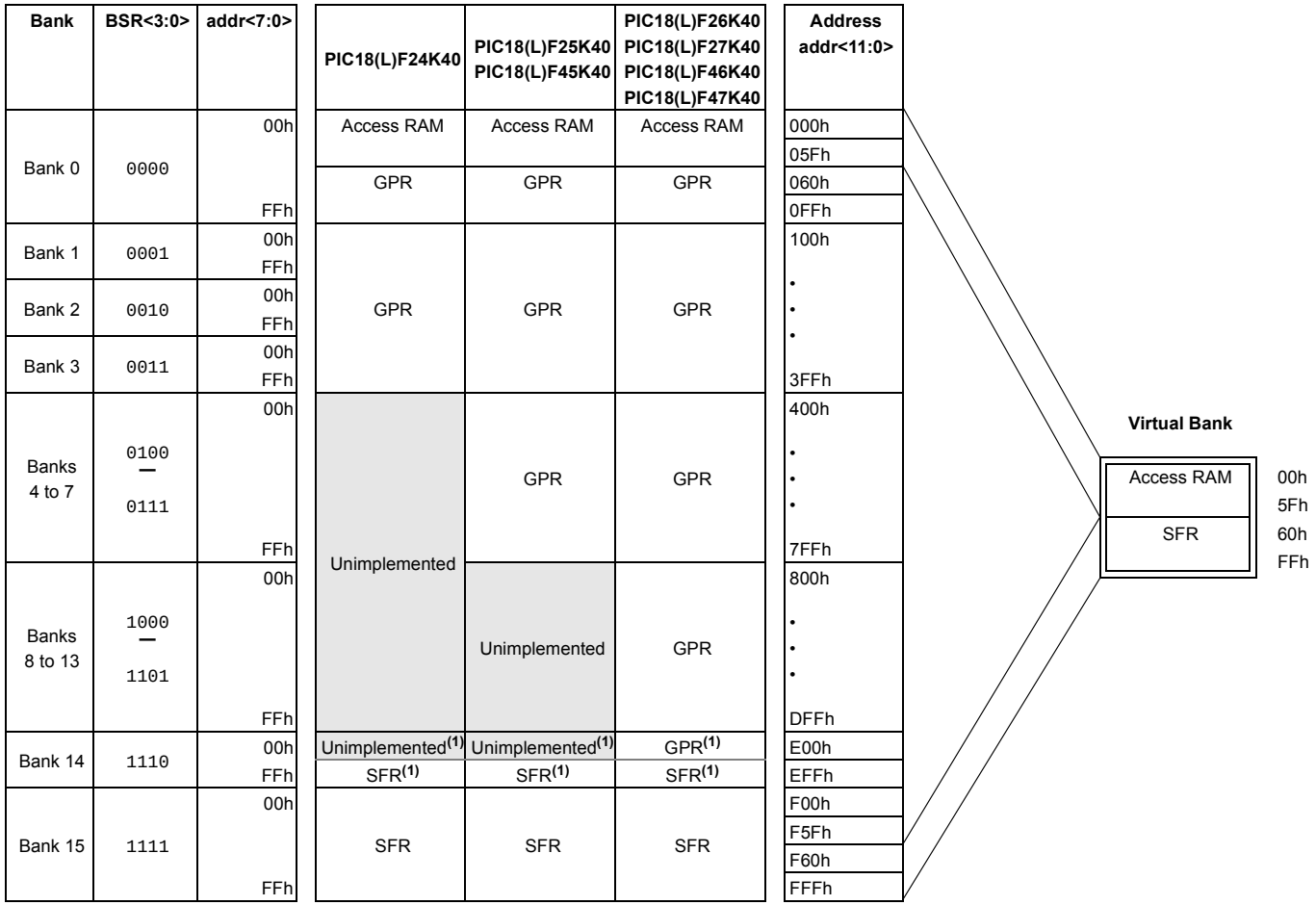


**FIGURE 10-4: DATA MEMORY MAP FOR PIC18(L)F2X/4XK40 DEVICES**




**Note 1:** It depends on the number of SFRs. Refer to Table 10-3 and Table 10-4.

### 10.4.5 STATUS REGISTER

The STATUS register, shown in Register 10-2, contains the arithmetic status of the ALU. As with any other SFR, it can be the operand for any instruction.

If the STATUS register is the destination for an instruction that affects the Z, DC, C, OV or N bits, the results of the instruction are not written; instead, the STATUS register is updated according to the instruction performed. Therefore, the result of an instruction with the STATUS register as its destination may be different than intended. As an example, `CLRF STATUS` will set the Z bit and leave the remaining Status bits unchanged (‘`000u u1uu`’).

It is recommended that only `BCF`, `BSF`, `SWAPF`, `MOVFF` and `MOVWF` instructions are used to alter the STATUS register, because these instructions do not affect the Z, C, DC, OV or N bits in the STATUS register.

For other instructions that do not affect Status bits, see the instruction set summaries in **Section 35.0 “Instruction Set Summary”** and Table 35-3.

| **Note:** | The C and DC bits operate as the borrow and digit borrow bits, respectively, in subtraction. |
|---|---|

**REGISTER 13-11: SCANCON0: SCANNER ACCESS CONTROL REGISTER 0**

| R/W-0/0 | R/W/HC-0/0 | R-0 | R-1 | R/W-0/0 | U-0 | R/W-0/0 | R/W-0/0 |
|---|---|---|---|---|---|---|---|
| SCANEN | SCANGO | BUSY | INVALID | INTM | — | MODE<1:0> | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| '1' = Bit is set | '0' = Bit is cleared | HC = Bit is cleared by hardware |

bit 7 **SCANEN:** Scanner Enable bit(1)
1 = Scanner is enabled
0 = Scanner is disabled, internal states are reset

bit 6 **SCANGO:** Scanner GO bit(2, 3)
1 = When the CRC sends a ready signal, NVM will be accessed according to MDx and data passed to the client peripheral.
0 = Scanner operations will not occur

bit 5 **BUSY:** Scanner Busy Indicator bit(4)
1 = Scanner cycle is in process
0 = Scanner cycle is complete (or never started)

bit 4 **INVALID:** Scanner Abort Signal bit
1 = SCANLADRL/H/U has incremented to an invalid address(6) or the scanner was not setup correctly(7)
0 = SCANLADRL/H/U points to a valid address

bit 3 **INTM:** NVM Scanner Interrupt Management Mode Select bit
If MODE = 10:
This bit is ignored
If MODE = 01 (CPU is stalled until all data is transferred):
1 = SCANGO is overridden (to zero) during interrupt operation; scanner resumes after returning from interrupt
0 = SCANGO is not affected by interrupts, the interrupt response will be affected
If MODE = 00 or 11:
1 = SCANGO is overridden (to zero) during interrupt operation; scan operations resume after returning from interrupt
0 = Interrupts do not prevent NVM access

bit 2 **Unimplemented:** Read as '0'

bit 1-0 **MODE<1:0>:** Memory Access Mode bits(5)
11 = Triggered mode
10 = Peek mode
01 = Burst mode
00 = Concurrent mode

**Note 1:** Setting SCANEN = 0 (SCANCON0 register) does not affect any other register content.
**2:** This bit is cleared when LADR > HADR (and a data cycle is not occurring).
**3:** If INTM = 1, this bit is overridden (to zero, but not cleared) during an interrupt response.
**4:** BUSY = 1 when the NVM is being accessed, or when the CRC sends a ready signal.
**5:** See Table 13-2 for more detailed information.
**6:** An invalid address can occur when the entire range of PFM is scanned and the value of LADR rolls over. An invalid address can also occur if the value in the Scan Low address registers points to a location that is not mapped in the memory map of the device.
**7:** CRCEN and CRCGO bits must be set before setting SCANGO bit. Refer to **Section 13.9 "Program Memory Scan Configuration"**.

**REGISTER 15-3: LATx: LATx REGISTER(1)**

| R/W-x/u | R/W-x/u | R/W-x/u | R/W-x/u | R/W-x/u | R/W-x/u | R/W-x/u | R/W-x/u |
|---|---|---|---|---|---|---|---|
| LATx7 | LATx6 | LATx5 | LATx4 | LATx3 | LATx2 | LATx1 | LATx0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |
| -n/n = Value at POR and BOR/Value at all other Resets | | |

bit 7-0 **LATx<7:0>:** Rx7:Rx0 Output Latch Value bits

**Note 1:** Writes to LATx are equivalent with writes to the corresponding PORTx register. Reads from LATx register return register values, not I/O pin values.

**TABLE 15-4: LAT REGISTERS**

| Name | Device | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| | 28 Pins | 40/44 Pins | | | | | | | | |
| LATA | X | X | LATA7 | LATA6 | LATA5 | LATA4 | LATA3 | LATA2 | LATA1 | LATA0 |
| LATB | X | X | LATB7 | LATB6 | LATB5 | LATB4 | LATB3 | LATB2 | LATB1 | LATB0 |
| LATC | X | X | LATC7 | LATC6 | LATC5 | LATC4 | LATC3 | LATC2 | LATC1 | LATC0 |
| LATD | X | | — | — | — | — | — | — | — | — |
| | | X | LATD7 | LATD6 | LATD5 | LATD4 | LATD3 | LATD2 | LATD1 | LATD0 |
| LATE | X | | — | — | — | — | — | — | — | — |
| | | X | — | — | — | — | — | LATE2 | LATE1 | LATE0 |

**REGISTER 15-4: ANSELx: ANALOG SELECT REGISTER**

| R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 |
|---|---|---|---|---|---|---|---|
| ANSELx7 | ANSELx6 | ANSELx5 | ANSELx4 | ANSELx3 | ANSELx2 | ANSELx1 | ANSELx0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |
| -n/n = Value at POR and BOR/Value at all other Resets | | |

bit 7-0 **ANSELx<7:0>**: Analog Select on Pins Rx<7:0>

1 = Digital Input buffers are disabled.

0 = ST and TTL input devices are enabled

**TABLE 15-5: ANALOG SELECT PORT REGISTERS**

| Name | Device | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| | 28 Pins | 40/44 Pins | | | | | | | | |
| ANSELA | X | X | ANSELA7 | ANSELA6 | ANSELA5 | ANSELA4 | ANSELA3 | ANSELA2 | ANSELA1 | ANSELA0 |
| ANSELB | X | X | ANSELB7 | ANSELB6 | ANSELB5 | ANSELB4 | ANSELB3 | ANSELB2 | ANSELB1 | ANSELB0 |
| ANSELC | X | X | ANSELC7 | ANSELC6 | ANSELC5 | ANSELC4 | ANSELC3 | ANSELC2 | ANSELC1 | ANSELC0 |
| ANSELD | X | | — | — | — | — | — | — | — | — |
| | | X | ANSELD7 | ANSELD6 | ANSELD5 | ANSELD4 | ANSELD3 | ANSELD2 | ANSELD1 | ANSELD0 |
| ANSELE | X | | — | — | — | — | — | — | — | — |
| | | X | — | — | — | — | — | ANSELE2 | ANSELE1 | ANSELE0 |

**TABLE 16-1: IOC REGISTERS**

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| IOCAP | IOCAP7 | IOCAP6 | IOCAP5 | IOCAP4 | IOCAP3 | IOCAP2 | IOCAP1 | IOCAP0 |
| IOCAN | IOCAN7 | IOCAN6 | IOCAN5 | IOCAN4 | IOCAN3 | IOCAN2 | IOCAN1 | IOCAN0 |
| IOCAF | IOCAF7 | IOCAF6 | IOCAF5 | IOCAF4 | IOCAF3 | IOCAF2 | IOCAF1 | IOCAF0 |
| IOCBP | IOCBP7 | IOCBP6 | IOCBP5 | IOCBP4 | IOCBP3 | IOCBP2 | IOCBP1 | IOCBP0 |
| IOCBN | IOCBN7 | IOCBN6 | IOCBN5 | IOCBN4 | IOCBN3 | IOCBN2 | IOCBN1 | IOCBN0 |
| IOCBF | IOCBF7 | IOCBF6 | IOCBF5 | IOCBF4 | IOCBF3 | IOCBF2 | IOCBF1 | IOCBF0 |
| IOCCP | IOCCP7 | IOCCP6 | IOCCP5 | IOCCP4 | IOCCP3 | IOCCP2 | IOCCP1 | IOCCP0 |
| IOCCN | IOCCN7 | IOCCN6 | IOCCN5 | IOCCN4 | IOCCN3 | IOCCN2 | IOCCN1 | IOCCN0 |
| IOCCF | IOCCF7 | IOCCF6 | IOCCF5 | IOCCF4 | IOCCF3 | IOCCF2 | IOCCF1 | IOCCF0 |
| IOCEP | — | — | — | — | IOCEP3(1) | — | — | — |
| IOCEN | — | — | — | — | IOCEN3(1) | — | — | — |
| IOCEF | — | — | — | — | IOCEF3(1) | — | — | — |

**Note 1:** If MCLRE = 1 or LVP = 1, RE3 port functionality is disabled and IOC on RE3 is not available.

**TABLE 16-2: SUMMARY OF REGISTERS ASSOCIATED WITH INTERRUPT-ON-CHANGE**

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Register on Page |
|---|---|---|---|---|---|---|---|---|---|
| INTCON | GIE/GIEH | PEIE/GIEL | IPEN | — | — | INT2EDG | INT1EDG | INT0EDG | 170 |
| IOCxF | IOCxF7 | IOCxF6 | IOCxF5 | IOCxF4 | IOCxF3 | IOCxF2 | IOCxF1 | IOCxF0 | 211 |
| IOCxN | IOCxN7 | IOCxN6 | IOCxN5 | IOCxN4 | IOCxN3 | IOCxN2 | IOCxN1 | IOCxN0 | 211 |
| IOCxP | IOCxP7 | IOCxP6 | IOCxP5 | IOCxP4 | IOCxP3 | IOCxP2 | IOCxP1 | IOCxP0 | 211 |

**Legend:** — = unimplemented location, read as '0'. Shaded cells are not used by interrupt-on-change.

### 20.5.9 EDGE-TRIGGERED MONOSTABLE MODES

The Edge-Triggered Monostable modes start the timer on an edge from the external Reset signal input, after the ON bit is set, and stop incrementing the timer when the timer matches the PRx period value. The following edges will start the timer:

- Rising edge (MODE<4:0> = 10001)
- Falling edge (MODE<4:0> = 10010)
- Rising or Falling edge (MODE<4:0> = 10011)

When an Edge-Triggered Monostable mode is used in conjunction with the CCP PWM operation the PWM drive goes active with the external Reset signal edge that starts the timer, but will not go active when the timer matches the PRx value. While the timer is incrementing, additional edges on the external Reset signal will not affect the CCP PWM.

## 22.0 PULSE-WIDTH MODULATION (PWM )

The PWM module generates a Pulse-Width Modulated signal determined by the duty cycle, period, and resolution that are configured by the following registers:

- PRx
- TxCON
- PWMxDCH
- PWMxDCL
- PWMxCON

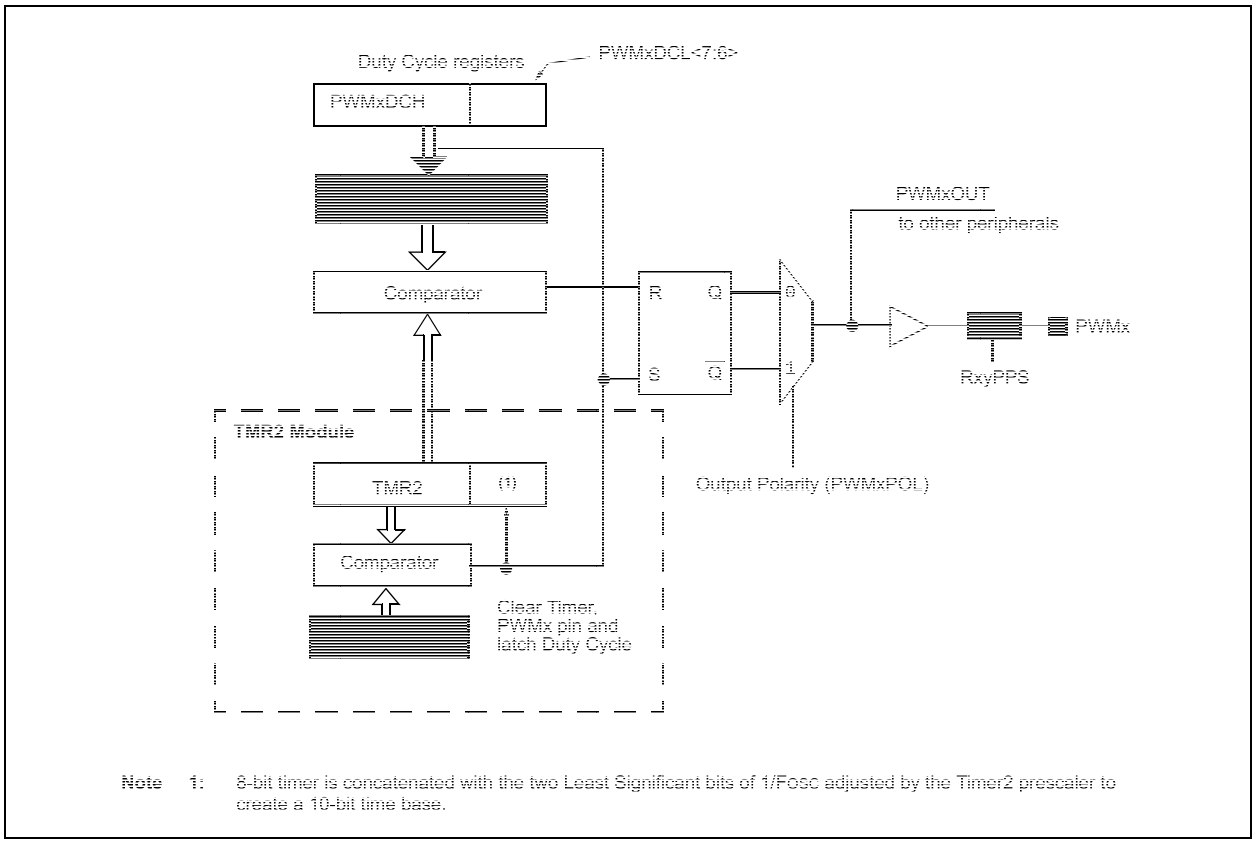
**Note:** The corresponding TRIS bit must be cleared to enable the PWM output on the PWMx pin.

Each PWM module can select the timer source that controls the module. Each module has an independent timer selection which can be accessed using the CCPTMRS register (Register 21-2). Please note that the PWM mode operation is described with respect to TMR2 in the following sections.

Figure 22-1 shows a simplified block diagram of PWM operation.

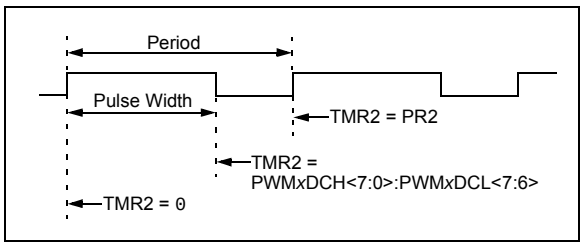
Figure 22-2 shows a typical waveform of the PWM signal.

**FIGURE 22-1: SIMPLIFIED PWM BLOCK DIAGRAM**




**Note** 1: 8-bit timer is concatenated with the two Least Significant bits of 1/Fosc adjusted by the Timer2 prescaler to create a 10-bit time base.

**FIGURE 22-2: PWM OUTPUT**




For a step-by-step procedure on how to set up this module for PWM operation, refer to **Section 22.1.9 "Setup for PWM Operation using PWMx Pins"**.

**REGISTER 22-2: CCPTMRS: CCP TIMERS CONTROL REGISTER**

| R/W-0/0 | R/W-1/1 | R/W-0/0 | R/W-1/1 | R/W-0/0 | R/W-1/1 | R/W-0/0 | R/W-1/1 |
|---|---|---|---|---|---|---|---|
| P4TSEL<1:0> | | P3TSEL<1:0> | | C2TSEL<1:0> | | C1TSEL<1:0> | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

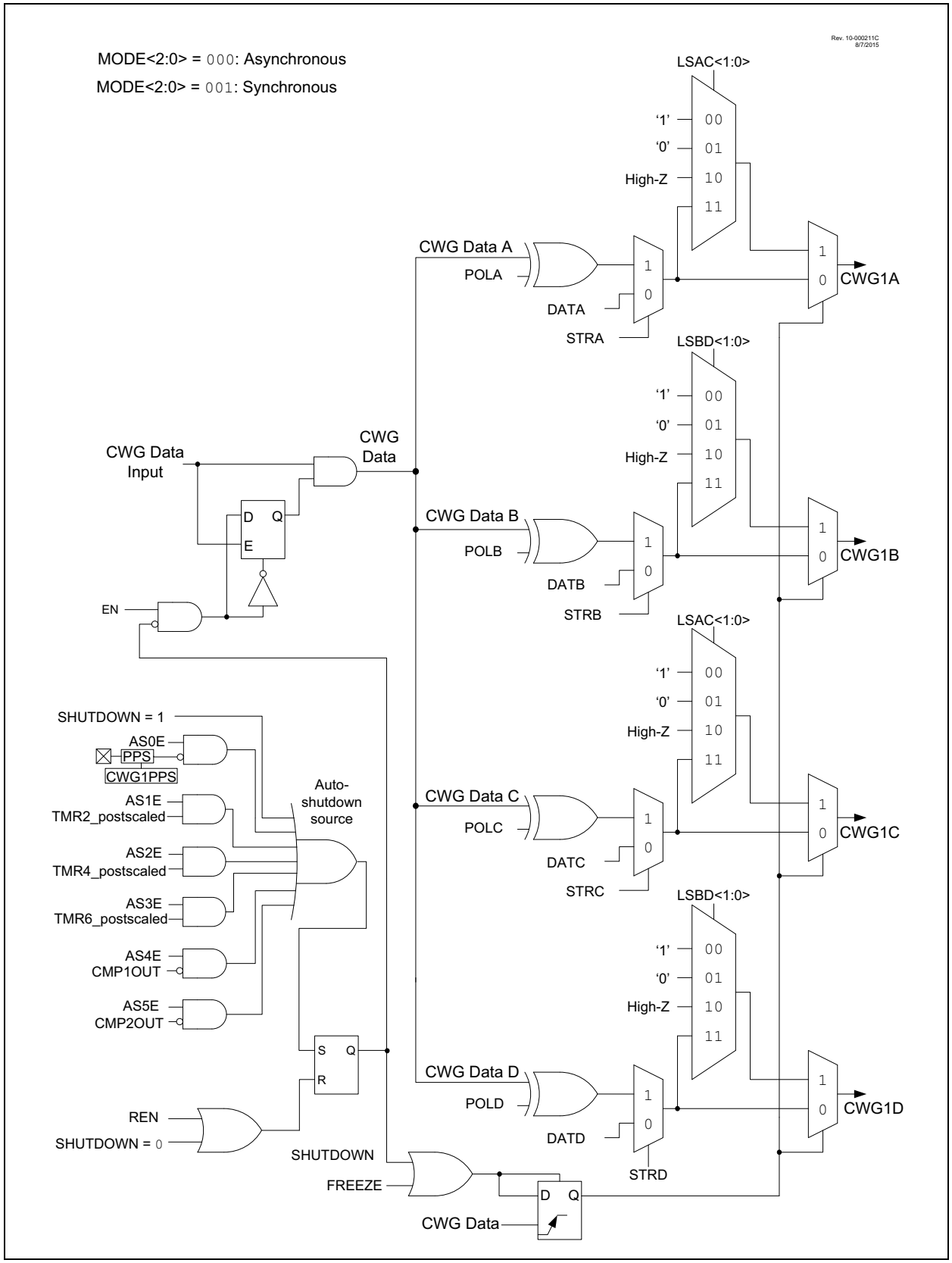
bit 7-6 **P4TSEL<1:0>:** PWM4 Timer Selection bits
11 = PWM4 based on TMR6
10 = PWM4 based on TMR4
01 = PWM4 based on TMR2
00 = Reserved

bit 5-4 **P3TSEL<1:0>:** PWM3 Timer Selection bits
11 = PWM3 based on TMR6
10 = PWM3 based on TMR4
01 = PWM3 based on TMR2
00 = Reserved

bit 3-2 **C2TSEL<1:0>:** CCP2 Timer Selection bits
11 = CCP2 is based off Timer5 in Capture/Compare mode and Timer6 in PWM mode
10 = CCP2 is based off Timer3 in Capture/Compare mode and Timer4 in PWM mode
01 = CCP2 is based off Timer1 in Capture/Compare mode and Timer2 in PWM mode
00 = Reserved

bit 1-0 **C1TSEL<1:0>:** CCP1 Timer Selection bits
11 = CCP1 is based off Timer5 in Capture/Compare mode and Timer6 in PWM mode
10 = CCP1 is based off Timer3 in Capture/Compare mode and Timer4 in PWM mode
01 = CCP1 is based off Timer1 in Capture/Compare mode and Timer2 in PWM mode
00 = Reserved

**FIGURE 24-11: SIMPLIFIED CWG BLOCK DIAGRAM (OUTPUT STEERING MODES)**



**REGISTER 25-2: MDCON1: MODULATION CONTROL REGISTER 1**

| U-0 | U-0 | R/W-0/0 | R/W-0/0 | U-0 | U-0 | R/W-0/0 | R/W-0/0 |
|---|---|---|---|---|---|---|---|
| — | — | CHPOL | CHSYNC | — | — | CLPOL | CLSYNC |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| ‘1’ = Bit is set | ‘0’ = Bit is cleared | |

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5 **CHPOL:** Modulator High Carrier Polarity Select bit
- 1 = Selected high carrier signal is inverted
- 0 = Selected high carrier signal is not inverted

bit 4 **CHSYNC:** Modulator High Carrier Synchronization Enable bit
- 1 = Modulator waits for a falling edge on the high time carrier signal before allowing a switch to the low time carrier
- 0 = Modulator output is not synchronized to the high time carrier signal(1)

bit 3-2 **Unimplemented:** Read as ‘0’

bit 1 **CLPOL:** Modulator Low Carrier Polarity Select bit
- 1 = Selected low carrier signal is inverted
- 0 = Selected low carrier signal is not inverted

bit 0 **CLSYNC:** Modulator Low Carrier Synchronization Enable bit
- 1 = Modulator waits for a falling edge on the low time carrier signal before allowing a switch to the high time carrier
- 0 = Modulator output is not synchronized to the low time carrier signal(1)

**Note 1:** Narrowed carrier pulse widths or spurs may occur in the signal stream if the carrier is not synchronized.

**REGISTER 31-32: ADACT: ADC AUTO CONVERSION TRIGGER CONTROL REGISTER**

| U-0 | U-0 | U-0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 |
|---|---|---|---|---|---|---|---|
| — | — | — | ADACT<4:0> | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| '1' = Bit is set | '0' = Bit is cleared | |

bit 7-5 **Unimplemented**: Read as '0'

bit 4-0 **ADACT<4:0>**: Auto-Conversion Trigger Select Bits
11111 = Software write to ADPCH
11110 = Reserved, do not use
11101 = Software read of ADRESH
11100 = Software read of ADERRH
11011 = Reserved, do not use
•
•
•
10000 = Reserved, do not use
01111 = Interrupt-on-change Interrupt Flag
01110 = C2_out
01101 = C1_out
01100 = PWM4_out
01011 = PWM3_out
01010 = CCP2_trigger
01001 = CCP1_trigger
01000 = TMR6_postscaled
00111 = TMR5_overflow
00110 = TMR4_postscaled
00101 = TMR3_overflow
00100 = TMR2_postscaled
00011 = TMR1_overflow
00010 = TMR0_overflow
00001 = Pin selected by ADACTPPS
00000 = External Trigger Disabled

### 35.1.1 STANDARD INSTRUCTION SET

**ADDLW** **ADD literal to W**

Syntax: ADDLW k

Operands: $0 \le k \le 255$

Operation: $(W) + k \rightarrow W$

Status Affected: N, OV, C, DC, Z

Encoding:

| 0000 | 1111 | kkkk | kkkk |
|---|---|---|---|

Description: The contents of W are added to the 8-bit literal 'k' and the result is placed in W.

Words: 1

Cycles: 1

Q Cycle Activity:

| Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|
| Decode | Read literal 'k' | Process Data | Write to W |

Example: `ADDLW 15h`

Before Instruction
W = 10h
After Instruction
W = 25h

**ADDWF** **ADD W to f**

Syntax: ADDWF f {,d {,a}}

Operands: $0 \le f \le 255$
$d \in [0,1]$
$a \in [0,1]$

Operation: $(W) + (f) \rightarrow dest$

Status Affected: N, OV, C, DC, Z

Encoding:

| 0010 | 01da | ffff | ffff |
|---|---|---|---|

Description: Add W to register 'f'. If 'd' is '0', the result is stored in W. If 'd' is '1', the result is stored back in register 'f' (default).
If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank.
If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See **Section 35.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode"** for details.

Words: 1

Cycles: 1

Q Cycle Activity:

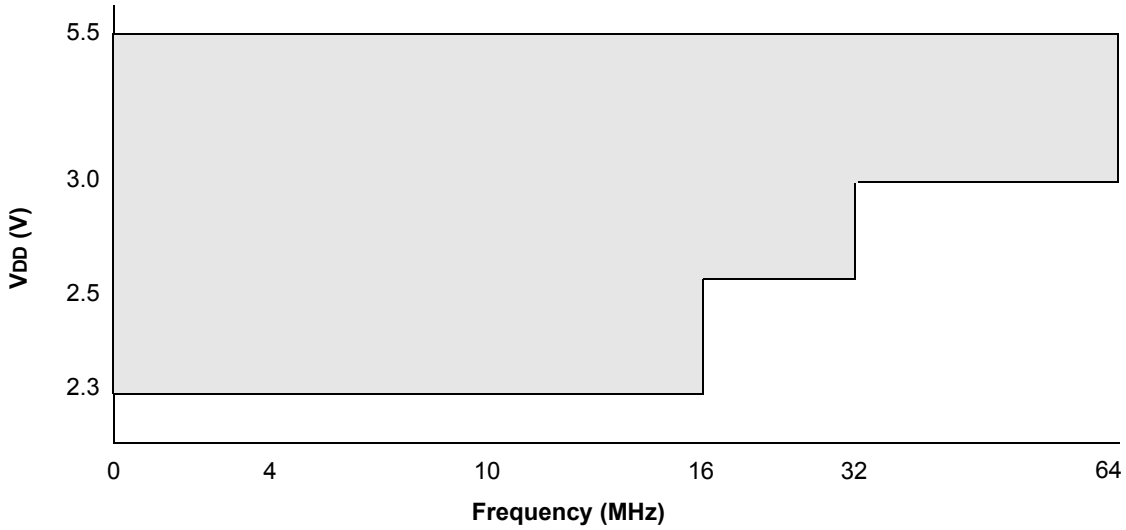
| Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|
| Decode | Read register 'f' | Process Data | Write to destination |

Example: `ADDWF REG, 0, 0`

Before Instruction
W = 17h
REG = 0C2h
After Instruction
W = 0D9h
REG = 0C2h

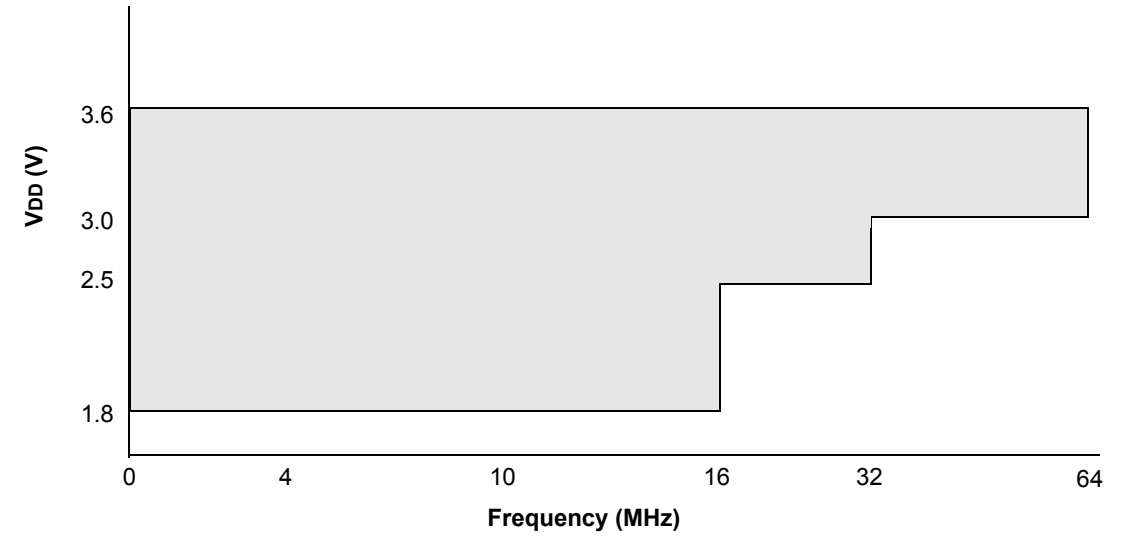
**Note:** All PIC18 instructions may take an optional label argument preceding the instruction mnemonic for use in symbolic addressing. If a label is used, the instruction format then becomes: {label} instruction argument(s).

**FIGURE 37-1: VOLTAGE FREQUENCY GRAPH, -40°C ≤ TA ≤ +125°C, PIC18F26/45/46K40 ONLY**




**Note 1:** The shaded region indicates the permissible combinations of voltage and frequency.
**2:** Refer to Table 37-7 for each Oscillator mode's supported frequencies.

**FIGURE 37-2: VOLTAGE FREQUENCY GRAPH, -40°C ≤ TA ≤ +125°C, PIC18LF26/45/46K40 ONLY**




**Note 1:** The shaded region indicates the permissible combinations of voltage and frequency.
**2:** Refer to Table 37-7 for each Oscillator mode's supported frequencies.