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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	64MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	3.6K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 24x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f26k40t-i-so

3.0 DEVICE CONFIGURATION

Device configuration consists of Configuration Words, Code Protection, Device ID and Rev ID.

3.1 Configuration Words

There are six Configuration Word bits that allow the user to setup the device with several choices of oscillators, Resets and memory protection options. These are implemented as Configuration Word 1 through Configuration Word 6 at 300000h through 30000Bh.

<p>Note: The <u>DEBUG</u> bit in Configuration Words is managed automatically by device development tools including debuggers and programmers. For normal device operation, this bit should be maintained as a '1'.</p>
--

TABLE 3-1: SUMMARY OF CONFIGURATION WORDS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default/ Unprogrammed Value
30 0000h	CONFIG1L	—	RSTOSC2	RSTOSC1	RSTOSC0	—	FEXTOSC2	FEXTOSC1	FEXTOSC0	1111 1111
30 0001h	CONFIG1H	—	—	FCMEN	—	CSWEN	—	—	CLKOUTEN	1111 1111
30 0002h	CONFIG2L	BOREN1	BOREN0	LPBOREN	—	—	—	PWRTE	MCLRE	1111 1111
30 0003h	CONFIG2H	XINST	—	DEBUG	STVREN	PPS1WAY	ZCD	BORV1	BORV0	1111 1111
30 0004h	CONFIG3L	—	WDTE<1:0>		WDTCP5<4:0>					1111 1111
30 0005h	CONFIG3H	—	—	WDTCCS<2:0>			WDTCCS<2:0>			1111 1111
30 0006h	CONFIG4L	WRT7	WRT6	WRT5	WRT4	WRT3	WRT2	WRT1	WRT0	1111 1111
30 0007h	CONFIG4H	—	—	LVP	SCANE	—	WRTD	WRTB	WRTC	1111 1111
30 0008h	CONFIG5L	—	—	—	—	—	—	CPD	CP	1111 1111
30 000Ah	CONFIG6L	EBTR7	EBTR6	EBTR5	EBTR4	EBTR3	EBTR2	EBTR1	EBTR0	1111 1111
30 000Bh	CONFIG6H	—	—	—	—	—	—	EBTRB	—	1111 1111

PIC18F26/45/46K40

TABLE 10-5: REGISTER FILE SUMMARY FOR PIC18(L)F26/45/46K40 DEVICES (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR
FE2h	FSR1H	—	—	—	—	Indirect Data Memory Address Pointer 1 High				----xxxx
FE1h	FSR1L	Indirect Data Memory Address Pointer 1 Low								xxxxxxxx
FE0h	BSR	—	—	—	—	Bank Select Register				----0000
FDFh	INDF2	Uses contents of FSR0 to address data memory – value of FSR2 not changed (not a physical register)								-----
FDEh	POSTINC2	Uses contents of FSR0 to address data memory – value of FSR2 post-incremented (not a physical register)								-----
FDDh	POSTDEC2	Uses contents of FSR0 to address data memory – value of FSR2 post-decremented (not a physical register)								-----
FDCh	PREINC2	Uses contents of FSR0 to address data memory – value of FSR2 pre-incremented (not a physical register)								-----
FDBh	PLUSW2	Uses contents of FSR0 to address data memory – value of FSR2 pre-incremented (not a physical register) – value of FSR0 offset by W								-----
FDAh	FSR2H	—	—	—	—	Indirect Data Memory Address Pointer 2 High				----xxxx
FD9h	FSR2L	Indirect Data Memory Address Pointer 2 Low								xxxxxxxx
FD8h	STATUS	—	\overline{TO}	\overline{PD}	N	OV	Z	DC	C	-1100000
FD7h	PCON0	STKOVF	STKUNF	\overline{WDTWV}	\overline{RWDT}	\overline{RMCLR}	\overline{RI}	\overline{POR}	\overline{BOR}	0011110 _q
FD6h	T0CON1	T0CS<2:0>			T0ASYNC	T0CKPS<3:0>				00000000
FD5h	T0CON0	T0EN	—	T0OUT	T016BIT	T0OUTPS<3:0>				0-000000
FD4h	TMR0H	Holding Register for the Most Significant Byte of the 16-bit TMR0 Register								11111111
FD3h	TMR0L	Holding Register for the Least Significant Byte of the 16-bit TMR0 Register								00000000
FD2h	T1CLK	—	—	—	—	CS<3:0>				----0000
FD1h	T1GATE	—	—	—	—	GSS<3:0>				----0000
FD0h	T1GCON	GE	GPOL	GTM	GSPM	GO/ \overline{DONE}	GVAL	—	—	00000x--
FCFh	T1CON	—	—	CKPS<1:0>		—	\overline{SYNC}	RD16	ON	--00-000
FCEh	TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								00000000
FCDh	TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								00000000
FCCh	T3CLK	—	—	—	—	CS<3:0>				----0000
FCBh	T3GATE	—	—	—	—	GSS<3:0>				----0000
FCAh	T3GCON	GE	GPOL	GTM	GSPM	GO/ \overline{DONE}	GVAL	—	—	00000x--
FC9h	T3CON	—	—	CKPS<1:0>		—	\overline{SYNC}	RD16	ON	--00-000
FC8h	TMR3H	Holding Register for the Most Significant Byte of the 16-bit TMR3 Register								00000000
FC7h	TMR3L	Holding Register for the Least Significant Byte of the 16-bit TMR3 Register								00000000
FC6h	TMR5CLK	—	—	—	—	CS<3:0>				----0000
FC5h	T5GATE	—	—	—	—	GSS<3:0>				----0000
FC4h	T5GCON	GE	GPOL	GTM	GSPM	GO/ \overline{DONE}	GVAL	—	—	00000x--
FC3h	T5CON	—	—	CKPS<1:0>		—	\overline{SYNC}	RD16	ON	--00-000
FC2h	TMR5H	Holding Register for the Most Significant Byte of the 16-bit TMR5 Register								00000000

Legend: x = unknown, u = unchanged, — = unimplemented, _q = value depends on condition

- Note**
- 1: Not available on LF devices.
 - 2: Not available on PIC18(L)F26K40 (28-pin variants).
 - 3: Not available on PIC18(L)F45K40 devices.

EXAMPLE 11-3: ERASING A PROGRAM FLASH MEMORY BLOCK

```
; This sample row erase routine assumes the following:
; 1. A valid address within the erase row is loaded in variables TBLPTR register
; 2. ADDR_H and ADDR_L are located in common RAM (locations 0x70 - 0x7F)
```

```

MOV LW CODE_ADDR_UPPER ; load TBLPTR with the base
MOV WF TBLPTRU          ; address of the memory block
MOV LW CODE_ADDR_HIGH
MOV WF TBLPTRH
MOV LW CODE_ADDR_LOW
MOV WF TBLPTRL

ERASE_BLOCK
BCF NVMCON1, NVMREG0 ; point to Program Flash Memory
BSF NVMCON1, NVMREG1 ; access Program Flash Memory
BSF NVMCON1, WREN     ; enable write to memory
BSF NVMCON1, FREE     ; enable block Erase operation
BCF INTCON, GIE       ; disable interrupts

Required    MOV LW 55h
Sequence  MOV WF NVMCON2 ; write 55h
MOV LW AAh
MOV WF NVMCON2 ; write AAh
BSF NVMCON1, WR ; start erase (CPU stalls)
BSF INTCON, GIE ; re-enable interrupts
```

13.11.7 IN-CIRCUIT DEBUG (ICD) INTERACTION

The scanner freezes when an ICD halt occurs, and remains frozen until user-mode operation resumes. The debugger may inspect the SCANCON0 and SCANLADR registers to determine the state of the scan.

The ICD interaction with each operating mode is summarized in Table 13-4.

TABLE 13-4: ICD AND SCANNER INTERACTIONS

ICD Halt	Scanner Operating Mode		
	Peek	Concurrent Triggered	Burst
External Halt	If scanner would peek an instruction that is not executed (because of ICD entry), the peek will occur after ICD exit, when the instruction executes.	If external halt is asserted during a scan cycle, the instruction (delayed by scan) may or may not execute before ICD entry, depending on external halt timing.	If external halt is asserted during the <code>BSF (SCANCON.GO)</code> , ICD entry occurs, and the burst is delayed until ICD exit. Otherwise, the current NVM-access cycle will complete, and then the scanner will be interrupted for ICD entry.
		If external halt is asserted during the cycle immediately prior to the scan cycle, both scan and instruction execution happen after the ICD exits.	If external halt is asserted during the burst, the burst is suspended and will resume with ICD exit.
PC Breakpoint		Scan cycle occurs before ICD entry and instruction execution happens after the ICD exits.	If PCPB (or single step) is on <code>BSF (SCANCON.GO)</code> , the ICD is entered before execution; execution of the burst will occur at ICD exit, and the burst will run to completion.
Data Breakpoint		The instruction with the dataBP executes and ICD entry occurs immediately after. If scan is requested during that cycle, the scan cycle is postponed until the ICD exits.	
Single Step		If a scan cycle is ready after the debug instruction is executed, the scan will read PFM and then the ICD is re-entered.	Note that the burst can be interrupted by an external halt.
SWBP and ICDINST		If scan would stall a SWBP, the scan cycle occurs and the ICD is entered.	If SWBP replaces <code>BSF (SCANCON.GO)</code> , the ICD will be entered; instruction execution will occur at ICD exit (from ICDINSTR register), and the burst will run to completion.

13.11.8 PERIPHERAL MODULE DISABLE

Both the CRC and scanner module can be disabled individually by setting the CRCMD and SCANMD bits of the PMD0 register (Register 7-1). The SCANMD can be used to enable or disable to the scanner module only if the SCANE bit of Configuration Word 4 is set. If the SCANE bit is cleared, then the scanner module is not available for use and the SCANMD bit is ignored.

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REGISTER 14-7: PIR5: PERIPHERAL INTERRUPT REQUEST (FLAG) REGISTER 5

U-0	U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	—	—	TMR5GIF	TMR3GIF	TMR1GIF
bit 7					bit 0		

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-3 **Unimplemented:** Read as '0'

bit 2 **TMR5GIF:** TMR5 Gate Interrupt Flag bit

1 = TMR5 gate interrupt occurred (must be cleared in software)

0 = No TMR5 gate occurred

bit 1 **TMR3GIF:** TMR3 Gate Interrupt Flag bit

1 = TMR3 gate interrupt occurred (must be cleared in software)

0 = No TMR3 gate occurred

bit 0 **TMR1GIF:** TMR1 Gate Interrupt Flag bit

1 = TMR1 gate interrupt occurred (must be cleared in software)

0 = No TMR1 gate occurred

REGISTER 19-2: TxGCON: TIMERx GATE CONTROL REGISTER

R/W-0/u	R/W-0/u	R/W-0/u	R/W-0/u	R/W-0/u	R-x	U-0	U-0
GE	GPOL	GTM	GSPM	GGO/DONE	GVAL	—	—
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7 **GE:** Timerx Gate Enable bit

If TMRxON = 1:

1 = Timerx counting is controlled by the Timerx gate function

0 = Timerx is always counting

If TMRxON = 0:

This bit is ignored

bit 6 **GPOL:** Timerx Gate Polarity bit

1 = Timerx gate is active-high (Timerx counts when gate is high)

0 = Timerx gate is active-low (Timerx counts when gate is low)

bit 5 **GTM:** Timerx Gate Toggle Mode bit

1 = Timerx Gate Toggle mode is enabled

0 = Timerx Gate Toggle mode is disabled and Toggle flip-flop is cleared

Timerx Gate Flip Flop Toggles on every rising edge

bit 4 **GSPM:** Timerx Gate Single Pulse Mode bit

1 = Timerx Gate Single Pulse mode is enabled and is controlling Timerx gate)

0 = Timerx Gate Single Pulse mode is disabled

bit 3 **GGO/DONE:** Timerx Gate Single Pulse Acquisition Status bit

1 = Timerx Gate Single Pulse Acquisition is ready, waiting for an edge

0 = Timerx Gate Single Pulse Acquisition has completed or has not been started.

This bit is automatically cleared when TxGSPM is cleared.

bit 2 **GVAL:** Timerx Gate Current State bit

Indicates the current state of the Timerx gate that could be provided to TMRxH:TMRxL

Unaffected by Timerx Gate Enable (TMRxGE)

bit 1-0 **Unimplemented:** Read as '0'

19.2 Timer1/3/5 Operation

The Timer1/3/5 module is a 16-bit incrementing counter which is accessed through the TMRxH:TMRxL register pair. Writes to TMRxH or TMRxL directly update the counter.

When used with an internal clock source, the module is a timer and increments on every instruction cycle. When used with an external clock source, the module can be used as either a timer or counter and increments on every selected edge of the external source.

Timer1/3/5 is enabled by configuring the ON and GE bits in the TxCON and TxGCON registers, respectively. Table 19-2 displays the Timer1/3/5 enable selections.

TABLE 19-2: TIMER1/3/5 ENABLE SELECTIONS

ON	GE	Timer1/3/5 Operation
1	1	Count Enabled
1	0	Always On
0	1	Off
0	0	Off

19.3 Clock Source Selection

The CS<3:0> bits of the TMRxCLK register (Register 19-3) are used to select the clock source for Timer1/3/5. The four TMRxCLK bits allow the selection of several possible synchronous and asynchronous clock sources. Register 19-3 displays the clock source selections.

19.3.1 INTERNAL CLOCK SOURCE

When the internal clock source is selected the TMRxH:TMRxL register pair will increment on multiples of FOSC as determined by the Timer1/3/5 prescaler.

When the FOSC internal clock source is selected, the Timer1/3/5 register value will increment by four counts every instruction clock cycle. Due to this condition, a 2 LSB error in resolution will occur when reading the Timer1/3/5 value. To utilize the full resolution of Timer1/3/5, an asynchronous input signal must be used to gate the Timer1/3/5 clock input.

The following asynchronous sources may be used at the Timer1/3/5 gate:

- Asynchronous event on the TxGPPS pin
- TMR0OUT
- TMR1/3/5OUT (excluding the TMR for which it is being used)
- TMR 2/4/6OUT (post-scaled)
- CCP1/2OUT
- PWM3/4OUT
- CMP1/2OUT
- ZCDOUT

Note: In Counter mode, a falling edge must be registered by the counter prior to the first incrementing rising edge after any one or more of the following conditions:

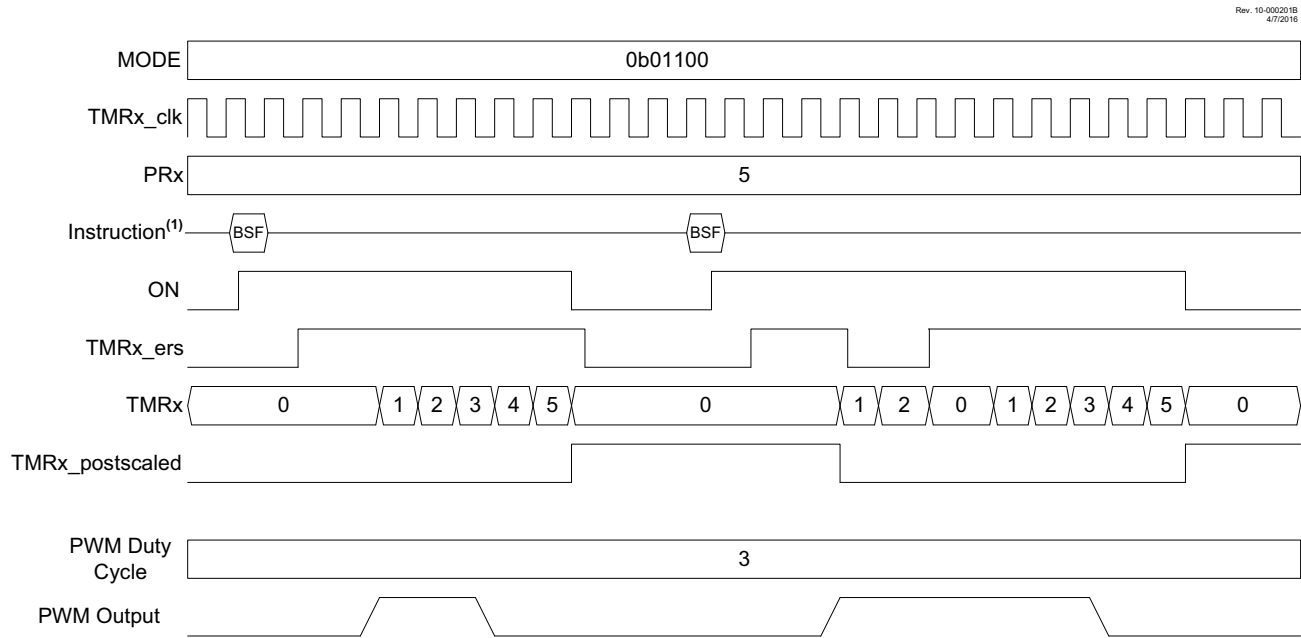
- Timer1/3/5 enabled after POR
- Write to TMRxH or TMRxL
- Timer1/3/5 is disabled
- Timer1/3/5 is disabled (TMRxON = 0) when TxCKI is high then Timer1/3/5 is enabled (TMRxON = 1) when TxCKI is low.

19.3.2 EXTERNAL CLOCK SOURCE

When the external clock source is selected, the Timer1/3/5 module may work as a timer or a counter.

When enabled to count, Timer1/3/5 is incremented on the rising edge of the external clock input of the TxCKIPPS pin. This external clock source can be synchronized to the microcontroller system clock or it can run asynchronously.

When used as a timer with a clock oscillator, an external 32.768 kHz crystal can be used in conjunction with the dedicated secondary internal oscillator circuit.

FIGURE 20-10: EDGE-TRIGGERED HARDWARE LIMIT ONE-SHOT MODE TIMING DIAGRAM (MODE = 01100)

Note 1: BSF and BCF represent Bit-Set File and Bit-Clear File instructions executed by the CPU to set or clear the ON bit of TxCON. CPU execution is asynchronous to the timer clock input.

REGISTER 20-2: TxHLT: TIMERx HARDWARE LIMIT CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
PSYNC	CPOL	CSYNC	MODE<4:0>				
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

- bit 7 **PSYNC:** Timerx Prescaler Synchronization Enable bit^(1, 2)
1 = TMRx Prescaler Output is synchronized to Fosc/4
0 = TMRx Prescaler Output is not synchronized to Fosc/4
- bit 6 **CPOL:** Timerx Clock Polarity Selection bit⁽³⁾
1 = Falling edge of input clock clocks timer/prescaler
0 = Rising edge of input clock clocks timer/prescaler
- bit 5 **CSYNC:** Timerx Clock Synchronization Enable bit^(4, 5)
1 = ON register bit is synchronized to TMR2_clk input
0 = ON register bit is not synchronized to TMR2_clk input
- bit 4-0 **MODE<4:0>:** Timerx Control Mode Selection bits^(6, 7)
See Table 20-1 for all operating modes.

- Note 1:** Setting this bit ensures that reading TMRx will return a valid data value.
- 2:** When this bit is '1', Timer2 cannot operate in Sleep mode.
- 3:** CKPOL should not be changed while ON = 1.
- 4:** Setting this bit ensures glitch-free operation when the ON is enabled or disabled.
- 5:** When this bit is set then the timer operation will be delayed by two TMRx input clocks after the ON bit is set.
- 6:** Unless otherwise indicated, all modes start upon ON = 1 and stop upon ON = 0 (stops occur without affecting the value of TMRx).
- 7:** When TMRx = PRx, the next clock clears TMRx, regardless of the operating mode.

FIGURE 24-12: DEAD-BAND OPERATION, CWG1DBR = 0x01, CWG1DBF = 0x02

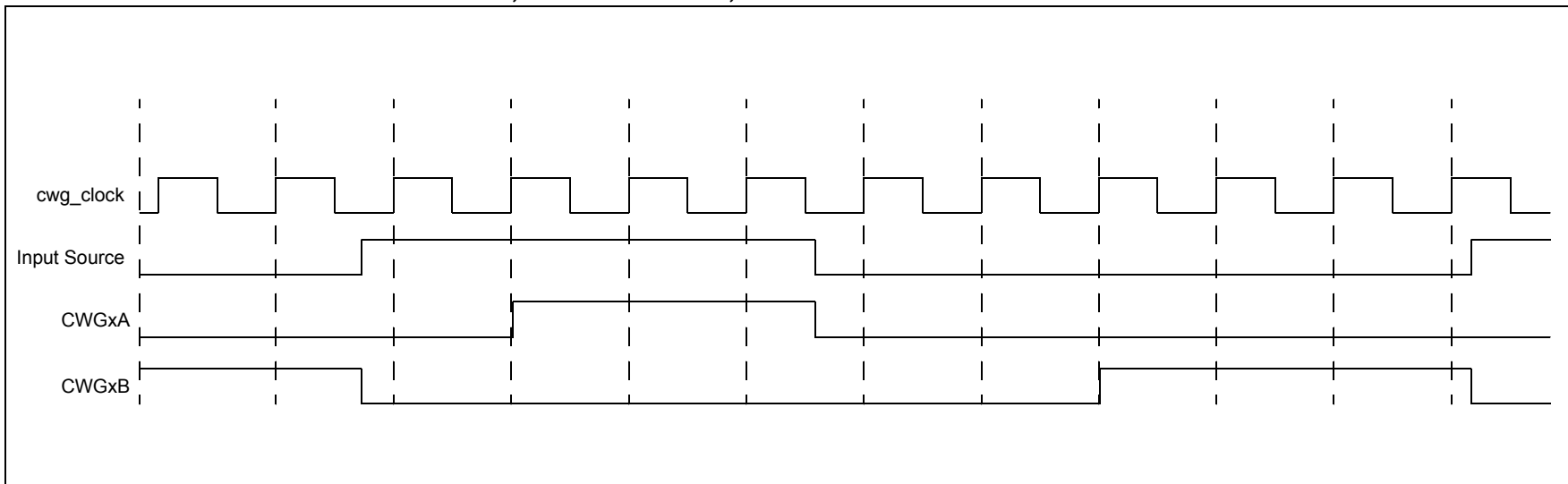
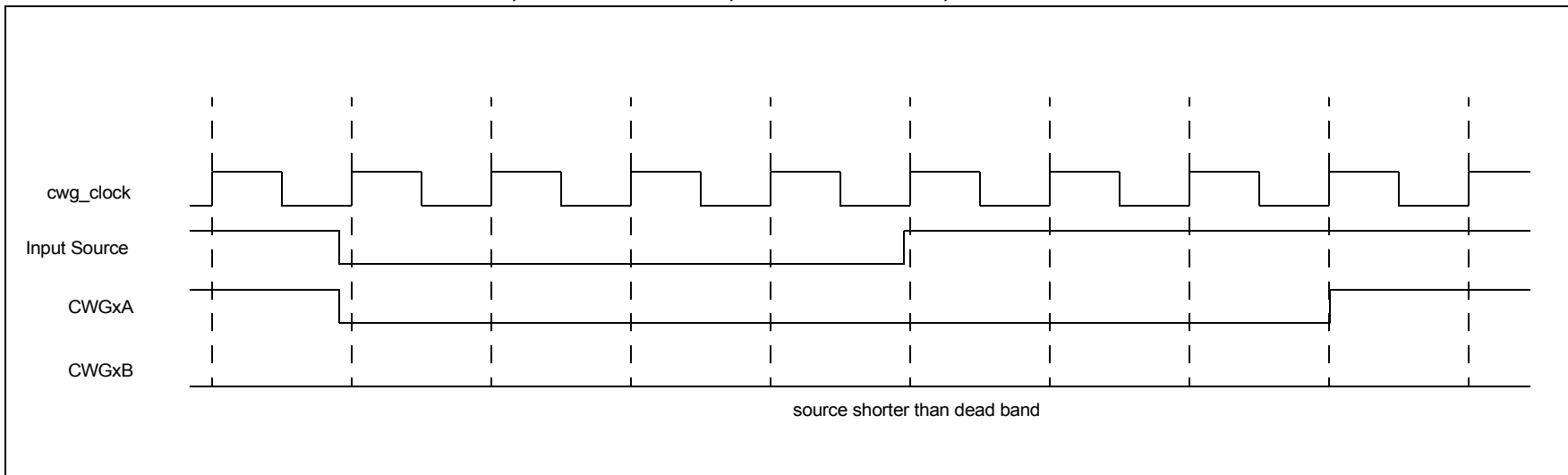


FIGURE 24-13: DEAD-BAND OPERATION, CWG1DBR = 0x03, CWG1DBF = 0x06, SOURCE SHORTER THAN DEAD BAND



REGISTER 25-2: MDCON1: MODULATION CONTROL REGISTER 1

U-0	U-0	R/W-0/0	R/W-0/0	U-0	U-0	R/W-0/0	R/W-0/0
—	—	CHPOL	CHSYNC	—	—	CLPOL	CLSYNC
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **CHPOL:** Modulator High Carrier Polarity Select bit

1 = Selected high carrier signal is inverted

0 = Selected high carrier signal is not inverted

bit 4 **CHSYNC:** Modulator High Carrier Synchronization Enable bit

1 = Modulator waits for a falling edge on the high time carrier signal before allowing a switch to the low time carrier

0 = Modulator output is not synchronized to the high time carrier signal⁽¹⁾

bit 3-2 **Unimplemented:** Read as '0'

bit 1 **CLPOL:** Modulator Low Carrier Polarity Select bit

1 = Selected low carrier signal is inverted

0 = Selected low carrier signal is not inverted

bit 0 **CLSYNC:** Modulator Low Carrier Synchronization Enable bit

1 = Modulator waits for a falling edge on the low time carrier signal before allowing a switch to the high time carrier

0 = Modulator output is not synchronized to the low time carrier signal⁽¹⁾

Note 1: Narrowed carrier pulse widths or spurs may occur in the signal stream if the carrier is not synchronized.

REGISTER 26-11: SSPxADD: MSSP ADDRESS REGISTER (I²C MASTER MODE)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADD<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

Master mode: I²C mode

bit 7-0 Baud Rate Clock Divider bits⁽¹⁾

$$\text{SCK/SCL pin clock period} = ((\text{SSPxADD}<7:0> + 1) * 4) / \text{Fosc}$$

10-Bit Slave mode – Most Significant Address Byte:

bit 7-3 **Not used:** Unused for Most Significant Address Byte. Bit state of this register is a don't care. Bit pattern sent by master is fixed by I²C specification and must be equal to, '11110'. However, those bits are compared by hardware and are not affected by the value in this register.

bit 2-1 **ADD<9:8>:** Two Most Significant bits of 10-bit Address

bit 0 **Not used:** Unused in this mode. Bit state is a don't care.

10-Bit Slave mode – Least Significant Address Byte:

bit 7-0 **ADD<7:0>:** Eight Least Significant bits of 10-bit Address

7-Bit Slave mode:

bit 7-1 7-bit Slave Address

bit 0 **Not used:** Unused in this mode. Bit state is a don't care.

Note 1: Values of 0x00, 0x01 and 0x02 are not valid for SSPxADD when used as a Baud Rate Generator for I²C. This is an implementation limitation.

REGISTER 26-12: SSPxMSK: MSSPx ADDRESS MASK REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
MSK<7:1>							MSK0
bit 7				bit 0			

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-1 **MSK<7:1>:** Mask bits

1 = The received address bit n is compared to SSPxADDn to detect I²C address match
0 = The received address bit n is not used to detect I²C address match

bit 0 **MSK0:** Mask bit for I²C Slave mode, 10-bit Address

I²C Slave mode, 10-bit address (SSPM<3:0> = 0111 or 1111):

1 = The received address bit 0 is compared to SSPxADD0 to detect I²C address match
0 = The received address bit 0 is not used to detect I²C address match

I²C Slave mode, 7-bit address, the bit is ignored.

26.9.2.1 7-bit Addressing Reception

This section describes a standard sequence of events for the MSSP module configured as an I²C slave in 7-bit Addressing mode. Figure 26-14 and Figure 26-15 is used as a visual reference for this description.

This is a step by step process of what typically must be done to accomplish I²C communication.

1. Start bit detected.
2. S bit of SSPxSTAT is set; SSPxIF is set if interrupt on Start detect is enabled.
3. Matching address with R/W bit clear is received.
4. The slave pulls SDA low sending an $\overline{\text{ACK}}$ to the master, and sets SSPxIF bit.
5. Software clears the SSPxIF bit.
6. Software reads received address from SSPxBUF clearing the BF flag.
7. If SEN = 1; Slave software sets CKP bit to release the SCL line.
8. The master clocks out a data byte.
9. Slave drives SDA low sending an $\overline{\text{ACK}}$ to the master, and sets SSPxIF bit.
10. Software clears SSPxIF.
11. Software reads the received byte from SSPxBUF clearing BF.
12. Steps 8-12 are repeated for all received bytes from the master.
13. Master sends Stop condition, setting P bit of SSPxSTAT, and the bus goes idle.

26.9.2.2 7-bit Reception with AHEN and DHEN

Slave device reception with AHEN and DHEN set operate the same as without these options with extra interrupts and clock stretching added after the eighth falling edge of SCL. These additional interrupts allow the slave software to decide whether it wants to $\overline{\text{ACK}}$ the receive address or data byte, rather than the hardware. This functionality adds support for PMBus™ that was not present on previous versions of this module.

This list describes the steps that need to be taken by slave software to use these options for I²C communication. Figure 26-16 displays a module using both address and data holding. Figure 26-17 includes the operation with the SEN bit of the SSPxCON2 register set.

1. S bit of SSPxSTAT is set; SSPxIF is set if interrupt on Start detect is enabled.
2. Matching address with R/W bit clear is clocked in. SSPxIF is set and CKP cleared after the eighth falling edge of SCL.
3. Slave clears the SSPxIF.
4. Slave can look at the ACKTIM bit of the SSPxCON3 register to determine if the SSPxIF was after or before the $\overline{\text{ACK}}$.
5. Slave reads the address value from SSPxBUF, clearing the BF flag.
6. Slave sets $\overline{\text{ACK}}$ value clocked out to the master by setting ACKDT.
7. Slave releases the clock by setting CKP.
8. SSPxIF is set after an $\overline{\text{ACK}}$, not after a NACK.
9. If SEN = 1 the slave hardware will stretch the clock after the $\overline{\text{ACK}}$.
10. Slave clears SSPxIF.

Note: SSPxIF is still set after the ninth falling edge of SCL even if there is no clock stretching and BF has been cleared. Only if NACK is sent to master is SSPxIF not set

11. SSPxIF set and CKP cleared after eighth falling edge of SCL for a received data byte.
12. Slave looks at ACKTIM bit of SSPxCON3 to determine the source of the interrupt.
13. Slave reads the received data from SSPxBUF clearing BF.
14. Steps 7-14 are the same for each received data byte.
15. Communication is ended by either the slave sending an $\overline{\text{ACK}} = 1$, or the master sending a Stop condition. If a Stop is sent and Interrupt on Stop Detect is disabled, the slave will only know by polling the P bit of the SSTSTAT register.

27.2.1.5 TSR Status

The TRMT bit of the TXxSTA register indicates the status of the TSR register. This is a read-only bit. The TRMT bit is set when the TSR register is empty and is cleared when a character is transferred to the TSR register from the TXxREG. The TRMT bit remains clear until all bits have been shifted out of the TSR register. No interrupt logic is tied to this bit, so the user has to poll this bit to determine the TSR status.

Note: The TSR register is not mapped in data memory, so it is not available to the user.

27.2.1.6 Transmitting 9-Bit Characters

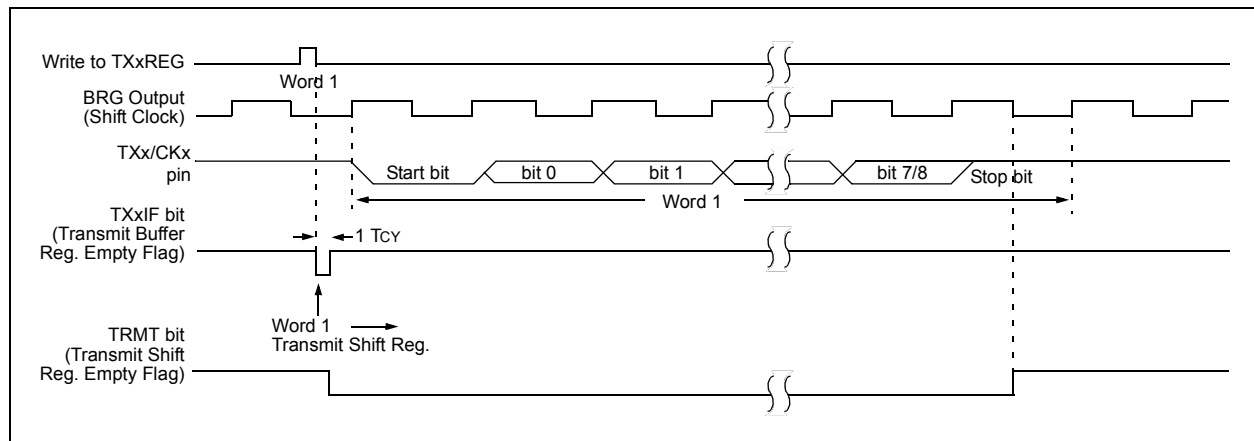
The EUSART supports 9-bit character transmissions. When the TX9 bit of the TXxSTA register is set, the EUSART will shift nine bits out for each character transmitted. The TX9D bit of the TXxSTA register is the ninth, and Most Significant data bit. When transmitting 9-bit data, the TX9D data bit must be written before writing the eight Least Significant bits into the TXxREG. All nine bits of data will be transferred to the TSR shift register immediately after the TXxREG is written.

A special 9-bit Address mode is available for use with multiple receivers. See **Section 27.2.2.7 “Address Detection”** for more information on the Address mode.

27.2.1.7 Asynchronous Transmission Setup:

1. Initialize the SPxBRGH, SPxBRGL register pair and the BRGH and BRG16 bits to achieve the desired baud rate (see **Section 27.4 “EUSART Baud Rate Generator (BRG)”**).
2. Enable the asynchronous serial port by clearing the SYNC bit and setting the SPEN bit.
3. If 9-bit transmission is desired, set the TX9 control bit. A set ninth data bit will indicate that the eight Least Significant data bits are an address when the receiver is set for address detection.
4. Set SCKP bit if inverted transmit is desired.
5. Enable the transmission by setting the TXEN control bit. This will cause the TXxIF interrupt bit to be set.
6. If interrupts are desired, set the TXxIE interrupt enable bit of the PIE3 register. An interrupt will occur immediately provided that the GIE and PEIE bits of the INTCON register are also set.
7. If 9-bit transmission is selected, the ninth bit should be loaded into the TX9D data bit.
8. Load 8-bit data into the TXxREG register. This will start the transmission.

FIGURE 27-3: ASYNCHRONOUS TRANSMISSION



27.3 Clock Accuracy with Asynchronous Operation

The factory calibrates the internal oscillator block output (INTOSC). However, the INTOSC frequency may drift as VDD or temperature changes, and this directly affects the asynchronous baud rate. Two methods may be used to adjust the baud rate clock, but both require a reference clock source of some kind.

The first (preferred) method uses the OSCTUNE register to adjust the INTOSC output. Adjusting the value in the OSCTUNE register allows for fine resolution changes to the system clock source. See **Section 4.3.2.3 “Internal Oscillator Frequency Adjustment”** for more information.

The other method adjusts the value in the Baud Rate Generator. This can be done automatically with the Auto-Baud Detect feature (see **Section 27.4.1 “Auto-Baud Detect”**). There may not be fine enough resolution when adjusting the Baud Rate Generator to compensate for a gradual change in the peripheral clock frequency.

29.4 ADC Acquisition Time

To ensure accurate temperature measurements, the user must wait at least 200 μ s after the ADC input multiplexer is connected to the temperature indicator output before the conversion is performed. In addition, the user must wait 200 μ s between consecutive conversions of the temperature indicator output.

TABLE 29-2: SUMMARY OF REGISTERS ASSOCIATED WITH THE TEMPERATURE INDICATOR

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
FVRCON	FVREN	FVRRDY	TSEN	TSRNG	CDFVR<1:0>		ADFVR<1:0>		423

Legend: — = Unimplemented location, read as '0'. Shaded cells are unused by the temperature indicator module.

31.3 ADC Acquisition Requirements

For the ADC to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The Analog Input model is shown in Figure 31-4. The source impedance (RS) and the internal sampling switch (RSS) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (RSS) impedance varies over the device voltage (VDD), refer to Figure 31-4. **The maximum recommended impedance for analog sources is 10 kΩ.** As the

source impedance is decreased, the acquisition time may be decreased. After the analog input channel is selected (or changed), an ADC acquisition must be completed before the conversion can be started. To calculate the minimum acquisition time, Equation 31-1 may be used. This equation assumes that 1/2 LSB error is used (1,024 steps for the ADC). The 1/2 LSB error is the maximum error allowed for the ADC to meet its specified resolution.

EQUATION 31-1: ACQUISITION TIME EXAMPLE

Assumptions: Temperature = 50°C and external impedance of 10kΩ 5.0V VDD

$$\begin{aligned} T_{ACQ} &= \text{Amplifier Settling Time} + \text{Hold Capacitor Charging Time} + \text{Temperature Coefficient} \\ &= T_{AMP} + T_C + T_{COFF} \\ &= 2\mu s + T_C + [(Temperature - 25^\circ C)(0.05\mu s/^\circ C)] \end{aligned}$$

The value for TC can be approximated with the following equations:

$$V_{APPLIED} \left(1 - \frac{1}{(2^{n+1}) - 1} \right) = V_{CHOLD} \quad ;[1] \text{ } V_{CHOLD} \text{ charged to within } 1/2 \text{ lsb}$$

$$V_{APPLIED} \left(1 - e^{\frac{-T_C}{RC}} \right) = V_{CHOLD} \quad ;[2] \text{ } V_{CHOLD} \text{ charge response to } V_{APPLIED}$$

$$V_{APPLIED} \left(1 - e^{\frac{-T_C}{RC}} \right) = V_{APPLIED} \left(1 - \frac{1}{(2^{n+1}) - 1} \right) \quad ;\text{combining [1] and [2]}$$

Note: Where n = number of bits of the ADC.

Solving for TC:

$$\begin{aligned} T_C &= -CHOLD(RIC + RSS + RS) \ln(1/2047) \\ &= -10pF(1k\Omega + 7k\Omega + 10k\Omega) \ln(0.0004885) \\ &= 1.37\mu s \end{aligned}$$

Therefore:

$$\begin{aligned} T_{ACQ} &= 2\mu s + 892ns + [(50^\circ C - 25^\circ C)(0.05\mu s/^\circ C)] \\ &= 4.62\mu s \end{aligned}$$

Note 1: The reference voltage (VREF) has no effect on the equation, since it cancels itself out.

2: The charge holding capacitor (CHOLD) is not discharged after each conversion.

3: The maximum recommended impedance for analog sources is 10 kΩ. This is required to meet the pin leakage specification.

REGISTER 31-27: ADERRL: ADC SETPOINT ERROR LOW BYTE REGISTER

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
ADERR<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **ADERR<7:0>**: ADC Setpoint Error LSB. Lower byte of ADC Setpoint Error calculation is determined by ADCALC bits of ADCON3, see Register 23-1 for more details.

REGISTER 31-28: ADLTHH: ADC LOWER THRESHOLD HIGH BYTE REGISTER

R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x
ADLTH<15:8>							
bit 7				bit 0			

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **ADLTH<15:8>**: ADC Lower Threshold MSB. ADLTH and ADUTH are compared with ADERR to set the ADUTHR and ADLTHR bits of ADSTAT. Depending on the setting of ADTMD, an interrupt may be triggered by the results of this comparison.

REGISTER 31-29: ADLTHL: ADC LOWER THRESHOLD LOW BYTE REGISTER

R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x
ADLTH<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **ADLTH<7:0>**: ADC Lower Threshold LSB. ADLTH and ADUTH are compared with ADERR to set the ADUTHR and ADLTHR bits of ADSTAT. Depending on the setting of ADTMD, an interrupt may be triggered by the results of this comparison.

PIC18(L)F26/45/46K40

TABLE 37-3: POWER-DOWN CURRENT (I_{PD})^(1,2)

PIC18LF26/45/46K40				Standard Operating Conditions (unless otherwise stated)					
PIC18F26/45/46K40				Standard Operating Conditions (unless otherwise stated) VREGPM = 1					
Param. No.	Symbol	Device Characteristics	Min.	Typ.†	Max. +85°C	Max. +125°C	Units	Conditions	
								V _{DD}	Note
D200	IPD	IPD Base	—	0.05	2	9	μA	3.0V	
D200	IPD	IPD Base	—	0.4	4	12	μA	3.0V	
D200A			—	20	—	—	μA	3.0V	VREGPM = 0
D201	IPD_WDT	Low-Frequency Internal Oscillator/ WDT	—	0.4	3	10	μA	3.0V	
D201	IPD_WDT	Low-Frequency Internal Oscillator/ WDT	—	0.6	5	13	μA	3.0V	
D202	IPD_SOSC	Secondary Oscillator (SOSC)	—	0.6	5	13	μA	3.0V	
D202	IPD_SOSC	Secondary Oscillator (SOSC)	—	0.8	8.5	15	μA	3.0V	
D203	IPD_FVR	FVR	—	31	—	—	μA	3.0V	FVRCON = 0X81 or 0x84
D203	IPD_FVR	FVR	—	32	—	—	μA	3.0V	FVRCON = 0X81 or 0x84
D204	IPD_BOR	Brown-out Reset (BOR)	—	9	14	18	μA	3.0V	
D204	IPD_BOR	Brown-out Reset (BOR)	—	14	19	21	μA	3.0V	
D205	IPD_LPBOR	Low-Power Brown-out Reset (LPBOR)	—	0.5	—	—	μA	3.0V	
D205	IPD_LPBOR	Low-Power Brown-out Reset (LPBOR)	—	0.7	—	—	μA	3.0V	
D206	IPD_HLVD	High/Low Voltage Detect (HLVD)	—	31	—	—	μA	3.0V	
D206	IPD_HLVD	High/Low Voltage Detect (HLVD)	—	32	—	—	μA	3.0V	
D207	IPD_ADCA	ADC - Active	—	250	—	—	μA	3.0V	ADC is converting ⁽⁴⁾
D207	IPD_ADCA	ADC - Active	—	280	—	—	μA	3.0V	ADC is converting ⁽⁴⁾
D208	IPD_CMP	Comparator	—	25	38	40	μA	3.0V	
D208	IPD_CMP	Comparator	—	28	50	60	μA	3.0V	

† Data in "Typ." column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

- Note** 1: The peripheral current is the sum of the base IDD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max. values should be used when calculating total current consumption.
- 2: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode with all I/O pins in high-impedance state and tied to V_{SS}.
- 3: All peripheral currents listed are on a per-peripheral basis if more than one instance of a peripheral is available.
- 4: ADC clock source is FRC.