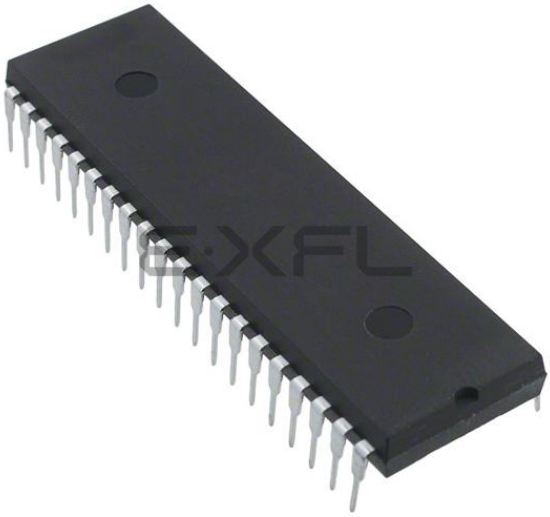


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	64MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 35x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f45k40-e-p

TO OUR VALUED CUSTOMERS

It is our intention to provide our valued customers with the best documentation possible to ensure successful use of your Microchip products. To this end, we will continue to improve our publications to better suit your needs. Our publications will be refined and enhanced as new volumes and updates are introduced.

If you have any questions or comments regarding this publication, please contact the Marketing Communications Department via E-mail at **docerrors@microchip.com**. We welcome your feedback.

Most Current Data Sheet

To obtain the most up-to-date version of this data sheet, please register at our Worldwide Website at:

http://www.microchip.com

You can determine the version of a data sheet by examining its literature number found on the bottom outside corner of any page. The last character of the literature number is the version number, (e.g., DS30000000A is version A of document DS30000000).

Errata

An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

To determine if an errata sheet exists for a particular device, please check with one of the following:

- Microchip's Worldwide Website; **http://www.microchip.com**
- Your local Microchip sales office (see last page)

When contacting a sales office, please specify which device, revision of silicon and data sheet (include literature number) you are using.

Customer Notification System

Register on our website at **www.microchip.com** to receive the most current information on all of our products.

3.2 Register Definitions: Configuration Words

REGISTER 3-1: Configuration Word 1L (30 0000h): Oscillators

U-1	R/W-1	R/W-1	R/W-1	U-1	R/W-1	R/W-1	R/W-1
—	RSTOSC<2:0>			—	FEXTOSC<2:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '1'	
-n = Value for blank device	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented:** Read as '1'

bit 6-4 **RSTOSC<2:0>:** Power-up Default Value for COSC bits
This value is the Reset default value for COSC and selects the oscillator first used by user software. Refer to COSC operation.
111 = EXTOSC operating per FEXTOSC bits (device manufacturing default)
110 = HFINTOSC with HFFRQ = 4 MHz (Register 4-5) and CDIV = 4:1 (Register 4-2)
101 = LFINTOSC
100 = SOSC
011 = Reserved
010 = EXTOSC with 4x PLL, with EXTOSC operating per FEXTOSC bits
001 = Reserved
000 = HFINTOSC with HFFRQ = 64 MHz (Register 4-5) and CDIV = 1:1 (Register 4-2). Resets COSC/NOSC to 3'b110.

bit 3 **Unimplemented:** Read as '1'

bit 2-0 **FEXTOSC<2:0>:** FEXTOSC External Oscillator Mode Selection bits
111 = EC (external clock) above 8 MHz; PFM set to high power (device manufacturing default)
110 = EC (external clock) for 500 kHz to 8 MHz; PFM set to medium power
101 = EC (external clock) below 500 kHz; PFM set to low power
100 = Oscillator not enabled
011 = Reserved (do not use)
010 = HS (crystal oscillator) above 8 MHz; PFM set to high power
001 = XT (crystal oscillator) above 500 kHz, below 8 MHz; PFM set to medium power
000 = LP (crystal oscillator) optimized for 32.768 kHz; PFM set to low power

REGISTER 3-2: Configuration Word 1H (30 0001h): Oscillators

U-1	U-1	R/W-1	U-1	R/W-1	U-1	U-1	R/W-1
—	—	FCMEN	—	CSWEN	—	—	$\overline{\text{CLKOUTEN}}$
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '1'	
-n = Value for blank device	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '1'

bit 5 **FCMEN:** Fail-Safe Clock Monitor Enable bit
1 = FSCM timer enabled
0 = FSCM timer disabled

bit 4 **Unimplemented:** Read as '1'

bit 3 **CSWEN:** Clock Switch Enable bit
1 = Writing to NOSC and NDIV is allowed
0 = The NOSC and NDIV bits cannot be changed by user software

bit 2-1 **Unimplemented:** Read as '1'

bit 0 **$\overline{\text{CLKOUTEN}}$:** Clock Out Enable bit
If FEXTOSC = HS, XT, LP, then this bit is ignored
Otherwise:
1 = CLKOUT function is disabled; I/O or oscillator function on OSC2
0 = CLKOUT function is enabled; FOSC/4 clock appears at OSC2

3.6 Device ID and Revision ID

The 16-bit device ID word is located at 3F FFFEh and the 16-bit revision ID is located at 3F FFFCh. These locations are read-only and cannot be erased or modified.

Development tools, such as device programmers and debuggers, may be used to read the Device ID, Revision ID and Configuration Words. Refer to **11.0 "Nonvolatile Memory (NVM) Control"** for more information on accessing these locations.

3.7 Register Definitions: Device and Revision

REGISTER 3-12: DEVICE ID: DEVICE ID REGISTER

R	R	R	R	R	R	R	R
DEV15	DEV14	DEV13	DEV12	DEV11	DEV10	DEV9	DEV8
bit 15							bit 8

R	R	R	R	R	R	R	R
DEV7	DEV6	DEV5	DEV4	DEV3	DEV2	DEV1	DEV0
bit 7							bit 0

Legend:			
R = Readable bit	'1' = Bit is set	0' = Bit is cleared	x = Bit is unknown

bit 15-0 **DEV<15:0>:** Device ID bits

Device	Device ID
PIC18F26K40	6980h
PIC18F45K40	6940h
PIC18F46K40	6920h
PIC18LF26K40	6A60h
PIC18LF45K40	6A20h
PIC18LF46K40	6A00h

REGISTER 7-2: PMD1: PMD CONTROL REGISTER 1

U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	TMR6MD	TMR5MD	TMR4MD	TMR3MD	TMR2MD	TMR1MD	TMR0MD
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7 **Unimplemented:** Read as '0'

bit 6 **TMR6MD:** Disable Timer TMR6 bit
- 1 = TMR6 module disabled
- 0 = TMR6 module enabled

bit 5 **TMR5MD:** Disable Timer TMR5 bit
- 1 = TMR5 module disabled
- 0 = TMR5 module enabled

bit 4 **TMR4MD:** Disable Timer TMR4 bit
- 1 = TMR4 module disabled
- 0 = TMR4 module enabled

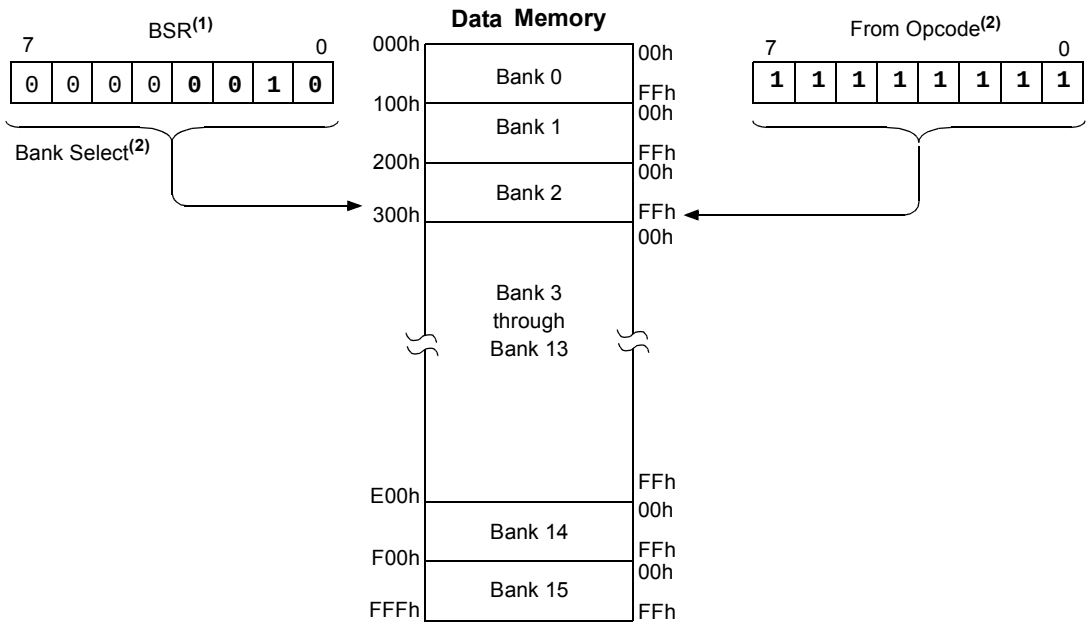
bit 3 **TMR3MD:** Disable Timer TMR3 bit
- 1 = TMR3 module disabled
- 0 = TMR3 module enabled

bit 2 **TMR2MD:** Disable Timer TMR2 bit
- 1 = TMR2 module disabled
- 0 = TMR2 module enabled

bit 1 **TMR1MD:** Disable Timer TMR1 bit
- 1 = TMR1 module disabled
- 0 = TMR1 module enabled

bit 0 **TMR0MD:** Disable Timer TMR0 bit
- 1 = TMR0 module disabled
- 0 = TMR0 module enabled

FIGURE 10-5: USE OF THE BANK SELECT REGISTER (DIRECT ADDRESSING)



Note 1: The Access RAM bit of the instruction can be used to force an override of the selected bank (BSR<3:0>) to the registers of the Access Bank.

2: The `MOVFF` instruction embeds the entire 12-bit address in the instruction.

TABLE 10-5: REGISTER FILE SUMMARY FOR PIC18(L)F26/45/46K40 DEVICES (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR
F26h	ANSELD(2)	ANSELD7	ANSELD6	ANSELD5	ANSELD4	ANSELD3	ANSELD2	ANSELD1	ANSELD0	11111111
F25h	WPUD(2)	WPUD7	WPUD6	WPUD5	WPUD4	WPUD3	WPUD2	WPUD1	WPUD0	00000000
F24h	ODCOND(2)	ODCD7	ODCD6	ODCD5	ODCD4	ODCD3	ODCD2	ODCD1	ODCD0	00000000
F23h	SLRCOND(2)	SLRD7	SLRD6	SLRD5	SLRD4	SLRD3	SLRD2	SLRD1	SLRD0	11111111
F22h	INLVLD(2)	INLVLD7	INLVLD6	INLVLD5	INLVLD4	INLVLD3	INLVLD2	INLVLD1	INLVLD0	10000000
F21h	ANSELC	ANSELC7	ANSELC6	ANSELC5	ANSELC4	ANSELC3	ANSELC2	ANSELC1	ANSELC0	11111111
F20h	WPUC	WPUC7	WPUC6	WPUC5	WPUC4	WPUC3	WPUC2	WPUC1	WPUC0	00000000
F1Fh	ODCONC	ODCC7	ODCC6	ODCC5	ODCC4	ODCC3	ODCC2	ODCC1	ODCC0	00000000
F1Eh	SLRCONC	SLRC7	SLRC6	SLRC5	SLRC4	SLRC3	SLRC2	SLRC1	SLRC0	11111111
F1Dh	INLVLC	INLVLC7	INLVLC6	INLVLC5	INLVLC4	INLVLC3	INLVLC2	INLVLC1	INLVLC0	11111111
F1Ch	IOCCP	IOCCP7	IOCCP6	IOCCP5	IOCCP4	IOCCP3	IOCCP2	IOCCP1	IOCCP0	00000000
F1Bh	IOCCN	IOCCN7	IOCCN6	IOCCN5	IOCCN4	IOCCN3	IOCCN2	IOCCN1	IOCCN0	00000000
F1Ah	IOCCF	IOCCF7	IOCCF6	IOCCF5	IOCCF4	IOCCF3	IOCCF2	IOCCF1	IOCCF0	00000000
F19h	ANSELB	ANSELB7	ANSELB6	ANSELB5	ANSELB4	ANSELB3	ANSELB2	ANSELB1	ANSELB0	11111111
F18h	WPUB	WPUB7	WPUB6	WPUB5	WPUB4	WPUB3	WPUB2	WPUB1	WPUB0	00000000
F17h	ODCONB	ODCB7	ODCB6	ODCB5	ODCB4	ODCB3	ODCB2	ODCB1	ODCB0	00000000
F16h	SLRCONB	SLRB7	SLRB6	SLRB5	SLRB4	SLRB3	SLRB2	SLRB1	SLRB0	11111111
F15h	INLVLB	INLVLB7	INLVLB6	INLVLB5	INLVLB4	INLVLB3	INLVLB2	INLVLB1	INLVLB0	11111111
F14h	IOCBP	IOCBP7	IOCBP6	IOCBP5	IOCBP4	IOCBP3	IOCBP2	IOCBP1	IOCBP0	00000000
F13h	IOCBN	IOCBN7	IOCBN6	IOCBN5	IOCBN4	IOCBN3	IOCBN2	IOCBN1	IOCBN0	00000000
F12h	IOCBF	IOCBF7	IOCBF6	IOCBF5	IOCBF4	IOCBF3	IOCBF2	IOCBF1	IOCBF0	00000000
F11h	ANSELA	ANSELA7	ANSELA6	ANSELA5	ANSELA4	ANSELA3	ANSELA2	ANSELA1	ANSELA0	11111111
F10h	WPUA	WPUA7	WPUA6	WPUA5	WPUA4	WPUA3	WPUA2	WPUA1	WPUA0	00000000
F0Fh	ODCONA	ODCA7	ODCA6	ODCA5	ODCA4	ODCA3	ODCA2	ODCA1	ODCA0	00000000
F0Eh	SLRCONA	SLRA7	SLRA6	SLRA5	SLRA4	SLRA3	SLRA2	SLRA1	SLRA0	11111111
F0Dh	INLVLA	INLVLA7	INLVLA6	INLVLA5	INLVLA4	INLVLA3	INLVLA2	INLVLA1	INLVLA0	11111111
F0Ch	IOCAP	IOCAP7	IOCAP6	IOCAP5	IOCAP4	IOCAP3	IOCAP2	IOCAP1	IOCAP0	00000000
F0Bh	IOCAN	IOCAN7	IOCAN6	IOCAN5	IOCAN4	IOCAN3	IOCAN2	IOCAN1	IOCAN0	00000000
F0Ah	IOCAF	IOCAF7	IOCAF6	IOCAF5	IOCAF4	IOCAF3	IOCAF2	IOCAF1	IOCAF0	00000000
F09h	RE2PPS(2)	—	—	—	RE2PPS<4:0>					---00000
F08h	RE1PPS(2)	—	—	—	RE1PPS<4:0>					---00000
F07h	RE0PPS(2)	—	—	—	RE0PPS<4:0>					---00000
F06h	RD7PPS(2)	—	—	—	RD7PPS<4:0>					---00000
F05h	RD6PPS(2)	—	—	—	RD6PPS<4:0>					---00000
F04h	RD5PPS(2)	—	—	—	RD5PPS<4:0>					---00000
F03h	RD4PPS(2)	—	—	—	RD4PPS<4:0>					---00000
F02h	RD3PPS(2)	—	—	—	RD3PPS<4:0>					---00000
F01h	RD2PPS(2)	—	—	—	RD2PPS<4:0>					---00000
F00h	RD1PPS(2)	—	—	—	RD1PPS<4:0>					---00000

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition

Note 1: Not available on LF devices.

2: Not available on PIC18(L)F26K40 (28-pin variants).

3: Not available on PIC18(L)F45K40 devices.

TABLE 10-5: REGISTER FILE SUMMARY FOR PIC18(L)F26/45/46K40 DEVICES (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR
EFFh	RD0PPS(2)	—	—	—	RD0PPS<4:0>					---00000
EFEh	RC7PPS	—	—	—	RC7PPS<4:0>					---00000
EFDh	RC6PPS	—	—	—	RC6PPS<4:0>					---00000
EFCh	RC5PPS	—	—	—	RC5PPS<4:0>					---00000
EFBh	RC4PPS	—	—	—	RC4PPS<4:0>					---00000
EFAh	RC3PPS	—	—	—	RC3PPS<4:0>					---00000
EF9h	RC2PPS	—	—	—	RC2PPS<4:0>					---00000
EF8h	RC1PPS	—	—	—	RC1PPS<4:0>					---00000
EF7h	RC0PPS	—	—	—	RC0PPS<4:0>					---00000
EF6h	RB7PPS	—	—	—	RB7PPS<4:0>					---00000
EF5h	RB6PPS	—	—	—	RB6PPS<4:0>					---00000
EF4h	RB5PPS	—	—	—	RB5PPS<4:0>					---00000
EF3h	RB4PPS	—	—	—	RB4PPS<4:0>					---00000
EF2h	RB3PPS	—	—	—	RB3PPS<4:0>					---00000
EF1h	RB2PPS	—	—	—	RB2PPS<4:0>					---00000
EF0h	RB1PPS	—	—	—	RB1PPS<4:0>					---00000
EEFh	RB0PPS	—	—	—	RB0PPS<4:0>					---00000
EEEh	RA7PPS	—	—	—	RA7PPS<4:0>					---00000
EEDh	RA6PPS	—	—	—	RA6PPS<4:0>					---00000
EECh	RA5PPS	—	—	—	RA5PPS<4:0>					---00000
EEBh	RA4PPS	—	—	—	RA4PPS<4:0>					---00000
EEAh	RA3PPS	—	—	—	RA3PPS<4:0>					---00000
EE9h	RA2PPS	—	—	—	RA2PPS<4:0>					---00000
EE8h	RA1PPS	—	—	—	RA1PPS<4:0>					---00000
EE7h	RA0PPS	—	—	—	RA0PPS<4:0>					---00000
EE6h	PMD5	—	—	—	—	—	—	—	DSMMD	-------0
EE5h	PMD4	UART2MD	UART1MD	MSSP2MD	MSSP1MD	—	—	—	CWG1MD	0000---0
EE4h	PMD3	—	—	—	—	PWM4MD	PWM3MD	CCP2MD	CCP1MD	----0000
EE3h	PMD2	—	DACMD	ADCMD	—	—	CMP2MD	CMP1MD	ZCDMD	-00--000
EE2h	PMD1	—	TMR6MD	TMR5MD	TMR4MD	TMR3MD	TMR2MD	TMR1MD	TMR0MD	-0000000
EE1h	PMD0	SYSCMD	FVRMD	HLVDMD	CRCMD	SCANMD	NVMMD	CLKRMD	IOCMD	00x00000
EE0h	BORCON	SBOREN	—	—	—	—	—	—	BORRDY	1------q
EDFh	VREGCON(1)	—	—	—	—	—	—	VREGPM	Reserved	------01
EDEh	OSCFRQ	—	—	—	—	HFFRQ<3:0>				----1111
EDDh	OSCTUNE	—	—	HFTUN<5:0>						--100000
EDCh	OSCEN	EXTOEN	HFOEN	MFOEN	LFOEN	SOSCEN	ADOEN	—	—	000000--
EDBh	OSCSTAT	EXTOR	HFOR	MFOR	LFOR	SOR	ADOR	—	PLLR	qqqqqq-q
EDAh	OSCCON3	CSWHOLD	SOSCPWR	—	ORDY	NOSCR	—	—	—	00-00---
ED9h	OSCCON2	—	COSC<2:0>			CDIV<3:0>				-qqqqqqq

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition

Note 1: Not available on LF devices.

2: Not available on PIC18(L)F26K40 (28-pin variants).

3: Not available on PIC18(L)F45K40 devices.

13.11.7 IN-CIRCUIT DEBUG (ICD) INTERACTION

The scanner freezes when an ICD halt occurs, and remains frozen until user-mode operation resumes. The debugger may inspect the SCANCON0 and SCANLADR registers to determine the state of the scan.

The ICD interaction with each operating mode is summarized in Table 13-4.

TABLE 13-4: ICD AND SCANNER INTERACTIONS

ICD Halt	Scanner Operating Mode		
	Peek	**Concurrent Triggered**	**Burst**
External Halt	If scanner would peek an instruction that is not executed (because of ICD entry), the peek will occur after ICD exit, when the instruction executes.	If external halt is asserted during a scan cycle, the instruction (delayed by scan) may or may not execute before ICD entry, depending on external halt timing.	If external halt is asserted during the BSF(SCANCON.GO), ICD entry occurs, and the burst is delayed until ICD exit. Otherwise, the current NVM-access cycle will complete, and then the scanner will be interrupted for ICD entry.
		If external halt is asserted during the cycle immediately prior to the scan cycle, both scan and instruction execution happen after the ICD exits.	If external halt is asserted during the burst, the burst is suspended and will resume with ICD exit.
PC Breakpoint		Scan cycle occurs before ICD entry and instruction execution happens after the ICD exits.	If PCPB (or single step) is on BSF(SCANCON.GO), the ICD is entered before execution; execution of the burst will occur at ICD exit, and the burst will run to completion. Note that the burst can be interrupted by an external halt.
Data Breakpoint		The instruction with the dataBP executes and ICD entry occurs immediately after. If scan is requested during that cycle, the scan cycle is postponed until the ICD exits.	
Single Step		If a scan cycle is ready after the debug instruction is executed, the scan will read PFM and then the ICD is re-entered.	
SWBP and ICDINST		If scan would stall a SWBP, the scan cycle occurs and the ICD is entered.	If SWBP replaces BSF(SCANCON.GO), the ICD will be entered; instruction execution will occur at ICD exit (from ICDINSTR register), and the burst will run to completion.

13.11.8 PERIPHERAL MODULE DISABLE

Both the CRC and scanner module can be disabled individually by setting the CRCMD and SCANMD bits of the PMD0 register (Register 7-1). The SCANMD can be used to enable or disable to the scanner module only if the SCANE bit of Configuration Word 4 is set. If the SCANE bit is cleared, then the scanner module is not available for use and the SCANMD bit is ignored.

REGISTER 18-3: TMR0L: TIMER0 COUNT REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
TMR0<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **TMR0<7:0>:** TMR0 Counter bits <7:0>

REGISTER 18-4: TMR0H: TIMER0 PERIOD REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
TMR0<15:8>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 When T016BIT = 0
PR0<7:0>: TMR0 Period Register Bits <7:0>
When T016BIT = 1
TMR0<15:8>: TMR0 Counter bits <15:8>

TABLE 18-1: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER0

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
TMR0L	TMR0<7:0>								226
TMR0H	TMR0<15:8>								226
T0CON0	T0EN	—	T0OUT	T016BIT	T0OUTPS<3:0>				224
T0CON1	T0CS<2:0>			T0ASYNC	T0CKPS<3:0>				225
T0CKIPPS	—	—	—	T0CKIPPS<4:0>					216
TMR0PPS	—	—	—	TMR0PPS<4:0>					216
INTCON	GIE/GIEH	PEIE/GIEL	IPEN	—	—	INT2EDG	INT1EDG	INT0EDG	170
PIR0	—	—	TMR0IF	IOCIF	—	INT2IF	INT1IF	INT0IF	171
PIE0	—	—	TMR0IE	IOCIE	—	INT2IE	INT1IE	INT0IE	179
IPR0	—	—	TMR0IP	IOCIP	—	INT2IP	INT1IP	INT0IP	187
PMD1	—	TMR6MD	TMR5MD	TMR4MD	TMR3MD	TMR2MD	TMR1MD	TMR0MD	69

Legend: — = Unimplemented location, read as ‘0’. Shaded cells are not used by the Timer0 module.

TABLE 22-4: SUMMARY OF REGISTERS ASSOCIATED WITH PWM

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
CCPTMRS	P4TSEL<1:0>		P3TSEL<1:0>		C2TSEL<1:0>		C1TSEL<1:0>		286
PWM3CON	EN	—	OUT	POL	—	—	—	—	285
PWM3DCH	DC<7:0>								287
PWM3DCL	DC<9:8>>		—	—	—	—	—	—	287
PWM4CON	EN	—	OUT	POL	—	—	—	—	285
PWM4DCH	DC<7:0>								287
PWM4DCL	DC<9:8>		—	—	—	—	—	—	287
INTCON	GIE/GIEH	PEIE/GIEL	IPEN	—	—	INT2EDG	INT1EDG	INT0EDG	170
PIE4	—	—	TMR6IE	TMR5IE	TMR4IE	TMR3IE	TMR2IE	TMR1IE	183
PIR4	—	—	TMR6IF	TMR5IF	TMR4IF	TMR3IF	TMR2IF	TMR1IF	175
IPR4	—	—	TMR6IP	TMR5IP	TMR4IP	TMR3IP	TMR2IP	TMR1IP	191
RxyPPS	—	—	—	RxyPPS<4:0>					218
TMR2	TMR2<7:0>								244*
PR2	PR2<7:0>								244*
T2CON	T2ON	T2CKPS<2:0>			T2OUTPS<3:0>				262
T2HLT	T2PSYNC	T2CPOL	T2CSYNC	T2MODE<4:0>					263
T2CLKCON	—	—	—	—	T2CS<3:0>				264
T2RST	—	—	—	—	T2RSEL<3:0>				265
PMD3	—	—	—	—	PWM4MD	PWM3MD	CCP2MD	CCP1MD	71

Legend: - = Unimplemented locations, read as '0', u = unchanged, x = unknown. Shaded cells are not used by the PWM.

* Not a physical location.

EQUATION 23-2: R-C CALCULATIONS

VPEAK = External voltage source peak voltage
f = External voltage source frequency
C = Series capacitor
R = Series resistor
V_C = Peak capacitor voltage
Φ = Capacitor induced zero crossing phase advance in radians
T_Φ = Time ZC event occurs before actual zero crossing

$$Z = \frac{V_{PEAK}}{3 \times 10^{-4}}$$

$$X_C = \frac{1}{2\pi fC}$$

$$R = \sqrt{Z^2 - X_C^2}$$

$$V_C = X_C(3 \times 10^{-4})$$

$$\Phi = \mathrm{Tan}^{-1}\left(\frac{X_C}{R}\right)$$

$$T\Phi = \frac{\Phi}{2\pi f}$$

EXAMPLE 23-1: R-C CALCULATIONS

VRMS = 120
VPEAK = VRMS *√2 = 169.7
f = 60 Hz
C = 0.1 µF

$$Z = \frac{V_{PEAK}}{3 \times 10^{-4}} = \frac{169.7}{3 \times 10^{-4}} = 565.7\text{k}\Omega$$

$$X_C = \frac{1}{2\pi fC} = \frac{1}{(2\pi \times 60 \times 1 \times 10^{-7})} = 26.53\text{k}\Omega$$

$$R = \sqrt{(Z^2 \times X_C^2)} = 565.1\text{k}\Omega \text{ (computed)}$$

$$R = 560\text{k}\Omega \text{ (used)}$$

$$Z_R = \sqrt{R^2 + X_C^2} = 560.6\text{k}\Omega \text{ (using actual resistor)}$$

$$I_{PEAK} = \frac{V_{PEAK}}{Z_R} = 302.7 \times 10^{-6}$$

$$V_C = X_C \times \mathrm{Ipeak} = 8.0\text{V}$$

$$\Phi = \mathrm{Tan}^{-1}\left(\frac{X_C}{R}\right) = 0.047 \text{ radians}$$

$$T\Phi = \frac{\Phi}{2\pi f} = 125.6\mu\text{s}$$

23.5.2 CORRECTION BY OFFSET CURRENT

When the waveform is varying relative to VSS, then the zero cross is detected too early as the waveform falls and too late as the waveform rises. When the waveform is varying relative to VDD, then the zero cross is detected too late as the waveform rises and too early as the waveform falls. The actual offset time can be determined for sinusoidal waveforms with the corresponding equations shown in Equation 23-3.

EQUATION 23-3: ZCD EVENT OFFSET

When External Voltage Source is relative to Vss:

$$T_{OFFSET} = \frac{\mathrm{asin}\left(\frac{V_{CPINV}}{V_{PEAK}}\right)}{2\pi \bullet Freq}$$

When External Voltage Source is relative to VDD:

$$T_{OFFSET} = \frac{\mathrm{asin}\left(\frac{V_{DD} - V_{CPINV}}{V_{PEAK}}\right)}{2\pi \bullet Freq}$$

This offset time can be compensated for by adding a pull-up or pull-down biasing resistor to the ZCD pin. A pull-up resistor is used when the external voltage source is varying relative to VSS. A pull-down resistor is used when the voltage is varying relative to VDD. The resistor adds a bias to the ZCD pin so that the target external voltage source must go to zero to pull the pin voltage to the VCPINV switching voltage. The pull-up or pull-down value can be determined with the equations shown in Equation 23-4.

EQUATION 23-4: ZCD PULL-UP/DOWN

When External Signal is relative to Vss:

$$R_{PULLUP} = \frac{R_{SERIES}(V_{PULLUP} - V_{CPINV})}{V_{CPINV}}$$

When External Signal is relative to VDD:

$$R_{PULLDOWN} = \frac{R_{SERIES}(V_{CPINV})}{(V_{DD} - V_{CPINV})}$$

FIGURE 24-6: SIMPLIFIED CWG BLOCK DIAGRAM (FORWARD AND REVERSE FULL-BRIDGE MODES)

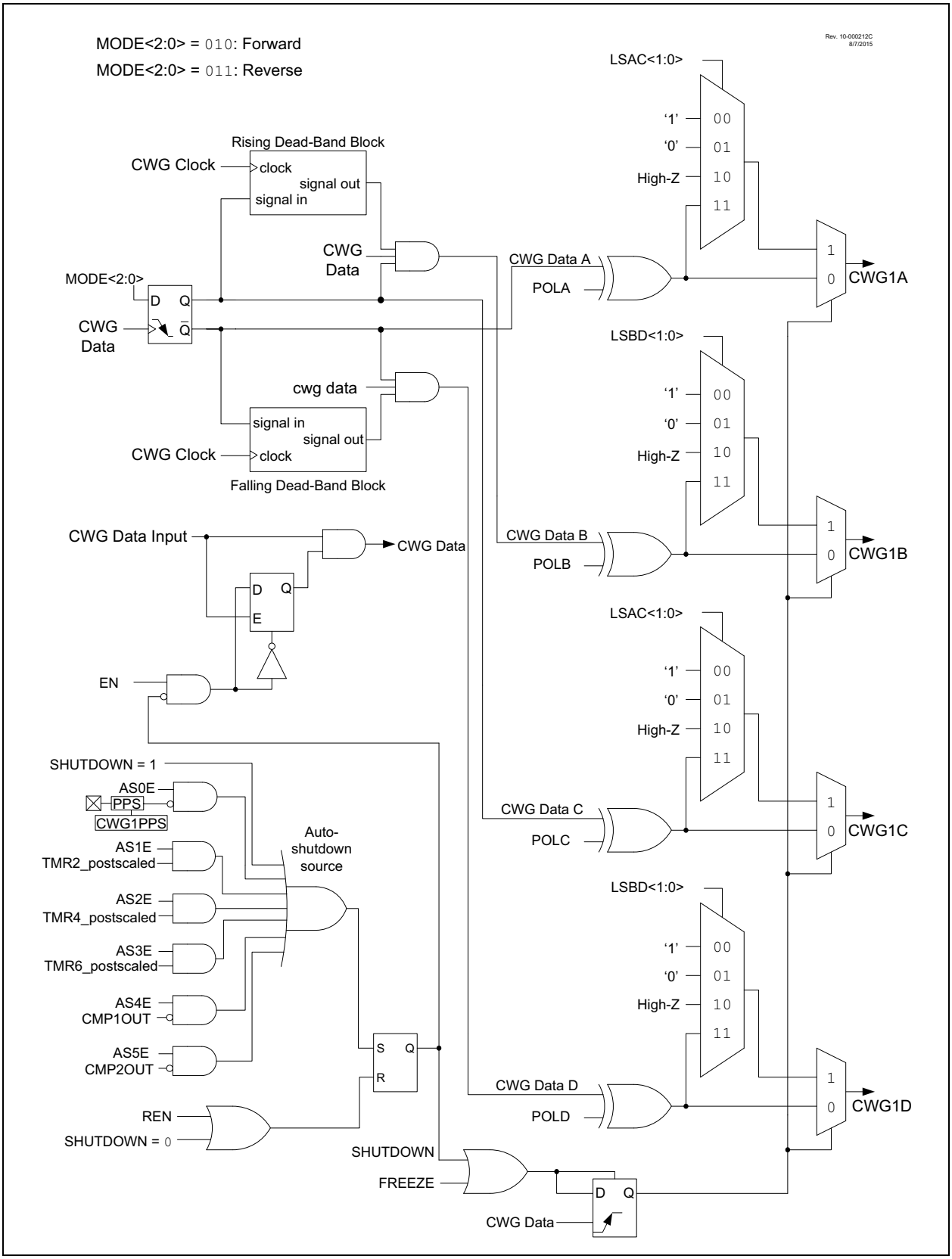


FIGURE 24-12: DEAD-BAND OPERATION, CWG1DBR = 0x01, CWG1DBF = 0x02

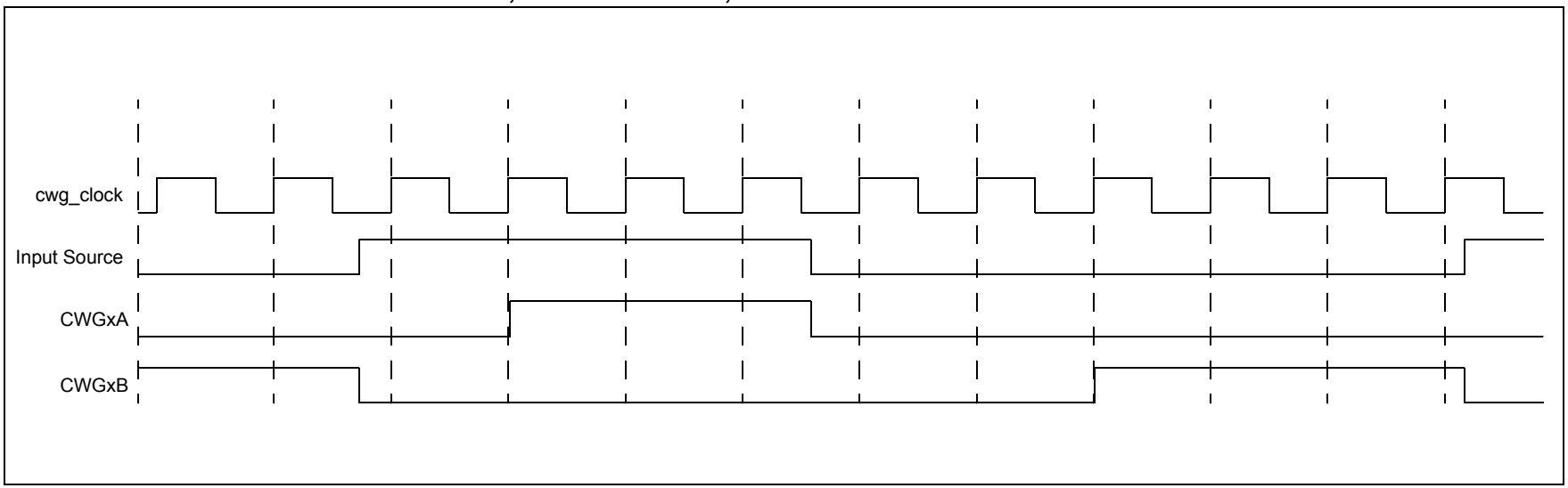


FIGURE 24-13: DEAD-BAND OPERATION, CWG1DBR = 0x03, CWG1DBF = 0x06, SOURCE SHORTER THAN DEAD BAND

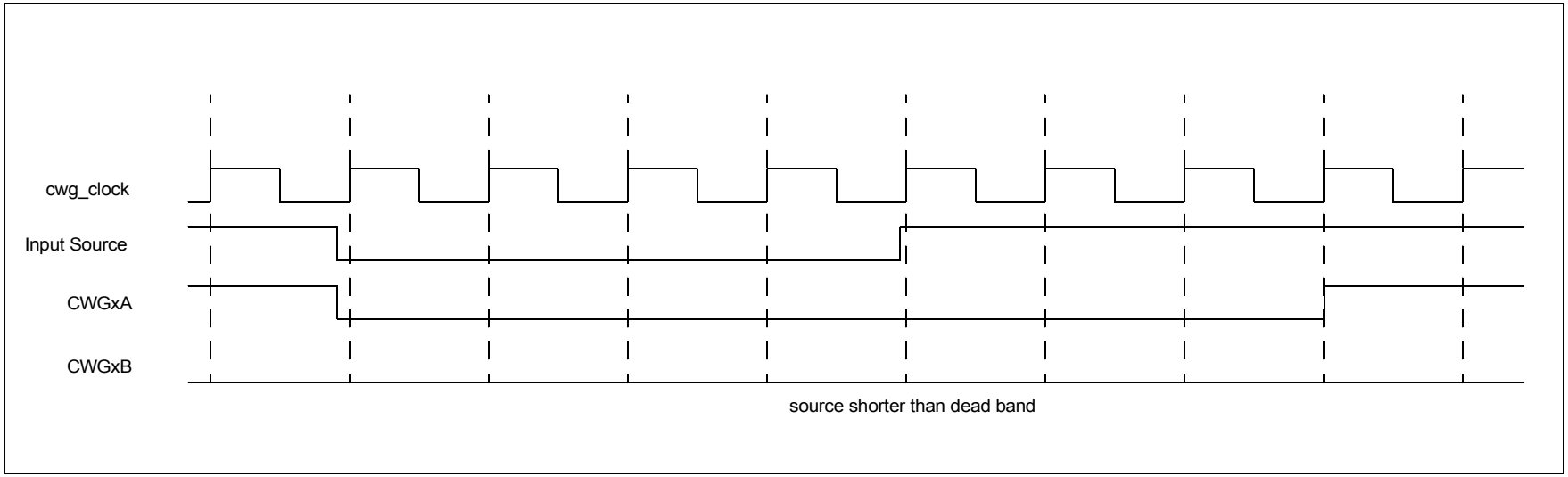
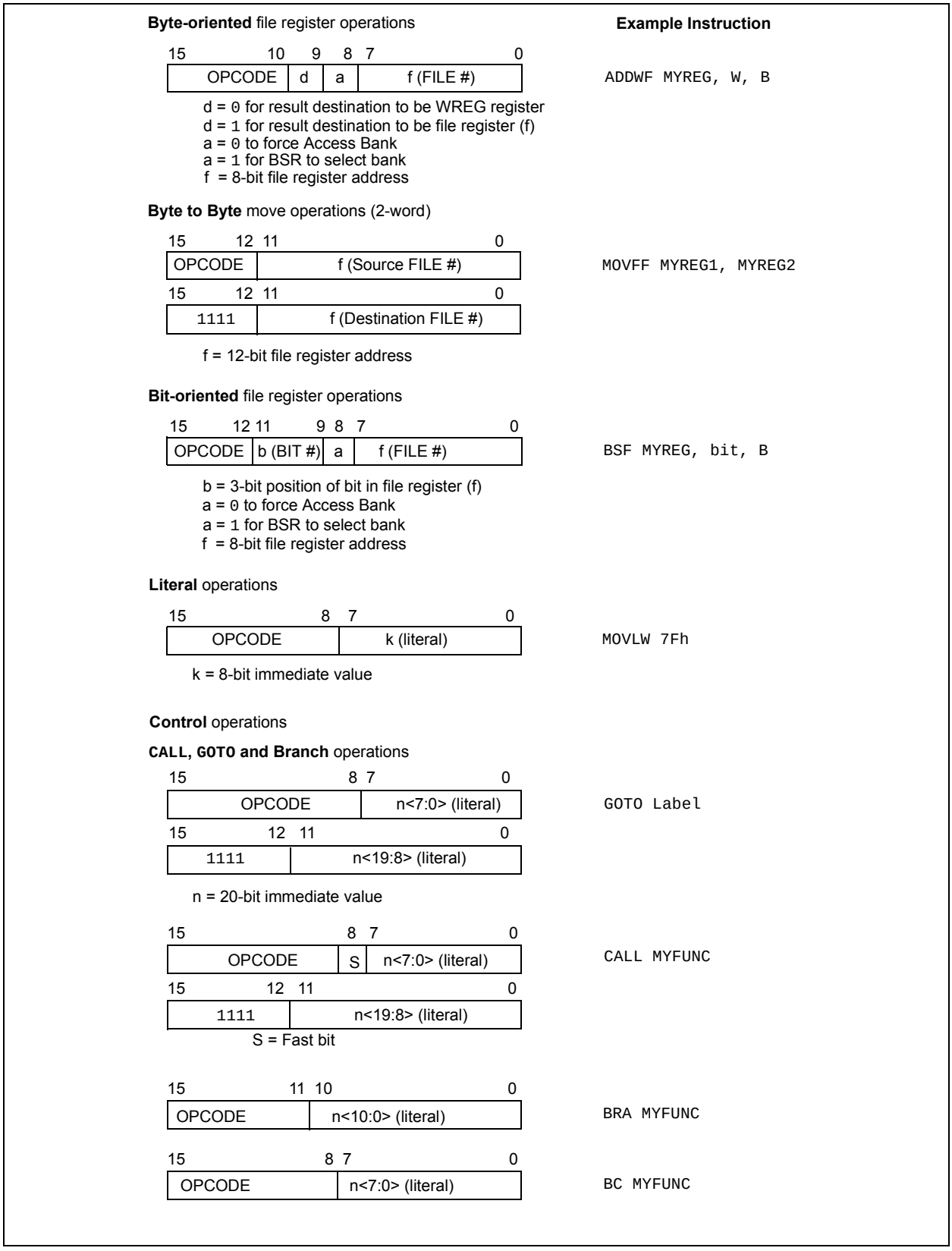


FIGURE 35-1: General Format for Instructions



ADDWFC **ADD W and CARRY bit to f**

Syntax: ADDWFC f {,d {,a}}

Operands: $0 \le f \le 255$
$d \in [0,1]$
$a \in [0,1]$

Operation: (W) + (f) + (C) → dest

Status Affected: N,OV, C, DC, Z

Encoding:

0010	00da	ffff	ffff

Description: Add W, the CARRY flag and data memory location 'f'. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is placed in data memory location 'f'.
If 'a' is '0', the Access Bank is selected.
If 'a' is '1', the BSR is used to select the GPR bank.
If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See **Section 35.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode"** for details.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

Example: `ADDWFC REG, 0, 1`

Before Instruction
CARRY bit = 1
REG = 02h
W = 4Dh
After Instruction
CARRY bit = 0
REG = 02h
W = 50h

ANDLW **AND literal with W**

Syntax: ANDLW k

Operands: $0 \le k \le 255$

Operation: (W) .AND. k → W

Status Affected: N, Z

Encoding:

0000	1011	kkkk	kkkk

Description: The contents of W are AND'ed with the 8-bit literal 'k'. The result is placed in W.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal 'k'	Process Data	Write to W

Example: `ANDLW 05Fh`

Before Instruction
W = A3h
After Instruction
W = 03h

LFSR **Load FSR**

Syntax: LFSR f, k

Operands: $0 \le f \le 2$
$0 \le k \le 4095$

Operation: $k \rightarrow FSRf$

Status Affected: None

Encoding:

1110 1111	1110 0000	00ff $k_7$kkk	k_{11}kkk kkkk

Description: The 12-bit literal 'k' is loaded into the File Select Register pointed to by 'f'.

Words: 2

Cycles: 2

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal 'k' MSB	Process Data	Write literal 'k' MSB to FSRfH
Decode	Read literal 'k' LSB	Process Data	Write literal 'k' to FSRfL

Example: `LFSR 2, 3ABh`

After Instruction
FSR2H = 03h
FSR2L = ABh

MOVF **Move f**

Syntax: MOVF f {,d {,a}}

Operands: $0 \le f \le 255$
$d \in [0,1]$
$a \in [0,1]$

Operation: $f \rightarrow dest$

Status Affected: N, Z

Encoding:

0101	00da	ffff	ffff

Description: The contents of register 'f' are moved to a destination dependent upon the status of 'd'. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is placed back in register 'f' (default). Location 'f' can be anywhere in the 256-byte bank.
If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank.
If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See **Section 35.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode"** for details.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write W

Example: `MOVF REG, 0, 0`

Before Instruction
REG = 22h
W = FFh
After Instruction
REG = 22h
W = 22h

ADDWF **ADD W to Indexed (Indexed Literal Offset mode)**

Syntax: ADDWF [k] {,d}

Operands: $0 \le k \le 95$
$d \in [0,1]$

Operation: (W) + ((FSR2) + k) → dest

Status Affected: N, OV, C, DC, Z

Encoding:

0010	01d0	kkkk	kkkk

Description: The contents of W are added to the contents of the register indicated by FSR2, offset by the value 'k'.
If 'd' is '0', the result is stored in W. If 'd' is '1', the result is stored back in register 'f' (default).

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read 'k'	Process Data	Write to destination

Example: ADDWF [OFST], 0

Before Instruction
W = 17h
OFST = 2Ch
FSR2 = 0A00h
Contents of 0A2Ch = 20h
After Instruction
W = 37h
Contents of 0A2Ch = 20h

BSF **Bit Set Indexed (Indexed Literal Offset mode)**

Syntax: BSF [k], b

Operands: $0 \le f \le 95$
$0 \le b \le 7$

Operation: 1 → ((FSR2) + k)<b>

Status Affected: None

Encoding:

1000	bbb0	kkkk	kkkk

Description: Bit 'b' of the register indicated by FSR2, offset by the value 'k', is set.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

Example: BSF [FLAG_OFST], 7

Before Instruction
FLAG_OFST = 0Ah
FSR2 = 0A00h
Contents of 0A0Ah = 55h
After Instruction
Contents of 0A0Ah = D5h

SETF **Set Indexed (Indexed Literal Offset mode)**

Syntax: SETF [k]

Operands: $0 \le k \le 95$

Operation: FFh → ((FSR2) + k)

Status Affected: None

Encoding:

0110	1000	kkkk	kkkk

Description: The contents of the register indicated by FSR2, offset by 'k', are set to FFh.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read 'k'	Process Data	Write register

Example: SETF [OFST]

Before Instruction
OFST = 2Ch
FSR2 = 0A00h
Contents of 0A2Ch = 00h
After Instruction
Contents of 0A2Ch = FFh

36.11 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

36.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent® and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika®

37.2 Standard Operating Conditions

The standard operating conditions for any device are defined as:

Operating Voltage: $V_{DDMIN} \leq V_{DD} \leq V_{DDMAX}$
Operating Temperature: $T_{A\_MIN} \leq T_A \leq T_{A\_MAX}$

V_{DD} — Operating Supply Voltage(1)

PIC18LF26/45/46K40

- V_{DDMIN} (Fosc ≤ 16 MHz) ..... +1.8V
- V_{DDMIN} (Fosc ≤ 32 MHz) ..... +2.5V
- V_{DDMIN} (Fosc ≤ 64 MHz) ..... +3.0V
- V_{DDMAX} ..... +3.6V

PIC18F26/45/46K40

- V_{DDMIN} (Fosc ≤ 16 MHz) ..... +2.3V
- V_{DDMIN} (Fosc ≤ 32 MHz) ..... +2.5V
- V_{DDMIN} (Fosc ≤ 64 MHz) ..... +3.0V
- V_{DDMAX} ..... +5.5V

T_A — Operating Ambient Temperature Range

Industrial Temperature

- T_{A_MIN} ..... -40°C
- T_{A_MAX} ..... +85°C

Extended Temperature

- T_{A_MIN} ..... -40°C
- T_{A_MAX} ..... +125°C

Note 1: See Parameter Supply Voltage, DS Characteristics: Supply Voltage.