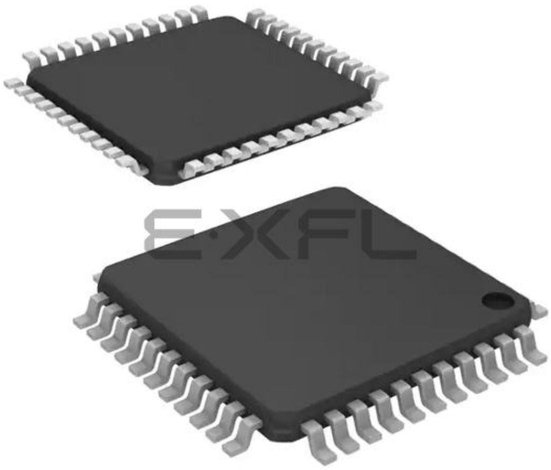

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	64MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 35x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f45k40-e-pt

PIC18(L)F2x/4xK40 Family Types

Device	Data Sheet Index	Program Memory Flash (bytes)	Data SRAM (bytes)	Data EEPROM (bytes)	I/O Pins	16-bit Timers	Comparators	10-bit ADC[2] with Computation (ch)	5-bit DAC	Zero-Cross Detect	CCP/10-bit PWM	CWG	8-bit TMR with HLT	Windowed Watchdog Timer	CRC with Memory Scan	EUSART	I^2C/SPI	PPS	Peripheral Module Disable	Temperature Indicator	Debug(1)
PIC18(L)F24K40	**(1)**	16k	1024	256	25	4	2	24	1	1	2/2	1	3	Y	Y	1	1	Y	Y	Y	I
PIC18(L)F25K40	**(1)**	32k	2048	256	25	4	2	24	1	1	2/2	1	3	Y	Y	1	1	Y	Y	Y	I
PIC18(L)F26K40	**(2)**	64k	3728	1024	25	4	2	24	1	1	2/2	1	3	Y	Y	2	2	Y	Y	Y	I
PIC18(L)F27K40	**(3)**	128k	3728	1024	25	4	2	24	1	1	2/2	1	3	Y	Y	2	2	Y	Y	Y	I
PIC18(L)F45K40	**(2)**	32k	2048	256	36	4	2	35	1	1	2/2	1	3	Y	Y	2	2	Y	Y	Y	I
PIC18(L)F46K40	**(2)**	64k	3728	1024	36	4	2	35	1	1	2/2	1	3	Y	Y	2	2	Y	Y	Y	I
PIC18(L)F47K40	**(3)**	128k	3728	1024	36	4	2	35	1	1	2/2	1	3	Y	Y	2	2	Y	Y	Y	I

Note 1: Debugging Methods: (I) – Integrated on Chip.

Data Sheet Index: (Unshaded devices are described in this document.)

1. DS40001843 PIC18(L)F24/25K40 Data Sheet, 28-Pin, 8-bit Flash Microcontrollers
2. DS40001816 PIC18(L)F26/45/46K40 Data Sheet, 28/40/44-Pin, 8-bit Flash Microcontrollers
3. DS40001844 PIC18(L)F27/47K40 Data Sheet, 28/40/44-Pin, 8-bit Flash Microcontrollers

Note: For other small form-factor package availability and marking information, please visit **http://www.microchip.com/packaging** or contact your local sales office.

REGISTER 7-6: PMD5: PMD CONTROL REGISTER 5

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0/0
—	—	—	—	—	—	—	DSMMD
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	q = Value depends on condition

bit 7-1 **Unimplemented:** Read as ‘0’

bit 0 **DSMMD:** Disable Data Signal Modulator bit
1 = DSM module disabled
0 = DSM module enabled

TABLE 7-1: SUMMARY OF REGISTERS ASSOCIATED WITH PMD

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
PMD0	SYSCMD	FVRMD	HLVDMD	CRCMD	SCANMD	NVMMD	CLKRMD	IOCMD	68
PMD1	—	TMR6MD	TMR5MD	TMR4MD	TMR3MD	TMR2MD	TMR1MD	TMR0MD	69
PMD2	—	DACMD	ADCMD	—	—	CMP2MD	CMP1MD	ZCDMD	70
PMD3	—	—	—	—	PWM4MD	PWM3MD	CCP2MD	CCP1MD	71
PMD4	UART2MD	UART1MD	MSSP2MD	MSSP1MD	—	—	—	CWG1MD	72
PMD5	—	—	—	—	—	—	—	DSMMD	73

Legend: — = unimplemented, read as ‘0’. Shaded cells are not used by the PMD.

The user needs to load the TBLPTR and TABLAT register with the address and data byte respectively before executing the write command. An unlock sequence needs to be followed for writing to the USER IDs/ DEVICE IDs/CONFIG words (Section 11.1.4, NVM Unlock Sequence). If WRTC = 0 or if TBLPTR points an invalid address location (see Table 11-3), WR bit is cleared without any effect and WRERR is set.

A single CONFIG word byte is written at once and the operation includes an implicit erase cycle for that byte (it is not necessary to set FREE). CPU execution is stalled and at the completion of the write cycle, the WR bit is cleared in hardware and the NVM Interrupt Flag bit (NVMIF) is set. The new CONFIG value takes effect when the CPU resumes operation.

TABLE 11-4: USER ID, DEV/REV ID AND CONFIGURATION WORD ACCESS (NVMREG<1:0> = X1)

Address	Function	Read Access	Write Access
20 0000h-20 000Fh	User IDs	Yes	Yes
3F FFFCh-3F FFFFh	Revision ID/Device ID	Yes	No
30 0000h-30 000Bh	Configuration Words 1-6	Yes	Yes

REGISTER 11-5: NVMDAT: DATA EEPROM MEMORY DATA

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
NVMDAT<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
x = Bit is unknown	‘0’ = Bit is cleared	‘1’ = Bit is set
-n = Value at POR		

bit 7-0 **NVMDAT<7:0>:** The value of the data memory word returned from NVMADR after a Read command, or the data written by a Write command.

TABLE 11-5: SUMMARY OF REGISTERS ASSOCIATED WITH DATA EEPROM MEMORY

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
NVMCON1	NVMREG<1:0>		—	FREE	WRERR	WREN	WR	RD	145
NVMCON2	Unlock Pattern								146
NVMADRL	NVMADR<7:0>								146
NVMADRH[(1)]	—	—	—	—	—	—	NVMADR<9:8>		146
NVMDAT	NVMDAT<7:0>								147
TBLPTRU	—	—	Program Memory Table Pointer (TBLPTR<21:16>)						127*
TBLPTRH	Program Memory Table Pointer (TBLPTR<15:8>)								127*
TBLPTRL	Program Memory Table Pointer (TBLPTR<7:0>)								127*
TABLAT	TABLAT								126*
INTCON	GIE/GIEH	PEIE/GIEL	IPEN	—	—	INT2EDG	INT1EDG	INT0EDG	170
PIE7	SCANIE	CRCIE	NVMIE	—	—	—	—	CWG1IE	186
PIR7	SCANIF	CRCIF	NVMIF	—	—	—	—	CWG1IF	178
IPR7	SCANIP	CRCIP	NVMIP	—	—	—	—	CWG1IP	194

Legend: — = unimplemented, read as ‘0’. Shaded bits are not used during EEPROM access.

*Page provides register information.

Note 1: The NVMADRH register is not implemented on PIC18(L)F26/45/46K40.

REGISTER 13-9: CRCXORH: CRC XOR HIGH BYTE REGISTER

R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x
X<15:8>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **X<15:8>**: XOR of Polynomial Term XN Enable bits

REGISTER 13-10: CRCXORL: CRC XOR LOW BYTE REGISTER

R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	U-1
X<7:1>							—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-1 **X<7:1>**: XOR of Polynomial Term XN Enable bits

bit 0 **Unimplemented:** Read as ‘1’

REGISTER 14-3: PIR1: PERIPHERAL INTERRUPT REQUEST (FLAG) REGISTER 1

R/W-0/0	R/W-0/0	U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0
OSCFIF	CSWIF(1)	—	—	—	—	ADTIF	ADIF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **OSCFIF:** Oscillator Fail Interrupt Flag bit
1 = Device oscillator failed, clock input has changed to HFINTOSC (must be cleared by software)
0 = Device clock operating

bit 6 **CSWIF:** Clock-Switch Interrupt Flag bit(1)
1 = New oscillator is ready for switch (must be cleared by software) (see Figure 4-6 and Figure 4-7)
0 = New oscillator is not ready for switch or has not been started

bit 5-2 **Unimplemented:** Read as ‘0’

bit 1 **ADTIF:** ADC Threshold Interrupt Flag bit
1 = ADC Threshold interrupt has occurred (must be cleared by software)
0 = ADC Threshold event is not complete or has not been started

bit 0 **ADIF:** ADC Interrupt Flag bit
1 = An A/D conversion completed (must be cleared by software)
0 = The A/D conversion is not complete or has not been started

Note 1: The CSWIF interrupt will not wake the system from Sleep. The system will sleep until another interrupt causes the wake-up.

REGISTER 14-25: IPR7: PERIPHERAL INTERRUPT PRIORITY REGISTER 7

R/W-1/1	R/W-1/1	R/W-1/1	U-0	U-0	U-0	U-0	R/W-1/1
SCANIP	CRCIP	NVMIP	—	—	—	—	CWG1IP
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **SCANIP:** SCAN Interrupt Priority bit
1 = High priority
0 = Low priority

bit 6 **CRCIP:** CRC Interrupt Priority bit
1 = High priority
0 = Low priority

bit 5 **NVMIP:** NVM Interrupt Priority bit
1 = High priority
0 = Low priority

bit 4-1 **Unimplemented:** Read as ‘0’

bit 0 **CWG1IP:** CWG Interrupt Priority bit
1 = High priority
0 = Low priority

17.3 Bidirectional Pins

PPS selections for peripherals with bidirectional signals on a single pin must be made so that the PPS input and PPS output select the same pin. Peripherals that have bidirectional signals include:

- EUSART (synchronous operation)
- MSSP (I^2C)
- CCP module

Note:	The I^2C default input pins are I^2C and SMBus compatible. RB1 and RB2 are additional pins. RC4 and RC3 are default MMP1 pins and are SMBus compatible. Clock and data signals can be routed to any pin, however pins without I^2C compatibility will operate at standard TTL/ST logic levels as selected by the INVLV register.

17.4 PPS Lock

The PPS includes a mode in which all input and output selections can be locked to prevent inadvertent changes. PPS selections are locked by setting the PPSLOCKED bit of the PPSLOCK register. Setting and clearing this bit requires a special sequence as an extra precaution against inadvertent changes. Examples of setting and clearing the PPSLOCKED bit are shown in Example 17-1.

EXAMPLE 17-1: PPS LOCK SEQUENCE

```
; Disable interrupts:
    BCF      INTCON,GIE

; Bank to PPSLOCK register
    BANKSEL  PPSLOCK
    MOVLB    PPSLOCK
    MOVLW    55h

; Required sequence, next 4 instructions
    MOVWF    PPSLOCK
    MOVLW    AAh
    MOVWF    PPSLOCK

; Set PPSLOCKED bit to disable writes
; Only a BSF instruction will work
    BSF      PPSLOCK,0

; Enable Interrupts
    BSF      INTCON,GIE
```

EXAMPLE 17-2: PPS UNLOCK SEQUENCE

```
; Disable interrupts:
    BCF      INTCON,GIE

; Bank to PPSLOCK register
    BANKSEL  PPSLOCK
    MOVLB    PPSLOCK
    MOVLW    55h

; Required sequence, next 4 instructions
    MOVWF    PPSLOCK
    MOVLW    AAh
    MOVWF    PPSLOCK

; Clear PPSLOCKED bit to enable writes
; Only a BCF instruction will work
    BCF      PPSLOCK,0

; Enable Interrupts
    BSF      INTCON,GIE
```

17.5 PPS One-Way Lock

Using the PPS1WAY Configuration bit, the PPS settings can be locked in. When this bit is set, the PPSLOCKED bit can only be cleared and set one time after a device Reset. This allows for clearing the PPSLOCKED bit so that the input and output selections can be made during initialization. When the PPSLOCKED bit is set after all selections have been made, it will remain set and cannot be cleared until after the next device Reset event.

17.6 Operation During Sleep

PPS input and output selections are unaffected by Sleep.

17.7 Effects of a Reset

A device Power-on-Reset (POR) clears all PPS input and output selections to their default values. All other Resets leave the selections unchanged. Default input selections are shown in the **Section “Pin Allocation Tables”**.The PPS one-way is also removed.

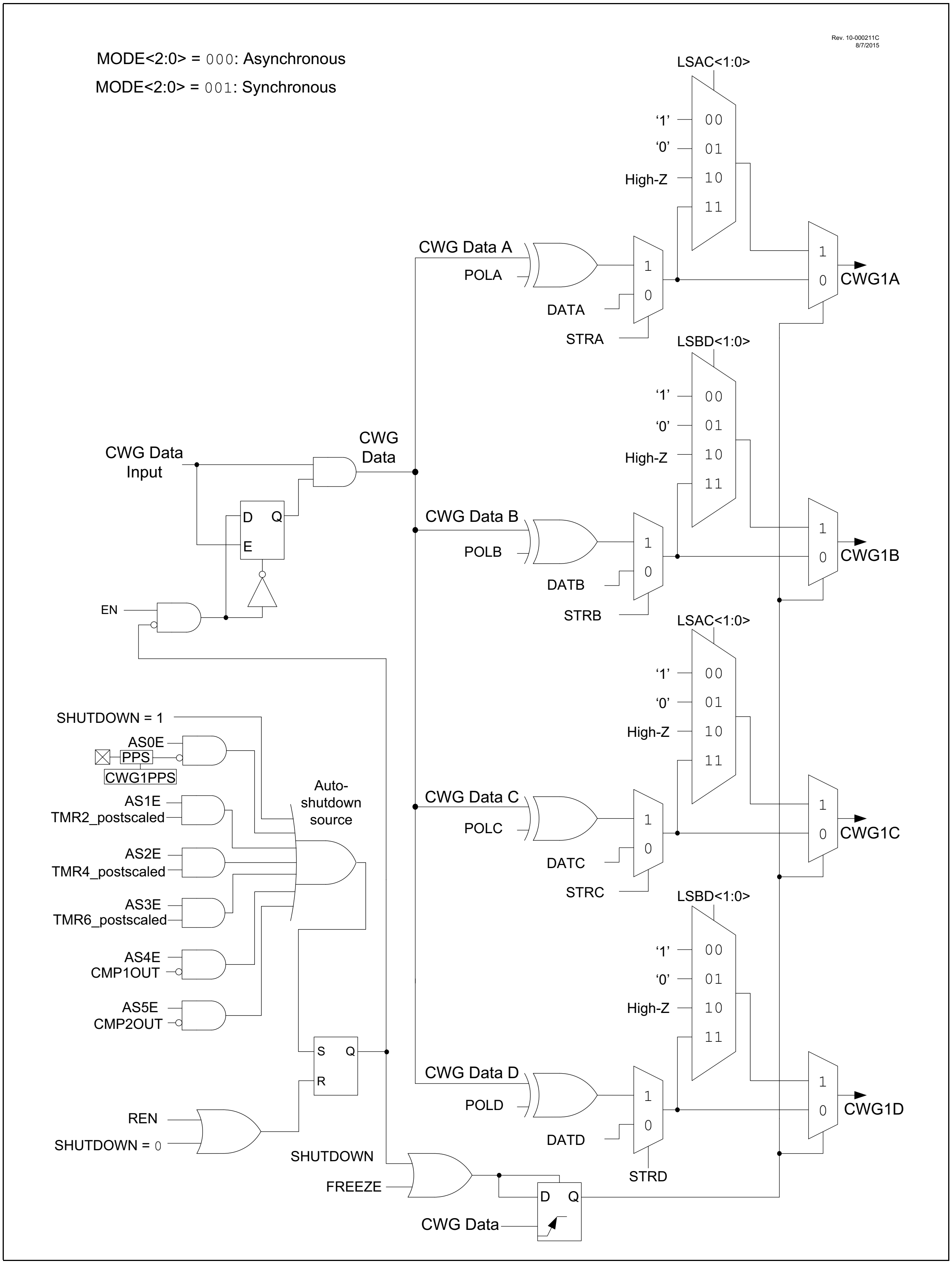
REGISTER 21-5: CCPRxH: CCPx REGISTER HIGH BYTE

R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x
CCPRx<15:8>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 MODE = Capture Mode:
CCPRxH<7:0>: MSB of captured TMR1 value
MODE = Compare Mode:
CCPRxH<7:0>: MSB compared to TMR1 value
MODE = PWM Mode && FMT = 0:
CCPRxH<7:2>: Not used
CCPRxH<1:0>: CCPW<9:8> – Pulse-Width MS 2 bits
MODE = PWM Mode && FMT = 1:
CCPRxH<7:0>: CCPW<9:2> – Pulse-Width MS 8 bits

FIGURE 24-11: SIMPLIFIED CWG BLOCK DIAGRAM (OUTPUT STEERING MODES)



REGISTER 25-2: MDCON1: MODULATION CONTROL REGISTER 1

U-0	U-0	R/W-0/0	R/W-0/0	U-0	U-0	R/W-0/0	R/W-0/0
—	—	CHPOL	CHSYNC	—	—	CLPOL	CLSYNC
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5 **CHPOL:** Modulator High Carrier Polarity Select bit
1 = Selected high carrier signal is inverted
0 = Selected high carrier signal is not inverted

bit 4 **CHSYNC:** Modulator High Carrier Synchronization Enable bit
1 = Modulator waits for a falling edge on the high time carrier signal before allowing a switch to the low time carrier
0 = Modulator output is not synchronized to the high time carrier signal(1)

bit 3-2 **Unimplemented:** Read as ‘0’

bit 1 **CLPOL:** Modulator Low Carrier Polarity Select bit
1 = Selected low carrier signal is inverted
0 = Selected low carrier signal is not inverted

bit 0 **CLSYNC:** Modulator Low Carrier Synchronization Enable bit
1 = Modulator waits for a falling edge on the low time carrier signal before allowing a switch to the high time carrier
0 = Modulator output is not synchronized to the low time carrier signal(1)

Note 1: Narrowed carrier pulse widths or spurs may occur in the signal stream if the carrier is not synchronized.

26.4 Register Definitions: MSSP Control

REGISTER 26-1: SSPxSTAT: MSSPx STATUS REGISTER (SPI MODE)

R/W-0	R/W-0	R-0	R-0	R-0	R-0	R-0	R-0
SMP	CKE(1)	D/$\overline{\text{A}}$	P	S	R/$\overline{\text{W}}$	UA	BF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **SMP:** Sample bit
<u>SPI Master mode:</u>
1 = Input data is sampled at the end of data output time
0 = Input data is sampled at the middle of data output time
<u>SPI Slave mode:</u>
SMP must be cleared when SPI is used in Slave mode.

bit 6 **CKE:** SPI Clock Select bit(1)
1 = Transmit occurs on the transition from active to Idle clock state
0 = Transmit occurs on the transition from Idle to active clock state

bit 5 **D/$\overline{\text{A}}$:** Data/$\overline{\text{Address}}$ bit
Used in I^2C mode only.

bit 4 **P:** Stop bit
Used in I^2C mode only. This bit is cleared when the MSSPx module is disabled; SSPEN is cleared.

bit 3 **S:** Start bit
Used in I^2C mode only.

bit 2 **R/$\overline{\text{W}}$:** Read/$\overline{\text{Write}}$ Information bit
Used in I^2C mode only.

bit 1 **UA:** Update Address bit
Used in I^2C mode only.

bit 0 **BF:** Buffer Full Status bit (Receive mode only)
1 = Receive is complete, SSPxBUF is full
0 = Receive is not complete, SSPxBUF is empty

Note 1: Polarity of clock state is set by the CKP bit (SSPxCON1<4>).

27.2.1.5 TSR Status

The TRMT bit of the TXxSTA register indicates the status of the TSR register. This is a read-only bit. The TRMT bit is set when the TSR register is empty and is cleared when a character is transferred to the TSR register from the TXxREG. The TRMT bit remains clear until all bits have been shifted out of the TSR register. No interrupt logic is tied to this bit, so the user has to poll this bit to determine the TSR status.

Note:	The TSR register is not mapped in data memory, so it is not available to the user.

27.2.1.6 Transmitting 9-Bit Characters

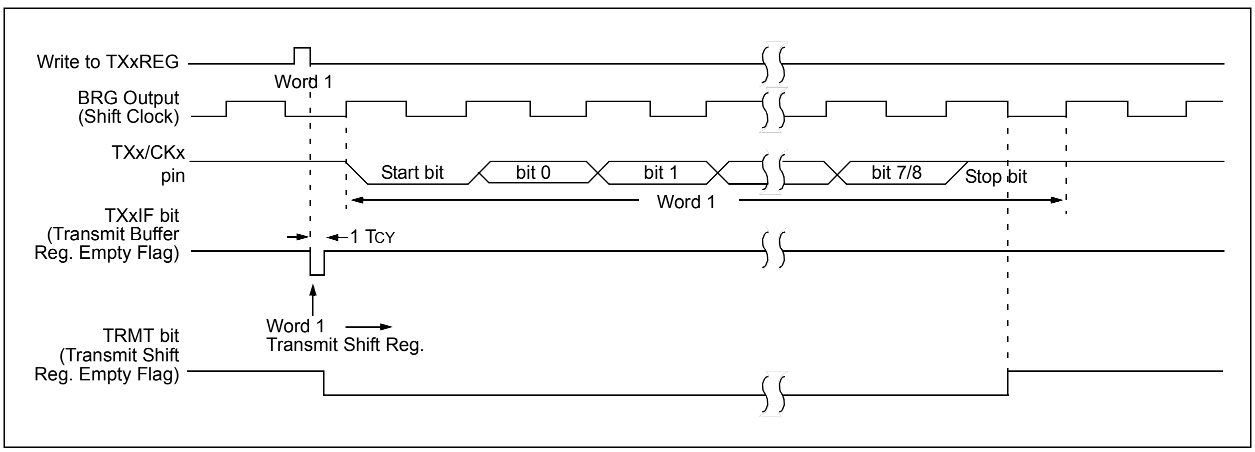
The EUSART supports 9-bit character transmissions. When the TX9 bit of the TXxSTA register is set, the EUSART will shift nine bits out for each character transmitted. The TX9D bit of the TXxSTA register is the ninth, and Most Significant data bit. When transmitting 9-bit data, the TX9D data bit must be written before writing the eight Least Significant bits into the TXxREG. All nine bits of data will be transferred to the TSR shift register immediately after the TXxREG is written.

A special 9-bit Address mode is available for use with multiple receivers. See **Section 27.2.2.7 “Address Detection”** for more information on the Address mode.

27.2.1.7 Asynchronous Transmission Setup:

1. Initialize the SPxBRGH, SPxBRGL register pair and the BRGH and BRG16 bits to achieve the desired baud rate (see **Section 27.4 “EUSART Baud Rate Generator (BRG)”**).
2. Enable the asynchronous serial port by clearing the SYNC bit and setting the SPEN bit.
3. If 9-bit transmission is desired, set the TX9 control bit. A set ninth data bit will indicate that the eight Least Significant data bits are an address when the receiver is set for address detection.
4. Set SCKP bit if inverted transmit is desired.
5. Enable the transmission by setting the TXEN control bit. This will cause the TXxIF interrupt bit to be set.
6. If interrupts are desired, set the TXxIE interrupt enable bit of the PIE3 register. An interrupt will occur immediately provided that the GIE and PEIE bits of the INTCON register are also set.
7. If 9-bit transmission is selected, the ninth bit should be loaded into the TX9D data bit.
8. Load 8-bit data into the TXxREG register. This will start the transmission.

FIGURE 27-3: ASYNCHRONOUS TRANSMISSION



30.6 Register Definitions: DAC Control

Long bit name prefixes for the DAC peripheral is shown in Table 30-1. Refer to **Section 1.4.2.2 "Long Bit Names"** for more information.

TABLE 30-1:

Peripheral	Bit Name Prefix
DAC	DAC

REGISTER 30-1: DAC1CON0: DAC CONTROL REGISTER

R/W-0/0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	R/W-0/0
EN	—	OE1	OE2	PSS<1:0>		—	NSS
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **EN:** DAC Enable bit
1 = DAC is enabled
0 = DAC is disabled

bit 6 **Unimplemented:** Read as '0'

bit 5 **OE1:** DAC Voltage Output Enable bit
1 = DAC voltage level is output on the DAC1OUT1 pin
0 = DAC voltage level is disconnected from the DAC1OUT1 pin

bit 4 **OE2:** DAC Voltage Output Enable bit
1 = DAC voltage level is output on the DAC1OUT2 pin
0 = DAC voltage level is disconnected from the DAC1OUT2 pin

bit 3-2 **PSS<1:0>:** DAC Positive Source Select bit
11 = Reserved
10 = FVR buffer
01 = VREF+
00 = AVDD

bit 1 **Unimplemented:** Read as '0'

bit 0 **NSS:** DAC Negative Source Select bit
1 = VREF-
0 = AVSS

31.3 ADC Acquisition Requirements

For the ADC to meet its specified accuracy, the charge holding capacitor (C_{HOLD}) must be allowed to fully charge to the input channel voltage level. The Analog Input model is shown in Figure 31-4. The source impedance (R_S) and the internal sampling switch (R_{SS}) impedance directly affect the time required to charge the capacitor C_{HOLD}. The sampling switch (R_{SS}) impedance varies over the device voltage (V_{DD}), refer to Figure 31-4. **The maximum recommended impedance for analog sources is 10 kΩ.** As the source impedance is decreased, the acquisition time may be decreased. After the analog input channel is selected (or changed), an ADC acquisition must be completed before the conversion can be started. To calculate the minimum acquisition time, Equation 31-1 may be used. This equation assumes that 1/2 LSb error is used (1,024 steps for the ADC). The 1/2 LSb error is the maximum error allowed for the ADC to meet its specified resolution.

EQUATION 31-1: ACQUISITION TIME EXAMPLE

Assumptions: Temperature = 50°C and external impedance of 10kΩ 5.0V V_{DD}

$$T_{ACQ} = \text{Amplifier Settling Time} + \text{Hold Capacitor Charging Time} + \text{Temperature Coefficient}$$
$$= T_{AMP} + T_C + T_{COFF}$$
$$= 2\mu s + T_C + [(\text{Temperature} - 25°C)(0.05\mu s/°C)]$$

The value for T_C can be approximated with the following equations:

$$V_{APPLIED}\left(1 - \frac{1}{(2^{n+1}) - 1}\right) = V_{CHOLD} \quad \text{;[1] } V_{CHOLD} \text{ charged to within 1/2 lsb}$$

$$V_{APPLIED}\left(1 - e^{\frac{-T_C}{RC}}\right) = V_{CHOLD} \quad \text{;[2] } V_{CHOLD} \text{ charge response to } V_{APPLIED}$$

$$V_{APPLIED}\left(1 - e^{\frac{-T_C}{RC}}\right) = V_{APPLIED}\left(1 - \frac{1}{(2^{n+1}) - 1}\right) \quad \text{;combining [1] and [2]}$$

Note: Where n = number of bits of the ADC.

Solving for T_C:

$$T_C = -C_{HOLD}(R_{IC} + R_{SS} + R_S)\ \ln(1/2047)$$
$$= -10pF(1k\Omega + 7k\Omega + 10k\Omega)\ \ln(0.0004885)$$
$$= 1.37\mu s$$

Therefore:

$$T_{ACQ} = 2\mu s + 892ns + [(50°C - 25°C)(0.05\mu s/°C)]$$
$$= 4.62\mu s$$

Note 1: The reference voltage (V_{REF}) has no effect on the equation, since it cancels itself out.

2: The charge holding capacitor (C_{HOLD}) is not discharged after each conversion.

3: The maximum recommended impedance for analog sources is 10 kΩ. This is required to meet the pin leakage specification.

TABLE 31-3: COMPUTATION MODES

		Bit Clear Conditions	Value after Trigger completion		Threshold Operations			Value at ADTIF interrupt		
Mode	ADMD	ADACC and ADCNT	ADACC	ADCNT	Retrigger	Threshold Test	Interrupt	ADAOV	ADFLTR	ADCNT
Basic	0	ADACLR = 1	Unchanged	Unchanged	No	Every Sample	If thresh-old=true	N/A	N/A	count
Accumulate	1	ADACLR = 1	S + ADACC or (S2-S1) + ADACC	If (ADCNT=FF): ADCNT, otherwise: ADCNT+1	No	Every Sample	If thresh-old=true	ADACC Overflow	$ADACC/2^{ADCRS}$	count
Average	2	ADACLR = 1 or ADCNT>=ADRPT at ADGO or retrigger	S + ADACC or (S2-S1) + ADACC	If (ADCNT=FF): ADCNT, otherwise: ADCNT+1	No	If ADCNT>= ADRPT	If thresh-old=true	ADACC Overflow	$ADACC/2^{ADCRS}$	count
Burst Average	3	ADACLR = 1 or ADGO set or retrigger	Each repetition: same as Average End with sum of all samples	Each repetition: same as Average End with ADCNT=ADRPT	Repeat while ADCNT<ADRPT	If ADCNT>= ADRPT	If thresh-old=true	ADACC Overflow	$ADACC/2^{ADCRS}$	ADRPT
Low-pass Filter	4	ADACLR = 1	$S+ADACC-ADACC/2^{ADCRS}$ or $(S2-S1)+ADACC-ADACC/2^{ADCRS}$	If (ADCNT=FF): ADCNT, otherwise: ADCNT+1	No	If ADCNT>= ADRPT	If thresh-old=true	ADACC Overflow	Filtered Value	count

Note: S1 and S2 are abbreviations for Sample 1 and Sample 2, respectively. When ADDSEN = 0, S1 = ADRES; When ADDSEN = 1, S1 = ADPREV and S2 = ADRES.

REGISTER 31-27: ADERRL: ADC SETPOINT ERROR LOW BYTE REGISTER

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
ADERR<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **ADERR<7:0>**: ADC Setpoint Error LSB. Lower byte of ADC Setpoint Error calculation is determined by ADCALC bits of ADCON3, see Register 23-1 for more details.

REGISTER 31-28: ADLTHH: ADC LOWER THRESHOLD HIGH BYTE REGISTER

R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x
ADLTH<15:8>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **ADLTH<15:8>**: ADC Lower Threshold MSB. ADLTH and ADUTH are compared with ADERR to set the ADUTHR and ADLTHR bits of ADSTAT. Depending on the setting of ADTMD, an interrupt may be triggered by the results of this comparison.

REGISTER 31-29: ADLTHL: ADC LOWER THRESHOLD LOW BYTE REGISTER

R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x
ADLTH<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **ADLTH<7:0>**: ADC Lower Threshold LSB. ADLTH and ADUTH are compared with ADERR to set the ADUTHR and ADLTHR bits of ADSTAT. Depending on the setting of ADTMD, an interrupt may be triggered by the results of this comparison.

REGISTER 33-2: HLVDCON0: HIGH/LOW-VOLTAGE DETECT CONTROL REGISTER 0

R/W-0/0	U-0	R-x	R-x	U-0	U-0	R/W-0/0	R/W-0/0
EN	—	OUT	RDY	—	—	INTH	INTL
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **EN:** High/Low-voltage Detect Power Enable bit
1 = Enables HLVD, powers up HLVD circuit and supporting reference circuitry
0 = Disables HLVD, powers down HLVD and supporting circuitry

bit 6 **Unimplemented:** Read as ‘0’

bit 5 **OUT:** HLVD Comparator Output bit
1 = Voltage ≤ selected detection limit (HLVDL<3:0>)
0 = Voltage ≥ selected detection limit (HLVDL<3:0>)

bit 4 **RDY:** Band Gap Reference Voltages Stable Status Flag bit
1 = Indicates HLVD Module is ready and output is stable
0 = Indicates HLVD Module is not ready

bit 3-2 **Unimplemented:** Read as ‘0’

bit 1 **INTH:** HLVD Positive going (High Voltage) Interrupt Enable
1 = HLVDIF will be set when voltage ≥ selected detection limit (HLVDSEL<3:0>)
0 = HLVDIF will not be set

bit 0 **INTL:** HLVD Negative going (Low Voltage) Interrupt Enable
1 = HLVDIF will be set when voltage ≤ selected detection limit (HLVDSEL<3:0>)
0 = HLVDIF will not be set

TABLE 33-2: REGISTERS ASSOCIATED WITH HIGH/LOW-VOLTAGE DETECT MODULE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
HLVDCON0	EN	—	OUT	RDY	—	—	INTH	INTL	482
HLVDCON1	—	—	—	—	SEL<3:0>				481
INTCON	GIE/GIEH	PEIE/GIEL	IPEN	—	—	INT2EDG	INT1EDG	INT0EDG	170
PIR2	HLVDIF	ZCDIF	—	—	—	—	C2IF	C1IF	173
PIE2	HLVDIE	ZCDIE	—	—	—	—	C2IE	C1IE	181
IPR2	HLVDIP	ZCDIP	—	—	—	—	C2IP	C1IP	189
PMD0	SYSCMD	FVRMD	HLVDMD	CRCMD	SCANMD	NVMMD	CLKRMD	IOCMD	68

Legend: — = unimplemented, read as ‘0’. Shaded cells are unused by the HLVD module.
Note 1: PORTA<7:6> and their direction bits are individually configured as port pins based on various primary oscillator modes. When disabled, these bits read as ‘0’.

TABLE 37-3: POWER-DOWN CURRENT (I_{PD})(1,2)

PIC18LF26/45/46K40				Standard Operating Conditions (unless otherwise stated)					
PIC18F26/45/46K40				**Standard Operating Conditions (unless otherwise stated)** VREGPM = 1					
Param. No.	**Symbol**	**Device Characteristics**	**Min.**	**Typ.†**	**Max. +85°C**	**Max. +125°C**	**Units**	**Conditions**	
								VDD	**Note**
D200	IPD	IPD Base	—	0.05	2	9	µA	3.0V	
D200	IPD	IPD Base	—	0.4	4	12	µA	3.0V	
D200A			—	20	—	—	µA	3.0V	VREGPM = 0
D201	IPD_WDT	Low-Frequency Internal Oscillator/ WDT	—	0.4	3	10	µA	3.0V	
D201	IPD_WDT	Low-Frequency Internal Oscillator/ WDT	—	0.6	5	13	µA	3.0V	
D202	IPD_SOSC	Secondary Oscillator (SOSC)	—	0.6	5	13	µA	3.0V	
D202	IPD_SOSC	Secondary Oscillator (SOSC)	—	0.8	8.5	15	µA	3.0V	
D203	IPD_FVR	FVR	—	31	—	—	µA	3.0V	FVRCON = 0X81 or 0x84
D203	IPD_FVR	FVR	—	32	—	—	µA	3.0V	FVRCON = 0X81 or 0x84
D204	IPD_BOR	Brown-out Reset (BOR)	—	9	14	18	µA	3.0V	
D204	IPD_BOR	Brown-out Reset (BOR)	—	14	19	21	µA	3.0V	
D205	IPD_LPBOR	Low-Power Brown-out Reset (LPBOR)	—	0.5	—	—	µA	3.0V	
D205	IPD_LPBOR	Low-Power Brown-out Reset (LPBOR)	—	0.7	—	—	µA	3.0V	
D206	IPD_HLVD	High/Low Voltage Detect (HLVD)	—	31	—	—	µA	3.0V	
D206	IPD_HLVD	High/Low Voltage Detect (HLVD)	—	32	—	—	µA	3.0V	
D207	IPD_ADCA	ADC - Active	—	250	—	—	µA	3.0V	ADC is converting (4)
D207	IPD_ADCA	ADC - Active	—	280	—	—	µA	3.0V	ADC is converting (4)
D208	IPD_CMP	Comparator	—	25	38	40	µA	3.0V	
D208	IPD_CMP	Comparator	—	28	50	60	µA	3.0V	

† Data in "Typ." column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

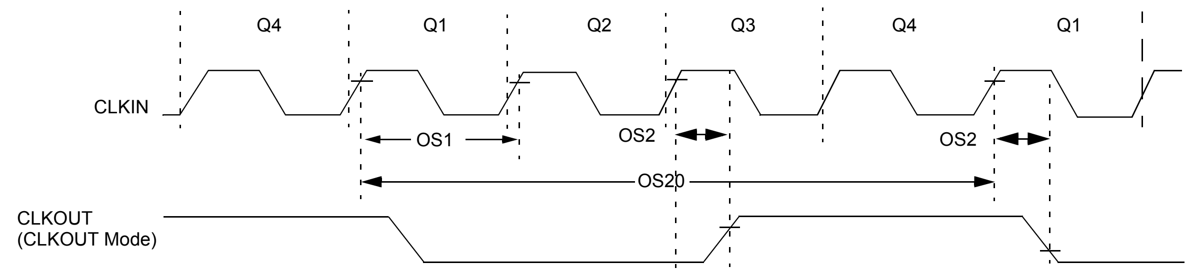
Note 1: The peripheral current is the sum of the base IDD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max. values should be used when calculating total current consumption.

2: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode with all I/O pins in high-impedance state and tied to VSS.

3: All peripheral currents listed are on a per-peripheral basis if more than one instance of a peripheral is available.

4: ADC clock source is FRC.

FIGURE 37-5: CLOCK TIMING



Note 1: See Table 37-7.

TABLE 37-7: EXTERNAL CLOCK/OSCILLATOR TIMING REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)							
Param No.	**Sym.**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
ECL Oscillator							
OS1	F_{ECL}	Clock Frequency	—	—	500	kHz	
OS2	T_{ECL_DC}	Clock Duty Cycle	40	—	60	%	
ECM Oscillator							
OS3	F_{ECM}	Clock Frequency	—	—	8	MHz	
OS4	T_{ECM_DC}	Clock Duty Cycle	40	—	60	%	
ECH Oscillator							
OS5	F_{ECH}	Clock Frequency	—	—	32	MHz	
OS6	T_{ECH_DC}	Clock Duty Cycle	40	—	60	%	
LP Oscillator							
OS7	F_{LP}	Clock Frequency	—	—	100	kHz	**Note 4**
XT Oscillator							
OS8	F_{XT}	Clock Frequency	—	—	4	MHz	**Note 4**
HS Oscillator							
OS9	F_{HS}	Clock Frequency	—	—	20	MHz	**Note 4**
Secondary Oscillator							
OS10	F_{SEC}	Clock Frequency	32.4	32.768	33.1	kHz	
System Oscillator							
OS20	F_{OSC}	System Clock Frequency	—	—	64	MHz	**(Note 2, Note 3)**

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min" values with an external clock applied to OSC1 pin. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

2: The system clock frequency (FOSC) is selected by the "main clock switch controls" as described in **Section 6.0 "Power-Saving Operation Modes"**.

3: The system clock frequency (FOSC) must meet the voltage requirements defined in the **Section 37.2 "Standard Operating Conditions"**.

4: LP, XT and HS oscillator modes require an appropriate crystal or resonator to be connected to the device. For clocking the device with the external square wave, one of the EC mode selections must be used.