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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

•XF

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	64MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	3.6K × 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18lf26k40t-i-ml

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Digital Peripherals (Continued)

- Programmable CRC with Memory Scan:
 - Reliable data/program memory monitoring for Fail-Safe operation (e.g., Class B)
 - Calculate CRC over any portion of Flash or EEPROM
- High-speed or background operation
- Hardware Limit Timer (TMR2/4/6+HLT):
- Hardware monitoring and Fault detection
- Peripheral Pin Select (PPS):
- Enables pin mapping of digital I/O
- Data Signal Modulator (DSM)

Analog Peripherals

- 10-Bit Analog-to-Digital Converter with Computation (ADC²):
 - 35 external channels
 - Conversion available during Sleep
 - Four internal analog channels
 - Internal and external trigger options
 - Automated math functions on input signals:
 - averaging, filter calculations, oversampling and threshold comparison
- Hardware Capacitive Voltage Divider (CVD) Support:
 - 8-bit precharge timer
 - Adjustable sample and hold capacitor array
 - Guard ring digital output drive
- Zero-Cross Detect (ZCD):
 - Detect when AC signal on pin crosses ground
- 5-Bit Digital-to-Analog Converter (DAC):
 - Output available externally
 - Programmable 5-bit voltage (% of VDD)
 - Internal connections to comparators, Fixed Voltage Reference and ADC
- Two Comparators (CMP):
 - Four external inputs
 - External output via PPS
- Fixed Voltage Reference (FVR) module:
 - 1.024V, 2.048V and 4.096V output levels

Clocking Structure

- High-Precision Internal Oscillator Block (HFINTOSC):
- Selectable frequency range up to 64 MHz
 ±1% at calibration
- 32 kHz Low-Power Internal Oscillator (LFINTOSC)
- External 32 kHz Crystal Oscillator (SOSC)
- External Oscillator Block:
 - Three crystal/resonator modes
 - 4x PLL with external sources
- Fail-Safe Clock Monitor:
 - Allows for safe shutdown if peripheral clock stops
- Oscillator Start-up Timer (OST)

Programming/Debug Features

- In-Circuit Debug Integrated On-Chip
- In-Circuit Serial Programming[™] (ICSP[™]) via Two Pins
- In-Circuit Debug (ICD) with Three Breakpoints via Two Pins

Features	PIC18(L)F26K40	PIC18(L)F45K40	PIC18(L)F46K40	
Program Memory (Bytes)	65536	32768	65536	
Program Memory (Instructions)	32768	16384	32768	
Data Memory (Bytes)	3720	2048	3720	
Data EEPROM Memory (Bytes)	1024	256	1024	
I/O Ports	A,B,C,E ⁽¹⁾	A,B,C,D,E	A,B,C,D,E	
Capture/Compare/PWM Modules (CCP)	2	2	2	
10-Bit Pulse-Width Modulator (PWM)	2	2	2	
10-Bit Analog-to-Digital Module (ADC ²) with Computation Accelerator	4 internal 24 external	4 internal 35 external	4 internal 35 external	
Packages	28-pin SPDIP 28-pin SOIC 28-pin SSOP 28-pin QFN 28-pin UQFN	40-pin PDIP 40-pin UQFN 44-pin QFN 44-pin TQFP	40-pin PDIP 40-pin UQFN 44-pin QFN 44-pin TQFP	
Interrupt Sources		36		
Timers (16-/8-bit)		4/3		
Serial Communications		2 MSSP, 2 EUSART		
Enhanced Complementary Waveform Generator (ECWG)		1		
Zero-Cross Detect (ZCD)		1		
Data Signal Modulator (DSM)		1		
Peripheral Pin Select (PPS)		Yes		
Peripheral Module Disable (PMD)		Yes		
16-bit CRC with NVMSCAN		Yes		
Programmable High/Low-Voltage Detect (HLVD)		Yes		
Programmable Brown-out Reset (BOR)		Yes		
Resets (and Delays)	POR, BOR, RESET Instruction, Stack Overflow, Stack Underflow (PWRT, OST),			
Instruction Set	83 with	75 Instructions; Extended Instruction Se	t enabled	
Operating Frequency				

TABLE 1-1: DEVICE FEATURES

Note 1: PORTE contains the single RE3 read-only bit.

6.0 POWER-SAVING OPERATION MODES

The purpose of the Power-Down modes is to reduce power consumption. There are three Power-Down modes:

- Doze mode
- Sleep mode
- Idle mode

6.1 Doze Mode

Doze mode allows for power saving by reducing CPU operation and program memory (PFM) access, without affecting peripheral operation. Doze mode differs from Sleep mode because the bandgap and system oscillators continue to operate, while only the CPU and PFM are affected. The reduced execution saves power by eliminating unnecessary operations within the CPU and memory.

When the Doze Enable (DOZEN) bit is set (DOZEN = 1), the CPU executes only one instruction cycle out of every N cycles as defined by the DOZE<2:0> bits of the CPUDOZE register. For example, if DOZE<2:0> = 001, the instruction cycle ratio is 1:4. The CPU and memory execute for one instruction cycle and then lay idle for three instruction cycles. During the unused cycles, the peripherals continue to operate at the system clock speed.

6.1.1 DOZE OPERATION

The Doze operation is illustrated in Figure 6-1. For this example:

- Doze enable (DOZEN) bit set (DOZEN = 1)
- DOZE<2:0> = 001 (1:4) ratio
- Recover-on-Interrupt (ROI) bit set (ROI = 1)

As with normal operation, the PFM fetches for the next instruction cycle. The Q-clocks to the peripherals continue throughout.

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	U-0	R/W-0/0
UART2MD	UART1MD	MSSP2MD	MSSP1MD	_	—		CWG1MD
bit 7	•	·	•				bit 0
Legend:							
R = Readable	e bit	W = Writable	bit	U = Unimplem	ented bit, read	as '0'	
u = Bit is unch	nanged	x = Bit is unkn	iown	-n/n = Value a	t POR and BOR	R/Value at all	other Resets
'1' = Bit is set		'0' = Bit is clea	ared	q = Value dep	ends on conditio	on	
L							
bit 7	UART2MD: Di	isable EUSART2	2 bit				
	1 = EUSART2	2 module disable	ed				
	0 = EUSARI2	2 module enable	d				
bit 6		Isable EUSARI 1 1 module disable	l bit				
	0 = EUSART'	1 module enable	ed ed				
bit 5	MSSP2MD: Di	isable MSSP2 b	it				
	1 = MSSP2 m	nodule disabled					
	0 = MSSP2 m	nodule enabled					
bit 4	MSSP1MD: D	isable MSSP1 b	it				
	1 = MSSP1 m 0 = MSSP1 m						
bit 3-1	Unimplement	ed: Read as '0'					
bit 0	CWG1MD: Die	sable CWG1 Mo	dule bit				
	1 = CWG1 m	odule disabled					
	0 = CWG1 module enabled						

REGISTER 7-5: PMD4: PMD CONTROL REGISTER 4

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
PCON0	STKOVF	STKUNF	WDTWV	RWDT	RMCLR	RI	POR	BOR	76
STATUS				TO	PD	Z	DC	С	118
WDTCON0					WDTPS<4:	PS<4:0> SEN			85
WDTCON1		v	VDTCS<2:0	>		WI	NDOW<2:0	>	86
WDTPSL				PSC	NT<7:0>				87
WDTPSH			PSCNT<15:8>					87	
WDTTMR		W	DTTMR<4:	0>		STATE	PSCNT	<17:16>	88

TABLE 9-3: SUMMARY OF REGISTERS ASSOCIATED WITH WINDOWED WATCHDOG TIMER

Legend: x = unknown, u = unchanged, – = unimplemented locations read as '0'. Shaded cells are not used by Windowed Watchdog Timer.

TABLE 9-4: SUMMARY OF CONFIGURATION WORD WITH WINDOWED WATCHDOG TIMER

Name	Bits Bit -/	7 Bit -/6	Bit 13/5	Bit 12/4	Bit 11/3	Bit 10/2	Bit 9/1	Bit 8/0	Register on Page
------	-------------	-----------	----------	----------	----------	----------	---------	---------	---------------------

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by Windowed Watchdog Timer.

EXAMPLE 11-3: ERASING A PROGRAM FLASH MEMORY BLOCK

; This sample row erase routine assumes the following:

; 1. A valid address within the erase row is loaded in variables TBLPTR register

; 2. ADDRH and ADDRL are located in common RAM (locations $0 \mathrm{x} 70$ - $0 \mathrm{x} 7 \mathrm{F})$

FRASE BLOC	MOVLW MOVWF MOVLW MOVLW MOVLW MOVWF	CODE_ADDR_UPPER TBLPTRU CODE_ADDR_HIGH TBLPTRH CODE_ADDR_LOW TBLPTRL	; load TBLPTR with the base ; address of the memory block
ERASE_BLUC	DOE	NEWGON1 NEWDEGO	t weight to Decemen Elech Mensue
	BCF	NVMCON1, NVMREGO	, point to program Flash Memory
	BSF	NVMCONI, NVMREGI	; access Program Flash Memory
	BSF	NVMCON1, WREN	; enable write to memory
	BSF	NVMCON1, FREE	; enable block Erase operation
	BCF	INTCON, GIE	; disable interrupts
Required	MOVLW	55h	
Sequence	MOVWF	NVMCON2	; write 55h
	MOVLW	AAh	
	MOVWF	NVMCON2	; write AAh
	BSF	NVMCON1, WR	; start erase (CPU stalls)
	BSF	INTCON, GIE	; re-enable interrupts

R/W-1/1	R/W-1/1	U-0	U-0	U-0	U-0	R/W-1/1	R/W-1/1
HLVDIP	ZCDIP	_	_	_	—	C2IP	C1IP
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	l as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
bit 7	HLVDIP: HLV	D Interrupt Pric	ority bit				
	1 = High prio	rity					
	0 = Low prior	rity					
bit 6	ZCDIP: Zero-	Cross Detect Ir	nterrupt Priorit	ty bit			
	1 = High prio	rity					
	0 = Low prior	nty					
bit 5-2	Unimplemen	ted: Read as '	כ'				
bit 1	C2IP: Compa	rator 2 Interrup	t Priority bit				
	1 = High priority						
	0 = Low prior	rity					
bit 0	C1IP: Compa	rator 1 Interrup	t Priority bit				
	1 = High prio	rity					
	0 = Low prior	rity					

REGISTER 14-20: IPR2: PERIPHERAL INTERRUPT PRIORITY REGISTER 2

16.6 Register Definitions: Interrupt-on-Change Control

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
IOCxP7	IOCxP6	IOCxP5	IOCxP4	IOCxP3	IOCxP2	IOCxP1	IOCxP0
bit 7							bit 0
Legend:							
R = Readable bit	t	W = Writable bi	t	U = Unimplem	ented bit, read as	'0'	
u = Bit is unchan	ged	x = Bit is unkno	wn	-n/n = Value at	POR and BOR/Va	alue at all other f	Resets
'1' = Bit is set		'0' = Bit is clear	ed				

REGISTER 16-1: IOCxP: INTERRUPT-ON-CHANGE POSITIVE EDGE REGISTER EXAMPLE

bit 7-0

IOCxP<7:0>: Interrupt-on-Change Positive Edge Enable bits

1 = Interrupt-on-Change enabled on the IOCx pin for a positive-going edge. Associated Status bit and interrupt flag will be set upon detecting an edge.

0 = Interrupt-on-Change disabled for the associated pin.

REGISTER 16-2: IOCxN: INTERRUPT-ON-CHANGE NEGATIVE EDGE REGISTER EXAMPLE

| R/W-0/0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| IOCxN7 | IOCxN6 | IOCxN5 | IOCxN4 | IOCxN3 | IOCxN2 | IOCxN1 | IOCxN0 |
| bit 7 | | | | | | | bit 0 |

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0

IOCxN<7:0>: Interrupt-on-Change Negative Edge Enable bits

1 = Interrupt-on-Change enabled on the IOCx pin for a negative-going edge. Associated Status bit and interrupt flag will be set upon detecting an edge.

0 = Interrupt-on-Change disabled for the associated pin

REGISTER 16-3: IOCxF: INTERRUPT-ON-CHANGE FLAG REGISTER EXAMPLE

| R/W/HS-0/0 |
|------------|------------|------------|------------|------------|------------|------------|------------|
| IOCxF7 | IOCxF6 | IOCxF5 | IOCxF4 | IOCxF3 | IOCxF2 | IOCxF1 | IOCxF0 |
| bit 7 | | | | | | | bit 0 |

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HS - Bit is set in hardware

bit 7-0

IOCxF<7:0>: Interrupt-on-Change Flag bits

1 = A enabled change was detected on the associated pin. Set when IOCP[n] = 1 and a positive edge was detected on the IOCn pin, or when IOCN[n] = 1 and a negative edge was detected on the IOCn pin

0 = No change was detected, or the user cleared the detected change

18.1 Timer0 Operation

Timer0 can operate as either an 8-bit timer/counter or a 16-bit timer/counter. The mode is selected with the T016BIT bit of the T0CON register.

18.1.1 16-BIT MODE

The register pair TMR0H:TMR0L, increments on the rising edge of the clock source. A 15-bit prescaler on the clock input gives several prescale options (see prescaler control bits, T0CKPS<3:0> in the T0CON1 register).

18.1.1.1 Timer0 Reads and Writes in 16-Bit Mode

In 16-bit mode, to avoid rollover between reading high and low registers, the TMR0H register is a buffered copy of the actual high byte of Timer0, which is neither directly readable nor writable (see Figure 18-1). TMR0H is updated with the contents of the high byte of Timer0 during a read of TMR0L. This provides the ability to read all 16 bits of Timer0 without having to verify that the read of the high and low byte was valid, due to a rollover between successive reads of the high and low byte.

Similarly, a write to the high byte of Timer0 must also take place through the TMR0H Buffer register. The high byte is updated with the contents of TMR0H when a write occurs to TMR0L. This allows all 16 bits of Timer0 to be updated at once.

18.1.2 8-BIT MODE

In normal operation, TMR0 increments on the rising edge of the clock source. A 15-bit prescaler on the clock input gives several prescale options (see prescaler control bits, T0CKPS<3:0> in the T0CON1 register).

In 8-bit mode, the value of TMR0L is compared to that of the Period buffer, a copy of TMR0H, on each clock cycle. When the two values match, the following events happen:

- TMR0_out goes high for one prescaled clock period
- TMR0L is reset
- The contents of TMR0H are copied to the period buffer

In 8-bit mode, the TMR0L and TMR0H registers are both directly readable and writable. The TMR0L register is cleared on any device Reset, while the TMR0H register initializes at FFh. Both the prescaler and postscaler counters are cleared on the following events:

- A write to the TMR0L register
- A write to either the T0CON0 or T0CON1 registers
- Any device Reset Power-on Reset (POR), MCLR Reset, Watchdog Timer Reset (WDTR) or
- Brown-out Reset (BOR)

18.1.3 COUNTER MODE

In Counter mode, the prescaler is normally disabled by setting the T0CKPS bits of the T0CON1 register to '0000'. Each rising edge of the clock input (or the output of the prescaler if the prescaler is used) increments the counter by '1'.

18.1.4 TIMER MODE

In Timer mode, the Timer0 module will increment every instruction cycle as long as there is a valid clock signal and the T0CKPS bits of the T0CON1 register (Register 18-2) are set to '0000'. When a prescaler is added, the timer will increment at the rate based on the prescaler value.

18.1.5 ASYNCHRONOUS MODE

When the TOASYNC bit of the TOCON1 register is set (TOASYNC = '1'), the counter increments with each rising edge of the input source (or output of the prescaler, if used). Asynchronous mode allows the counter to continue operation during Sleep mode provided that the clock also continues to operate during Sleep.

18.1.6 SYNCHRONOUS MODE

When the T0ASYNC bit of the T0CON1 register is clear (T0ASYNC = 0), the counter clock is synchronized to the system clock (Fosc/4). When operating in Synchronous mode, the counter clock frequency cannot exceed Fosc/4.

18.2 Clock Source Selection

The T0CS<2:0> bits of the T0CON1 register are used to select the clock source for Timer0. Register 18-2 displays the clock source selections.

18.2.1 INTERNAL CLOCK SOURCE

When the internal clock source is selected, Timer0 operates as a timer and will increment on multiples of the clock source, as determined by the Timer0 prescaler.

18.2.2 EXTERNAL CLOCK SOURCE

When an external clock source is selected, Timer0 can operate as either a timer or a counter. Timer0 will increment on multiples of the rising edge of the external clock source, as determined by the Timer0 prescaler.

25.0 DATA SIGNAL MODULATOR (DSM) MODULE

The Data Signal Modulator (DSM) is a peripheral which allows the user to mix a data stream, also known as a modulator signal, with a carrier signal to produce a modulated output.

Both the carrier and the modulator signals are supplied to the DSM module either internally, from the output of a peripheral, or externally through an input pin.

The modulated output signal is generated by performing a logical "AND" operation of both the carrier and modulator signals and then provided to the MDOUT pin.

The carrier signal is comprised of two distinct and separate signals. A carrier high (CARH) signal and a carrier low (CARL) signal. During the time in which the modulator (MOD) signal is in a logic high state, the DSM mixes the carrier high signal with the modulator signal. When the modulator signal is in a logic low state, the DSM mixes the carrier low signal with the modulator signal.

Using this method, the DSM can generate the following types of Key Modulation schemes:

- Frequency-Shift Keying (FSK)
- Phase-Shift Keying (PSK)
- On-Off Keying (OOK)

Additionally, the following features are provided within the DSM module:

- Carrier Synchronization
- · Carrier Source Polarity Select
- Programmable Modulator Data
- · Modulated Output Polarity Select
- Peripheral Module Disable, which provides the ability to place the DSM module in the lowest power consumption mode

Figure 25-1 shows a Simplified Block Diagram of the Data Signal Modulator peripheral.





25.6 Carrier Source Polarity Select

The signal provided from any selected input source for the carrier high and carrier low signals can be inverted. Inverting the signal for the carrier high source is enabled by setting the MDCHPOL bit of the MDCON1 register. Inverting the signal for the carrier low source is enabled by setting the MDCLPOL bit of the MDCON1 register.

25.7 Programmable Modulator Data

The MDBIT of the MDCON0 register can be selected as the source for the modulator signal. This gives the user the ability to program the value used for modulation.

25.8 Modulated Output Polarity

The modulated output signal provided on the DSM pin can also be inverted. Inverting the modulated output signal is enabled by setting the MDOPOL bit of the MDCON0 register.

25.9 Operation in Sleep Mode

The DSM module is not affected by Sleep mode. The DSM can still operate during Sleep, if the Carrier and Modulator input sources are also still operable during Sleep. Refer to **Section 6.0 "Power-Saving Operation Modes"** for more details.

25.10 Effects of a Reset

Upon any device Reset, the DSM module is disabled. The user's firmware is responsible for initializing the module before enabling the output. The registers are reset to their default values.

25.11 Peripheral Module Disable

The DSM module can be completely disabled using the PMD module to achieve maximum power saving. The DSMMD bit of PMD5 (Register 7-6) when set disables the DSM module completely. When enabled again all the registers of the DSM module default to POR status.

26.0 MASTER SYNCHRONOUS SERIAL PORT MODULE

Note: The PIC18(L)F26/45/46K40 devices have two MSSP. Therefore, all information in this section refers to both MSSP1 and MSSP2.

26.1 MSSP Module Overview

The Master Synchronous Serial Port (MSSP) module is a serial interface useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be serial EEPROMs, shift registers, display drivers, A/D converters, etc. The PIC18(L)F26/45/46K40 devices have two MSSP modules that can operate in one of two modes:

- Serial Peripheral Interface (SPI)
- Inter-Integrated Circuit (I²C)

The SPI interface supports the following modes and features:

- Master mode
- Slave mode
- · Clock Parity
- Slave Select Synchronization (Slave mode only)
- · Daisy-chain connection of slave devices

The I^2C interface supports the following modes and features:

- · Master mode
- Slave mode
- Byte NACKing (Slave mode)
- · Limited multi-master support
- 7-bit and 10-bit addressing
- Start and Stop interrupts
- · Interrupt masking
- Clock stretching
- · Bus collision detection
- · General call address matching
- · Address masking
- Address Hold and Data Hold modes
- Selectable SDA hold times

26.2 SPI Mode Overview

The Serial Peripheral Interface (SPI) bus is a synchronous serial data communication bus that operates in Full-Duplex mode. Devices communicate in a master/slave environment where the master device initiates the communication. A slave device is controlled through a Chip Select known as Slave Select.

The SPI bus specifies four signal connections:

- Serial Clock (SCK)
- Serial Data Out (SDO)
- Serial Data In (SDI)
- Slave Select (SS)

Figure 26-1 shows the block diagram of the MSSP module when operating in SPI mode.

26.9.3.3 7-bit Transmission with Address Hold Enabled

Setting the AHEN bit of the SSPxCON3 register enables additional clock stretching and interrupt generation after the eighth falling edge of a received matching address. Once a matching address has been clocked in, CKP is cleared and the SSPxIF interrupt is set.

Figure 26-19 displays a standard waveform of a 7-bit address slave transmission with AHEN enabled.

- 1. Bus starts Idle.
- Master sends Start condition; the S bit of SSPxSTAT is set; SSPxIF is set if interrupt on Start detect is enabled.
- Master sends matching address with R/W bit set. After the eighth falling edge of the SCL line the CKP bit is cleared and SSPxIF interrupt is generated.
- 4. Slave software clears SSPxIF.
- Slave software reads the <u>ACKTIM</u> bit of SSPxCON3 register, and R/W and D/A of the SSPxSTAT register to determine the source of the interrupt.
- 6. Slave reads the address value from the SSPxBUF register clearing the BF bit.
- Slave software decides from this information if it wishes to ACK or not ACK and sets the ACKDT bit of the SSPxCON2 register accordingly.
- 8. Slave sets the CKP bit releasing SCL.
- 9. Master clocks in the \overline{ACK} value from the slave.
- 10. Slave hardware automatically clears the CKP bit and sets SSPxIF after the ACK if the R/W bit is set.
- 11. Slave software clears SSPxIF.
- 12. Slave loads value to transmit to the master into SSPxBUF setting the BF bit.

Note: <u>SSPxBUF</u> cannot be loaded until after the ACK.

- 13. Slave sets the CKP bit releasing the clock.
- 14. Master clocks out the data from the slave and sends an ACK value on the ninth SCL pulse.
- 15. Slave hardware copies the ACK value into the ACKSTAT bit of the SSPxCON2 register.
- 16. Steps 10-15 are repeated for each byte transmitted to the master from the slave.
- 17. If the master sends a not ACK the slave releases the bus allowing the master to send a Stop and end the communication.

Note: Master must send a not ACK on the last byte to ensure that the slave releases the SCL line to receive a Stop.

26.10.13.1 Bus Collision During a Start Condition

During a Start condition, a bus collision occurs if:

- a) SDA or SCL are sampled low at the beginning of the Start condition (Figure 26-33).
- b) SCL is sampled low before SDA is asserted low (Figure 26-34).

During a Start condition, both the SDA and the SCL pins are monitored.

If the SDA pin is already low, or the SCL pin is already low, then all of the following occur:

- · the Start condition is aborted,
- the BCLxIF flag is set and
- the MSSP module is reset to its Idle state (Figure 26-33).

The Start condition begins with the SDA and SCL pins deasserted. When the SDA pin is sampled high, the Baud Rate Generator is loaded and counts down. If the SCL pin is sampled low while SDA is high, a bus collision occurs because it is assumed that another master is attempting to drive a data '1' during the Start condition.

If the SDA pin is sampled low during this count, the BRG is reset and the SDA line is asserted early (Figure 26-35). If, however, a '1' is sampled on the SDA pin, the SDA pin is asserted low at the end of the BRG count. The Baud Rate Generator is then reloaded and counts down to zero; if the SCL pin is sampled as '0' during this time, a bus collision does not occur. At the end of the BRG count, the SCL pin is asserted low.

Note: The reason that bus collision is not a factor during a Start condition is that no two bus masters can assert a Start condition at the exact same time. Therefore, one master will always assert SDA before the other. This condition does not cause a bus collision because the two masters must be allowed to arbitrate the first address following the Start condition. If the address is the same, arbitration must be allowed to continue into the data portion, Repeated Start or Stop conditions.





27.5.2.3 EUSART Synchronous Slave Reception

The operation of the Synchronous Master and Slave modes is identical (Section 27.5.1.5 "Synchronous Master Reception"), with the following exceptions:

- Sleep
- CREN bit is always set, therefore the receiver is never idle
- SREN bit, which is a "don't care" in Slave mode

A character may be received while in Sleep mode by setting the CREN bit prior to entering Sleep. Once the word is received, the RSR register will transfer the data to the RCxREG register. If the RCxIE enable bit is set, the interrupt generated will wake the device from Sleep and execute the next instruction. If the GIE bit is also set, the program will branch to the interrupt vector.

- 27.5.2.4 Synchronous Slave Reception Setup:
- 1. Set the SYNC and SPEN bits and clear the CSRC bit.
- 2. Clear the ANSEL bit for both the CKx and DTx pins (if applicable).
- 3. If interrupts are desired, set the RCxIE bit of the PIE3 register and the GIE and PEIE bits of the INTCON register.
- 4. If 9-bit reception is desired, set the RX9 bit.
- 5. Set the CREN bit to enable reception.
- The RCxIF bit will be set when reception is complete. An interrupt will be generated if the RCxIE bit was set.
- 7. If 9-bit mode is enabled, retrieve the Most Significant bit from the RX9D bit of the RCxSTA register.
- 8. Retrieve the eight Least Significant bits from the receive FIFO by reading the RCxREG register.
- 9. If an overrun error occurs, clear the error by either clearing the CREN bit of the RCxSTA register or by clearing the SPEN bit which resets the EUSART.

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
BAUDxCON	ABDOVF	RCIDL		SCKP	BRG16	—	WUE	ABDEN	395
INTCON	GIE/GIEH	PEIE/GIEL	IPEN	—	_	INT2EDG	INT1EDG	INT0EDG	170
PIE3	RC2IE	TX2IE	RC1IE	TX1IE	BCL2IE	SSP2IE	BCL1IE	SSP1IE	182
PIR3	RC2IF	TX2IF	RC1IF	TX1IF	BCL2IF	SSP2IF	BCL1IF	SSP1IF	174
IPR3	RC2IP	TX2IP	RC1IP	TX1IP	BCL2IP	SSP2IP	BCL1IP	SSP1IP	190
RCxREG	EUSART Receive Data Register							399*	
RCxSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	394
RxyPPS	—	—		RxyPPS<4:0>					218
RXxPPS	—	—	_	RXPPS<4:0>				216	
TXxSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	393

TABLE 27-10: SUMMARY OF REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE RECEPTION

Legend: — = unimplemented location, read as '0'. Shaded cells are not used for synchronous slave reception.
* Page provides register information.

30.0 5-BIT DIGITAL-TO-ANALOG CONVERTER (DAC) MODULE

The Digital-to-Analog Converter supplies a variable voltage reference, ratiometric with the input source, with 32 selectable output levels.

The positive input source (VSOURCE+) of the DAC can be connected to:

- FVR Buffer
- External VREF+ pin
- VDD supply voltage

The negative input source (VSOURCE-) of the DAC can be connected to:

- External VREF- pin
- Vss

The output of the DAC (DACx_output) can be selected as a reference voltage to the following:

- · Comparator positive input
- ADC input channel
- DACxOUT1 pin
- DACxOUT2 pin

The Digital-to-Analog Converter (DAC) can be enabled by setting the DACEN bit of the DAC1CON0 register.

-000026F 8/7/2015 Reserved 11 VSOURCE+ DACR<4:0> FVR Buffer 10 5 R VREF+ 01 AVdd 00 R DACPSS R R 32-to-1 MUX DACx_output 32 To Peripherals Steps . . DACEN R DACxOUT1⁽¹⁾ R DACOE1 R DACxOUT2⁽¹⁾ **VREF-**1 VSOURCE-DACOE2 0 AVss DACNSS Note 1: The unbuffered DACx output is provided on the DACxOUT pin(s).

FIGURE 30-1: DIGITAL-TO-ANALOG CONVERTER BLOCK DIAGRAM

REGISTER 31-19: ADRESL: ADC RESULT REGISTER LOW, ADFM = 1

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	
	ADRES<7:0>							
bit 7							bit 0	
Legend:								
R = Readable	bit	W = Writable I	bit	U = Unimpler	nented bit, rea	d as '0'		
u = Bit is unch	anged	x = Bit is unkn	iown	-n/n = Value a	at POR and BC	R/Value at all	other Resets	
'1' = Bit is set		'0' = Bit is clea	ared					

bit 7-0 **ADRES<7:0>**: ADC Result Register bits. Lower eight bits of 10-bit conversion result.

REGISTER 31-20: ADPREVH: ADC PREVIOUS RESULT REGISTER

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
			ADPRE	V<15:8>			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 ADPREV<15:8>: Previous ADC Results bits If ADPSIS = 1: Upper byte of ADFLTR at the start of current ADC conversion If ADPSIS = 0: Upper bits of ADRES at the start of current ADC conversion⁽¹⁾

Note 1: If ADPSIS = 0, ADPREVH and ADPREVL are formatted the same way as ADRES is, depending on the ADFM bit.

PIC18(L)F26/45/46K40

CPF	SEQ	Compare	Compare f with W, skip if f = W						
Synta	ax:	CPFSEQ	CPFSEQ f {,a}						
Operands:		0 ≤ f ≤ 255 a ∈ [0,1]	0 ≤ f ≤ 255 a ∈ [0,1]						
Operation:		(f) - (W), skip if $(f) = ($ (unsigned c	(f) - (W), skip if $(f) = (W)$ (unsigned comparison)						
Statu	s Affected:	None	None						
Enco	dina:	0110	0110 001a ffff ffff						
Description:		Compares t location 'f' t performing If 'f' = W, th	Compares the contents of data memory location 'f' to the contents of W by performing an unsigned subtraction. If 'f' = W, then the fetched instruction is						
		instead, ma	king this a 2-c	ycle					
		lf 'a' is '0', tl lf 'a' is '1', tl	If 'a' is '0', the Access Bank is selected.						
		GPR bank.							
		If 'a' is '0' a	nd the extende	ed instruction					
		set is enabl	ed, this instruc Literal Offset A	tion operates					
		mode when	ever $f \le 95$ (5F	⁻ h). See Sec-					
		tion 35.2.3	"Byte-Oriente	ed and Bit-					
		Oriented In	Oriented Instructions in Indexed Lit-						
Word	le.			alls.					
Cycle	10. 	1(2)							
Oyoic		Note: 3 cy	cles if skip an	d followed					
		by a	a 2-word instru	iction.					
QC	ycle Activity:								
	Q1	Q2	Q3	Q4					
	Decode	Read	Process	No					
lf old	in:	register 'f'	Data	operation					
II SK	ip. Q1	Q2	Q3	Q4					
	No	No	No	No					
	operation	operation	operation	operation					
lf sk	ip and followed	d by 2-word in	struction:	04					
	Q1	Q2	Q3	Q4					
	operation	operation	operation	operation					
	No	No	No	No					
	operation	operation	operation	operation					
Example:		HERE NEQUAL EQUAL	HERE CPFSEQ REG, 0 NEQUAL : EQUAL :						
Before Instruction									
PC Addres		SS = HERE							
W		= ?							
REG		= ?							
		۳۱ ۰۰۰							
If REG		= VV; = Address (EOUAL)							
lf REG		≠ W;							
	PC	= Ad	dress (NEQUA	AL)					

44-Lead Plastic Thin Quad Flatpack (PT) - 10x10x1.0 mm Body [TQFP]



Microchip Technology Drawing C04-076C Sheet 1 of 2