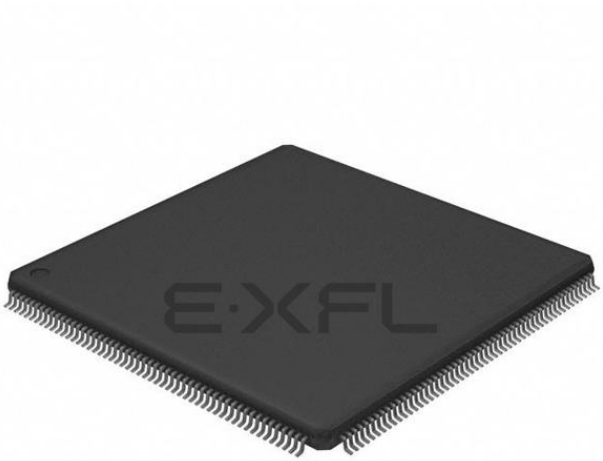

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Program Memory Type	FLASH
EEPROM Size	-
RAM Size	96K x 8
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Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
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Supplier Device Package	208-LQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2478fbd208-551

Table 3. Pin allocation table *…continued*

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
9	P1[23]/USB_RX_DP1/ LCDVD[9]/LCDVD[13]/ PWM1[4]/MISO0	10	V_{SSCORE}	11	$V_{DD(DCDC)(3V3)}$	12	V_{SSIO}
13	P2[15]/$\overline{CS3}$/ CAP2[1]/SCL1	14	P4[17]/A17	15	P4[18]/A18	16	P4[19]/A19
17	$V_{DD(3V3)}$		-		-		-
Row R							
1	P0[12]/$\overline{USB\_PPWR2}$/ MISO1/AD0[6]	2	P0[13]/USB_UP_LED2/ MOSI1/AD0[7]	3	P0[28]/SCL0	4	P2[25]/CKEOUT1
5	P3[24]/D24/ CAP0[1]/PWM1[1]	6	P0[30]/USB_D−1	7	P2[19]/CLKOUT1	8	P1[21]/USB_TX_DM1/ LCDVD[7]/LCDVD[11]/ PWM1[3]/SSEL0
9	V_{SSIO}	10	P1[26]/$\overline{USB\_SSPND1}$/ LCDVD[12]/LCDVD[20]/ PWM1[6]/CAP0[0]	11	P2[16]/$\overline{CAS}$	12	P2[14]/$\overline{CS2}$/CAP2[0]/ SDA1
13	P2[17]/$\overline{RAS}$	14	P0[11]/RXD2/SCL2/ MAT3[1]	15	P4[4]/A4	16	P4[5]/A5
17	P4[20]/A20/SDA2/SCK1		-		-		-
Row T							
1	P0[27]/SDA0	2	P0[31]/USB_D+2	3	P3[26]/D26/ MAT0[1]/PWM1[3]	4	P2[26]/CKEOUT2/ MAT3[0]/MISO0
5	V_{SSIO}	6	P3[23]/D23/ CAP0[0]/PCAP1[0]	7	P0[14]/$\overline{USB\_HSTEN2}$/ USB_CONNECT2/ SSEL1	8	P2[20]/$\overline{DYCS0}$
9	P1[24]/USB_RX_DM1/ LCDVD[10]/LCDVD[14]/ PWM1[5]/MOSI0	10	P1[25]/$\overline{USB\_LS1}$/ $\overline{LCDVD[11]}$/$\overline{LCDVD[15]}$/ $\overline{USB\_HSTEN1}$/MAT1[1]	11	P4[2]/A2	12	P1[27]/$\overline{USB\_INT1}$/ $\overline{LCDVD[13]}$/$\overline{LCDVD[21]}$/ $\overline{USB\_OVRCR1}$/CAP0[1]
13	P1[28]/USB_SCL1/ LCDVD[14]/LCDVD[22]/ PCAP1[0]/MAT0[0]	14	P0[1]/TD1/RXD3/SCL1	15	P0[10]/TXD2/SDA2/ MAT3[0]	16	P2[13]/$\overline{EINT3}$/ LCDVD[5]/LCDVD[9]/ LCDVD[19]/MCIDAT3/ I2STX_SDA
17	P2[11]/$\overline{EINT1}$/ LCDCLKIN/ MCIDAT1/I2STX_CLK		-		-		-
Row U							
1	USB_D−2	2	P3[25]/D25/ MAT0[0]/PWM1[2]	3	P2[18]/CLKOUT0	4	P0[29]/USB_D+1
5	P2[23]/$\overline{DYCS3}$/ CAP3[1]/SSEL0	6	$\overline{P1[19]}$/$\overline{USB\_TX\_E1}$/ $\overline{USB\_PPWR1}$/CAP1[1]	7	P1[20]/USB_TX_DP1/ LCDVD[6]/LCDVD[10]/ PWM1[2]/SCK0	8	P1[22]/USB_RCV1/ LCDVD[8]/LCDVD[12]/ USB_PWRD1/MAT1[0]
9	P4[0]/A0	10	P4[1]/A1	11	P2[21]/$\overline{DYCS1}$	12	P2[22]/$\overline{DYCS2}$/ CAP3[0]/SCK0
13	$V_{DD(3V3)}$	14	P1[29]/USB_SDA1/ LCDVD[15]/LCDVD[23]/ PCAP1[1]/MAT0[1]	15	P0[0]/RD1/TXD3/SDA1	16	P4[3]/A3
17	P4[16]/A16		-		-		-

Table 4. Pin description *…continued*

Symbol	Pin	Ball	Type	Description
P0[7]/I2STX_CLK/ LCDVD[9]/SCK1/ MAT2[1]	162[1]	C13[1]	I/O	**P0[7] —** General purpose digital input/output pin.
			I/O	**I2STX_CLK —** I^2S transmit clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*.[17]
			O	**LCDVD[9] —** LCD data.[17]
			I/O	**SCK1 —** Serial Clock for SSP1.
			O	**MAT2[1] —** Match output for Timer 2, channel 1.
P0[8]/I2STX_WS/ LCDVD[16]/ MISO1/MAT2[2]	160[1]	A15[1]	I/O	**P0[8] —** General purpose digital input/output pin.
			I/O	**I2STX_WS —** I^2S Transmit word select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.[17]
			O	**LCDVD[16] —** LCD data.[17]
			I/O	**MISO1 —** Master In Slave Out for SSP1.
			O	**MAT2[2] —** Match output for Timer 2, channel 2.
P0[9]/I2STX_SDA/ LCDVD[17]/ MOSI1/MAT2[3]	158[1]	C14[1]	I/O	**P0[9] —** General purpose digital input/output pin.
			I/O	**I2STX_SDA —** I^2S transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.[17]
			O	**LCDVD[17] —** LCD data.[17]
			I/O	**MOSI1 —** Master Out Slave In for SSP1.
			O	**MAT2[3] —** Match output for Timer 2, channel 3.
P0[10]/TXD2/ SDA2/MAT3[0]	98[1]	T15[1]	I/O	**P0[10] —** General purpose digital input/output pin.
			O	**TXD2 —** Transmitter output for UART2.
			I/O	**SDA2 —** I^2C2 data input/output (this is not an open-drain pin).
			O	**MAT3[0] —** Match output for Timer 3, channel 0.
P0[11]/RXD2/ SCL2/MAT3[1]	100[1]	R14[1]	I/O	**P0[11] —** General purpose digital input/output pin.
			I	**RXD2 —** Receiver input for UART2.
			I/O	**SCL2 —** I^2C2 clock input/output (this is not an open-drain pin).
			O	**MAT3[1] —** Match output for Timer 3, channel 1.
P0[12]/ USB_PPWR2/ MISO1/AD0[6]	41[2]	R1[2]	I/O	**P0[12] —** General purpose digital input/output pin.
			O	**$\overline{\text{USB\_PPWR2}}$ —** Port Power enable signal for USB port 2.
			I/O	**MISO1 —** Master In Slave Out for SSP1.
			I	**AD0[6] —** A/D converter 0, input 6.
P0[13]/ USB_UP_LED2/ MOSI1/AD0[7]	45[2]	R2[2]	I/O	**P0[13] —** General purpose digital input/output pin.
			O	**USB_UP_LED2 —** USB port 2 GoodLink LED indicator. It is LOW when device is configured (non-control endpoints enabled), or when host is enabled and has detected a device on the bus. It is HIGH when the device is not configured, or when host is enabled and has not detected a device on the bus, or during global suspend. It transitions between LOW and HIGH (flashes) when host is enabled and detects activity on the bus.
			I/O	**MOSI1 —** Master Out Slave In for SSP1.
			I	**AD0[7] —** A/D converter 0, input 7.

Table 4. Pin description *…continued*

Symbol	Pin	Ball	Type	Description
P0[14]/ USB_HSTEN2/ USB_CONNECT2/ SSEL1	69[1]	T7[1]	I/O	**P0[14] —** General purpose digital input/output pin.
			O	**USB_HSTEN2 —** Host Enabled status for USB port 2.
			O	**USB_CONNECT2 —** SoftConnect control for USB port 2. Signal used to switch an external 1.5 kΩ resistor under software control. Used with the SoftConnect USB feature.
			I/O	**SSEL1 —** Slave Select for SSP1.
P0[15]/TXD1/ SCK0/SCK	128[1]	J16[1]	I/O	**P0[15] —** General purpose digital input/output pin.
			O	**TXD1 —** Transmitter output for UART1.
			I/O	**SCK0 —** Serial clock for SSP0.
			I/O	**SCK —** Serial clock for SPI.
P0[16]/RXD1/ SSEL0/SSEL	130[1]	J14[1]	I/O	**P0 [16] —** General purpose digital input/output pin.
			I	**RXD1 —** Receiver input for UART1.
			I/O	**SSEL0 —** Slave Select for SSP0.
			I/O	**SSEL —** Slave Select for SPI.
P0[17]/CTS1/ MISO0/MISO	126[1]	K17[1]	I/O	**P0[17] —** General purpose digital input/output pin.
			I	**CTS1 —** Clear to Send input for UART1.
			I/O	**MISO0 —** Master In Slave Out for SSP0.
			I/O	**MISO —** Master In Slave Out for SPI.
P0[18]/DCD1/ MOSI0/MOSI	124[1]	K15[1]	I/O	**P0[18] —** General purpose digital input/output pin.
			I	**DCD1 —** Data Carrier Detect input for UART1.
			I/O	**MOSI0 —** Master Out Slave In for SSP0.
			I/O	**MOSI —** Master Out Slave In for SPI.
P0[19]/DSR1/ MCICLK/SDA1	122[1]	L17[1]	I/O	**P0[19] —** General purpose digital input/output pin.
			I	**DSR1 —** Data Set Ready input for UART1.
			O	**MCICLK —** Clock output line for SD/MMC interface.
			I/O	**SDA1 —** I^2C1 data input/output (this is not an open-drain pin).
P0[20]/DTR1/ MCICMD/SCL1	120[1]	M17[1]	I/O	**P0[20] —** General purpose digital input/output pin.
			O	**DTR1 —** Data Terminal Ready output for UART1.
			I/O	**MCICMD —** Command line for SD/MMC interface.
			I/O	**SCL1 —** I^2C1 clock input/output (this is not an open-drain pin).
P0[21]/RI1/ MCIPWR/RD1	118[1]	M16[1]	I/O	**P0[21] —** General purpose digital input/output pin.
			I	**RI1 —** Ring Indicator input for UART1.
			O	**MCIPWR —** Power Supply Enable for external SD/MMC power supply.
			I	**RD1 —** CAN1 receiver input.
P0[22]/RTS1/ MCIDAT0/TD1	116[1]	N17[1]	I/O	**P0[22] —** General purpose digital input/output pin.
			O	**RTS1 —** Request to Send output for UART1.
			I/O	**MCIDAT0 —** Data line 0 for SD/MMC interface.
			O	**TD1 —** CAN1 transmitter output.

Table 4. Pin description *…continued*

Symbol	Pin	Ball	Type	Description
P1[24]/ USB_RX_DM1/ LCDVD[10]/ LCDVD[14]/ PWM1[5]/MOSI0	78[1]	T9[1]	I/O	**P1[24] —** General purpose digital input/output pin.
			I	**USB_RX_DM1 —** D− receive data for USB port 1 (OTG transceiver).[18]
			O	**LCDVD[10]/LCDVD[14] —** LCD data.[18]
			O	**PWM1[5] —** Pulse Width Modulator 1, channel 5 output.
			I/O	**MOSI0 —** Master Out Slave in for SSP0.
P1[25]/$\overline{\text{USB\_LS1}}$/ LCDVD[11]/ $\overline{\text{LCDVD[15]}}$/ $\overline{\text{USB\_HSTEN1}}$/ MAT1[1]	80[1]	T10[1]	I/O	**P1[25] —** General purpose digital input/output pin.
			O	**$\overline{\text{USB\_LS1}}$ —** Low Speed status for USB port 1 (OTG transceiver).[18]
			O	**LCDVD[11]/LCDVD[15] —** LCD data.[18]
			O	**$\overline{\text{USB\_HSTEN1}}$ —** Host Enabled status for USB port 1.
			O	**MAT1[1] —** Match output for Timer 1, channel 1.
P1[26]/ $\overline{\text{USB\_SSPND1}}$/ LCDVD[12]/ LCDVD[20]/ PWM1[6]/CAP0[0]	82[1]	R10[1]	I/O	**P1[26] —** General purpose digital input/output pin.
			O	**$\overline{\text{USB\_SSPND1}}$ —** USB port 1 Bus Suspend status (OTG transceiver).[18]
			O	**LCDVD[12]/LCDVD[20] —** LCD data.[18]
			O	**PWM1[6] —** Pulse Width Modulator 1, channel 6 output.
			I	**CAP0[0] —** Capture input for Timer 0, channel 0.
P1[27]/$\overline{\text{USB\_INT1}}$/ LCDVD[13]/ $\overline{\text{LCDVD[21]}}$/ $\overline{\text{USB\_OVRCR1}}$/ CAP0[1]	88[1]	T12[1]	I/O	**P1[27] —** General purpose digital input/output pin.
			I	**$\overline{\text{USB\_INT1}}$ —** USB port 1 OTG transceiver interrupt (OTG transceiver).[18]
			O	**LCDVD[13]/LCDVD[21] —** LCD data.[18]
			I	**$\overline{\text{USB\_OVRCR1}}$ —** USB port 1 Over-Current status.
			I	**CAP0[1] —** Capture input for Timer 0, channel 1.
P1[28]/USB_SCL1/ LCDVD[14]/ LCDVD[22]/ PCAP1[0]/MAT0[0]	90[1]	T13[1]	I/O	**P1[28] —** General purpose digital input/output pin.
			I/O	**USB_SCL1 —** USB port 1 I^2C-bus serial clock (OTG transceiver).[18]
			O	**LCDVD[14]/LCDVD[22] —** LCD data.[18]
			I	**PCAP1[0] —** Capture input for PWM1, channel 0.
			O	**MAT0[0] —** Match output for Timer 0, channel 0.
P1[29]/USB_SDA1/ LCDVD[15]/ LCDVD[23]/ PCAP1[1]/MAT0[1]	92[1]	U14[1]	I/O	**P1[29] —** General purpose digital input/output pin.
			I/O	**USB_SDA1 —** USB port 1 I^2C-bus serial data (OTG transceiver).[18]
			O	**LCDVD[15]/LCDVD[23] —** LCD data.[18]
			I	**PCAP1[1] —** Capture input for PWM1, channel 1.
			O	**MAT0[1] —** Match output for Timer 0, channel 0.
P1[30]/ USB_PWRD2/ V_{BUS}/AD0[4]	42[2]	P2[2]	I/O	**P1[30] —** General purpose digital input/output pin.
			I	**USB_PWRD2 —** Power Status for USB port 2.
			I	**V_{BUS} —** Monitors the presence of USB bus power. **Note:** This signal must be HIGH for USB reset to occur.
			I	**AD0[4] —** A/D converter 0, input 4.
P1[31]/ $\overline{\text{USB\_OVRCR2}}$/ SCK1/AD0[5]	40[2]	P1[2]	I/O	**P1[31] —** General purpose digital input/output pin.
			I	**$\overline{\text{USB\_OVRCR2}}$ —** Over-Current status for USB port 2.
			I/O	**SCK1 —** Serial Clock for SSP1.
			I	**AD0[5] —** A/D converter 0, input 5.

Table 4. Pin description *…continued*

Symbol	Pin	Ball	Type	Description
P2[16]/$\overline{\text{CAS}}$	87[1]	R11[1]	I/O	**P2[16] —** General purpose digital input/output pin.
			O	**$\overline{\text{CAS}}$ —** LOW active SDRAM Column Address Strobe.
P2[17]/$\overline{\text{RAS}}$	95[1]	R13[1]	I/O	**P2[17] —** General purpose digital input/output pin.
			O	**$\overline{\text{RAS}}$ —** LOW active SDRAM Row Address Strobe.
P2[18]/ CLKOUT0	59[1]	U3[1]	I/O	**P2[18] —** General purpose digital input/output pin.
			O	**CLKOUT0 —** SDRAM clock 0.
P2[19]/ CLKOUT1	67[1]	R7[1]	I/O	**P2[19] —** General purpose digital input/output pin.
			O	**CLKOUT1 —** SDRAM clock 1.
P2[20]/$\overline{\text{DYCS0}}$	73[1]	T8[1]	I/O	**P2[20] —** General purpose digital input/output pin.
			O	**$\overline{\text{DYCS0}}$ —** SDRAM chip select 0.
P2[21]/$\overline{\text{DYCS1}}$	81[1]	U11[1]	I/O	**P2[21] —** General purpose digital input/output pin.
			O	**$\overline{\text{DYCS1}}$ —** SDRAM chip select 1.
P2[22]/$\overline{\text{DYCS2}}$/ CAP3[0]/SCK0	85[1]	U12[1]	I/O	**P2[22] —** General purpose digital input/output pin.
			O	**$\overline{\text{DYCS2}}$ —** SDRAM chip select 2.
			I	**CAP3[0] —** Capture input for Timer 3, channel 0.
			I/O	**SCK0 —** Serial clock for SSP0.
P2[23]/$\overline{\text{DYCS3}}$/ CAP3[1]/SSEL0	64[1]	U5[1]	I/O	**P2[23] —** General purpose digital input/output pin.
			O	**$\overline{\text{DYCS3}}$ —** SDRAM chip select 3.
			I	**CAP3[1] —** Capture input for Timer 3, channel 1.
			I/O	**SSEL0 —** Slave Select for SSP0.
P2[24]/ CKEOUT0	53[1]	P5[1]	I/O	**P2[24] —** General purpose digital input/output pin.
			O	**CKEOUT0 —** SDRAM clock enable 0.
P2[25]/ CKEOUT1	54[1]	R4[1]	I/O	**P2[25] —** General purpose digital input/output pin.
			O	**CKEOUT1 —** SDRAM clock enable 1.
P2[26]/ CKEOUT2/ MAT3[0]/MISO0	57[1]	T4[1]	I/O	**P2[26] —** General purpose digital input/output pin.
			O	**CKEOUT2 —** SDRAM clock enable 2.
			O	**MAT3[0] —** Match output for Timer 3, channel 0.
			I/O	**MISO0 —** Master In Slave Out for SSP0.
P2[27]/ CKEOUT3/ MAT3[1]/MOSI0	47[1]	P3[1]	I/O	**P2[27] —** General purpose digital input/output pin.
			O	**CKEOUT3 —** SDRAM clock enable 3.
			O	**MAT3[1] —** Match output for Timer 3, channel 1.
			I/O	**MOSI0 —** Master Out Slave In for SSP0.
P2[28]/ DQMOUT0	49[1]	P4[1]	I/O	**P2[28] —** General purpose digital input/output pin.
			O	**DQMOUT0 —** Data mask 0 used with SDRAM and static devices.
P2[29]/ DQMOUT1	43[1]	N3[1]	I/O	**P2[29] —** General purpose digital input/output pin.
			O	**DQMOUT1 —** Data mask 1 used with SDRAM and static devices.
P2[30]/ DQMOUT2/ MAT3[2]/SDA2	31[1]	L4[1]	I/O	**P2[30] —** General purpose digital input/output pin.
			O	**DQMOUT2 —** Data mask 2 used with SDRAM and static devices.
			O	**MAT3[2] —** Match output for Timer 3, channel 2.
			I/O	**SDA2 —** I^2C2 data input/output (this is not an open-drain pin).

Table 4. Pin description *…continued*

Symbol	Pin	Ball	Type	Description
P3[16]/D16/ PWM0[1]/TXD1	137[1]	F17[1]	I/O	**P3[16] —** General purpose digital input/output pin.
			I/O	**D16 —** External memory data line 16.
			O	**PWM0[1] —** Pulse Width Modulator 0, output 1.
			O	**TXD1 —** Transmitter output for UART1.
P3[17]/D17/ PWM0[2]/RXD1	143[1]	F15[1]	I/O	**P3[17] —** General purpose digital input/output pin.
			I/O	**D17 —** External memory data line 17.
			O	**PWM0[2] —** Pulse Width Modulator 0, output 2.
			I	**RXD1 —** Receiver input for UART1.
P3[18]/D18/ PWM0[3]/CTS1	151[1]	C15[1]	I/O	**P3[18] —** General purpose digital input/output pin.
			I/O	**D18 —** External memory data line 18.
			O	**PWM0[3] —** Pulse Width Modulator 0, output 3.
			I	**CTS1 —** Clear to Send input for UART1.
P3[19]/D19/ PWM0[4]/DCD1	161[1]	B14[1]	I/O	**P3[19] —** General purpose digital input/output pin.
			I/O	**D19 —** External memory data line 19.
			O	**PWM0[4] —** Pulse Width Modulator 0, output 4.
			I	**DCD1 —** Data Carrier Detect input for UART1.
P3[20]/D20/ PWM0[5]/DSR1	167[1]	A13[1]	I/O	**P3[20] —** General purpose digital input/output pin.
			I/O	**D20 —** External memory data line 20.
			O	**PWM0[5] —** Pulse Width Modulator 0, output 5.
			I	**DSR1 —** Data Set Ready input for UART1.
P3[21]/D21/ PWM0[6]/DTR1	175[1]	C10[1]	I/O	**P3[21] —** General purpose digital input/output pin.
			I/O	**D21 —** External memory data line 21.
			O	**PWM0[6] —** Pulse Width Modulator 0, output 6.
			O	**DTR1 —** Data Terminal Ready output for UART1.
P3[22]/D22/ PCAP0[0]/RI1	195[1]	C6[1]	I/O	**P3[22] —** General purpose digital input/output pin.
			I/O	**D22 —** External memory data line 22.
			I	**PCAP0[0] —** Capture input for PWM0, channel 0.
			I	**RI1 —** Ring Indicator input for UART1.
P3[23]/D23/ CAP0[0]/ PCAP1[0]	65[1]	T6[1]	I/O	**P3[23] —** General purpose digital input/output pin.
			I/O	**D23 —** External memory data line 23.
			I	**CAP0[0] —** Capture input for Timer 0, channel 0.
			I	**PCAP1[0] —** Capture input for PWM1, channel 0.
P3[24]/D24/ CAP0[1]/ PWM1[1]	58[1]	R5[1]	I/O	**P3[24] —** General purpose digital input/output pin.
			I/O	**D24 —** External memory data line 24.
			I	**CAP0[1] —** Capture input for Timer 0, channel 1.
			O	**PWM1[1] —** Pulse Width Modulator 1, output 1.
P3[25]/D25/ MAT0[0]/ PWM1[2]	56[1]	U2[1]	I/O	**P3[25] —** General purpose digital input/output pin.
			I/O	**D25 —** External memory data line 25.
			O	**MAT0[0] —** Match output for Timer 0, channel 0.
			O	**PWM1[2] —** Pulse Width Modulator 1, output 2.

Table 4. Pin description *…continued*

Symbol	Pin	Ball	Type	Description
P4[23]/A23/ RXD2/MOSI1	129[1]	J15[1]	I/O	**P4[23] —** General purpose digital input/output pin.
			I/O	**A23 —** External memory address line 23.
			I	**RXD2 —** Receiver input for UART2.
			I/O	**MOSI1 —** Master Out Slave In for SSP1.
P4[24]/$\overline{OE}$	183[1]	B8[1]	I/O	**P4[24] —** General purpose digital input/output pin.
			O	**$\overline{OE}$ —** LOW active Output Enable signal.
P4[25]/$\overline{WE}$	179[1]	B9[1]	I/O	**P4[25] —** General purpose digital input/output pin.
			O	**$\overline{WE}$ —** LOW active Write Enable signal.
P4[26]/BLS0	119[1]	L15[1]	I/O	**P4[26] —** General purpose digital input/output pin.
			O	**BLS0 —** LOW active Byte Lane select signal 0.
P4[27]/BLS1	139[1]	G15[1]	I/O	**P4[27] —** General purpose digital input/output pin.
			O	**BLS1 —** LOW active Byte Lane select signal 1.
P4[28]/BLS2/ MAT2[0]/LCDVD[6]/ LCDVD[10]/ LCDVD[2]/ TXD3	170[1]	C11[1]	I/O	**P4 [28] —** General purpose digital input/output pin.
			O	**BLS2 —** LOW active Byte Lane select signal 2.
			O	**MAT2[0] —** Match output for Timer 2, channel 0.[21]
			O	**LCDVD[6]/LCDVD[10]/LCDVD[2] —** LCD data.[21]
			O	**TXD3 —** Transmitter output for UART3.
P4[29]/BLS3/ MAT2[1] LCDVD[7]/ LCDVD[11]/ LCDVD[3]/RXD3	176[1]	B10[1]	I/O	**P4[29] —** General purpose digital input/output pin.
			O	**BLS3 —** LOW active Byte Lane select signal 3.
			O	**MAT2[1] —** Match output for Timer 2, channel 1.[21]
			O	**LCDVD[7]/LCDVD[11]/LCDVD[3] —** LCD data.[21]
			I	**RXD3 —** Receiver input for UART3.
P4[30]/$\overline{CS0}$	187[1]	B7[1]	I/O	**P4[30] —** General purpose digital input/output pin.
			O	**$\overline{CS0}$ —** LOW active Chip Select 0 signal.
P4[31]/$\overline{CS1}$	193[1]	A4[1]	I/O	**P4[31] —** General purpose digital input/output pin.
			O	**$\overline{CS1}$ —** LOW active Chip Select 1 signal.
ALARM	37[8]	N1[8]	O	**ALARM —** RTC controlled output. This is a 1.8 V pin. It goes HIGH when a RTC alarm is generated.
USB_D−2	52	U1	I/O	**USB_D−2 —** USB port 2 bidirectional D− line.
DBGEN	9[1][22]	F4[1][22]	I	**DBGEN —** JTAG interface control signal. Also used for boundary scanning.
TDO	2[1][23]	D3[1][23]	O	**TDO —** Test Data Out for JTAG interface.
TDI	4[1][22]	C2[1][22]	I	**TDI —** Test Data In for JTAG interface.
TMS	6[1][22]	E3[1][22]	I	**TMS —** Test Mode Select for JTAG interface.
$\overline{TRST}$	8[1][22]	D1[1][22]	I	**$\overline{TRST}$ —** Test Reset for JTAG interface.
TCK	10[1][23]	E2[1][23]	I	**TCK —** Test Clock for JTAG interface. This clock must be slower than $\frac{1}{6}$ of the CPU clock (CCLK) for the JTAG interface to operate.
RTCK	206[1][22]	C3[1][22]	I/O	**RTCK —** JTAG interface control signal. **Note:** LOW on this pin while $\overline{RESET}$ is LOW enables ETM pins (P2[9:0]) to operate as Trace port after reset.
$\overline{RSTOUT}$	29	K3	O	**$\overline{RSTOUT}$ —** This is a 3.3 V pin. LOW on this pin indicates LPC2478 being in Reset state.

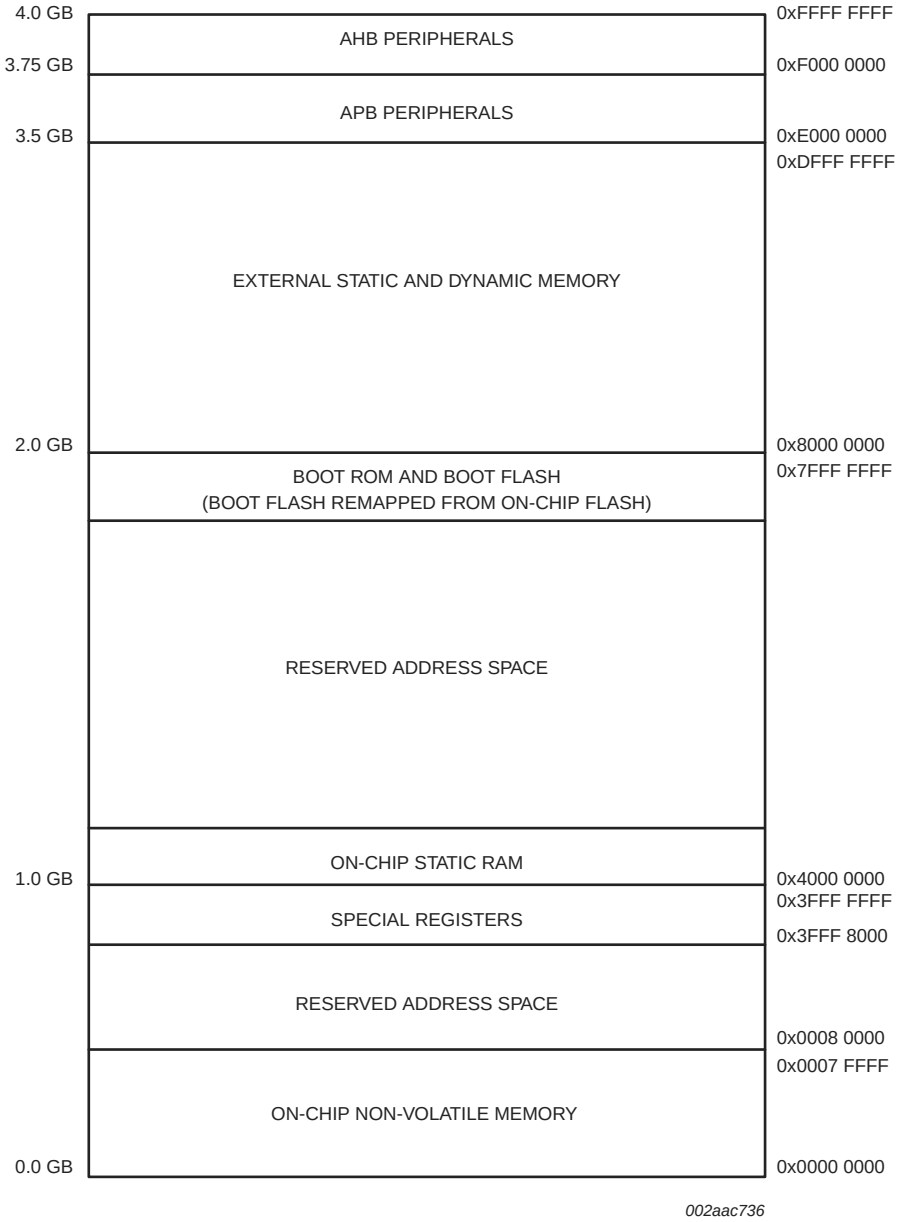


Fig 4. LPC2478 memory map

7.5 Interrupt controller

The ARM processor core has two interrupt inputs called Interrupt Request (IRQ) and Fast Interrupt Request (FIQ). The VIC takes 32 interrupt request inputs which can be programmed as FIQ or vectored IRQ types. The programmable assignment scheme means that priorities of interrupts from the various peripherals can be dynamically assigned and adjusted.

FIQs have the highest priority. If more than one request is assigned to FIQ, the VIC ORs the requests to produce the FIQ signal to the ARM processor. The fastest possible FIQ latency is achieved when only one request is classified as FIQ, because then the FIQ

7.12 USB interface

The Universal Serial Bus (USB) is a 4-wire bus that supports communication between a host and one or more (up to 127) peripherals. The host controller allocates the USB bandwidth to attached devices through a token-based protocol. The bus supports hot plugging and dynamic configuration of the devices. All transactions are initiated by the host controller.

The LPC2478 USB interface includes a device, host, and OTG controller. Details on typical USB interfacing solutions can be found in Section 14.2 “Suggested USB interface solutions” on page 77

7.12.1 USB device controller

The device controller enables 12 Mbit/s data exchange with a USB host controller. It consists of a register interface, serial interface engine, endpoint buffer memory, and a DMA controller. The serial interface engine decodes the USB data stream and writes data to the appropriate endpoint buffer. The status of a completed USB transfer or error condition is indicated via status registers. An interrupt is also generated if enabled. When enabled, the DMA controller transfers data between the endpoint buffer and the USB RAM.

7.12.1.1 Features

- Fully compliant with *USB 2.0 Specification* (full speed).
- Supports 32 physical (16 logical) endpoints with a 4 kB endpoint buffer RAM.
- Supports Control, Bulk, Interrupt and Isochronous endpoints.
- Scalable realization of endpoints at run time.
- Endpoint Maximum packet size selection (up to USB maximum specification) by software at run time.
- Supports SoftConnect and GoodLink features.
- While USB is in the Suspend mode, the LPC2478 can enter one of the reduced power modes and wake up on USB activity.
- Supports DMA transfers with the DMA RAM of 16 kB on all non-control endpoints.
- Allows dynamic switching between CPU-controlled and DMA modes.
- Double buffer implementation for Bulk and Isochronous endpoints.

7.12.2 USB host controller

The host controller enables full- and low-speed data exchange with USB devices attached to the bus. It consists of register interface, serial interface engine and DMA controller. The register interface complies with the Open Host Controller Interface (OHCI) specification.

7.12.2.1 Features

- OHCI compliant
- Two downstream ports
- Supports per-port power switching

- UART3 includes an IrDA mode to support infrared communication.

7.17 SPI serial I/O controller

The LPC2478 contains one SPI controller. SPI is a full duplex serial interface designed to handle multiple masters and slaves connected to a given bus. Only a single master and a single slave can communicate on the interface during a given data transfer. During a data transfer the master always sends 8 bits to 16 bits of data to the slave, and the slave always sends 8 bits to 16 bits of data to the master.

7.17.1 Features

- Compliant with SPI specification
- Synchronous, Serial, Full Duplex Communication
- Combined SPI master and slave
- Maximum data bit rate of one eighth of the input clock rate
- 8 bits to 16 bits per transfer

7.18 SSP serial I/O controller

The LPC2478 contains two SSP controllers. The SSP controller is capable of operation on a SPI, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. The SSP supports full duplex transfers, with frames of 4 bits to 16 bits of data flowing from the master to the slave and from the slave to the master. In practice, often only one of these data flows carries meaningful data.

7.18.1 Features

- Compatible with Motorola SPI, 4-wire TI SSI, and National Semiconductor Microwire buses
- Synchronous serial communication
- Master or slave operation
- 8-frame FIFOs for both transmit and receive
- 4-bit to 16-bit frame
- Maximum SPI bus data bit rate of one half (Master mode) and one twelfth (Slave mode) of the input clock rate
- DMA transfers supported by GPDMA

7.19 SD/MMC card interface

The Secure Digital and Multimedia Card Interface (MCI) allows access to external SD memory cards. The SD card interface conforms to the *SD Multimedia Card Specification Version 2.11*.

7.19.1 Features

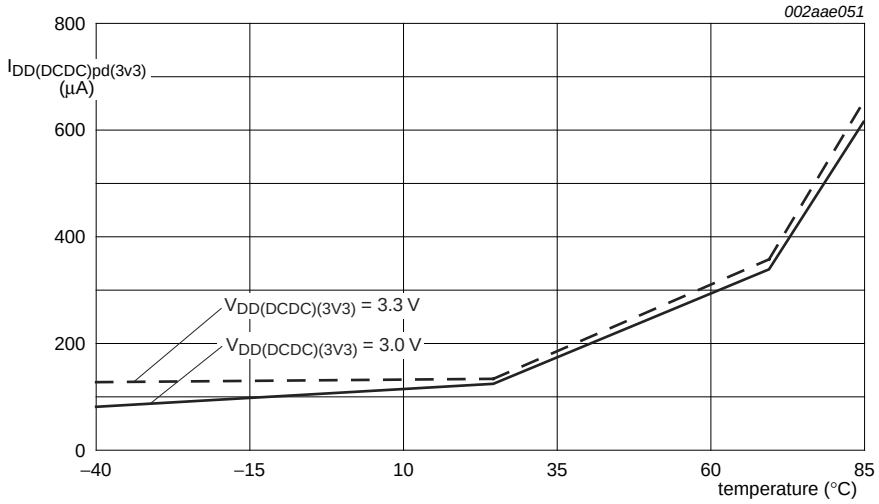
- The MCI provides all functions specific to the SD/MMC memory card. These include the clock generation unit, power management control, and command and data transfer.

10. Static characteristics

Table 9. Static characteristics

T_{amb} = −40 °C to +85 °C for commercial applications, unless otherwise specified.

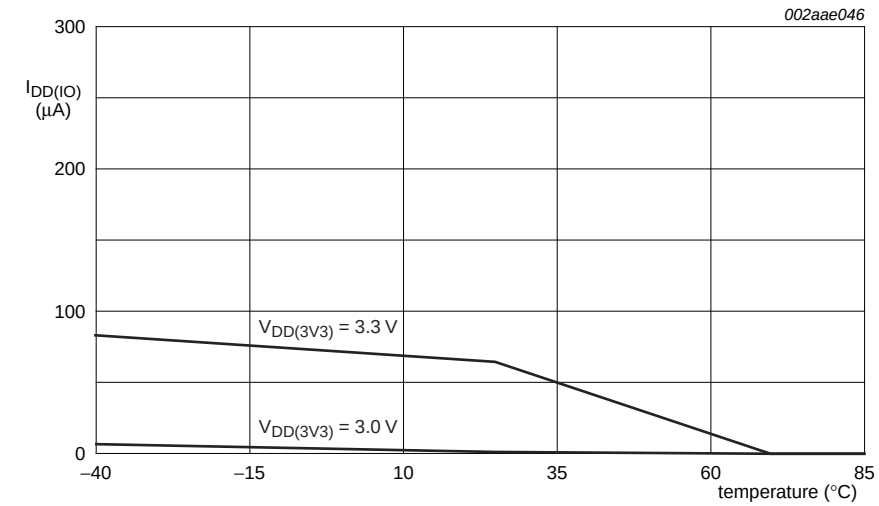
Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$V_{DD(3V3)}$	supply voltage (3.3 V)	core and external rail		3.0	3.3	3.6	V
$V_{DD(DCDC)(3V3)}$	DC-to-DC converter supply voltage (3.3 V)			3.0	3.3	3.6	V
V_{DDA}	analog 3.3 V pad supply voltage			3.0	3.3	3.6	V
$V_{i(VBAT)}$	input voltage on pin VBAT		[2]	2.0	3.3	3.6	V
$V_{i(VREF)}$	input voltage on pin VREF			2.5	3.3	V_{DDA}	V
$I_{DD(DCDC)act(3V3)}$	active mode DC-to-DC converter supply current (3.3 V)	$V_{DD(DCDC)(3V3)}$ = 3.3 V; T_{amb} = 25 °C; code `while(1){}` executed from flash; no peripherals enabled; PCLK = CCLK					
		CCLK = 10 MHz		-	15	-	mA
		CCLK = 72 MHz		-	63	-	mA
		all peripherals enabled; PCLK = CCLK / 8					
		CCLK = 10 MHz		-	21	-	mA
		CCLK = 72 MHz		-	92	-	mA
		all peripherals enabled; PCLK = CCLK					
		CCLK = 10 MHz		-	27	-	mA
		CCLK = 72 MHz		-	125	-	mA
$I_{DD(DCDC)pd(3V3)}$	Power-down mode DC-to-DC converter supply current (3.3 V)	$V_{DD(DCDC)(3V3)}$ = 3.3 V; T_{amb} = 25 °C	[3]	-	113	-	μA
$I_{DD(DCDC)dpd(3V3)}$	Deep power-down mode DC-to-DC converter supply current (3.3 V)		[3]	-	20	-	μA
I_{BATact}	active mode battery supply current		[4]	-	20	-	μA
I_{BAT}	battery supply current	Deep power-down mode	[3]	-	20	-	μA



$V_{DD(3V3)} = V_{i(VBAT)} = 3.3$ V; $T_{amb} = 25$ °C.

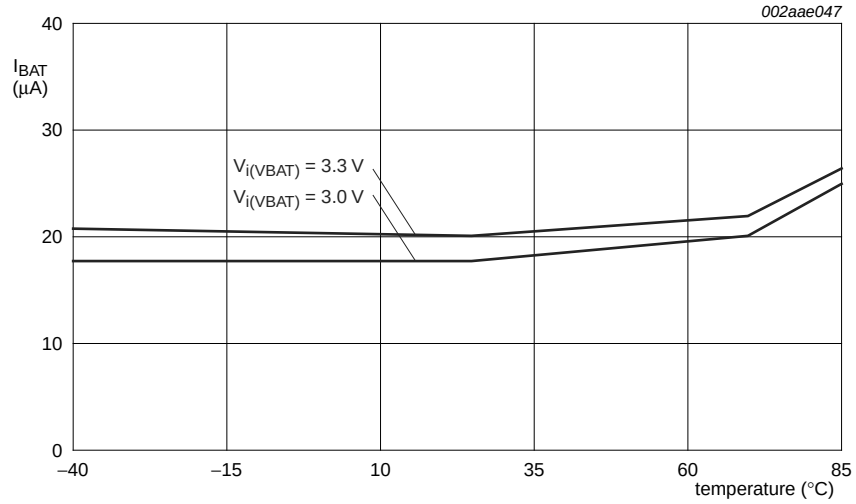
Fig 7. Total DC-to-DC converter supply current $I_{DD(DCDC)pd(3V3)}$ at different temperatures in Power-down mode

10.2 Deep power-down mode



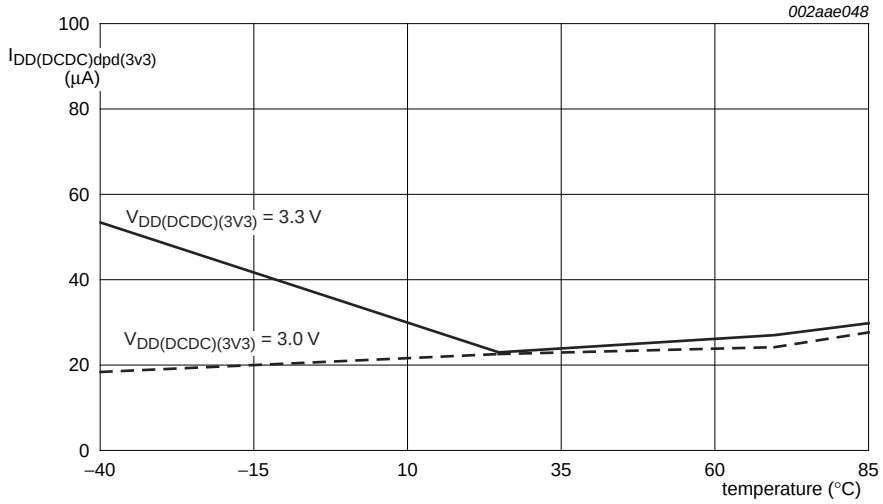
$V_{DD(3V3)} = V_{DD(DCDC)(3V3)} = 3.3$ V; $T_{amb} = 25$ °C.

Fig 8. I/O maximum supply current $I_{DD(IO)}$ versus temperature in Deep power-down mode



$V_{DD(3V3)} = V_{DD(DCDC)(3V3)} = 3.3$ V; $T_{amb} = 25$ °C

Fig 9. RTC battery maximum supply current I_{BAT} versus temperature in Deep power-down mode



$V_{DD(3V3)} = V_{i(VBAT)} = 3.3$ V; $T_{amb} = 25$ °C.

Fig 10. Total DC-to-DC converter maximum supply current $I_{DD(DCDC)dpd(3V3)}$ versus temperature in Deep power-down mode

11.5 Static external memory interface

Table 15. Dynamic characteristics: Static external memory interface
C_L = 30 pF, T_{amb} = −40 °C to 85 °C, $V_{DD(DCDC)(3V3)}$ = $V_{DD(3V3)}$ = 3.0 V to 3.6 V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Common to read and write cycles[1]						
t_{CSLAV}	$\overline{CS}$ LOW to address valid time		−0.29	0.20	2.54	ns
Read cycle parameters[1][2]						
t_{OELAV}	$\overline{OE}$ LOW to address valid time		−0.29	0.20	2.54	ns
t_{CSLOEL}	$\overline{CS}$ LOW to $\overline{OE}$ LOW time		−0.78 + $T_{cy(CCLK)}$ × WAITOEN	0 + $T_{cy(CCLK)}$ × WAITOEN	0.49 + $T_{cy(CCLK)}$ × WAITOEN	ns
t_{am}	memory access time	[3][4]	(WAITRD − WAITOEN + 1) × $T_{cy(CCLK)}$ − 12.70	(WAITRD − WAITOEN + 1) × $T_{cy(CCLK)}$ − 9.57	(WAITRD − WAITOEN + 1) × $T_{cy(CCLK)}$ − 8.11	ns
$t_{h(D)}$	data input hold time	[5]	0	-	-	ns
t_{CSHOEH}	$\overline{CS}$ HIGH to $\overline{OE}$ HIGH time		−0.49	0	0.20	ns
t_{OEHANV}	$\overline{OE}$ HIGH to address invalid time		−0.20	0.20	2.44	ns
t_{OELOEH}	$\overline{OE}$ LOW to $\overline{OE}$ HIGH time		−0.59 + (WAITRD − WAITOEN + 1) × $T_{cy(CCLK)}$	0 + (WAITRD − WAITOEN + 1) × $T_{cy(CCLK)}$	0.10 + (WAITRD − WAITOEN + 1) × $T_{cy(CCLK)}$	
t_{BLSLAV}	$\overline{BLS}$ LOW to address valid time		−0.39	0	2.54	ns
$t_{CSHBLSH}$	$\overline{CS}$ HIGH to $\overline{BLS}$ HIGH time		−0.88	0.49	0.68	ns
Write cycle parameters[1][6]						
t_{CSLWEL}	$\overline{CS}$ LOW to $\overline{WE}$ LOW time		−0.88 + $T_{cy(CCLK)}$ × (1 + WAITWEN)	0.10 + $T_{cy(CCLK)}$ × (1 + WAITWEN)	0.20 + $T_{cy(CCLK)}$ × (1 + WAITWEN)	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW time		−0.88	0.49	0.98	ns
t_{WELDV}	$\overline{WE}$ LOW to data valid time		0.68	2.54	5.86	ns
t_{CSLDV}	$\overline{CS}$ LOW to data valid time		0	2.64	4.79	ns
t_{WELWEH}	$\overline{WE}$ LOW to $\overline{WE}$ HIGH time	[3]	−0.78 + $T_{cy(CCLK)}$ × (WAITWR − WAITWEN + 1)	0 + $T_{cy(CCLK)}$ × (WAITWR − WAITWEN + 1)	0.10 + $T_{cy(CCLK)}$ × (WAITWR − WAITWEN + 1)	ns
$t_{BLSLBLSH}$	$\overline{BLS}$ LOW to $\overline{BLS}$ HIGH time	[3]	−0.88 + $T_{cy(CCLK)}$ × (WAITWR − WAITWEN + 3)	0 + $T_{cy(CCLK)}$ × (WAITWR − WAITWEN + 3)	0.59 + $T_{cy(CCLK)}$ × (WAITWR − WAITWEN + 3)	ns
t_{WEHANV}	$\overline{WE}$ HIGH to address invalid time	[3]	0 + $T_{cy(CCLK)}$	0.20 + $T_{cy(CCLK)}$	2.74 + $T_{cy(CCLK)}$	ns

11.7 Timing

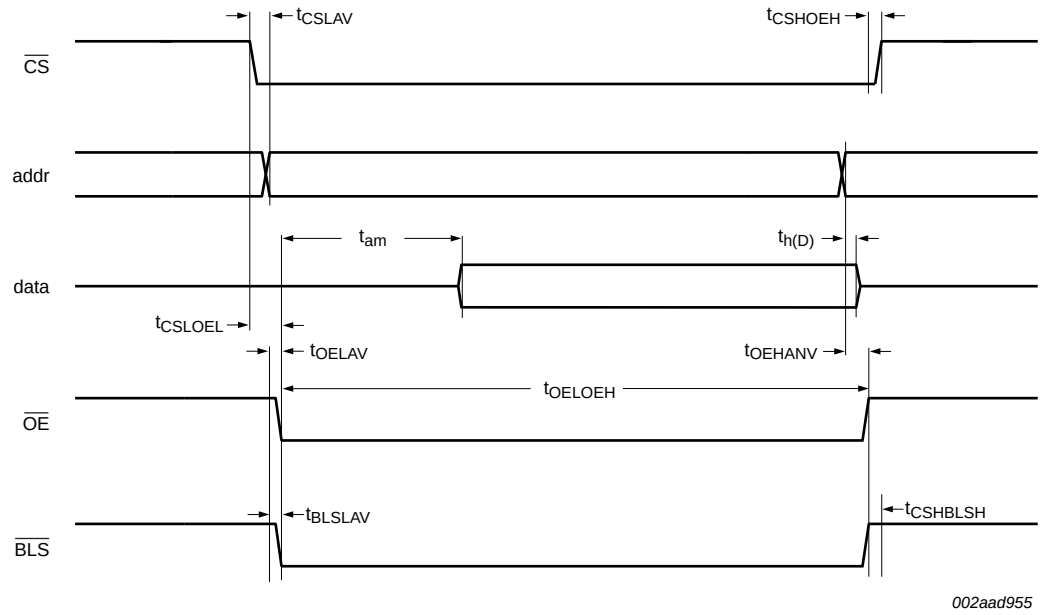


Fig 14. External memory read access

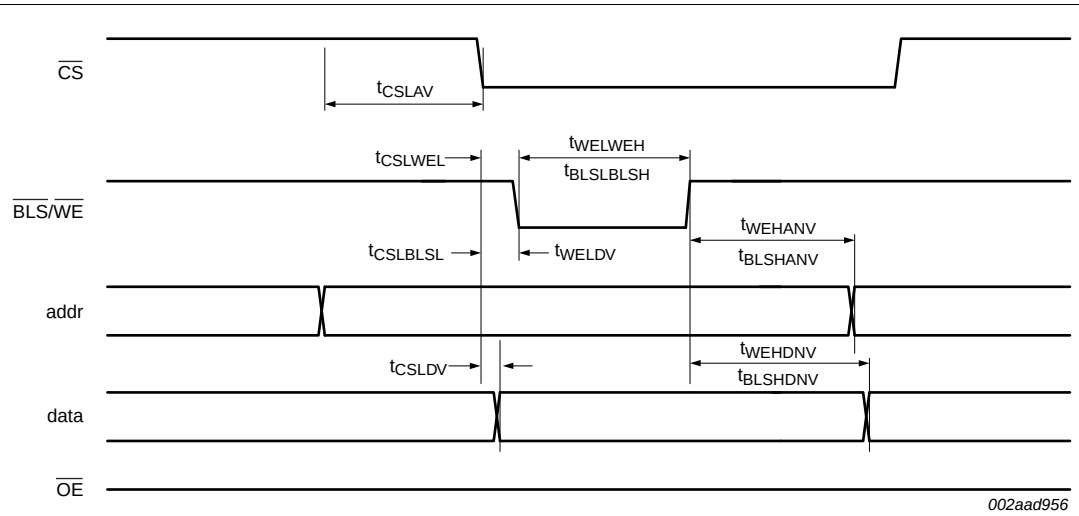


Fig 15. External memory write access

12. ADC electrical characteristics

Table 18. ADC static characteristics

V_{DDA} = 2.5 V to 3.6 V; T_{amb} = −40 °C to +85 °C unless otherwise specified; ADC frequency 4.5 MHz.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IA}	analog input voltage			0	-	V_{DDA}	V
C_{ia}	analog input capacitance			-	-	1	pF
E_D	differential linearity error		[1][2][3]	-	-	±1	LSB
$E_{L(adj)}$	integral non-linearity		[1][4]	-	-	±2	LSB
E_O	offset error		[1][5]	-	-	±3	LSB
E_G	gain error		[1][6]	-	-	±0.5	%
E_T	absolute error		[1][7]	-	-	±4	LSB
R_{vsi}	voltage source interface resistance		[8]	-	-	40	kΩ

[1] Conditions: V_{SSA} = 0 V, V_{DDA} = 3.3 V.

[2] The ADC is monotonic, there are no missing codes.

[3] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 19.

[4] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 19.

[5] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 19.

[6] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 19.

[7] The absolute error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 19.

[8] See Figure 20.

Table 21. LCD panel connections for STN dual panel mode

External pin	4-bit mono STN dual panel		8-bit mono STN dual panel		Color STN dual panel	
	LPC2478 pin used	LCD function	LPC2478 pin used	LCD function	LPC2478 pin used	LCD function
LCDVD[23]	-	-	-	-	-	-
LCDVD[22]	-	-	-	-	-	-
LCDVD[21]	-	-	-	-	-	-
LCDVD[20]	-	-	-	-	-	-
LCDVD[19]	-	-	-	-	-	-
LCDVD[18]	-	-	-	-	-	-
LCDVD[17]	-	-	-	-	-	-
LCDVD[16]	-	-	-	-	-	-
LCDVD[15]	-	-	P1[29][4]	LD[7]	P1[29][4]	LD[7]
LCDVD[14]	-	-	P1[28][4]	LD[6]	P1[28][4]	LD[6]
LCDVD[13]	-	-	P1[27][4]	LD[5]	P1[27][4]	LD[5]
LCDVD[12]		-	P1[26][4]	LD[4]	P1[26][4]	LD[4]
LCDVD[11]	P4[29][3]	LD[3]	P1[25][4]	LD[3]	P1[25][4]	LD[3]
LCDVD[10]	P4[28][3]	LD[2]	P1[24][4]	LD[2]	P1[24][4]	LD[2]
LCDVD[9]	P2[13][2]	LD[1]	P1[23][4]	LD[1]	P1[23][4]	LD[1]
LCDVD[8]	P2[12][2]	LD[0]	P1[22][4]	LD[0]	P1[22][4]	LD[0]
LCDVD[7]	-	-	P1[21][4]	UD[7]	P1[21][4]	UD[7]
LCDVD[6]	-	-	P1[20][4]	UD[6]	P1[20][4]	UD[6]
LCDVD[5]	-	-	P2[13][2]	UD[5]	P2[13][2]	UD[5]
LCDVD[4]	-	-	P2[12][2]	UD[4]	P2[12][2]	UD[4]
LCDVD[3]	P2[9][1]	UD[3]	P2[9][1]	UD[3]	P2[9][1]	UD[3]
LCDVD[2]	P2[8][1]	UD[2]	P2[8][1]	UD[2]	P2[8][1]	UD[2]
LCDVD[1]	P2[7][1]	UD[1]	P2[7][1]	UD[1]	P2[7][1]	UD[1]
LCDVD[0]	P2[6][1]	UD[0]	P2[6][1]	UD[0]	P2[6][1]	UD[0]
LCDLP	P2[5][1]	LCDLP	P2[5][1]	LCDLP	P2[5][1]	LCDLP
LCDENAB/ LCDM	P2[4][1]	LCDENAB/ LCDM	P2[4][1]	LCDENAB/ LCDM	P2[4][1]	LCDENAB/ LCDM
LCDFP	P2[3][1]	LCDFP	P2[3][1]	LCDFP	P2[3][1]	LCDFP
LCDDCLK	P2[2][1]	LCDDCLK	P2[2][1]	LCDDCLK	P2[2][1]	LCDDCLK
LCDLE	P2[1][1]	LCDLE	P2[1][1]	LCDLE	P2[1][1]	LCDLE
LCDPWR	P2[0][1]	LCDPWR	P2[0][1]	LCDPWR	P2[0][1]	LCDPWR
LCDCLKIN	P2[11][2]	LCDCLKIN	P2[11][2]	LCDCLKIN	P2[11][2]	LCDCLKIN

[1] ETM replaced by LCD pins.

[2] External interrupt pins $\overline{\text{EINT1}}$, $\overline{\text{EINT2}}$, $\overline{\text{EINT3}}$ replaced with LCD pins.

[3] Timer pins MAT2[0] and MAT2[1] replaced with LCD pins.

[4] USB OTG pins replaced by LCD pins.

14.5 XTAL and RTCX Printed Circuit Board (PCB) layout guidelines

The crystal should be connected on the PCB as close as possible to the oscillator input and output pins of the chip. Take care that the load capacitors C_{x1}, C_{x2}, and C_{x3} in case of third overtone crystal usage have a common ground plane. The external components must also be connected to the ground plain. Loops must be made as small as possible in order to keep the noise coupled in via the PCB as small as possible. Also parasitics should stay as small as possible. Values of C_{x1} and C_{x2} should be chosen smaller accordingly to the increase in parasitics of the PCB layout.

14.6 Standard I/O pin configuration

Figure 30 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver
- Digital input: Pull-up enabled/disabled
- Digital input: Pull-down enabled/disabled
- Analog input (for ADC input channels)

The default configuration for standard I/O pins is input with pull-up enabled. The weak MOS devices provide a drive capability equivalent to pull-up and pull-down resistors.

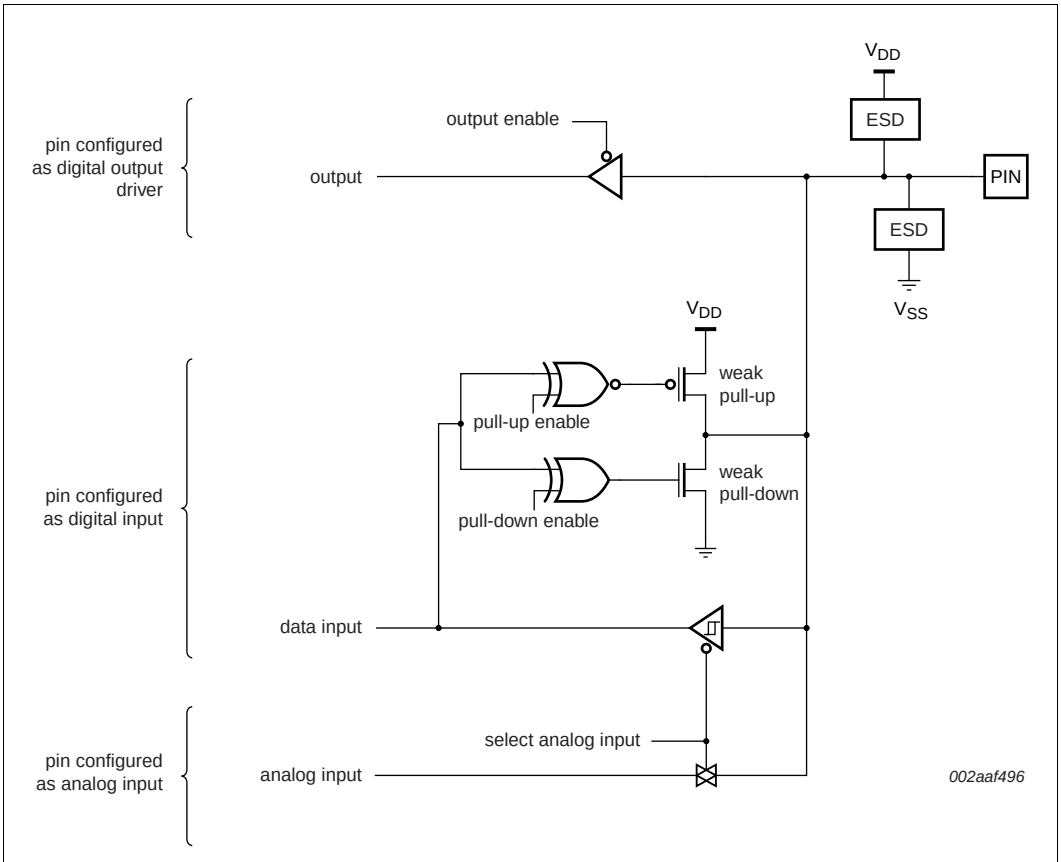


Fig 30. Standard I/O pin configuration with analog input

14.7 Reset pin configuration

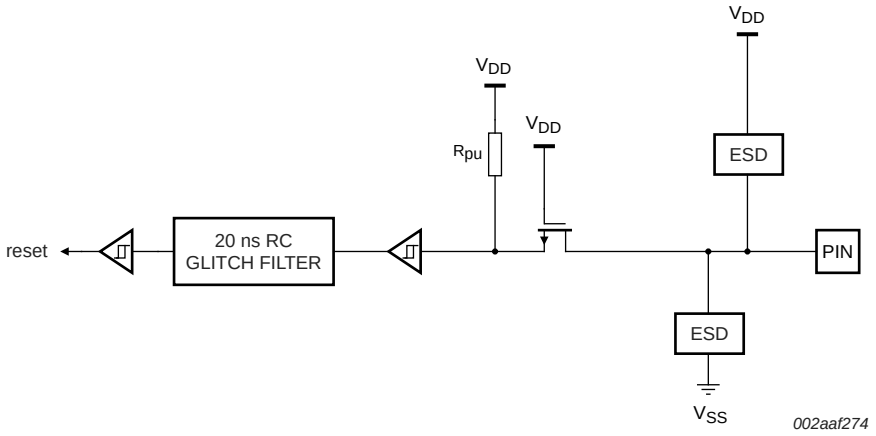
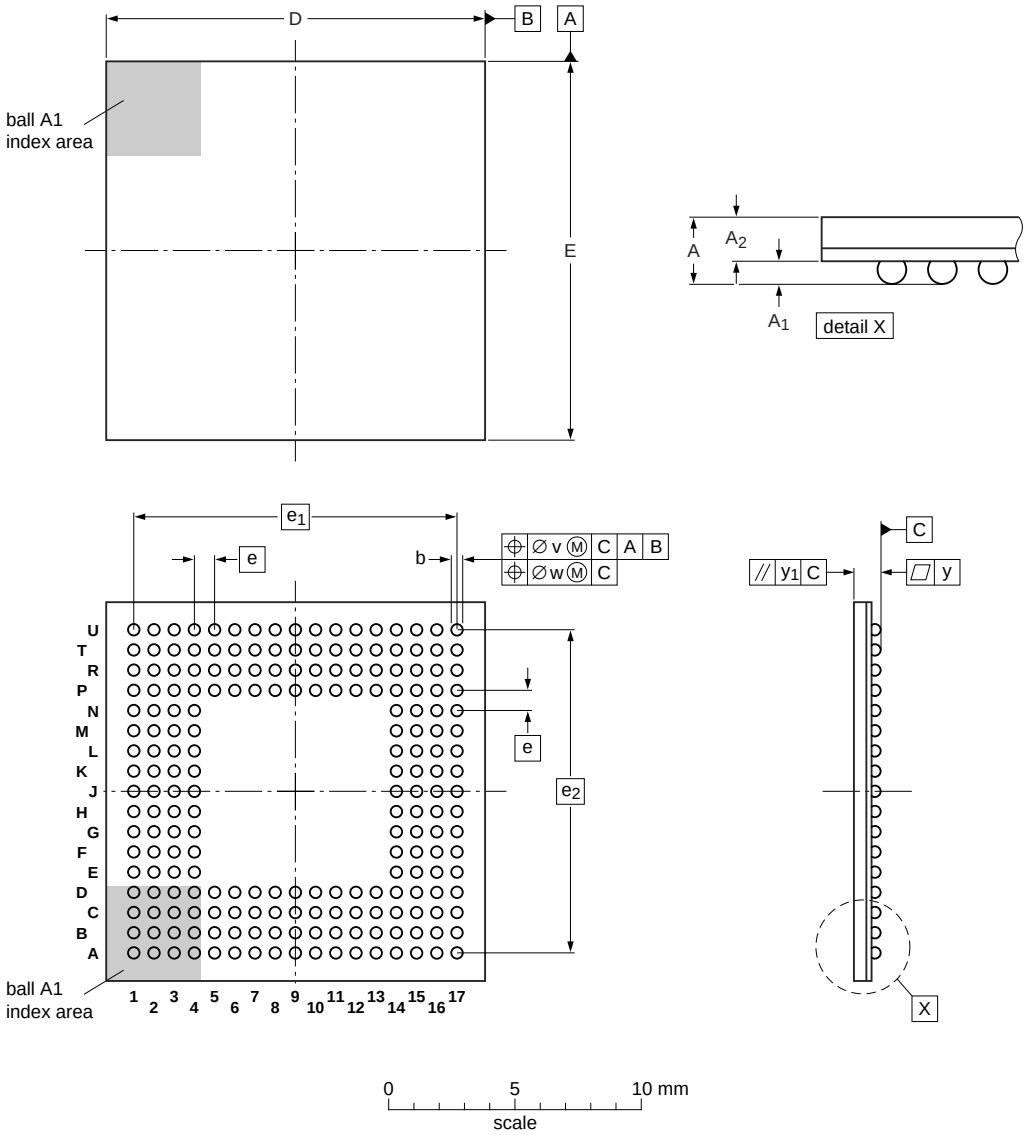


Fig 31. Reset pin configuration

TFBGA208: plastic thin fine-pitch ball grid array package; 208 balls; body 15 x 15 x 0.7 mm **SOT950-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.2	0.4 0.3	0.8 0.6	0.5 0.4	15.1 14.9	15.1 14.9	0.8	12.8	12.8	0.15	0.08	0.12	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT950-1		- - -				~~06-06-01~~ 06-06-14

Fig 33. Package outline SOT950-1 (TFBGA208)