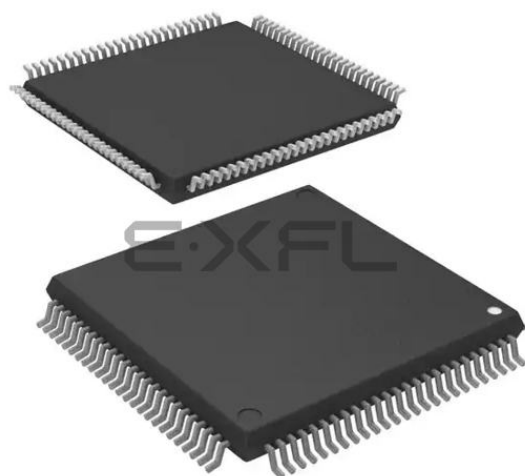




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Details

Product Status	Not For New Designs
Core Processor	R32C/100
Core Size	16/32-Bit
Speed	50MHz
Connectivity	EBI/EMI, I ² C, IEBus, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	82
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	63K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f64111dfb-u0

1.3 Block Diagram

Figures 1.2 and 1.3 show block diagram of the R32C/111 Group.

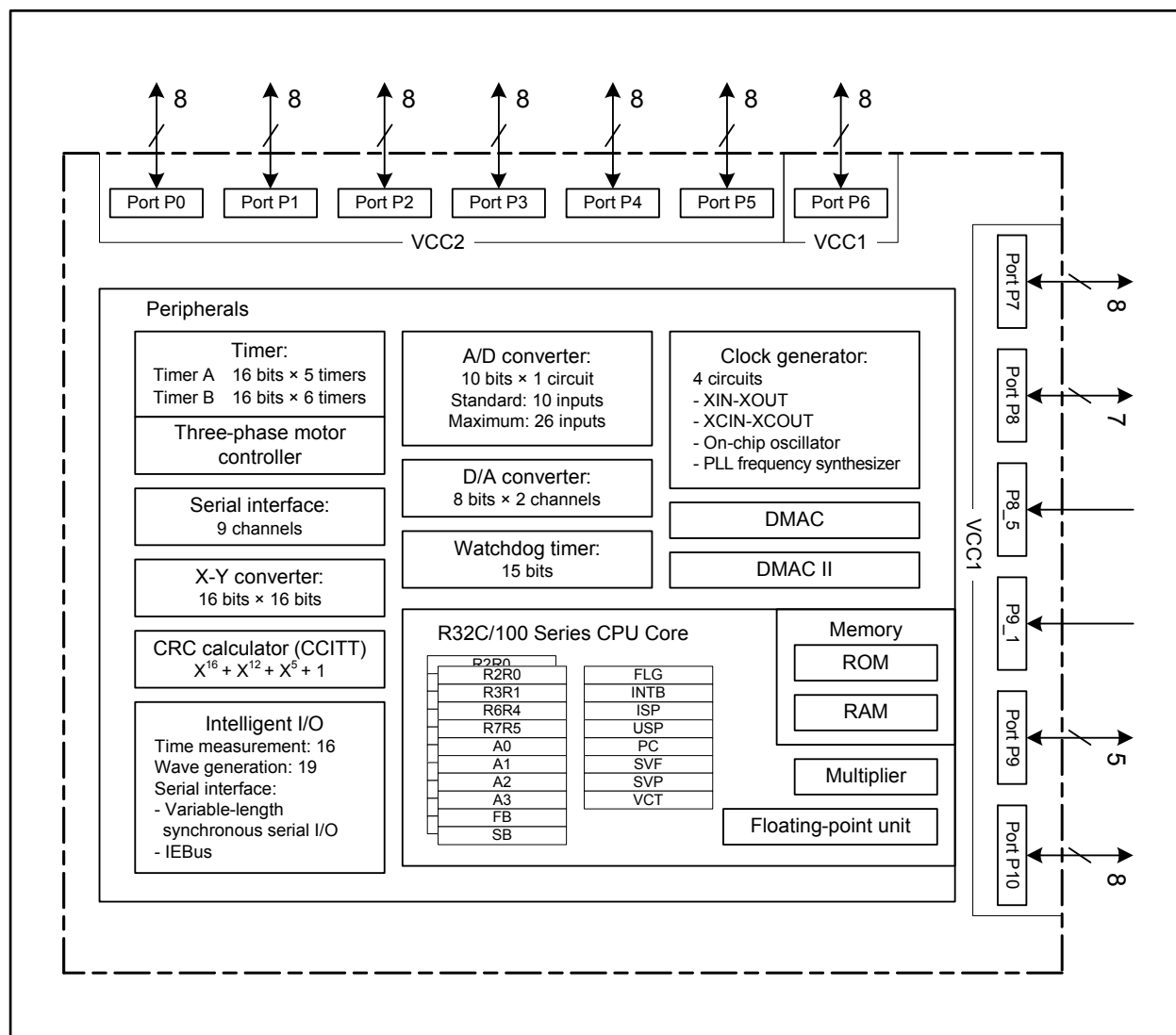


Figure 1.2 R32C/111 Group Block Diagram for the 100-pin Package

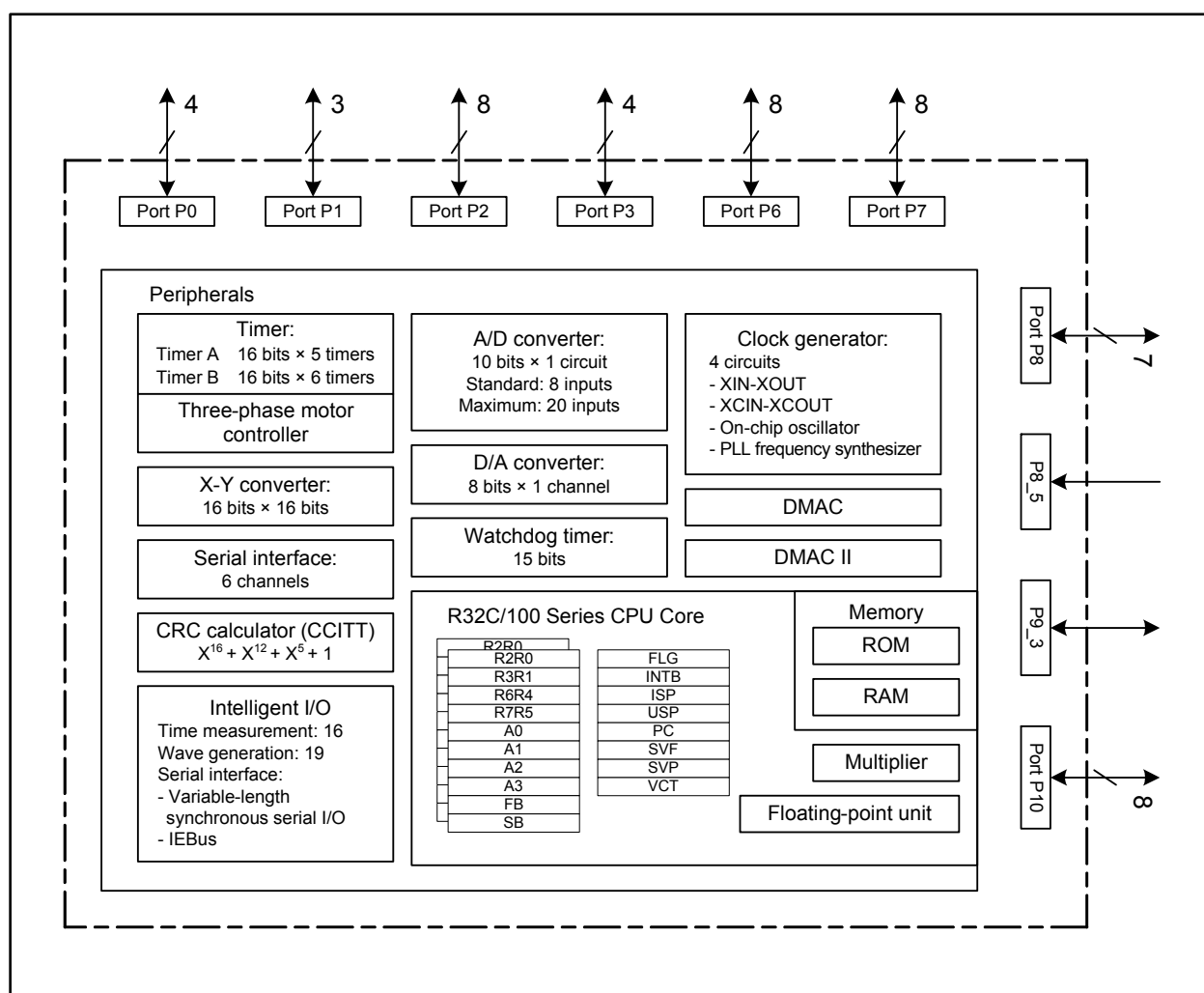


Figure 1.3 R32C/111 Group Block Diagram for the 64-pin Package

1.5 Pin Definitions and Functions

Tables 1.11 to 1.17 show the pin definitions and functions.

Table 1.11 Pin Definitions and Functions for the 100-pin Package (1/4)

Function	Symbol	I/O	Power Supply	Description
Power supply	VCC1, VCC2, VSS	I	—	Applicable as follows: VCC1 and VCC2 = 3.0 to 5.5 V ($VCC1 \geq VCC2$), VSS = 0 V
Connecting pins for decoupling capacitor	VDC0, VDC1	—	—	A decoupling capacitor for internal voltage should be connected between VDC0 and VDC1
Analog power supply	AVCC, AVSS	I	VCC1	Power supply for the A/D converter. AVCC and AVSS should be connected to VCC1 and VSS, respectively
Reset input	RESET	I	VCC1	The MCU is reset when this pin is driven low
CNVSS	CNVSS	I	VCC1	This pin should be connected to VSS via a resistor
Debug port	NSD	I/O	VCC1	This pin is to communicate with a debugger. It should be connected to VCC1 via a resistor of 1 to 4.7 k Ω
Main clock input	XIN	I	VCC1	Input/output for the main clock oscillator. A crystal, or a ceramic resonator should be connected between pins XIN and XOUT. An external clock should be input at the XIN while leaving the XOUT open
Main clock output	XOUT	O	VCC1	
Sub clock input	XCIN	I	VCC1	Input/output for the sub clock oscillator. A crystal oscillator should be connected between pins XCIN and XCOU. An external clock should be input at the XCIN while leaving the XCOU open
Sub clock output	XCOU	O	VCC1	
BCLK output	BCLK	O	VCC2	BCLK output
Clock output	CLKOUT	O	VCC2	Output of the clock with the same frequency as low speed clocks, f8, or f32
External interrupt input	INT0 to INT5	I	VCC1 VCC2	Input for external interrupts
NMI input	P8_5/NMI	I	VCC1	Input for NMI
Key input interrupt	KI0 to KI3	I	VCC1	Input for the key input interrupt
Bus control pins	D0 to D7	I/O	VCC2	Input/output of data (D0 to D7) while accessing an external memory space with a separate bus
	D8 to D15	I/O	VCC2	Input/output of data (D8 to D15) while accessing an external memory space with 16-bit separate bus
	A0 to A23	O	VCC2	Output of address bits A0 to A23

Table 4.2 SFR List (2)

Address	Register	Symbol	Reset Value
000060h			
000061h	Timer B5 Interrupt Control Register	TB5IC	XXXX X000b
000062h	UART5 Transmit/NACK Interrupt Control Register	S5TIC	XXXX X000b
000063h	UART2 Receive/ACK Interrupt Control Register	S2RIC	XXXX X000b
000064h	UART6 Transmit/NACK Interrupt Control Register	S6TIC	XXXX X000b
000065h	UART3 Receive/ACK Interrupt Control Register	S3RIC	XXXX X000b
000066h	UART5/6 Bus Collision, START Condition/STOP Condition Detection Interrupt Control Register	BCN5IC/BCN6IC	XXXX X000b
000067h	UART4 Receive/ACK Interrupt Control Register	S4RIC	XXXX X000b
000068h	DMA0 Transfer Complete Interrupt Control Register	DM0IC	XXXX X000b
000069h	UART0/3 Bus Collision, START Condition/STOP Condition Detection Interrupt Control Register	BCN0IC/BCN3IC	XXXX X000b
00006Ah	DMA2 Transfer Complete Interrupt Control Register	DM2IC	XXXX X000b
00006Bh	A/D Converter 0 Convert Completion Interrupt Control Register	AD0IC	XXXX X000b
00006Ch	Timer A0 Interrupt Control Register	TA0IC	XXXX X000b
00006Dh	Intelligent I/O Interrupt Control Register 0	IIO0IC	XXXX X000b
00006Eh	Timer A2 Interrupt Control Register	TA2IC	XXXX X000b
00006Fh	Intelligent I/O Interrupt Control Register 2	IIO2IC	XXXX X000b
000070h	Timer A4 Interrupt Control Register	TA4IC	XXXX X000b
000071h	Intelligent I/O Interrupt Control Register 4	IIO4IC	XXXX X000b
000072h	UART0 Receive/ACK Interrupt Control Register	S0RIC	XXXX X000b
000073h	Intelligent I/O Interrupt Control Register 6	IIO6IC	XXXX X000b
000074h	UART1 Receive/ACK Interrupt Control Register	S1RIC	XXXX X000b
000075h	Intelligent I/O Interrupt Control Register 8	IIO8IC	XXXX X000b
000076h	Timer B1 Interrupt Control Register	TB1IC	XXXX X000b
000077h	Intelligent I/O Interrupt Control Register 10	IIO10IC	XXXX X000b
000078h	Timer B3 Interrupt Control Register	TB3IC	XXXX X000b
000079h			
00007Ah	INT5 Interrupt Control Register	INT5IC	XX00 X000b
00007Bh			
00007Ch	INT3 Interrupt Control Register	INT3IC	XX00 X000b
00007Dh			
00007Eh	INT1 Interrupt Control Register	INT1IC	XX00 X000b
00007Fh			
000080h			
000081h	UART2 Transmit/NACK Interrupt Control Register	S2TIC	XXXX X000b
000082h	UART5 Receive/ACK Interrupt Control Register	S5RIC	XXXX X000b
000083h	UART3 Transmit/NACK Interrupt Control Register	S3TIC	XXXX X000b
000084h	UART6 Receive/ACK Interrupt Control Register	S6RIC	XXXX X000b
000085h	UART4 Transmit/NACK Interrupt Control Register	S4TIC	XXXX X000b
000086h			
000087h	UART2 Bus Collision, START Condition/STOP Condition Detection Interrupt Control Register	BCN2IC	XXXX X000b

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.9 SFR List (9)

Address	Register	Symbol	Reset Value
0001A0h	Group 0 Base Timer Register	G0BT	XXXXh
0001A1h			
0001A2h	Group 0 Base Timer Control Register 0	G0BCR0	0000 0000b
0001A3h	Group 0 Base Timer Control Register 1	G0BCR1	0000 0000b
0001A4h	Group 0 Time Measurement Prescaler Register 6	G0TPR6	00h
0001A5h	Group 0 Time Measurement Prescaler Register 7	G0TPR7	00h
0001A6h	Group 0 Function Enable Register	G0FE	00h
0001A7h	Group 0 Function Select Register	G0FS	00h
0001A8h			
0001A9h			
0001AAh			
0001ABh			
0001ACh			
0001ADh			
0001AEh			
0001AFh			
0001B0h			
0001B1h			
0001B2h			
0001B3h			
0001B4h			
0001B5h			
0001B6h			
0001B7h			
0001B8h			
0001B9h			
0001BAh			
0001BBh			
0001BCh			
0001BDh			
0001BEh			
0001BFh			
0001C0h			
0001C1h			
0001C2h			
0001C3h			
0001C4h	UART5 Special Mode Register 4	U5SMR4	00h
0001C5h	UART5 Special Mode Register 3	U5SMR3	00h
0001C6h	UART5 Special Mode Register 2	U5SMR2	00h
0001C7h	UART5 Special Mode Register	U5SMR	00h
0001C8h	UART5 Transmit/Receive Mode Register	U5MR	00h
0001C9h	UART5 Bit Rate Register	U5BRG	XXh
0001CAh	UART5 Transmit Buffer Register	U5TB	XXXXh
0001CBh			
0001CCh	UART5 Transmit/Receive Control Register 0	U5C0	0000 1000b
0001CDh	UART5 Transmit/Receive Control Register 1	U5C1	0000 0010b
0001CEh	UART5 Receive Buffer Register	U5RB	XXXXh
0001CFh			

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.16 SFR List (16)

Address	Register	Symbol	Reset Value
0003B0h			
0003B1h			
0003B2h			
0003B3h			
0003B4h			
0003B5h			
0003B6h			
0003B7h			
0003B8h			
0003B9h			
0003BAh			
0003BBh			
0003BCh			
0003BDh			
0003BEh			
0003BFh			
0003C0h	Port P0 Register	P0	XXh
0003C1h	Port P1 Register	P1	XXh
0003C2h	Port P0 Direction Register	PD0	0000 0000b
0003C3h	Port P1 Direction Register	PD1	0000 0000b
0003C4h	Port P2 Register	P2	XXh
0003C5h	Port P3 Register	P3	XXh
0003C6h	Port P2 Direction Register	PD2	0000 0000b
0003C7h	Port P3 Direction Register	PD3	0000 0000b
0003C8h	Port P4 Register	P4	XXh
0003C9h	Port P5 Register	P5	XXh
0003CAh	Port P4 Direction Register	PD4	0000 0000b
0003CBh	Port P5 Direction Register	PD5	0000 0000b
0003CCh	Port P6 Register	P6	XXh
0003CDh	Port P7 Register	P7	XXh
0003CEh	Port P6 Direction Register	PD6	0000 0000b
0003CFh	Port P7 Direction Register	PD7	0000 0000b
0003D0h	Port P8 Register	P8	XXh
0003D1h	Port P9 Register	P9	XXh
0003D2h	Port P8 Direction Register	PD8	00X0 0000b
0003D3h	Port P9 Direction Register	PD9	0000 0000b
0003D4h	Port P10 Register	P10	XXh
0003D5h			
0003D6h	Port P10 Direction Register	PD10	0000 0000b
0003D7h			
0003D8h			
0003D9h			
0003DAh			
0003DBh			
0003DCh			
0003DDh			
0003DEh			
0003DFh			

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.22 SFR List (22)

Address	Register	Symbol	Reset Value
0400F0h	Port P10_0 Function Select Register	P10_0S	0XXX X000b
0400F1h			
0400F2h	Port P10_1 Function Select Register	P10_1S	0XXX X000b
0400F3h			
0400F4h	Port P10_2 Function Select Register	P10_2S	0XXX X000b
0400F5h			
0400F6h	Port P10_3 Function Select Register	P10_3S	0XXX X000b
0400F7h			
0400F8h	Port P10_4 Function Select Register	P10_4S	0XXX X000b
0400F9h			
0400FAh	Port P10_5 Function Select Register	P10_5S	0XXX X000b
0400FBh			
0400FCh	Port P10_6 Function Select Register	P10_6S	0XXX X000b
0400FDh			
0400FEh	Port P10_7 Function Select Register	P10_7S	0XXX X000b
0400FFh			
040100h			
040101h			
040102h			
040103h			
040104h			
040105h			
040106h			
040107h			
040108h			
040109h			
04010Ah			
04010Bh			
04010Ch			
04010Dh			
04010Eh			
04010Fh			
040110h			
040111h			
040112h			
040113h			
040114h			
040115h			
040116h			
040117h			
040118h			
040119h			
04011Ah			
04011Bh			
04011Ch			
04011Dh			
04011Eh			
04011Fh			

X: Undefined

Blanks are reserved. No access is allowed.

Table 5.9 Power Supply Circuit Timing Characteristics
 ($V_{CC1} = V_{CC2} = 3.0$ to 5.5 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted)

Symbol	Characteristic	Measurement Condition	Value			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Internal power supply start-up stabilization time after the main power supply is turned on				2	ms

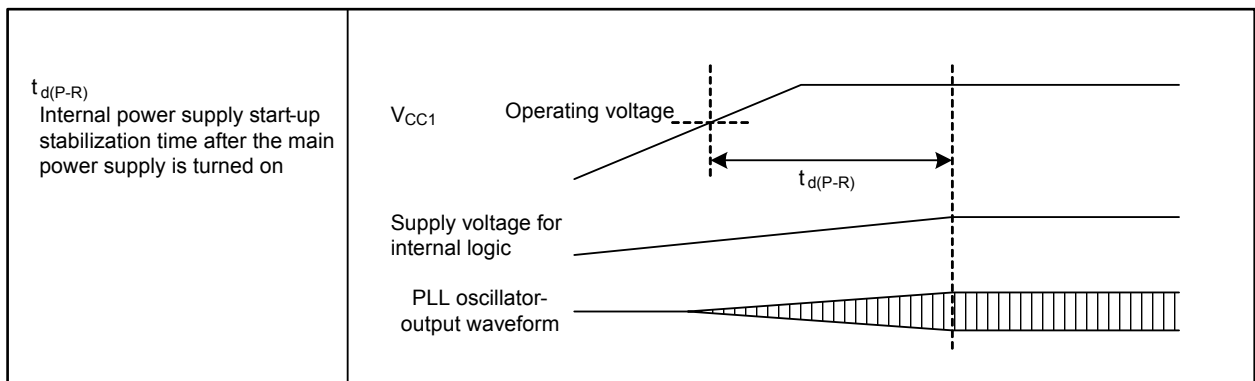


Figure 5.3 Power Supply Circuit Timing

Table 5.10 Electrical Characteristics of Voltage Regulator for Internal Logic
 ($V_{CC1} = V_{CC2} = 3.0$ to 5.5 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted)

Symbol	Characteristics	Measurement Condition	Value			Unit
			Min.	Typ.	Max.	
V_{VDC1}	Output voltage			1.5		V

Table 5.11 Electrical Characteristics of Low Voltage Detector
 ($V_{CC1} = V_{CC2} = 4.2$ to 5.5 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted)

Symbol	Characteristics	Measurement Condition	Value			Unit
			Min.	Typ.	Max.	
ΔV_{det}	Detected voltage error				± 0.3	V
$V_{det(R)} - V_{det(F)}$	Hysteresis width		0			V
—	Self-consuming current	$V_{CC1} = 5.0$ V, low voltage detector enabled		4		μA
$t_{d(E-A)}$	Operation start time of low voltage detector				150	μs

$$V_{CC1} = V_{CC2} = 5\text{ V}$$

Timing Requirements ($V_{CC1} = V_{CC2} = 4.2$ to 5.5 V , $V_{SS} = 0\text{ V}$, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.20 External Clock Input

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{C(X)}$	External clock input period	62.5	250	ns
$t_{W(XH)}$	External clock input high level pulse width	25		ns
$t_{W(XL)}$	External clock input low level pulse width	25		ns
$t_{r(X)}$	External clock input rise time		5	ns
$t_{f(X)}$	External clock input fall time		5	ns
t_W / t_C	External clock input duty	40	60	%

Table 5.21 External Bus Timing

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{su(D-R)}$	Data setup time before read	40		ns
$t_{h(R-D)}$	Data hold time after read	0		ns
$t_{dis(R-D)}$	Data disable time after read		$0.5 \times t_{C(Base)} + 10$	ns

$$V_{CC1} = V_{CC2} = 5\text{ V}$$

Timing Requirements ($V_{CC1} = V_{CC2} = 4.2$ to 5.5 V , $V_{SS} = 0\text{ V}$, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.22 Timer A Input (counting input in event counter mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{C(TA)}$	TAiIN input clock cycle time	200		ns
$t_{W(TAH)}$	TAiIN input high level pulse width	80		ns
$t_{W(TAL)}$	TAiIN input low level pulse width	80		ns

Table 5.23 Timer A Input (gating input in timer mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{C(TA)}$	TAiIN input clock cycle time	400		ns
$t_{W(TAH)}$	TAiIN input high level pulse width	180		ns
$t_{W(TAL)}$	TAiIN input low level pulse width	180		ns

Table 5.24 Timer A Input (external trigger input in one-shot timer mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{C(TA)}$	TAiIN input clock cycle time	200		ns
$t_{W(TAH)}$	TAiIN input high level pulse width	80		ns
$t_{W(TAL)}$	TAiIN input low level pulse width	80		ns

Table 5.25 Timer A Input (external trigger input in pulse-width modulation mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{W(TAH)}$	TAiIN input high level pulse width	80		ns
$t_{W(TAL)}$	TAiIN input low level pulse width	80		ns

Table 5.26 Timer A Input (increment/decrement switching input in event counter mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{C(UP)}$	TAiOUT input clock cycle time	2000		ns
$t_{W(UPH)}$	TAiOUT input high level pulse width	1000		ns
$t_{W(UPL)}$	TAiOUT input low level pulse width	1000		ns
$t_{Su(UP-TIN)}$	TAiOUT input setup time	400		ns
$t_h(TIN-UP)$	TAiOUT input hold time	400		ns

$$V_{CC1} = V_{CC2} = 5 \text{ V}$$

Timing Requirements ($V_{CC1} = V_{CC2} = 4.2$ to 5.5 V , $V_{SS} = 0 \text{ V}$, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.27 Timer B Input (counting input in event counter mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{C(TB)}$	TBiIN input clock cycle time (one edge counting)	200		ns
$t_{W(TBH)}$	TBiIN input high level pulse width (one edge counting)	80		ns
$t_{W(TBL)}$	TBiIN input low level pulse width (one edge counting)	80		ns
$t_{C(TB)}$	TBiIN input clock cycle time (both edges counting)	200		ns
$t_{W(TBH)}$	TBiIN input high level pulse width (both edges counting)	80		ns
$t_{W(TBL)}$	TBiIN input low level pulse width (both edges counting)	80		ns

Table 5.28 Timer B Input (pulse period measure mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{C(TB)}$	TBiIN input clock cycle time	400		ns
$t_{W(TBH)}$	TBiIN input high level pulse width	180		ns
$t_{W(TBL)}$	TBiIN input low level pulse width	180		ns

Table 5.29 Timer B Input (pulse-width measure mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{C(TB)}$	TBiIN input clock cycle time	400		ns
$t_{W(TBH)}$	TBiIN input high level pulse width	180		ns
$t_{W(TBL)}$	TBiIN input low level pulse width	180		ns

$$V_{CC1} = V_{CC2} = 5\text{ V}$$

Timing Requirements ($V_{CC1} = V_{CC2} = 4.2$ to 5.5 V , $V_{SS} = 0\text{ V}$, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.30 Serial Interface

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{C(CK)}$	CLKi input clock cycle time	200		ns
$t_{W(CKH)}$	CLKi input high level pulse width	80		ns
$t_{W(CKL)}$	CLKi input low level pulse width	80		ns
$t_{Su(D-C)}$	RXD _i input setup time	80		ns
$t_{h(C-D)}$	RXD _i input hold time	90		ns

Table 5.31 A/D Trigger Input

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{W(ADH)}$	ADTRG input high level pulse width Hardware trigger input high level pulse width	$\frac{3}{\phi_{AD}}$		ns
$t_{W(ADL)}$	ADTRG input low level pulse width Hardware trigger input high level pulse width	125		ns

Table 5.32 External Interrupt $\overline{INT}_i$ Input

Symbol	Characteristic		Value		Unit
			Min.	Max.	
$t_{W(INH)}$	INT _i input high level pulse width	Edge sensitive	250		ns
		Level sensitive	$t_{C(CPU)} + 200$		ns
$t_{W(INL)}$	INT _i input low level pulse width	Edge sensitive	250		ns
		Level sensitive	$t_{C(CPU)} + 200$		ns

Table 5.33 Intelligent I/O

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{C(ISCLK2)}$	ISCLK2 input clock cycle time	600		ns
$t_{W(ISCLK2H)}$	ISCLK2 input high level pulse width	270		ns
$t_{W(ISCLK2L)}$	ISCLK2 input low level pulse width	270		ns
$t_{Su(RXD-ISCLK2)}$	ISRXD2 input setup time	150		ns
$t_{h(ISCLK2-RXD)}$	ISRXD2 input hold time	100		ns

$$V_{CC1} = V_{CC2} = 5 \text{ V}$$

Switching Characteristics ($V_{CC1} = V_{CC2} = 4.2$ to 5.5 V , $V_{SS} = 0 \text{ V}$, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.34 External Bus Timing (separate bus)

Symbol	Characteristic	Measurement Condition	Value		Unit
			Min.	Max.	
$t_{su(S-R)}$	Chip-select setup time before read	Refer to Figure 5.6	(1)		ns
$t_{h(R-S)}$	Chip-select hold time after read		$t_{c(Base)} - 10$		ns
$t_{su(A-R)}$	Address setup time before read		(1)		ns
$t_{h(R-A)}$	Address hold time after read		$t_{c(Base)} - 10$		ns
$t_{w(R)}$	Read pulse width		(1)		ns
$t_{su(S-W)}$	Chip-select setup time before write		(1)		ns
$t_{h(W-S)}$	Chip-select hold time after write		$1.5 \times t_{c(Base)} - 10$		ns
$t_{su(A-W)}$	Address setup time before write		(1)		ns
$t_{h(W-A)}$	Address hold time after write		$1.5 \times t_{c(Base)} - 10$		ns
$t_{w(W)}$	Write pulse width		(1)		ns
$t_{su(D-W)}$	Data setup time before write		(1)		ns
$t_{h(W-D)}$	Data hold time after write		0		ns

Note:

- The value is calculated using the formulas below based on the base clock cycles ($t_{c(Base)}$) and respective cycles of $T_{su(A-R)}$, $T_{w(R)}$, $T_{su(A-W)}$, and $T_{w(W)}$ set by registers EBC0 to EBC3. If the calculation results in a negative value, modify the value to be set. For details on how to set values, refer to the User's manual.

$$t_{su(S-R)} = t_{su(A-R)} = T_{su(A-R)} \times t_{c(Base)} - 15 \text{ [ns]}$$

$$t_{w(R)} = T_{w(R)} \times t_{c(Base)} - 10 \text{ [ns]}$$

$$t_{su(S-W)} = t_{su(A-W)} = T_{su(A-W)} \times t_{c(Base)} - 15 \text{ [ns]}$$

$$t_{w(W)} = t_{su(D-W)} = T_{w(W)} \times t_{c(Base)} - 10 \text{ [ns]}$$

$$V_{CC1} = V_{CC2} = 3.3 \text{ V}$$

Table 5.40 Electrical Characteristics (3/3)

($V_{CC1} = V_{CC2} = 3.0$ to 3.6 V , $V_{SS} = 0 \text{ V}$, and $T_a = T_{opr}$, unless otherwise noted)

Symbol	Characteristic	Measurement Condition	Value			Unit
			Min.	Typ.	Max.	
I_{CC}	Power supply current	In single-chip mode, output pins are left open and others are connected to V_{SS}				
		$f_{(CPU)} = 50 \text{ MHz}$, $f_{(BCLK)} = 25 \text{ MHz}$, $f_{(XIN)} = 8 \text{ MHz}$, Active: XIN, PLL, Stopped: XCIN, OCO		28	40	mA
		XIN-XOUT Drive strength: low		7		mA
		$f_{(CPU)} = f_{SO(PLL)}/24 \text{ MHz}$, Active: PLL (self-oscillation), Stopped: XIN, XCIN, OCO				
		XCIN-XCOUT Drive strength: low				
		$f_{(CPU)} = f_{(BCLK)} = f_{(XIN)}/256 \text{ MHz}$, $f_{(XIN)} = 8 \text{ MHz}$, Active: XIN, Stopped: PLL, XCIN, OCO		670		μA
		$f_{(CPU)} = f_{(BCLK)} = 32.768 \text{ kHz}$, Active: XCIN, Stopped: XIN, PLL, OCO, Main regulator: shutdown		180		μA
		$f_{(CPU)} = f_{(BCLK)} = f_{(OCO)}/4 \text{ kHz}$, Active: OCO, Stopped: XIN, PLL, XCIN, Main regulator: shutdown		190		μA
		$f_{(CPU)} = f_{(BCLK)} = f_{(XIN)}/256 \text{ MHz}$, $f_{(XIN)} = 8 \text{ MHz}$, Active: XIN, Stopped: PLL, XCIN, OCO, $T_a = 25^\circ\text{C}$, Wait mode		500	900	μA
I_{CC}	Power supply current	$f_{(CPU)} = f_{(BCLK)} = 32.768 \text{ kHz}$, Active: XCIN, Stopped: XIN, PLL, OCO, Main regulator: shutdown, $T_a = 25^\circ\text{C}$, Wait mode		8	140	μA
		$f_{(CPU)} = f_{(BCLK)} = f_{(OCO)}/4 \text{ kHz}$, Active: OCO, Stopped: XIN, PLL, XCIN, Main regulator: shutdown, $T_a = 25^\circ\text{C}$, Wait mode		10	150	μA
		Stopped: all clocks, Main regulator: shutdown, $T_a = 25^\circ\text{C}$		5	70	μA

$$V_{CC1} = V_{CC2} = 3.3 \text{ V}$$

Timing Requirements ($V_{CC1} = V_{CC2} = 3.0$ to 3.6 V , $V_{SS} = 0 \text{ V}$, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.50 Timer B Input (counting input in event counter mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input clock cycle time (one edge counting)	200		ns
$t_{w(TBH)}$	TBiIN input high level pulse width (one edge counting)	80		ns
$t_{w(TBL)}$	TBiIN input low level pulse width (one edge counting)	80		ns
$t_{c(TB)}$	TBiIN input clock cycle time (both edges counting)	200		ns
$t_{w(TBH)}$	TBiIN input high level pulse width (both edges counting)	80		ns
$t_{w(TBL)}$	TBiIN input low level pulse width (both edges counting)	80		ns

Table 5.51 Timer B Input (pulse period measure mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input clock cycle time	400		ns
$t_{w(TBH)}$	TBiIN input high level pulse width	180		ns
$t_{w(TBL)}$	TBiIN input low level pulse width	180		ns

Table 5.52 Timer B Input (pulse-width measure mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input clock cycle time	400		ns
$t_{w(TBH)}$	TBiIN input high level pulse width	180		ns
$t_{w(TBL)}$	TBiIN input low level pulse width	180		ns

$$V_{CC1} = V_{CC2} = 3.3 \text{ V}$$

Switching Characteristics ($V_{CC1} = V_{CC2} = 3.0$ to 3.6 V , $V_{SS} = 0 \text{ V}$, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.58 External Bus Timing (multiplexed bus)

Symbol	Characteristic	Measurement Condition	Value		Unit
			Min.	Max.	
$t_{su(S-ALE)}$	Chip-select setup time before ALE	Refer to Figure 5.6	(1)		ns
$t_{h(R-S)}$	Chip-select hold time after read		$1.5 \times t_{c(Base)} - 10$		ns
$t_{su(A-ALE)}$	Address setup time before ALE		(1)		ns
$t_{h(ALE-A)}$	Address hold time after ALE		$0.5 \times t_{c(Base)} - 5$		ns
$t_{h(R-A)}$	Address hold time after read		$1.5 \times t_{c(Base)} - 10$		ns
$t_{d(ALE-R)}$	ALE-read delay time		$0.5 \times t_{c(Base)} - 5$	$0.5 \times t_{c(Base)} + 10$	ns
$t_{w(ALE)}$	ALE pulse width		(1)		ns
$t_{dis(R-A)}$	Address disable time after read			8	ns
$t_{w(R)}$	Read pulse width		(1)		ns
$t_{h(W-S)}$	Chip-select hold time after write		$1.5 \times t_{c(Base)} - 10$		ns
$t_{h(W-A)}$	Address hold time after write		$1.5 \times t_{c(Base)} - 10$		ns
$t_{d(ALE-W)}$	ALE-write delay time		$0.5 \times t_{c(Base)} - 5$	$0.5 \times t_{c(Base)} + 10$	ns
$t_{w(W)}$	Write pulse width		(1)		ns
$t_{su(D-W)}$	Data setup time before write		(1)		ns
$t_{h(W-D)}$	Data hold time after write		$0.5 \times t_{c(Base)}$		ns

Note:

- The value is calculated using the formulas below based on the base clock cycles ($t_{c(Base)}$) and respective cycles of $T_{su(A-R)}$, $T_{w(R)}$, $T_{su(A-W)}$, and $T_{w(W)}$ set by registers EBC0 to EBC3. If the calculation results in a negative value, modify the value to be set. For details on how to set values, refer to the User's manual.

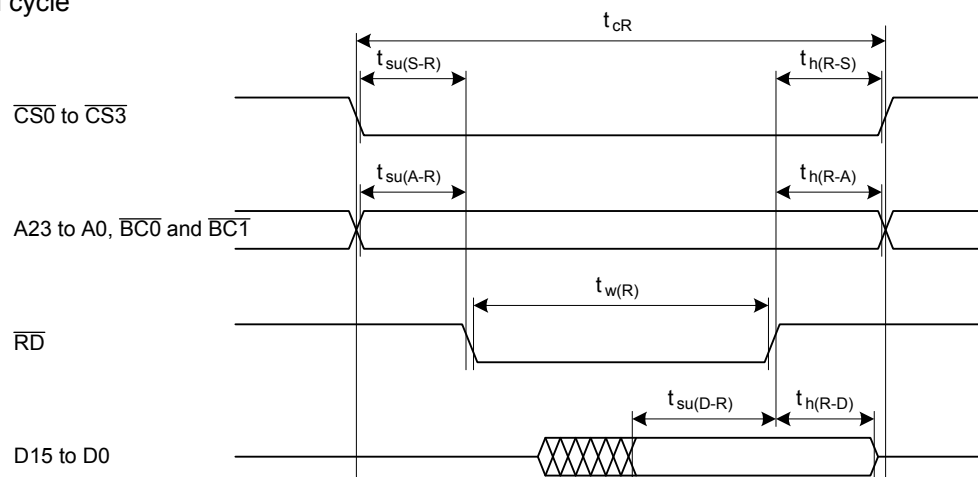
$$t_{su(S-ALE)} = t_{su(A-ALE)} = t_{w(ALE)} = (T_{su(A-R)} - 0.5) \times t_{c(Base)} - 15 \text{ [ns]}$$

$$t_{w(R)} = T_{w(R)} \times t_{c(Base)} - 10 \text{ [ns]}$$

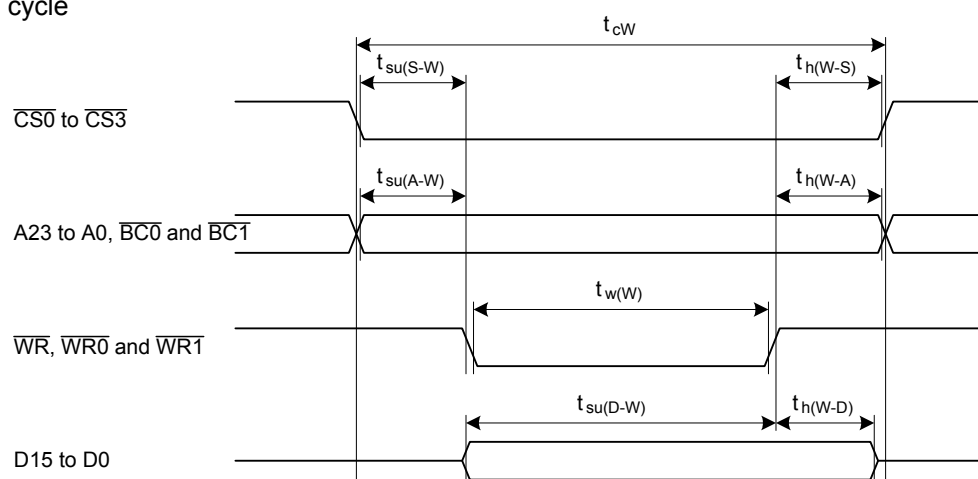
$$t_{w(W)} = t_{su(D-W)} = T_{w(W)} \times t_{c(Base)} - 10 \text{ [ns]}$$

External bus timing (separate bus)

Read cycle



Write cycle



Measurement conditions

Item		$V_{CC1} = V_{CC2} = 4.2 \text{ to } 5.5 \text{ V}$	$V_{CC1} = V_{CC2} = 3.0 \text{ to } 3.6 \text{ V}$
Criterion for input voltage	V_{IH}	2.5 V	1.5 V
	V_{IL}	0.8 V	0.5 V
Criterion for output voltage	V_{OH}	2.0 V	2.4 V
	V_{OL}	0.8 V	0.5 V

Figure 5.8 External Bus Timing for Separate Bus

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Rev.	Date	Description	
		Page	Summary
		8	- Completed “under development” phase of part numbers R5F64110DFB, R5F64111DFB, R5F64112DFB, R5F64114DFB, R5F64115DFB, and R5F64116DFB in Table 1.7 - Added product information for 100-pin LGA and 80-/64-pin packages to Table 1.7
		9	- Added product information for 100-pin LGA and 80-/64-pin packages, and 32-Kbyte RAM to Figure 1.1 - Deleted hyphenation for part number in Figure 1.1
		11, 12, 14, 18, 21	Added Figures 1.3, 1.4, and 1.6 to 1.8 to provide block diagrams and pin assignment for 100-pin LGA and 80-/64-pin packages
		13	Changed the order of Notes in Figures 1.5
		15-17	Added pin No. for 100-pin LGA package to Tables 1.8 to 1.10
		19, 20, 22, 23	Added Tables 1.11 to 1.14 to provide pin characteristics for 80-/64-pin packages.
		24	Changed the following expression: “A ceramic resonator or a crystal oscillator” for “Main clock input/output” in Table 1.15, to “A crystal, or a ceramic resonator”
		25	Modified descriptions for $\overline{\text{HLDA}}$ and $\overline{\text{RDY}}$ of “Bus control pins” in Table 1.16
		26	- Changed the following expression: “selected” for “Input port” in Table 1.17, to “selectable” - Modified description “TXD2” for TXD0 to TXD8 of “Serial interface” in Table 1.17, to “TXD2 output”
		28-30	Added Tables 1.19 to 1.21 to provide pin definitions and functions for 80-/64-pin packages
		Chapter 2. CPU	
		—	Made major text modifications to this chapter
		33	Changed the following expression: “a requested interrupt’s priority level” in line 2 of 2.1.8.11, to “the interrupt request level”
		Chapter 3. Memory	
		35	- Made major text modifications to this chapter - Changed RAM size “40” in line 7 of this chapter, to “63”, and address “0000A3FFh” in line 8, to “0000FFFFh” - Added descriptions for 32-Kbyte RAM and 128-Kbyte ROM to Figure 3.1 - Changed two “can be”s in Notes 3 and 4 of Figure 3.1, to “becomes”s
		Chapter 4. SFRs	
		36	- Changed hexadecimal format of reset values for registers CCR and FMCR in Table 4.1, to binary - Added FEBC3 register to addresses 000010h-000011h in Table 4.1 - Changed FEBC register for addresses 00001Ch-00001Dh, to FEBC0 in Table 4.1 - Modified the following register name in Table 4.1: “Chip-select Boundary (between n and n + 1) Setting Register”, to “Chip-select n and n + 1 Boundary Setting Register”

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Rev.	Date	Description	
		Page	Summary
		37, 38	• Changed register names associated with “Start/Stop Condition” for BCNiIC in Tables 4.2 and 4.3, to “Start Condition/Stop Condition”
		45	• Modified reset values “XXXX XXXXb” and “XXXX 000Xb” for registers U7RB and U8RB in Table 4.10, to “XXXXh”
		46	• Changed expression of register name “Xi Register Yi Register” (i = 0 to 15) and register symbol “XiR, YiR” in Table 4.11, to “Xi Register/Yi Register” and “XiR/YiR”, respectively
		51	• Changed hexadecimal format of reset values for PDi in Table 4.16, to binary
		54	• Modified Note 1 in Table 4.19
		55	• Merged addresses 40090h to 40093h in Table 4.20, into previous page
		55-57	• Modified reset values for IFS0 and IFS2 in Table 4.20; Added Notes 1 to 3 for 80-/64-pin packages and IFS7 register
		59	• Modified the following register name in Tables 4.20 to 4.22: “Port Pi_j Port Function Select Register”, to “Port Pi_j Function Select Register” • Modified register name “DMAi Request Source Select Register 1” in Table 4.24, to “DMAi Request Source Select Register” • Changed register names “Wake-up Interrupt Priority Level Control Register 2” and “Wake-up Interrupt Priority Level Control Register 1” in Table 4.24, to “Wake-up IPL Setting Register 2” and “Wake-up IPL Setting Register 1”, respectively
		Chapter 5. Electrical Characteristics	
		60	• Added Notes 2 and 3 for 80-/64-pin packages to Table 5.1
		61	• Added specification of “dV_{CC1}/dt” to Table 5.2; Added Notes 2, 4, and 5 for 80-/64-pin packages
		62	• Added Note 2 for Table 5.3
		63	• Added Note 3 for 80-/64-pin packages to Table 5.4
		65	• Modified description “V_{CC}”s in Table 5.6, to “V_{CC1}”s and “V_{CC2}”s
		66	• Added Table 5.7 to provide RAM electrical characteristics • Deleted specification of “t_{PS}” from Table 5.8
		67	• Deleted measurement condition for power supply circuit timing characteristics in Table 5.9 • Added “Supply voltage for internal logic” to Figure 5.3 and deleted “CPU clock” from the figure • Changed voltage condition for Table 5.11, from “V_{CC1} = V_{CC2} = 3.3 to 5.5 V” to “V_{CC1} = V_{CC2} = 4.2 to 5.5 V”; Clarified maximum value for “ΔV_{det}” in Table 5.11; Modified self-consuming current “V_{CC}”, to “V_{CC1}”
		68	• Changed typical value and maximum value for f_{SO(PLL)} in Table 5.12, to “55” and “80” respectively • Changed the following expressions: “PLL frequency synthesizer stabilization time” in Table 5.12, to “PLL lock time” and “t_{OSC(PLL)}”, to “t_{LOCK(PLL)}” • Modified description for Note1 of Table 5.13