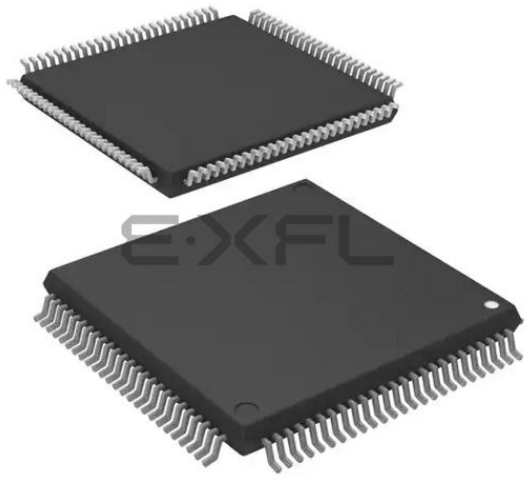
Renesas Electronics America Inc - R5F64112DFB#U0 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	R32C/100
Core Size	16/32-Bit
Speed	50MHz
Connectivity	EBI/EMI, I²C, IEBus, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	82
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	63K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f64112dfb-u0

Table 1.6 Pin Characteristics for the 100-pin Package (1/3)

Pin No.		Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
QFP	LGA								
1	A1		P9_4		TB4IN	CTS4/RTS4/SS4		DA1	
2	E4		P9_3		TB3IN			DA0	
3	B1	VDC0							
4	D3		P9_1						
5	C2	VDC1							
6	C1	NSD							
7	D2	CNVSS							
8	D1	XCIN	P8_7						
9	E3	XCOUT	P8_6						
10	E2	RESET							
11	E1	XOUT							
12	F3	VSS							
13	F2	XIN							
14	F1	VCC1							
15	G2		P8_5	NMI					
16	F5		P8_4	INT2					
17	G3		P8_3	INT1					
18	G1		P8_2	INT0					
19	F4		P8_1		TA4IN/U	CTS5/RTS5/SS5	IIO1_5/UD0B/UD1B		
20	H1		P8_0		TA4OUT/U	RXD5/SCL5/STXD5	UD0A/UD1A		
21	H2		P7_7		TA3IN	CLK5	IIO1_4/UD0B/UD1B		
22	G4		P7_6		TA3OUT	TXD5/SDA5/ SRXD5/CTS8/RTS8	IIO1_3/UD0A/UD1A		
23	H3		P7_5		TA2IN/W	RXD8	IIO1_2		
24	J1		P7_4		TA2OUT/W	CLK8	IIO1_1		
25	J2		P7_3		TA1IN/V	CTS2/RTS2/SS2/ TXD8	IIO1_0		
26	K1		P7_2		TA1OUT/V	CLK2			
27	K2		P7_1		TA0IN/ TB5IN	RXD2/SCL2/STXD2	IIO1_7/OUTC2_2/ ISRXD2/IEIN		
28	J3		P7_0		TA0OUT	TXD2/SDA2/SRXD2	IIO1_6/OUTC2_0/ ISTXD2/IEOUT		
29	H4		P6_7			TXD1/SDA1/SRXD1			
30	K3		P6_6			RXD1/SCL1/STXD1			
31	G5		P6_5			CLK1			
32	J4		P6_4			CTS1/RTS1/SS1	OUTC2_1/ISCLK2		
33	K4		P6_3			TXD0/SDA0/SRXD0			
34	H5		P6_2		TB2IN	RXD0/SCL0/STXD0			
35	J5		P6_1		TB1IN	CLK0			
36	K5		P6_0		TB0IN	CTS0/RTS0/SS0			
37	G6		P5_7			CTS7/RTS7			RDY/CS3
38	H6		P5_6			RXD7			ALE/CS2
39	J6		P5_5			CLK7			HOLD

Table 1.7 Pin Characteristics for the 100-pin Package (2/3)

Pin No.		Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
QFP	LGA								
40	K6		P5_4			TXD7			$\overline{HLDA}$/$\overline{CS1}$
41	H7		P5_3						CLKOUT/ BCLK
42	J7		P5_2						$\overline{RD}$
43	K7		P5_1						$\overline{WR1}$/$\overline{BC1}$
44	K8		P5_0						$\overline{WR0}$/$\overline{WR}$
45	G7		P4_7			TXD6/SDA6/SRXD6			$\overline{CS0}$/A23
46	J8		P4_6			RXD6/SCL6/STXD6			$\overline{CS1}$/A22
47	H8		P4_5			CLK6			$\overline{CS2}$/A21
48	G8		P4_4			$\overline{CTS6}$/$\overline{RTS6}$/$\overline{SS6}$			$\overline{CS3}$/A20
49	K9		P4_3			TXD3/SDA3/SRXD3	OUTC2_0/ISTXD2/ IEOUT		A19
50	K10		P4_2			RXD3/SCL3/STXD3	ISRXD2/IEIN		A18
51	J10		P4_1			CLK3			A17
52	J9		P4_0			$\overline{CTS3}$/$\overline{RTS3}$/$\overline{SS3}$			A16
53	H9		P3_7		TA4IN/$\overline{U}$				A15(/D15)
54	H10		P3_6		TA4OUT/U				A14(/D14)
55	F6		P3_5		TA2IN/$\overline{W}$				A13(/D13)
56	F7		P3_4		TA2OUT/W				A12(/D12)
57	G9		P3_3		TA1IN/$\overline{V}$				A11(/D11)
58	G10		P3_2		TA1OUT/V				A10(/D10)
59	F8		P3_1		TA3OUT		UD0B/UD1B		A9(/D9)
60	F9	VCC2							
61	F10		P3_0		TA0OUT		UD0A/UD1A		A8(/D8)
62	E8	VSS							
63	E9		P2_7					AN2_7	A7(/D7)
64	E10		P2_6					AN2_6	A6(/D6)
65	E7		P2_5					AN2_5	A5(/D5)
66	D7		P2_4					AN2_4	A4(/D4)
67	D8		P2_3					AN2_3	A3(/D3)
68	D10		P2_2					AN2_2	A2(/D2)
69	D9		P2_1					AN2_1	A1(/D1)
70	C10		P2_0					AN2_0	A0(/D0)/ $\overline{BC0}$(/D0)
71	C9		P1_7	$\overline{INT5}$			IIO0_7/IIO1_7		D15
72	E6		P1_6	$\overline{INT4}$			IIO0_6/IIO1_6		D14
73	B9		P1_5	$\overline{INT3}$			IIO0_5/IIO1_5		D13
74	B10		P1_4				IIO0_4/IIO1_4		D12
75	A10		P1_3				IIO0_3/IIO1_3		D11
76	A9		P1_2				IIO0_2/IIO1_2		D10
77	C8		P1_1				IIO0_1/IIO1_1		D9
78	C7		P1_0				IIO0_0/IIO1_0		D8
79	A8		P0_7					AN0_7	D7

Table 1.9 Pin Characteristics for the 64-pin Package (1/2)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Intelligent I/O Pin	Analog Pin
1	VDC1						
2	NSD						
3	CNVSS						
4	XCIN	P8_7					
5	XCOUT	P8_6					
6	$\overline{\text{RESET}}$						
7	XOUT						
8	VSS						
9	XIN						
10	VCC1						
11		P8_5	$\overline{\text{NMI}}$				
12		P8_4	$\overline{\text{INT2}}$				
13		P8_3	$\overline{\text{INT1}}$				
14		P8_2	$\overline{\text{INT0}}$				
15		P8_1		TA4IN/$\overline{\text{U}}$	$\overline{\text{CTS5}}$/$\overline{\text{RTS5}}$/$\overline{\text{SS5}}$	IIO1_5/UD0B/UD1B	
16		P8_0		TA4OUT/U	RXD5/SCL5/STXD5	UD0A/UD1A	
17		P7_7		TA3IN	CLK5	IIO1_4/UD0B/UD1B	
18		P7_6		TA3OUT	TXD5/SDA5/SRXD5/ $\overline{\text{CTS8}}$/$\overline{\text{RTS8}}$	IIO1_3/UD0A/UD1A	
19		P7_5		TA2IN/$\overline{\text{W}}$	RXD8	IIO1_2	
20		P7_4		TA2OUT/W	CLK8	IIO1_1	
21		P7_3		TA1IN/$\overline{\text{V}}$	$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$/$\overline{\text{SS2}}$/TXD8	IIO1_0	
22		P7_2		TA1OUT/V	CLK2		
23		P7_1		TA0IN/ TB5IN	RXD2/SCL2/STXD2	IIO1_7/OUTC2_2/ ISRXD2/IEIN	
24		P7_0		TA0OUT	TXD2/SDA2/SRXD2	IIO1_6/OUTC2_0/ ISTXD2/IEOUT	
25		P6_7			TXD1/SDA1/SRXD1		
26		P6_6			RXD1/SCL1/STXD1		
27		P6_5			CLK1		
28		P6_4			$\overline{\text{CTS1}}$/$\overline{\text{RTS1}}$/$\overline{\text{SS1}}$	OUTC2_1/ISCLK2	
29		P3_3		TA1IN/$\overline{\text{V}}$	$\overline{\text{CTS3}}$/$\overline{\text{RTS3}}$/$\overline{\text{SS3}}$		
30		P3_2		TA1OUT/V	TXD3/SDA3/SRXD3		
31		P3_1		TA3OUT	RXD3/SCL3/STXD3	UD0B/UD1B	
32		P3_0		TA0OUT	CLK3	UD0A/UD1A	
33		P6_3			TXD0/SDA0/SRXD0		
34		P6_2		TB2IN	RXD0/SCL0/STXD0		
35		P6_1		TB1IN	CLK0		
36		P6_0		TB0IN	$\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$/$\overline{\text{SS0}}$		
37		P2_7				IIO0_7	AN2_7
38		P2_6				IIO0_6	AN2_6
39		P2_5				IIO0_5	AN2_5
40		P2_4				IIO0_4	AN2_4

1.5 Pin Definitions and Functions

Tables 1.11 to 1.17 show the pin definitions and functions.

Table 1.11 Pin Definitions and Functions for the 100-pin Package (1/4)

Function	Symbol	I/O	Power Supply	Description
Power supply	VCC1, VCC2, VSS	I	—	Applicable as follows: VCC1 and VCC2 = 3.0 to 5.5 V (VCC1 ≥ VCC2), VSS = 0 V
Connecting pins for decoupling capacitor	VDC0, VDC1	—	—	A decoupling capacitor for internal voltage should be connected between VDC0 and VDC1
Analog power supply	AVCC, AVSS	I	VCC1	Power supply for the A/D converter. AVCC and AVSS should be connected to VCC1 and VSS, respectively
Reset input	$\overline{\text{RESET}}$	I	VCC1	The MCU is reset when this pin is driven low
CNVSS	CNVSS	I	VCC1	This pin should be connected to VSS via a resistor
Debug port	NSD	I/O	VCC1	This pin is to communicate with a debugger. It should be connected to VCC1 via a resistor of 1 to 4.7 kΩ
Main clock input	XIN	I	VCC1	Input/output for the main clock oscillator. A crystal, or a ceramic resonator should be connected between pins XIN and XOUT. An external clock should be input at the XIN while leaving the XOUT open
Main clock output	XOUT	O	VCC1	
Sub clock input	XCIN	I	VCC1	Input/output for the sub clock oscillator. A crystal oscillator should be connected between pins XCIN and XCOUT. An external clock should be input at the XCIN while leaving the XCOUT open
Sub clock output	XCOUT	O	VCC1	
BCLK output	BCLK	O	VCC2	BCLK output
Clock output	CLKOUT	O	VCC2	Output of the clock with the same frequency as low speed clocks, f8, or f32
External interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT5}}$	I	VCC1 VCC2	Input for external interrupts
NMI input	P8_5/$\overline{\text{NMI}}$	I	VCC1	Input for NMI
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	VCC1	Input for the key input interrupt
Bus control pins	D0 to D7	I/O	VCC2	Input/output of data (D0 to D7) while accessing an external memory space with a separate bus
	D8 to D15	I/O	VCC2	Input/output of data (D8 to D15) while accessing an external memory space with 16-bit separate bus
	A0 to A23	O	VCC2	Output of address bits A0 to A23

2.2 Fast Interrupt Registers

The following three registers are provided to minimize the overhead of the interrupt sequence.

2.2.1 Save Flag Register (SVF)

This 32-bit register is used to save the flag register when a fast interrupt occurs.

2.2.2 Save PC Register (SVP)

This 32-bit register is used to save the program counter when a fast interrupt occurs.

2.2.3 Vector Register (VCT)

This 32-bit register is used to indicate a jump address when a fast interrupt occurs.

2.3 DMAC-associated Registers

There are seven types of DMAC-associated registers.

2.3.1 DMA Mode Registers (DMD0, DMD1, DMD2, and DMD3)

These 32-bit registers are used to set DMA transfer mode, bit rate, etc.

2.3.2 DMA Terminal Count Registers (DCT0, DCT1, DCT2, and DCT3)

These 24-bit registers are used to set the number of DMA transfers.

2.3.3 DMA Terminal Count Reload Registers (DCR0, DCR1, DCR2, and DCR3)

These 24-bit registers are used to set the reloaded values for DMA terminal count registers.

2.3.4 DMA Source Address Registers (DSA0, DSA1, DSA2, and DSA3)

These 32-bit registers are used to set DMA source addresses.

2.3.5 DMA Source Address Reload Registers (DSR0, DSR1, DSR2, and DSR3)

These 32-bit registers are used to set the reloaded values for DMA source address registers.

2.3.6 DMA Destination Address Registers (DDA0, DDA1, DDA2, and DDA3)

These 32-bit registers are used to set DMA destination addresses.

2.3.7 DMA Destination Address Reload Registers (DDR0, DDR1, DDR2, and DDR3)

These 32-bit registers are used to set reloaded values for DMA destination address registers.

3. Memory

Figure 3.1 shows the memory map of the R32C/111 Group.
The R32C/111 Group provides a 4-Gbyte address space from 00000000h to FFFFFFFFh.

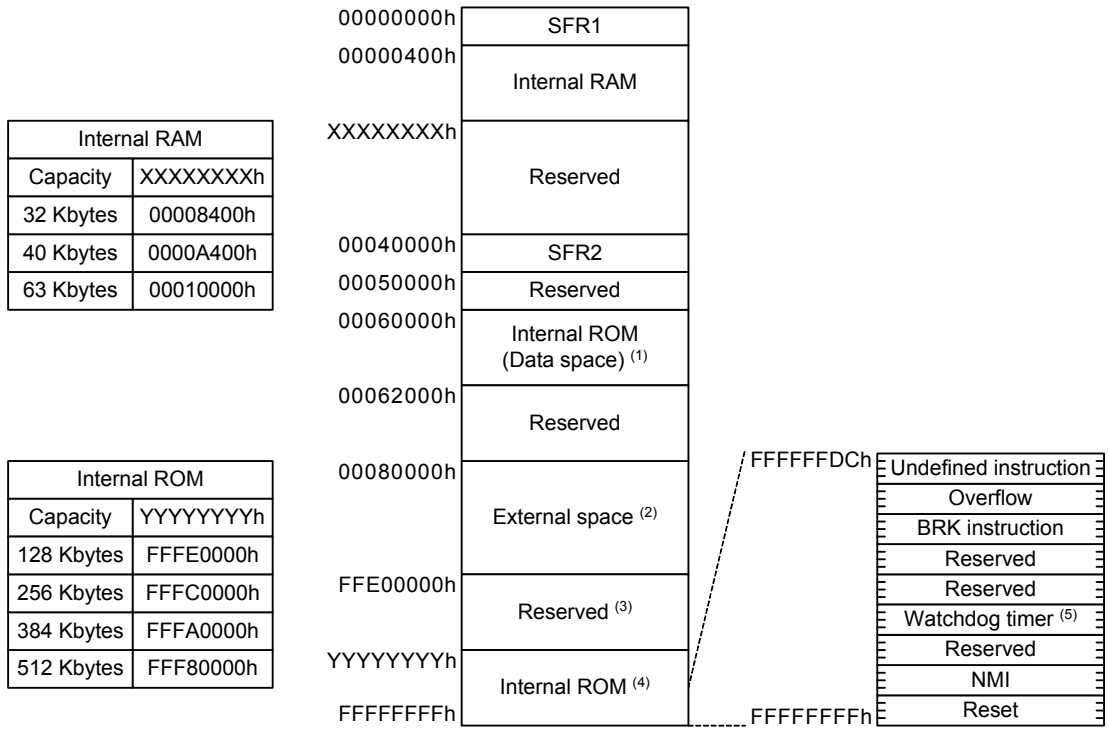
The internal ROM is mapped from address FFFFFFFFh in the inferior direction. For example, the 512-Kbyte internal ROM is mapped from FFF80000h to FFFFFFFFh.
The fixed interrupt vector table contains the start address of interrupt handlers and is mapped from FFFFFFDCh to FFFFFFFFh.
The internal RAM is mapped from address 00000400h in the superior direction. For example, the 63-Kbyte internal RAM is mapped from 00000400h to 0000FFFFh. Besides being used for data storage, the internal RAM functions as a stack(s) for subroutine calls and/or interrupt handlers.

Special function registers (SFRs), which are control registers for peripheral functions, are mapped from 00000000h to 000003FFh, and from 00040000h to 0004FFFFh. Unoccupied SFR locations are reserved, and no access is allowed.

In memory expansion mode or microprocessor mode, some spaces are reserved for internal use and should not be accessed.

Internal RAM	
Capacity	XXXXXXXXh
32 Kbytes	00008400h
40 Kbytes	0000A400h
63 Kbytes	00010000h

Internal ROM	
Capacity	YYYYYYYYh
128 Kbytes	FFFE0000h
256 Kbytes	FFFC0000h
384 Kbytes	FFFA0000h
512 Kbytes	FFF80000h



Notes:
1. The flash memory version provides two additional 4-Kbyte spaces (blocks A and B) for storing data.
2. This space can be used in memory expansion mode or microprocessor mode. Addresses from 02000000h to FDFFFFFFh are inaccessible.
3. This space is reserved in memory expansion mode. It becomes an external space in microprocessor mode.
4. This space can be used in single-chip mode or memory expansion mode. It becomes an external space in microprocessor mode.
5. The watchdog timer interrupt shares a vector with the oscillator stop detection interrupt and low voltage detection interrupt.

Figure 3.1 Memory Map

4. Special Function Registers (SFRs)

SFRs are memory-mapped peripheral registers that control the operation of peripherals. Tables 4.1 SFR List (1) to 4.24 SFR List (24) list the SFR details.

Table 4.1 SFR List (1)

Address	Register	Symbol	Reset Value
000000h			
000001h			
000002h			
000003h			
000004h	Clock Control Register	CCR	0001 1000b
000005h			
000006h	Flash Memory Control Register	FMCR	0000 0001b
000007h	Protect Release Register	PRR	00h
000008h			
000009h			
00000Ah			
00000Bh			
00000Ch			
00000Dh			
00000Eh			
00000Fh			
000010h	External Bus Control Register 3/Flash Memory Rewrite Bus Control Register 3	EBC3/FEBC3	0000h
000011h			
000012h	Chip Selects 2 and 3 Boundary Setting Register	CB23	00h
000013h			
000014h	External Bus Control Register 2	EBC2	0000h
000015h			
000016h	Chip Selects 1 and 2 Boundary Setting Register	CB12	00h
000017h			
000018h	External Bus Control Register 1	EBC1	0000h
000019h			
00001Ah	Chip Selects 0 and 1 Boundary Setting Register	CB01	00h
00001Bh			
00001Ch	External Bus Control Register 0/Flash Memory Rewrite Bus Control Register 0	EBC0/FEBC0	0000h
00001Dh			
00001Eh	Peripheral Bus Control Register	PBC	0504h
00001Fh			
000020h to 00005Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.4 SFR List (4)

Address	Register	Symbol	Reset Value
0000B0h	Intelligent I/O Interrupt Enable Register 0	IIO0IE	00h
0000B1h	Intelligent I/O Interrupt Enable Register 1	IIO1IE	00h
0000B2h	Intelligent I/O Interrupt Enable Register 2	IIO2IE	00h
0000B3h	Intelligent I/O Interrupt Enable Register 3	IIO3IE	00h
0000B4h	Intelligent I/O Interrupt Enable Register 4	IIO4IE	00h
0000B5h	Intelligent I/O Interrupt Enable Register 5	IIO5IE	00h
0000B6h	Intelligent I/O Interrupt Enable Register 6	IIO6IE	00h
0000B7h	Intelligent I/O Interrupt Enable Register 7	IIO7IE	00h
0000B8h	Intelligent I/O Interrupt Enable Register 8	IIO8IE	00h
0000B9h	Intelligent I/O Interrupt Enable Register 9	IIO9IE	00h
0000BAh	Intelligent I/O Interrupt Enable Register 10	IIO10IE	00h
0000BBh	Intelligent I/O Interrupt Enable Register 11	IIO11IE	00h
0000BCh			
0000BDh			
0000BEh			
0000BFh			
0000C0h			
0000C1h			
0000C2h			
0000C3h			
0000C4h			
0000C5h			
0000C6h			
0000C7h			
0000C8h			
0000C9h			
0000CAh			
0000CBh			
0000CCh			
0000CDh			
0000CEh			
0000CFh			
0000D0h			
0000D1h			
0000D2h			
0000D3h			
0000D4h			
0000D5h			
0000D6h			
0000D7h			
0000D8h			
0000D9h			
0000DAh			
0000DBh			
0000DCh			
0000DDh	UART7 Transmit Interrupt Control Register	S7TIC	XXXX X000b
0000DEh			
0000DFh	UART8 Transmit Interrupt Control Register	S8TIC	XXXX X000b

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.9 SFR List (9)

Address	Register	Symbol	Reset Value
0001A0h	Group 0 Base Timer Register	G0BT	XXXXh
0001A1h			
0001A2h	Group 0 Base Timer Control Register 0	G0BCR0	0000 0000b
0001A3h	Group 0 Base Timer Control Register 1	G0BCR1	0000 0000b
0001A4h	Group 0 Time Measurement Prescaler Register 6	G0TPR6	00h
0001A5h	Group 0 Time Measurement Prescaler Register 7	G0TPR7	00h
0001A6h	Group 0 Function Enable Register	G0FE	00h
0001A7h	Group 0 Function Select Register	G0FS	00h
0001A8h			
0001A9h			
0001AAh			
0001ABh			
0001ACh			
0001ADh			
0001AEh			
0001AFh			
0001B0h			
0001B1h			
0001B2h			
0001B3h			
0001B4h			
0001B5h			
0001B6h			
0001B7h			
0001B8h			
0001B9h			
0001BAh			
0001BBh			
0001BCh			
0001BDh			
0001BEh			
0001BFh			
0001C0h			
0001C1h			
0001C2h			
0001C3h			
0001C4h	UART5 Special Mode Register 4	U5SMR4	00h
0001C5h	UART5 Special Mode Register 3	U5SMR3	00h
0001C6h	UART5 Special Mode Register 2	U5SMR2	00h
0001C7h	UART5 Special Mode Register	U5SMR	00h
0001C8h	UART5 Transmit/Receive Mode Register	U5MR	00h
0001C9h	UART5 Bit Rate Register	U5BRG	XXh
0001CAh	UART5 Transmit Buffer Register	U5TB	XXXXh
0001CBh			
0001CCh	UART5 Transmit/Receive Control Register 0	U5C0	0000 1000b
0001CDh	UART5 Transmit/Receive Control Register 1	U5C1	0000 0010b
0001CEh	UART5 Receive Buffer Register	U5RB	XXXXh
0001CFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.15 SFR List (15)

Address	Register	Symbol	Reset Value
000380h	A/D0 Register 0	AD00	00XXh
000381h			
000382h	A/D0 Register 1	AD01	00XXh
000383h			
000384h	A/D0 Register 2	AD02	00XXh
000385h			
000386h	A/D0 Register 3	AD03	00XXh
000387h			
000388h	A/D0 Register 4	AD04	00XXh
000389h			
00038Ah	A/D0 Register 5	AD05	00XXh
00038Bh			
00038Ch	A/D0 Register 6	AD06	00XXh
00038Dh			
00038Eh	A/D0 Register 7	AD07	00XXh
00038Fh			
000390h			
000391h			
000392h	A/D0 Control Register 4	AD0CON4	XXXX 00XXb
000393h			
000394h	A/D0 Control Register 2	AD0CON2	XX0X X000b
000395h	A/D0 Control Register 3	AD0CON3	XXXX X000b
000396h	A/D0 Control Register 0	AD0CON0	00h
000397h	A/D0 Control Register 1	AD0CON1	00h
000398h	D/A Register 0	DA0	XXh
000399h			
00039Ah	D/A Register 1	DA1	XXh
00039Bh			
00039Ch	D/A Control Register	DACON	XXXX XX00b
00039Dh			
00039Eh			
00039Fh			
0003A0h			
0003A1h			
0003A2h			
0003A3h			
0003A4h			
0003A5h			
0003A6h			
0003A7h			
0003A8h			
0003A9h			
0003AAh			
0003ABh			
0003ACh			
0003ADh			
0003AEh			
0003AFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.16 SFR List (16)

Address	Register	Symbol	Reset Value
0003B0h			
0003B1h			
0003B2h			
0003B3h			
0003B4h			
0003B5h			
0003B6h			
0003B7h			
0003B8h			
0003B9h			
0003BAh			
0003BBh			
0003BCh			
0003BDh			
0003BEh			
0003BFh			
0003C0h	Port P0 Register	P0	XXh
0003C1h	Port P1 Register	P1	XXh
0003C2h	Port P0 Direction Register	PD0	0000 0000b
0003C3h	Port P1 Direction Register	PD1	0000 0000b
0003C4h	Port P2 Register	P2	XXh
0003C5h	Port P3 Register	P3	XXh
0003C6h	Port P2 Direction Register	PD2	0000 0000b
0003C7h	Port P3 Direction Register	PD3	0000 0000b
0003C8h	Port P4 Register	P4	XXh
0003C9h	Port P5 Register	P5	XXh
0003CAh	Port P4 Direction Register	PD4	0000 0000b
0003CBh	Port P5 Direction Register	PD5	0000 0000b
0003CCh	Port P6 Register	P6	XXh
0003CDh	Port P7 Register	P7	XXh
0003CEh	Port P6 Direction Register	PD6	0000 0000b
0003CFh	Port P7 Direction Register	PD7	0000 0000b
0003D0h	Port P8 Register	P8	XXh
0003D1h	Port P9 Register	P9	XXh
0003D2h	Port P8 Direction Register	PD8	00X0 0000b
0003D3h	Port P9 Direction Register	PD9	0000 0000b
0003D4h	Port P10 Register	P10	XXh
0003D5h			
0003D6h	Port P10 Direction Register	PD10	0000 0000b
0003D7h			
0003D8h			
0003D9h			
0003DAh			
0003DBh			
0003DCh			
0003DDh			
0003DEh			
0003DFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.22 SFR List (22)

Address	Register	Symbol	Reset Value
0400F0h	Port P10_0 Function Select Register	P10_0S	0XXX X000b
0400F1h			
0400F2h	Port P10_1 Function Select Register	P10_1S	0XXX X000b
0400F3h			
0400F4h	Port P10_2 Function Select Register	P10_2S	0XXX X000b
0400F5h			
0400F6h	Port P10_3 Function Select Register	P10_3S	0XXX X000b
0400F7h			
0400F8h	Port P10_4 Function Select Register	P10_4S	0XXX X000b
0400F9h			
0400FAh	Port P10_5 Function Select Register	P10_5S	0XXX X000b
0400FBh			
0400FCh	Port P10_6 Function Select Register	P10_6S	0XXX X000b
0400FDh			
0400FEh	Port P10_7 Function Select Register	P10_7S	0XXX X000b
0400FFh			
040100h			
040101h			
040102h			
040103h			
040104h			
040105h			
040106h			
040107h			
040108h			
040109h			
04010Ah			
04010Bh			
04010Ch			
04010Dh			
04010Eh			
04010Fh			
040110h			
040111h			
040112h			
040113h			
040114h			
040115h			
040116h			
040117h			
040118h			
040119h			
04011Ah			
04011Bh			
04011Ch			
04011Dh			
04011Eh			
04011Fh			

X: Undefined
Blanks are reserved. No access is allowed.

$V_{CC1} = V_{CC2} = 5\ V$

Table 5.16 Electrical Characteristics (2/3)
($V_{CC1} = V_{CC2} = 4.2$ to 5.5 V, $V_{SS} = 0$ V, $T_a = T_{opr}$, and $f_{(CPU)} = 50$ MHz, unless otherwise noted)

Symbol	Characteristic		Measurement Condition	Value			Unit
				Min.	Typ.	Max.	
$V_{T+} - V_{T-}$	Hysteresis	HOLD, RDY, NMI, INT0 to INT5, KI0 to KI3, TA0IN to TA4IN, TA0OUT to TA4OUT, TB0IN to TB5IN, CTS0 to CTS8, CLK0 to CLK8, RXD0 to RXD8, SCL0 to SCL6, SDA0 to SDA6, SS0 to SS6, SRXD0 to SRXD6, ADTRG, IIO0_0 to IIO0_7, IIO1_0 to IIO1_7, UD0A, UD0B, UD1A, UD1B, ISCLK2, ISRXD2, IEIN (1)		0.2		1.0	V
		RESET		0.2		1.8	V
I_{IH}	High level input current	XIN, RESET, CNVSS, NSD, P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_1, P9_3 to P9_7, P10_0 to P10_7 (2)	$V_I = 5$ V			5.0	µA
I_{IL}	Low level input current	XIN, RESET, CNVSS, NSD, P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_1, P9_3 to P9_7, P10_0 to P10_7 (2)	$V_I = 0$ V			-5.0	µA
R_{PULLUP}	Pull-up resistor	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_1, P9_3 to P9_7, P10_0 to P10_7 (2)	$V_I = 0$ V	30	50	170	kΩ
R_{fXIN}	Feedback resistor	XIN			1.5		MΩ
R_{fXCIN}	Feedback resistor	XCIN			15		MΩ

Notes:
1. Pins TB4IN, CTS4, CLK4, RXD4, SCL4, SDA4, SS4, SRXD4, and UART6, and UART7 are available in the 100-pin package only.
2. Ports P0_4 to P0_7, P1_0 to P1_4, P3_4 to P3_7, P4, P5, P9_1, and P9_4 to P9_7 are available in the 100-pin package only.

$V_{CC1} = V_{CC2} = 5\ V$

Table 5.19 D/A Conversion Characteristics ($V_{CC1} = V_{CC2} = AV_{CC} = V_{REF}$ = 4.2 to 5.5 V, $V_{SS} = AV_{SS}$ = 0 V, and $T_a = T_{opr}$, unless otherwise noted)

Symbol	Characteristic	Measurement Condition	Value			Unit
			Min.	Typ.	Max.	
—	Resolution				8	Bits
—	Absolute precision				1.0	%
t_S	Settling time				3	µs
R_O	Output resistance		4	10	20	kΩ
I_{VREF}	Reference input current	See Note 1			1.5	mA

Note:
1. One D/A converter is used. The DAi register (i = 0, 1) of the other unused converter is set to 00h. The resistor ladder for the A/D converter is not considered.
Even when the VCUT bit in the AD0CON1 register is set to 0 (V_{REF} disconnected), I_{VREF} is supplied.

$V_{CC1} = V_{CC2} = 5\ V$

Timing Requirements ($V_{CC1} = V_{CC2} = 4.2$ to 5.5 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.20 External Clock Input

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(X)}$	External clock input period	62.5	250	ns
$t_{w(XH)}$	External clock input high level pulse width	25		ns
$t_{w(XL)}$	External clock input low level pulse width	25		ns
$t_{r(X)}$	External clock input rise time		5	ns
$t_{f(X)}$	External clock input fall time		5	ns
t_w / t_c	External clock input duty	40	60	%

Table 5.21 External Bus Timing

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{su(D-R)}$	Data setup time before read	40		ns
$t_{h(R-D)}$	Data hold time after read	0		ns
$t_{dis(R-D)}$	Data disable time after read		$0.5 \times t_{c(Base)} + 10$	ns

$V_{CC1} = V_{CC2} = 3.3$ V

Table 5.42 D/A Conversion Characteristics ($V_{CC1} = V_{CC2} = AV_{CC} = V_{REF}$ = 3.0 to 3.6 V, $V_{SS} = AV_{SS}$ = 0 V, and $T_a = T_{opr}$, unless otherwise noted)

Symbol	Characteristic	Measurement Condition	Value			Unit
			Min.	Typ.	Max.	
—	Resolution				8	Bits
—	Absolute precision				1.0	%
t_S	Settling time				3	µs
R_O	Output resistance		4	10	20	kΩ
I_{VREF}	Reference input current	See Note 1			1.0	mA

Note:
1. One D/A converter is used. The DAi register (i = 0, 1) of the other unused converter is set to 00h. The resistor ladder for the A/D converter is not considered.
Even when the VCUT bit in the AD0CON1 register is set to 0 (V_{REF} disconnected), I_{VREF} is supplied.

V_{CC1} = V_{CC2} = 3.3 V

Timing Requirements (V_{CC1} = V_{CC2} = 3.0 to 3.6 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Table 5.50 Timer B Input (counting input in event counter mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input clock cycle time (one edge counting)	200		ns
$t_{w(TBH)}$	TBiIN input high level pulse width (one edge counting)	80		ns
$t_{w(TBL)}$	TBiIN input low level pulse width (one edge counting)	80		ns
$t_{c(TB)}$	TBiIN input clock cycle time (both edges counting)	200		ns
$t_{w(TBH)}$	TBiIN input high level pulse width (both edges counting)	80		ns
$t_{w(TBL)}$	TBiIN input low level pulse width (both edges counting)	80		ns

Table 5.51 Timer B Input (pulse period measure mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input clock cycle time	400		ns
$t_{w(TBH)}$	TBiIN input high level pulse width	180		ns
$t_{w(TBL)}$	TBiIN input low level pulse width	180		ns

Table 5.52 Timer B Input (pulse-width measure mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input clock cycle time	400		ns
$t_{w(TBH)}$	TBiIN input high level pulse width	180		ns
$t_{w(TBL)}$	TBiIN input low level pulse width	180		ns

V_{CC1} = V_{CC2} = 3.3 V

Switching Characteristics (V_{CC1} = V_{CC2} = 3.0 to 3.6 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Table 5.58 External Bus Timing (multiplexed bus)

Symbol	Characteristic	Measurement Condition	Value		Unit
			Min.	Max.	
$t_{su(S-ALE)}$	Chip-select setup time before ALE	Refer to Figure 5.6	(1)		ns
$t_{h(R-S)}$	Chip-select hold time after read		1.5 × $t_{c(Base)}$ - 10		ns
$t_{su(A-ALE)}$	Address setup time before ALE		(1)		ns
$t_{h(ALE-A)}$	Address hold time after ALE		0.5 × $t_{c(Base)}$ - 5		ns
$t_{h(R-A)}$	Address hold time after read		1.5 × $t_{c(Base)}$ - 10		ns
$t_{d(ALE-R)}$	ALE-read delay time		0.5 × $t_{c(Base)}$ - 5	0.5 × $t_{c(Base)}$ + 10	ns
$t_{w(ALE)}$	ALE pulse width		(1)		ns
$t_{dis(R-A)}$	Address disable time after read			8	ns
$t_{w(R)}$	Read pulse width		(1)		ns
$t_{h(W-S)}$	Chip-select hold time after write		1.5 × $t_{c(Base)}$ - 10		ns
$t_{h(W-A)}$	Address hold time after write		1.5 × $t_{c(Base)}$ - 10		ns
$t_{d(ALE-W)}$	ALE-write delay time		0.5 × $t_{c(Base)}$ - 5	0.5 × $t_{c(Base)}$ + 10	ns
$t_{w(W)}$	Write pulse width		(1)		ns
$t_{su(D-W)}$	Data setup time before write		(1)		ns
$t_{h(W-D)}$	Data hold time after write		0.5 × $t_{c(Base)}$		ns

Note:

1. The value is calculated using the formulas below based on the base clock cycles ($t_{c(Base)}$) and respective cycles of Tsu(A-R), Tw(R), Tsu(A-W), and Tw(W) set by registers EBC0 to EBC3. If the calculation results in a negative value, modify the value to be set. For details on how to set values, refer to the User's manual.

   $t_{su(S-ALE)}$ = $t_{su(A-ALE)}$ = $t_{w(ALE)}$ = (Tsu(A-R) - 0.5) × $t_{c(Base)}$ -15 [ns]

   $t_{w(R)}$ = Tw(R) × $t_{c(Base)}$ -10 [ns]

   $t_{w(W)}$ = $t_{su(D-W)}$ = Tw(W) × $t_{c(Base)}$ -10 [ns]

$V_{CC1} = V_{CC2} = 3.3$ V

Switching Characteristics ($V_{CC1} = V_{CC2} = 3.0$ to 3.6 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.59 Serial Interface

Symbol	Characteristic	Measurement Condition	Value		Unit
			Min.	Max.	
$t_{d(C-Q)}$	TXDi output delay time	Refer to Figure 5.6		80	ns
$t_{h(C-Q)}$	TXDi output hold time		0		ns

Table 5.60 Intelligent I/O

Symbol	Characteristic	Measurement Condition	Value		Unit
			Min.	Max.	
$t_{d(ISCLK2-TXD)}$	ISTXD2 output delay time	Refer to Figure 5.6		180	ns
$t_{h(ISCLK2-RXD)}$	ISTXD2 output hold time		0		ns

Rev.	Date	Description	
		Page	Summary
		37, 38	• Changed register names associated with “Start/Stop Condition” for BCNiIC in **Tables 4.2 and 4.3**, to “Start Condition/Stop Condition”
		45	• Modified reset values “XXXX XXXXb” and “XXXX 000Xb” for registers U7RB and U8RB in **Table 4.10**, to “XXXXh”
		46	• Changed expression of register name “Xi Register Yi Register” (i = 0 to 15) and register symbol “XiR, YiR” in **Table 4.11**, to “Xi Register/Yi Register” and “XiR/YiR”, respectively
		51	• Changed hexadecimal format of reset values for PDi in **Table 4.16**, to binary
		54	• Modified Note 1 in **Table 4.19**
		55	• Merged addresses 40090h to 40093h in **Table 4.20**, into previous page • Modified reset values for IFS0 and IFS2 in **Table 4.20**; Added Notes 1 to 3 for 80-/64-pin packages and IFS7 register
		55-57	• Modified the following register name in **Tables 4.20 to 4.22**: “Port Pi_j Port Function Select Register”, to “Port Pi_j Function Select Register”
		59	• Modified register name “DMAi Request Source Select Register 1” in **Table 4.24**, to “DMAi Request Source Select Register” • Changed register names “Wake-up Interrupt Priority Level Control Register 2” and “Wake-up Interrupt Priority Level Control Register 1” in **Table 4.24**, to “Wake-up IPL Setting Register 2” and “Wake-up IPL Setting Register 1”, respectively
			Chapter 5. Electrical Characteristics
		60	• Added Notes 2 and 3 for 80-/64-pin packages to **Table 5.1**
		61	• Added specification of “dV_{CC1}/dt” to **Table 5.2**; Added Notes 2, 4, and 5 for 80-/64-pin packages
		62	• Added Note 2 for **Table 5.3**
		63	• Added Note 3 for 80-/64-pin packages to **Table 5.4**
		65	• Modified description “V_{CC}”s in **Table 5.6**, to “V_{CC1}”s and “V_{CC2}”s
		66	• Added **Table 5.7** to provide RAM electrical characteristics • Deleted specification of “t_{PS}” from **Table 5.8**
		67	• Deleted measurement condition for power supply circuit timing characteristics in **Table 5.9** • Added “Supply voltage for internal logic” to **Figure 5.3** and deleted “CPU clock” from the figure • Changed voltage condition for **Table 5.11**, from “V_{CC1} = V_{CC2} = 3.3 to 5.5 V” to “V_{CC1} = V_{CC2} = 4.2 to 5.5 V”; Clarified maximum value for “ΔVdet” in **Table 5.11**; Modified self-consuming current “V_{CC}”, to “V_{CC1}”
		68	• Changed typical value and maximum value for $f_{SO(PLL)}$ in **Table 5.12**, to “55” and “80” respectively • Changed the following expressions: “PLL frequency synthesizer stabilization time” in **Table 5.12**, to “PLL lock time” and “$t_{OSC(PLL)}$”, to “$t_{LOCK(PLL)}$” • Modified description for Note1 of **Table 5.13**