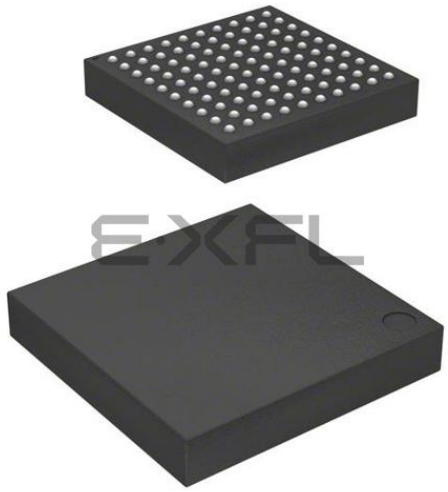

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	R32C/100
Core Size	16/32-Bit
Speed	50MHz
Connectivity	EBI/EMI, I²C, IEBus, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	82
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	63K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFLGA
Supplier Device Package	100-TFLGA (5.5x5.5)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f64112nlg-u0

1.1.2 Performance Overview

Tables 1.1 to 1.4 show the performance overview of the R32C/111 Group.

Table 1.1 Performance Overview for the 100-pin Package (1/2)

Unit	Function	Explanation
CPU	Central processing unit	R32C/100 Series CPU Core • Basic instructions: 108 • Minimum instruction execution time: 20 ns (f(CPU) = 50 MHz) • Multiplier: 32-bit × 32-bit → 64-bit • Multiply-accumulate unit: 32-bit × 32-bit + 64-bit → 64-bit • IEEE-754 compatible FPU: Single precision • 32-bit barrel shifter • Operating mode: Single-chip mode, memory expansion mode, microprocessor mode (optional (1))
Memory		Flash memory: 256 to 512 Kbytes RAM: 32 to 63 Kbytes Data flash: 4 Kbytes × 2 blocks Refer to Table 1.5 for memory size of each product group
Voltage Detector	Low voltage detector	Optional (1) Low voltage detection interrupt
Clock	Clock generator	• 4 circuits (main clock, sub clock, PLL, on-chip oscillator) • Oscillation stop detector: Main clock oscillator stop/restart detection • Frequency divide circuit: Divide-by-2 to divide-by-24 selectable • Low power modes: Wait mode, stop mode
External Bus Expansion	Bus and memory expansion	• Address space: 4 Gbytes (of which up to 64 Mbytes is user accessible) • External bus Interface: Support for wait-state insertion, 4 chip select outputs, 3V/5V interface • Bus format: Separate bus/Multiplexed bus selectable, data bus width selectable (8/16 bits)
Interrupts		Interrupt vectors: 261 External interrupt inputs: $\overline{\text{NMI}}$, $\overline{\text{INT}}$ × 6, key input × 4 Interrupt priority levels: 7
Watchdog Timer		15 bits × 1 (selectable input frequency from prescaler output)
DMA	DMAC	4 channels • Cycle-steal transfer mode • Request sources: 51 • 2 transfer modes: Single transfer, repeat transfer
	DMAC II	• Triggered by an interrupt request of any peripheral • 3 characteristic transfer functions: Immediate data transfer, calculation result transfer, chain transfer
I/O Ports	Programmable I/O ports	• 2 input-only ports • 82 CMOS I/O ports • 2 N-channel open drain ports • A pull-up resistor is selectable for every 4 input ports

Note:
1. Contact a Renesas Electronics sales office to use the optional features.

1.3 Block Diagram

Figures 1.2 and 1.3 show block diagram of the R32C/111 Group.

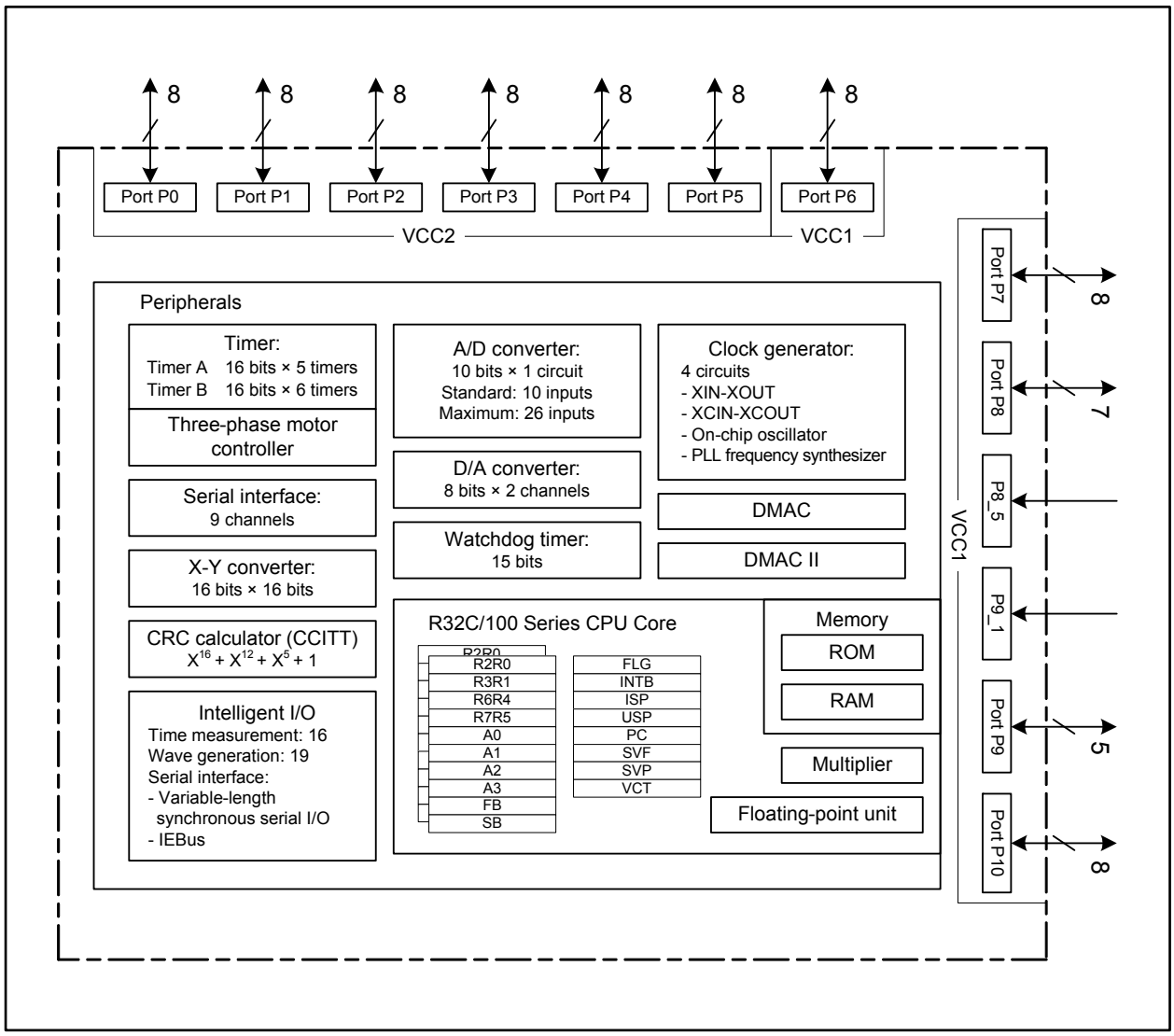


Figure 1.2 R32C/111 Group Block Diagram for the 100-pin Package

Table 1.12 Pin Definitions and Functions for the 100-pin Package (2/4)

Function	Symbol	I/O	Power Supply	Description
Bus control pins	A0/D0 to A7/D7	I/O	VCC2	Output of address bits (A0 to A7) and input/output of data (D0 to D7) by time-division while accessing an external memory space with multiplexed bus
	A8/D8 to A15/D15	I/O	VCC2	Output of address bits (A8 to A15) and input/output of data (D8 to D15) by time-division while accessing an external memory space with 16-bit multiplexed bus
	$\overline{BC0}$/D0	I/O	VCC2	Output of byte control ($\overline{BC0}$) and input/output of data (D0) by time-division while accessing an external memory space with multiplexed bus
	$\overline{CS0}$ to $\overline{CS3}$	O	VCC2	Chip select output
	$\overline{WR0}$/$\overline{WR1}$/$\overline{WR}$/ $\overline{BC0}$/$\overline{BC1}$/$\overline{RD}$	O	VCC2	Output of write, byte control, and read signals. Either $\overline{WRx}$ or $\overline{WR}$ and $\overline{BCx}$ can be selected by a program. Data is read when $\overline{RD}$ is low. • When $\overline{WR0}$, $\overline{WR1}$, and $\overline{RD}$ are selected, data is written to the following address: an even address, when $\overline{WR0}$ is low an odd address, when $\overline{WR1}$ is low on 16-bit external data bus • When $\overline{WR}$, $\overline{BC0}$, $\overline{BC1}$, and $\overline{RD}$ are selected, data is written, when $\overline{WR}$ is low and the following address is accessed: an even address, when $\overline{BC0}$ is low an odd address, when $\overline{BC1}$ is low on 16-bit external data bus
	ALE	O	VCC2	Latch enable signal in multiplexed bus format
	$\overline{HOLD}$	I	VCC2	The MCU is in a hold state while this pin is held low
	$\overline{HLDA}$	O	VCC2	This pin is driven low while the MCU is held in a hold state
	$\overline{RDY}$	I	VCC2	Bus cycle is extended by the CPU if this pin is low on the falling edge of BCLK

Table 1.16 Pin Definitions and Functions for the 64-pin Package (2/3)

Function	Symbol	I/O	Description
Serial interface	$\overline{CTS0}$ to $\overline{CTS3}$, $\overline{CTS5}$, $\overline{CTS8}$	I	Handshake input
	$\overline{RTS0}$ to $\overline{RTS3}$, $\overline{RTS5}$, $\overline{RTS8}$	O	Handshake output
	CLK0 to CLK3, CLK5, CLK8	I/O	Transmit/receive clock input/output
	RXD0 to RXD3, RXD5, RXD8	I	Serial data input
	TXD0 to TXD3, TXD5, TXD8	O	Serial data output. TXD2 output is N-channel open drain
I^2C-bus (simplified)	SDA0 to SDA3, SDA5	I/O	Serial data input/output. SDA2 output is N-channel open drain
	SCL0 to SCL3, SCL5	I/O	Transmit/receive clock input/output. SCL2 output is N-channel open drain
Serial interface special functions	STXD0 to STXD3, STXD5	O	Serial data output in slave mode. STXD2 is N-channel open drain
	SRXD0 to SRXD3, SRXD5	I	Serial data input in slave mode
	$\overline{SS0}$ to $\overline{SS3}$, $\overline{SS5}$	I	Input to control serial interface special functions
A/D converter	AN_0 to AN_7, AN0_0 to AN0_3, AN2_0 to AN2_7	I	Analog input for the A/D converter
	$\overline{ADTRG}$	I	External trigger input for the A/D converter
D/A converter	DA0	O	Output for the D/A converter
Reference voltage input	VREF	I	Reference voltage input for the A/D converter and D/A converter

2. Central Processing Unit (CPU)

The CPU contains the registers shown below. There are two register banks each consisting of registers R2R0, R3R1, R6R4, R7R5, A0 to A3, SB, and FB.

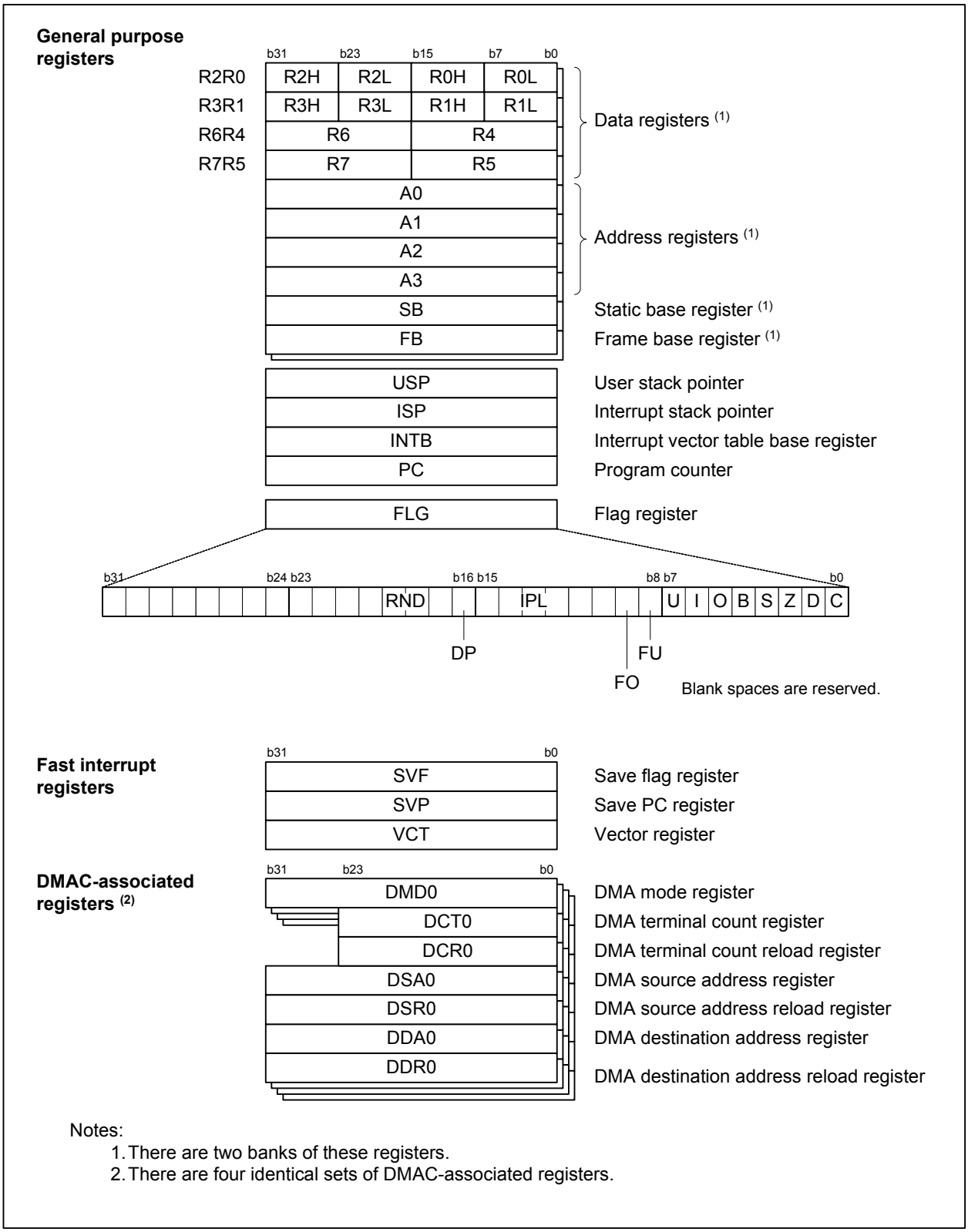


Figure 2.1 CPU Registers

2.1 General Purpose Registers

2.1.1 Data Registers (R2R0, R3R1, R6R4, and R7R5)

These 32-bit registers are primarily used for transfers and arithmetic/logic operations.
Each of the registers can be divided into upper and lower 16-bit registers, e.g. R2R0 can be divided into R2 and R0, R3R1 can be divided into R3 and R1, etc.
Moreover, data registers R2R0 and R3R1 can be divided into four 8-bit data registers: upper (R2H and R3H), mid-upper (R2L and R3L), mid-lower (R0H and R1H), and lower (R0L and R1L).

2.1.2 Address Registers (A0, A1, A2, and A3)

These 32-bit registers have functions similar to data registers. They are also used for address register indirect addressing and address register relative addressing.

2.1.3 Static Base Register (SB)

This 32-bit register is used for SB relative addressing.

2.1.4 Frame Base Register (FB)

This 32-bit register is used for FB relative addressing.

2.1.5 Program Counter (PC)

This 32-bit counter indicates the address of the instruction to be executed next.

2.1.6 Interrupt Vector Table Base Register (INTB)

This 32-bit register indicates the start address of a relocatable vector table.

2.1.7 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

Two types of 32-bit stack pointers (SPs) are provided: user stack pointer (USP) and interrupt stack pointer (ISP).
Use the stack pointer select flag (U flag) to select either the user stack pointer (USP) or the interrupt stack pointer (ISP). The U flag is bit 7 in the flag register (FLG). Refer to 2.1.8 “Flag Register (FLG)” for details.
To minimize the overhead of interrupt sequence due to less memory access, set the user stack pointer (USP) or the interrupt stack pointer (ISP) to a multiple of 4.

2.1.8 Flag Register (FLG)

This 32-bit register indicates the CPU status.

2.1.8.1 Carry Flag (C flag)

This flag retains a carry, borrow, or shifted-out bit generated by the arithmetic logic unit (ALU).

2.1.8.2 Debug Flag (D flag)

This flag is only for debugging. Only set this bit to 0.

2.1.8.3 Zero Flag (Z flag)

This flag becomes 1 when the result of an operation is 0; otherwise it is 0.

2.1.8.4 Sign Flag (S flag)

This flag becomes 1 when the result of an operation is a negative value; otherwise it is 0.

2.1.8.5 Register Bank Select Flag (B flag)

This flag selects a register bank. It indicates 0 when register bank 0 is selected, and 1 when register bank 1 is selected.

2.1.8.6 Overflow Flag (O flag)

This flag becomes 1 when the result of an operation overflows; otherwise it is 0.

2.1.8.7 Interrupt Enable Flag (I flag)

This flag enables maskable interrupts. To disable maskable interrupts, set this flag to 0. To enable them, set this flag to 1. When an interrupt is accepted, the flag becomes 0.

2.1.8.8 Stack Pointer Select Flag (U flag)

To select the interrupt stack pointer (ISP), set this flag to 0. To select the user stack pointer (USP), set this flag to 1.
It becomes 0 when a hardware interrupt is accepted or when an INT instruction designated by a software interrupt number from 0 to 127 is executed.

2.1.8.9 Floating-point Underflow Flag (FU flag)

This flag becomes 1 when an underflow occurs in a floating-point operation; otherwise it is 0. It also becomes 1 when the operand contains invalid numbers (subnormal numbers).

2.1.8.10 Floating-point Overflow Flag (FO flag)

This flag becomes 1 when an overflow occurs in a floating-point operation; otherwise it is 0. It also becomes 1 when the operand contains invalid numbers (subnormal numbers).

2.1.8.11 Processor Interrupt Priority Level (IPL)

The processor interrupt priority level (IPL), consisting of 3 bits, selects a processor interrupt priority level from level 0 to 7. An interrupt is enabled when the interrupt request level is higher than the selected IPL.
When the processor interrupt priority level (IPL) is set to 111b (level 7), all interrupts are disabled.

2.1.8.12 Fixed-point Radix Point Designation Bit (DP bit)

This bit designates the radix point. It also specifies which portion of the fixed-point multiplication result to extract. It is used for the MULX instruction.

2.1.8.13 Floating-point Rounding Mode (RND)

The 2-bit floating-point rounding mode selects a rounding mode for floating-point calculation results.

2.1.8.14 Reserved

Only set this bit to 0. The read value is undefined.

Table 4.14 SFR List (14)

Address	Register	Symbol	Reset Value
000350h	Timer B0 Register	TB0	XXXXh
000351h			
000352h	Timer B1 Register	TB1	XXXXh
000353h			
000354h	Timer B2 Register	TB2	XXXXh
000355h			
000356h	Timer A0 Mode Register	TA0MR	0000 0000b
000357h	Timer A1 Mode Register	TA1MR	0000 0000b
000358h	Timer A2 Mode Register	TA2MR	0000 0000b
000359h	Timer A3 Mode Register	TA3MR	0000 0000b
00035Ah	Timer A4 Mode Register	TA4MR	0000 0000b
00035Bh	Timer B0 Mode Register	TB0MR	00XX 0000b
00035Ch	Timer B1 Mode Register	TB1MR	00XX 0000b
00035Dh	Timer B2 Mode Register	TB2MR	00XX 0000b
00035Eh	Timer B2 Special Mode Register	TB2SC	XXXX XXX0b
00035Fh	Count Source Prescaler Register	TCSPR	0000 0000b
000360h			
000361h			
000362h			
000363h			
000364h	UART0 Special Mode Register 4	U0SMR4	00h
000365h	UART0 Special Mode Register 3	U0SMR3	00h
000366h	UART0 Special Mode Register 2	U0SMR2	00h
000367h	UART0 Special Mode Register	U0SMR	00h
000368h	UART0 Transmit/Receive Mode Register	U0MR	00h
000369h	UART0 Bit Rate Register	U0BRG	XXh
00036Ah	UART0 Transmit Buffer Register	U0TB	XXXXh
00036Bh			
00036Ch	UART0 Transmit/Receive Control Register 0	U0C0	0000 1000b
00036Dh	UART0 Transmit/Receive Control Register 1	U0C1	0000 0010b
00036Eh	UART0 Receive Buffer Register	U0RB	XXXXh
00036Fh			
000370h			
000371h			
000372h			
000373h			
000374h			
000375h			
000376h			
000377h			
000378h			
000379h			
00037Ah			
00037Bh			
00037Ch	CRC Data Register	CRCD	XXXXh
00037Dh			
00037Eh	CRC Input Register	CRCIN	XXh
00037Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.17 SFR List (17)

Address	Register	Symbol	Reset Value
0003E0h			
0003E1h			
0003E2h			
0003E3h			
0003E4h			
0003E5h			
0003E6h			
0003E7h			
0003E8h			
0003E9h			
0003EAh			
0003EBh			
0003ECh			
0003EDh			
0003EEh			
0003EFh			
0003F0h	Pull-up Control Register 0	PUR0	0000 0000b
0003F1h	Pull-up Control Register 1	PUR1	XXXX 0000b
0003F2h	Pull-up Control Register 2	PUR2	0000 0000b
0003F3h	Pull-up Control Register 3	PUR3	XXXX XX00b
0003F4h			
0003F5h			
0003F6h			
0003F7h			
0003F8h			
0003F9h			
0003FAh			
0003FBh			
0003FCh			
0003FDh			
0003FEh			
0003FFh	Port Control Register	PCR	XXXX XXX0b

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.20 SFR List (20)

Address	Register	Symbol	Reset Value
040094h			
040095h			
040096h			
040097h	Three-phase Output Buffer Control Register	IOBC	0XXX XXXXb
040098h	Input Function Select Register 0	IFS0	X000 0000b (1)
040099h			
04009Ah	Input Function Select Register 2	IFS2	0000 00X0b (2)
04009Bh	Input Function Select Register 3	IFS3	XXXX XX00b
04009Ch			
04009Dh			
04009Eh			
04009Fh	Input Function Select Register 7 (3)	IFS7	XXXX XX0Xb
0400A0h	Port P0_0 Function Select Register	P0_0S	0XXX X000b
0400A1h	Port P1_0 Function Select Register	P1_0S	XXXX X000b
0400A2h	Port P0_1 Function Select Register	P0_1S	0XXX X000b
0400A3h	Port P1_1 Function Select Register	P1_1S	XXXX X000b
0400A4h	Port P0_2 Function Select Register	P0_2S	0XXX X000b
0400A5h	Port P1_2 Function Select Register	P1_2S	XXXX X000b
0400A6h	Port P0_3 Function Select Register	P0_3S	0XXX X000b
0400A7h	Port P1_3 Function Select Register	P1_3S	XXXX X000b
0400A8h	Port P0_4 Function Select Register	P0_4S	0XXX X000b
0400A9h	Port P1_4 Function Select Register	P1_4S	XXXX X000b
0400AAh	Port P0_5 Function Select Register	P0_5S	0XXX X000b
0400ABh	Port P1_5 Function Select Register	P1_5S	XXXX X000b
0400ACh	Port P0_6 Function Select Register	P0_6S	0XXX X000b
0400ADh	Port P1_6 Function Select Register	P1_6S	XXXX X000b
0400AEh	Port P0_7 Function Select Register	P0_7S	0XXX X000b
0400AFh	Port P1_7 Function Select Register	P1_7S	XXXX X000b
0400B0h	Port P2_0 Function Select Register	P2_0S	0XXX X000b
0400B1h	Port P3_0 Function Select Register	P3_0S	XXXX X000b
0400B2h	Port P2_1 Function Select Register	P2_1S	0XXX X000b
0400B3h	Port P3_1 Function Select Register	P3_1S	XXXX X000b
0400B4h	Port P2_2 Function Select Register	P2_2S	0XXX X000b
0400B5h	Port P3_2 Function Select Register	P3_2S	XXXX X000b
0400B6h	Port P2_3 Function Select Register	P2_3S	0XXX X000b
0400B7h	Port P3_3 Function Select Register	P3_3S	XXXX X000b
0400B8h	Port P2_4 Function Select Register	P2_4S	0XXX X000b
0400B9h	Port P3_4 Function Select Register	P3_4S	XXXX X000b
0400BAh	Port P2_5 Function Select Register	P2_5S	0XXX X000b
0400BBh	Port P3_5 Function Select Register	P3_5S	XXXX X000b
0400BCh	Port P2_6 Function Select Register	P2_6S	0XXX X000b
0400BDh	Port P3_6 Function Select Register	P3_6S	XXXX X000b
0400BEh	Port P2_7 Function Select Register	P2_7S	0XXX X000b
0400BFh	Port P3_7 Function Select Register	P3_7S	XXXX X000b

X: Undefined
Blanks are reserved. No access is allowed.

Notes:
1. The reset value is 0000 0000b in the 64-pin package.
2. The reset value is 0000 000Xb in the 64-pin package.
3. This register is provided for the 64-pin package only. No access is allowed in the 100-pin package.

Table 5.3 Operating Conditions (2/5)
(V_{CC1} = V_{CC2} = 3.0 to 5.5 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted) (1)

Symbol	Characteristic		Value (2)			Unit
			Min.	Typ.	Max.	
C_{VDC}	Decoupling capacitance for voltage regulator	Inter-pin voltage: 1.5 V	2.4		10.0	µF

Notes:
1. The device is operationally guaranteed under these operating conditions.
2. This value should be met with due consideration to the following conditions: operating temperature, DC bias, aging, etc.

Table 5.6 Operating Conditions (5/5)

(V_{CC1} = V_{CC2} = 3.0 to 5.5 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted) (1)

Symbol	Characteristic		Value			Unit
			Min.	Typ.	Max.	
$V_{r(VCC1)}$	Allowable ripple voltage	V_{CC1} = 5.0 V			0.5	Vp-p
		V_{CC1} = 3.0 V			0.3	Vp-p
$V_{r(VCC2)}$	Allowable ripple voltage	V_{CC2} = 5.0 V			0.5	Vp-p
		V_{CC2} = 3.0 V			0.3	Vp-p
$dV_{r(VCC1)}/dt$	Ripple voltage gradient	V_{CC1} = 5.0 V			±0.3	V/ms
		V_{CC1} = 3.0 V			±0.3	V/ms
$dV_{r(VCC2)}/dt$	Ripple voltage gradient	V_{CC2} = 5.0 V			±0.3	V/ms
		V_{CC2} = 3.0 V			±0.3	V/ms
$f_{r(VCC1)}$	Allowable ripple frequency				10	kHz
$f_{r(VCC2)}$	Allowable ripple frequency				10	kHz

Note:
1. The device is operationally guaranteed under these operating conditions.

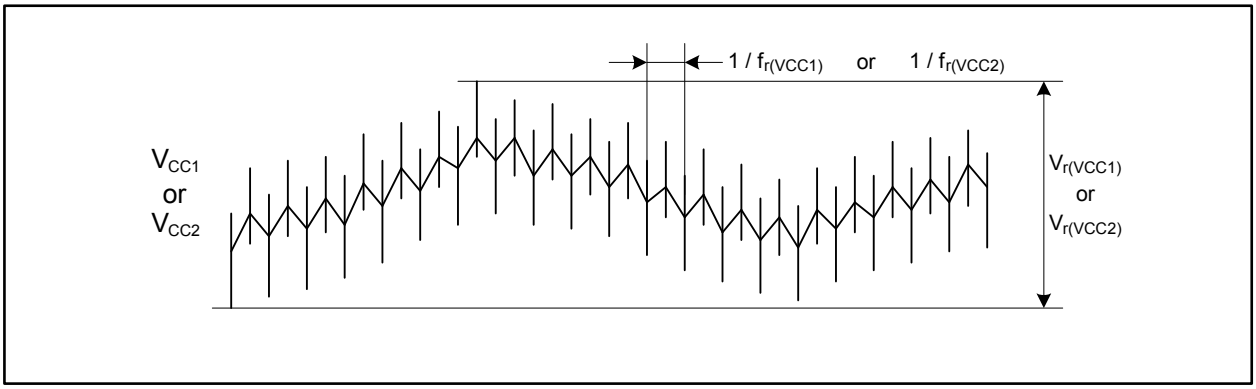


Figure 5.2 Ripple Waveform

$V_{CC1} = V_{CC2} = 5\ V$

Table 5.15 Electrical Characteristics (1/3)
($V_{CC1} = V_{CC2} = 4.2$ to 5.5 V, $V_{SS} = 0$ V, $T_a = T_{opr}$, and $f_{(CPU)} = 50$ MHz, unless otherwise noted)

Symbol	Characteristic		Measurement Condition	Value (2)			Unit
				Min.	Typ.	Max.	
V_{OH}	High level output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7 (1)	I_{OH} = -5 mA	V_{CC2} -2.0		V_{CC2}	V
		P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_3 to P9_7, P10_0 to P10_7 (1)	I_{OH} = -5 mA	V_{CC1} -2.0		V_{CC1}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7 (1)	I_{OH} = -200 µA	V_{CC2} -0.3		V_{CC2}	V
		P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_3 to P9_7, P10_0 to P10_7 (1)	I_{OH} = -200 µA	V_{CC1} -0.3		V_{CC1}	V
V_{OL}	Low level output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_3 to P9_7, P10_0 to P10_7 (1)	I_{OL} = 5 mA			2.0	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_3 to P9_7, P10_0 to P10_7 (1)	I_{OL} = 200 µA			0.45	V

Notes:
1. Ports P0_4 to P0_7, P1_0 to P1_4, P3_4 to P3_7, P4, P5, and P9_4 to P9_7 are available in the 100-pin package only.
2. The V_{CC2} pin is available in the 100-pin package only. It should be considered as V_{CC1} in the 64-pin package.

$V_{CC1} = V_{CC2} = 5\ V$

Switching Characteristics ($V_{CC1} = V_{CC2}$ = 4.2 to 5.5 V, V_{SS} = 0 V, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.35 External Bus Timing (multiplexed bus)

Symbol	Characteristic	Measurement Condition	Value		Unit
			Min.	Max.	
$t_{su(S-ALE)}$	Chip-select setup time before ALE	Refer to Figure 5.6	(1)		ns
$t_{h(R-S)}$	Chip-select hold time after read		$1.5 \times t_{c(Base)} - 10$		ns
$t_{su(A-ALE)}$	Address setup time before ALE		(1)		ns
$t_{h(ALE-A)}$	Address hold time after ALE		$0.5 \times t_{c(Base)} - 5$		ns
$t_{h(R-A)}$	Address hold time after read		$1.5 \times t_{c(Base)} - 10$		ns
$t_{d(ALE-R)}$	ALE-read delay time		$0.5 \times t_{c(Base)} - 5$	$0.5 \times t_{c(Base)} + 10$	ns
$t_{w(ALE)}$	ALE pulse width		(1)		ns
$t_{dis(R-A)}$	Address disable time after read			8	ns
$t_{w(R)}$	Read pulse width		(1)		ns
$t_{h(W-S)}$	Chip-select hold time after write		$1.5 \times t_{c(Base)} - 10$		ns
$t_{h(W-A)}$	Address hold time after write		$1.5 \times t_{c(Base)} - 10$		ns
$t_{d(ALE-W)}$	ALE-write delay time		$0.5 \times t_{c(Base)} - 5$	$0.5 \times t_{c(Base)} + 10$	ns
$t_{w(W)}$	Write pulse width		(1)		ns
$t_{su(D-W)}$	Data setup time before write		(1)		ns
$t_{h(W-D)}$	Data hold time after write		$0.5 \times t_{c(Base)}$		ns

Note:

1. The value is calculated using the formulas below based on the base clock cycles ($t_{c(Base)}$) and respective cycles of Tsu(A-R), Tw(R), Tsu(A-W), and Tw(W) set by registers EBC0 to EBC3. If the calculation results in a negative value, modify the value to be set. For details on how to set values, refer to the User's manual.

   $t_{su(S-ALE)} = t_{su(A-ALE)} = t_{w(ALE)} = (Tsu(A-R) - 0.5) \times t_{c(Base)} - 15$ [ns]

   $t_{w(R)} = Tw(R) \times t_{c(Base)} - 10$ [ns]

   $t_{w(W)} = t_{su(D-W)} = Tw(W) \times t_{c(Base)} - 10$ [ns]

$V_{CC1} = V_{CC2} = 3.3$ V

Table 5.38 Electrical Characteristics (1/3) ($V_{CC1} = V_{CC2} = 3.0$ to 3.6 V, $V_{SS} = 0$ V, $T_a = T_{opr}$, and $f_{(CPU)} = 50$ MHz, unless otherwise noted)

Symbol	Characteristic		Measurement Condition	Value (2)			Unit
				Min.	Typ.	Max.	
V_{OH}	High level output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7 (1)	I_{OH} = -1 mA	V_{CC2} - 0.6		V_{CC2}	V
		P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_3 to P9_7, P10_0 to P10_7 (1)	I_{OH} = -1 mA	V_{CC1} - 0.6		V_{CC1}	V
V_{OL}	Low level output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_3 to P9_7, P10_0 to P10_7 (1)	I_{OL} = 1 mA			0.5	V

Notes:
1. Ports P0_4 to P0_7, P1_0 to P1_4, P3_4 to P3_7, P4, P5, and P9_4 to P9_7 are available in the 100-pin package only.
2. The V_{CC2} pin is available in the 100-pin package only. It should be considered as V_{CC1} in the 64-pin package.

V_{CC1} = V_{CC2} = 3.3 V

Switching Characteristics (V_{CC1} = V_{CC2} = 3.0 to 3.6 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Table 5.57 External Bus Timing (separate bus)

Symbol	Characteristic	Measurement Condition	Value		Unit
			Min.	Max.	
$t_{su(S-R)}$	Chip-select setup time before read	Refer to Figure 5.6	(1)		ns
$t_{h(R-S)}$	Chip-select hold time after read		$t_{c(Base)}$ - 10		ns
$t_{su(A-R)}$	Address setup time before read		(1)		ns
$t_{h(R-A)}$	Address hold time after read		$t_{c(Base)}$ - 10		ns
$t_{w(R)}$	Read pulse width		(1)		ns
$t_{su(S-W)}$	Chip-select setup time before write		(1)		ns
$t_{h(W-S)}$	Chip-select hold time after write		1.5 × $t_{c(Base)}$ - 10		ns
$t_{su(A-W)}$	Address setup time before write		(1)		ns
$t_{h(W-A)}$	Address hold time after write		1.5 × $t_{c(Base)}$ - 10		ns
$t_{w(W)}$	Write pulse width		(1)		ns
$t_{su(D-W)}$	Data setup time before write		(1)		ns
$t_{h(W-D)}$	Data hold time after write		0		ns

Note:

1. The value is calculated using the formulas below based on the base clock cycles ($t_{c(Base)}$) and respective cycles of Tsu(A-R), Tw(R), Tsu(A-W), and Tw(W) set by registers EBC0 to EBC3. If the calculation results in a negative value, modify the value to be set. For details on how to set values, refer to the User's manual.

   $t_{su(S-R)}$ = $t_{su(A-R)}$ = Tsu(A-R) × $t_{c(Base)}$ - 15 [ns]

   $t_{w(R)}$ = Tw(R) × $t_{c(Base)}$ - 10 [ns]

   $t_{su(S-W)}$ = $t_{su(A-W)}$ = Tsu(A-W) × $t_{c(Base)}$ - 15 [ns]

   $t_{w(W)}$ = $t_{su(D-W)}$ = Tw(W) × $t_{c(Base)}$ - 10 [ns]

V_{CC1} = V_{CC2} = 3.3 V

Switching Characteristics (V_{CC1} = V_{CC2} = 3.0 to 3.6 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Table 5.58 External Bus Timing (multiplexed bus)

Symbol	Characteristic	Measurement Condition	Value		Unit
			Min.	Max.	
$t_{su(S-ALE)}$	Chip-select setup time before ALE	Refer to Figure 5.6	(1)		ns
$t_{h(R-S)}$	Chip-select hold time after read		1.5 × $t_{c(Base)}$ - 10		ns
$t_{su(A-ALE)}$	Address setup time before ALE		(1)		ns
$t_{h(ALE-A)}$	Address hold time after ALE		0.5 × $t_{c(Base)}$ - 5		ns
$t_{h(R-A)}$	Address hold time after read		1.5 × $t_{c(Base)}$ - 10		ns
$t_{d(ALE-R)}$	ALE-read delay time		0.5 × $t_{c(Base)}$ - 5	0.5 × $t_{c(Base)}$ + 10	ns
$t_{w(ALE)}$	ALE pulse width		(1)		ns
$t_{dis(R-A)}$	Address disable time after read			8	ns
$t_{w(R)}$	Read pulse width		(1)		ns
$t_{h(W-S)}$	Chip-select hold time after write		1.5 × $t_{c(Base)}$ - 10		ns
$t_{h(W-A)}$	Address hold time after write		1.5 × $t_{c(Base)}$ - 10		ns
$t_{d(ALE-W)}$	ALE-write delay time		0.5 × $t_{c(Base)}$ - 5	0.5 × $t_{c(Base)}$ + 10	ns
$t_{w(W)}$	Write pulse width		(1)		ns
$t_{su(D-W)}$	Data setup time before write		(1)		ns
$t_{h(W-D)}$	Data hold time after write		0.5 × $t_{c(Base)}$		ns

Note:

1. The value is calculated using the formulas below based on the base clock cycles ($t_{c(Base)}$) and respective cycles of Tsu(A-R), Tw(R), Tsu(A-W), and Tw(W) set by registers EBC0 to EBC3. If the calculation results in a negative value, modify the value to be set. For details on how to set values, refer to the User's manual.

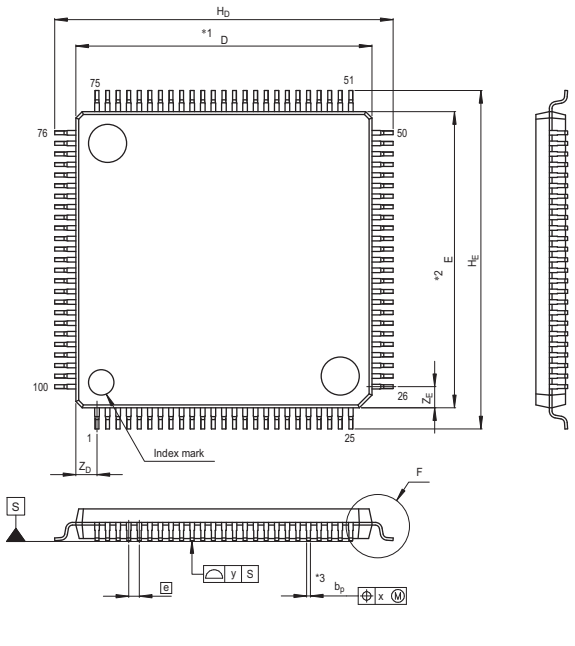
   $t_{su(S-ALE)}$ = $t_{su(A-ALE)}$ = $t_{w(ALE)}$ = (Tsu(A-R) - 0.5) × $t_{c(Base)}$ -15 [ns]

   $t_{w(R)}$ = Tw(R) × $t_{c(Base)}$ -10 [ns]

   $t_{w(W)}$ = $t_{su(D-W)}$ = Tw(W) × $t_{c(Base)}$ -10 [ns]

Appendix 1. Package Dimensions

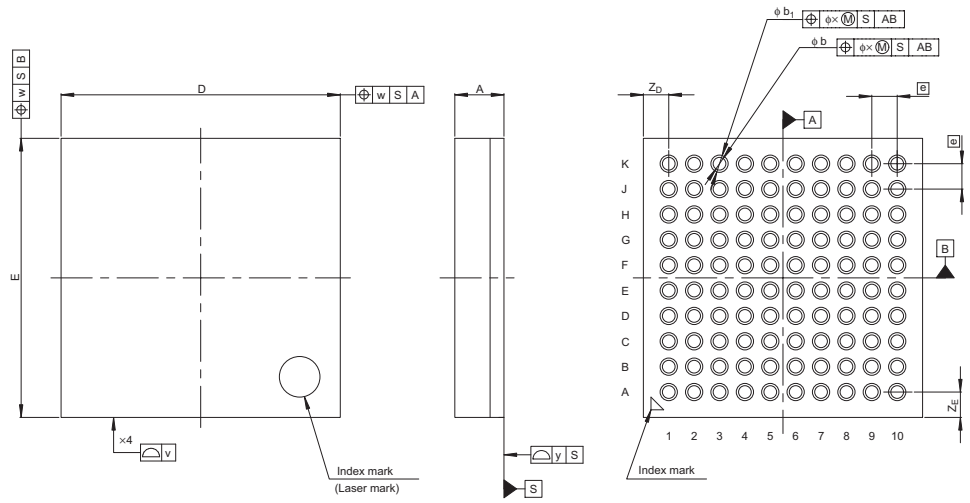
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP100-14x14-0.50	PLQP0100KB-A	100P6Q-A / FP-100U / FP-100UV	0.6g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.35	0.5	0.65
L_1	—	1.0	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TFLGA100-5.5x5.5-0.50	PTLG0100KA-A	100F0M	0.1g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	5.5	—
E	—	5.5	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.05
e	—	0.5	—
b	0.21	0.25	0.29
b_1	0.29	0.34	0.39
x	—	—	0.08
y	—	—	0.10
Z_D	—	0.5	—
Z_E	—	0.5	—

Rev.	Date	Description	
		Page	Summary
		15, 16	• "Interrupt table register" in **Figure 2.1** and **2.1.6** changed to "Interrupt vector table base register"
		18	• Scribal error: "24 bit" in **2.2.2** corrected to "32 bit"
			Chapter 3
		19	• Descriptions for this chapter and **Figure 3.1** modified
			Chapter 4
		20	• "(SFR)" of chapter title changed to "(SFRs)" • Description for initial paragraph of **Chapter 4** modified • Reset value for CCR and PBC in **Table 4.1** changed
		21, 22	• "UARTi Bus Collision Detection Interrupt Control Register" (i = 0 to 6) in **Tables 4.2 and 4.3** changed to "UARTi Bus Collision, Start/Stop Condition Detection Interrupt Control Register" • "DMAi interrupt" in **Tables 4.2 and 4.3** changed to "DMAi transfer complete interrupt"
		22	• Reset value for IIO3IR and IIO8IR to IIO11R in **Table 4.3** modified
		25	• Scribal error: address "00010Fh" added to **Table 4.6**
		32	• "Upward/Downward Counting Select Register" in **Table 4.13** changed to "Increment/Decrement Counting Select Register"
		38	• CSOP2 for address 040056h in **Table 4.19** deleted • Reset value for CM3 in **Table 4.19** changed
		43	• "DMAi Source Select Register i" in **Table 4.24** changed to "DMAi Request Source Select Register i"
			Chapter 5
		—	• This chapter newly added
			Appendix 1
		81	• "Package Dimension" as title changed to "Package Dimensions"
1.10	Sep 17, 2009	—	Third edition released
		—	The manual in general • Added 100-pin plastic molded LGA and 80- and 64-pin plastic molded LQFP packages • When new tables/figures are added for 80-/64-pin packages, add the following description: "(for the 100-pin package)" to the title of corresponding current tables/figures
			Chapter 1. Overview
		1	• Added description for 100-pin LGA and 80-/64-pin packages to lines 12 and 13 of **1.1**; Added description "a maximum of" to "nine channels of serial interface"; Deleted the whole description of "Notes to users"
		2	• Changed minimum RAM size "40" in **Table 1.1**, to "32" • Modified description for "External Bus Expansion", to **Table 1.1**; Moved this unit below "Clock"
		3	• Added "(optional)" for IEBus mode for "Intelligent I/O" in **Table 1.2** • Modified description for "Flash memory" in **Tables 1.2** • Added "100-pin plastic molded TFLGA (PTLG0100KA-A)" to **Table 1.2**
		4-7	• Added **Tables 1.3 to 1.6** to provide specifications for 80-/64-pin packages

Revision History	R32C/111 Group Datasheet

Rev.	Date	Description	
		Page	Summary
		8	• Completed “under development” phase of part numbers R5F64110DFB, R5F64111DFB, R5F64112DFB, R5F64114DFB, R5F64115DFB, and R5F64116DFB in **Table 1.7** • Added product information for 100-pin LGA and 80-/64-pin packages to **Table 1.7**
		9	• Added product information for 100-pin LGA and 80-/64-pin packages, and 32-Kbyte RAM to **Figure 1.1** • Deleted hyphenation for part number in **Figure 1.1**
		11, 12, 14, 18, 21	• Added **Figures 1.3, 1.4, and 1.6 to 1.8** to provide block diagrams and pin assignment for 100-pin LGA and 80-/64-pin packages
		13	• Changed the order of Notes in **Figures 1.5**
		15-17	• Added pin No. for 100-pin LGA package to **Tables 1.8 to 1.10**
		19, 20, 22, 23	• Added **Tables 1.11 to 1.14** to provide pin characteristics for 80-/64-pin packages.
		24	• Changed the following expression: “A ceramic resonator or a crystal oscillator” for “Main clock input/output” in **Table 1.15**, to “A crystal, or a ceramic resonator”
		25	• Modified descriptions for $\overline{\text{HLDA}}$ and $\overline{\text{RDY}}$ of “Bus control pins” in **Table 1.16**
		26	• Changed the following expression: “selected” for “Input port” in **Table 1.17**, to “selectable” • Modified description “TXD2” for TXD0 to TXD8 of “Serial interface” in **Table 1.17**, to “TXD2 output”
		28-30	• Added **Tables 1.19 to 1.21** to provide pin definitions and functions for 80-/64-pin packages
			Chapter 2. CPU
		—	• Made major text modifications to this chapter
		33	• Changed the following expression: “a requested interrupt’s priority level” in line 2 of **2.1.8.11**, to “the interrupt request level”
			Chapter 3. Memory
		35	• Made major text modifications to this chapter • Changed RAM size “40” in line 7 of this chapter, to “63”, and address “0000A3FFh” in line 8, to “0000FFFFh” • Added descriptions for 32-Kbyte RAM and 128-Kbyte ROM to **Figure 3.1** • Changed two “can be”s in Notes 3 and 4 of **Figure 3.1**, to “becomes”s
			Chapter 4. SFRs
		36	• Changed hexadecimal format of reset values for registers CCR and FMCR in **Table 4.1**, to binary • Added FEBC3 register to addresses 000010h-000011h in **Table 4.1** • Changed FEBC register for addresses 00001Ch-00001Dh, to FEBC0 in **Table 4.1** • Modified the following register name in **Table 4.1**: “Chip-select Boundary (between n and n + 1) Setting Register”, to “Chip-select n and n + 1 Boundary Setting Register”