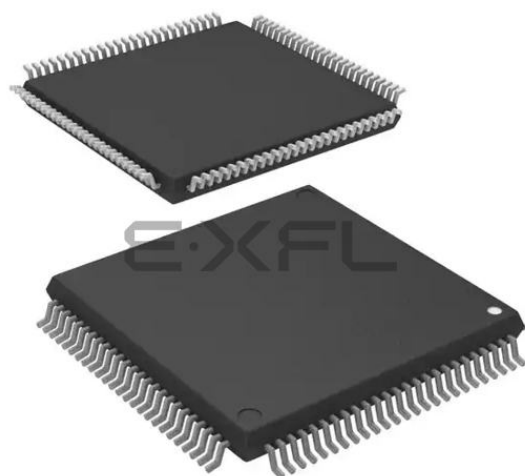




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Details

Product Status	Not For New Designs
Core Processor	R32C/100
Core Size	16/32-Bit
Speed	50MHz
Connectivity	EBI/EMI, I ² C, IEBus, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	82
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	40K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f64114dfb-u0

1.1.2 Performance Overview

Tables 1.1 to 1.4 show the performance overview of the R32C/111 Group.

Table 1.1 Performance Overview for the 100-pin Package (1/2)

Unit	Function	Explanation
CPU	Central processing unit	R32C/100 Series CPU Core • Basic instructions: 108 • Minimum instruction execution time: 20 ns ($f(\text{CPU}) = 50 \text{ MHz}$) • Multiplier: 32-bit $\times$ 32-bit $\rightarrow$ 64-bit • Multiply-accumulate unit: 32-bit $\times$ 32-bit + 64-bit $\rightarrow$ 64-bit • IEEE-754 compatible FPU: Single precision • 32-bit barrel shifter • Operating mode: Single-chip mode, memory expansion mode, microprocessor mode (optional ⁽¹⁾)
Memory		Flash memory: 256 to 512 Kbytes RAM: 32 to 63 Kbytes Data flash: 4 Kbytes $\times$ 2 blocks Refer to Table 1.5 for memory size of each product group
Voltage Detector	Low voltage detector	Optional ⁽¹⁾ Low voltage detection interrupt
Clock	Clock generator	• 4 circuits (main clock, sub clock, PLL, on-chip oscillator) • Oscillation stop detector: Main clock oscillator stop/restart detection • Frequency divide circuit: Divide-by-2 to divide-by-24 selectable • Low power modes: Wait mode, stop mode
External Bus Expansion	Bus and memory expansion	• Address space: 4 Gbytes (of which up to 64 Mbytes is user accessible) • External bus Interface: Support for wait-state insertion, 4 chip select outputs, 3V/5V interface • Bus format: Separate bus/Multiplexed bus selectable, data bus width selectable (8/16 bits)
Interrupts		Interrupt vectors: 261 External interrupt inputs: $\overline{\text{NMI}}$, $\overline{\text{INT}} \times 6$, key input $\times 4$ Interrupt priority levels: 7
Watchdog Timer		15 bits $\times$ 1 (selectable input frequency from prescaler output)
DMA	DMAC	4 channels • Cycle-steal transfer mode • Request sources: 51 • 2 transfer modes: Single transfer, repeat transfer
	DMAC II	• Triggered by an interrupt request of any peripheral • 3 characteristic transfer functions: Immediate data transfer, calculation result transfer, chain transfer
I/O Ports	Programmable I/O ports	• 2 input-only ports • 82 CMOS I/O ports • 2 N-channel open drain ports • A pull-up resistor is selectable for every 4 input ports

Note:

1. Contact a Renesas Electronics sales office to use the optional features.

Table 1.3 Performance Overview for the 64-pin Package (1/2)

Unit	Function	Explanation
CPU	Central processing unit	R32C/100 Series CPU Core • Basic instructions: 108 • Minimum instruction execution time: 20 ns ($f(\text{CPU}) = 50 \text{ MHz}$) • Multiplier: 32-bit $\times$ 32-bit $\rightarrow$ 64-bit • Multiply-accumulate unit: 32-bit $\times$ 32-bit + 64-bit $\rightarrow$ 64-bit • IEEE-754 compatible FPU: Single precision • 32-bit barrel shifter • Operating mode: Single-chip mode
Memory		Flash memory: 128/256 Kbytes RAM: 32 Kbytes Data flash: 4 Kbytes $\times$ 2 blocks Refer to Table 1.5 for memory size of each product group
Voltage Detector	Low voltage detector	Optional ⁽¹⁾ Low voltage detection interrupt
Clock	Clock generator	• 4 circuits (main clock, sub clock, PLL, on-chip oscillator) • Oscillation stop detector: Main clock oscillator stop/restart detection • Frequency divide circuit: Divide-by-2 to divide-by-24 selectable • Low power modes: Wait mode, stop mode
Interrupts		Interrupt vectors: 261 External interrupt inputs: $\overline{\text{NMI}}$, $\overline{\text{INT}} \times 6$, key input $\times 4$ Interrupt priority levels: 7
Watchdog Timer		15 bits $\times$ 1 (selectable input frequency from prescaler output)
DMA	DMAC	4 channels • Cycle-steal transfer mode • Request sources: 45 • 2 transfer modes: Single transfer, repeat transfer
	DMAC II	• Triggered by an interrupt request of any peripheral • 3 characteristic transfer functions: Immediate data transfer, calculation result transfer, chain transfer
I/O Ports	Programmable I/O ports	• 1 input-only port • 49 CMOS I/O ports • 2 N-channel open drain ports • A pull-up resistor is selectable for every 4 input ports

Note:

1. Contact a Renesas Electronics sales office to use the optional features.

1.2 Product Information

Table 1.5 lists the product information and Figure 1.1 shows the details of the part number.

Table 1.5 R32C/111 Group Product List

As of March, 2014

Part Number	Package Code ⁽¹⁾	ROM Capacity ⁽²⁾	RAM Capacity	Remarks
R5F64110DFB	PLQP0100KB-A	256 Kbytes +8 Kbytes	63 Kbytes	-40°C to 85°C (D version)
R5F64111DFB		384 Kbytes +8 Kbytes		
R5F64112DFB		512 Kbytes +8 Kbytes		
R5F64114DFB		256 Kbytes +8 Kbytes	40 Kbytes	
R5F64115DFB		384 Kbytes +8 Kbytes		
R5F64116DFB		512 Kbytes +8 Kbytes		
R5F64111NLG	PTLG0100KA-A	384 Kbytes +8 Kbytes	63 Kbytes	-20°C to 85°C (N version)
R5F64112NLG		512 Kbytes +8 Kbytes		
R5F6411FNLG		256 Kbytes +8 Kbytes	32 Kbytes	
R5F6411EDFN	PLQP064KB-A	128 Kbytes +8 Kbytes	32 Kbytes	-40°C to 85°C (D version)
R5F6411FDFN		256 Kbytes +8 Kbytes		

Notes:

- The old package codes are as follows:
 PLQP0100KB-A: 100P6Q-A
 PTLG0100KA-A: 100F0M
 PLQP0064KB-A: 64P6Q-A
- " + 8 Kbytes" in the ROM capacity column indicates the data flash capacity.

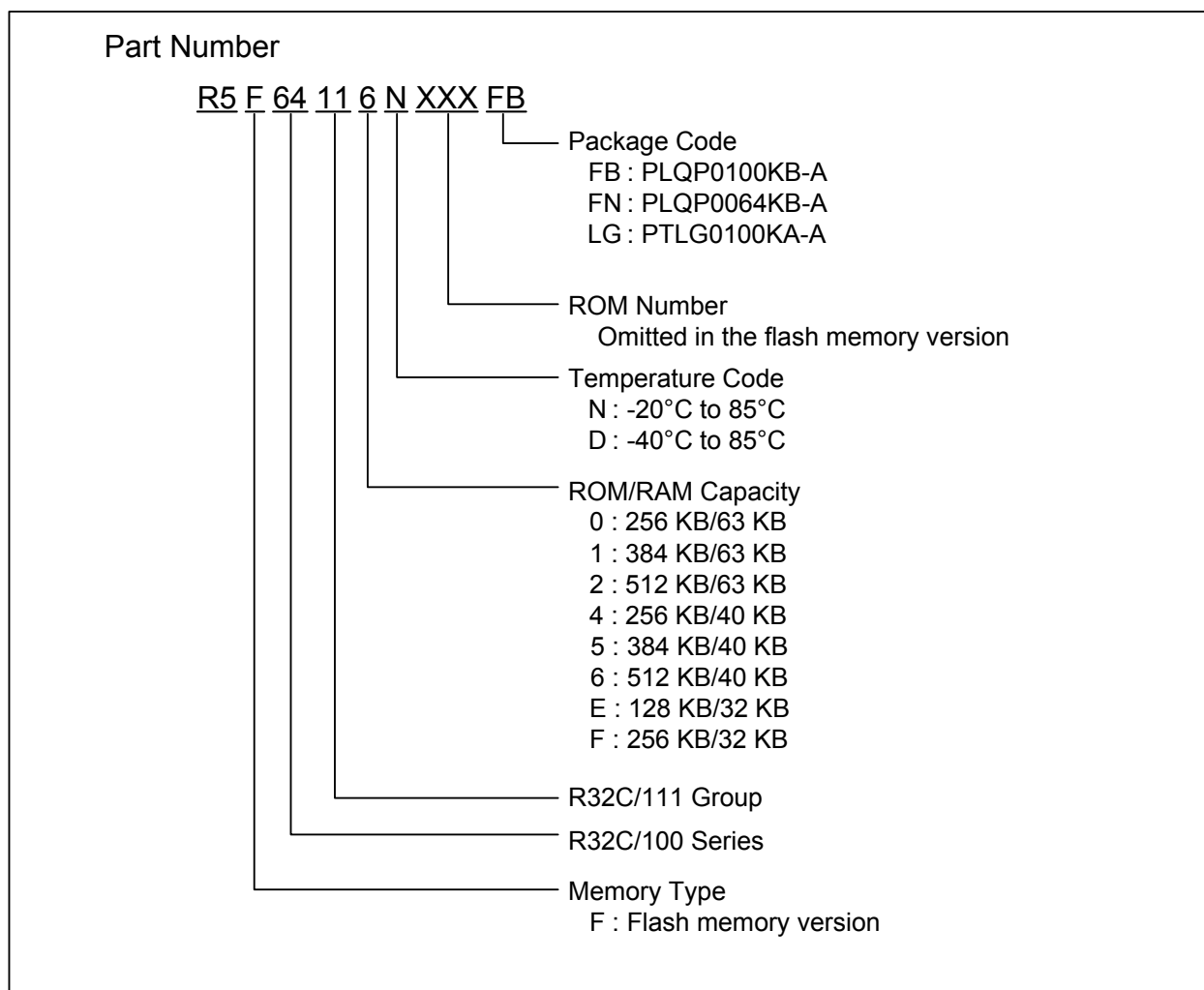


Figure 1.1 Part Numbering

2.2 Fast Interrupt Registers

The following three registers are provided to minimize the overhead of the interrupt sequence.

2.2.1 Save Flag Register (SVF)

This 32-bit register is used to save the flag register when a fast interrupt occurs.

2.2.2 Save PC Register (SVP)

This 32-bit register is used to save the program counter when a fast interrupt occurs.

2.2.3 Vector Register (VCT)

This 32-bit register is used to indicate a jump address when a fast interrupt occurs.

2.3 DMAC-associated Registers

There are seven types of DMAC-associated registers.

2.3.1 DMA Mode Registers (DMD0, DMD1, DMD2, and DMD3)

These 32-bit registers are used to set DMA transfer mode, bit rate, etc.

2.3.2 DMA Terminal Count Registers (DCT0, DCT1, DCT2, and DCT3)

These 24-bit registers are used to set the number of DMA transfers.

2.3.3 DMA Terminal Count Reload Registers (DCR0, DCR1, DCR2, and DCR3)

These 24-bit registers are used to set the reloaded values for DMA terminal count registers.

2.3.4 DMA Source Address Registers (DSA0, DSA1, DSA2, and DSA3)

These 32-bit registers are used to set DMA source addresses.

2.3.5 DMA Source Address Reload Registers (DSR0, DSR1, DSR2, and DSR3)

These 32-bit registers are used to set the reloaded values for DMA source address registers.

2.3.6 DMA Destination Address Registers (DDA0, DDA1, DDA2, and DDA3)

These 32-bit registers are used to set DMA destination addresses.

2.3.7 DMA Destination Address Reload Registers (DDR0, DDR1, DDR2, and DDR3)

These 32-bit registers are used to set reloaded values for DMA destination address registers.

Table 4.7 SFR List (7)

Address	Register	Symbol	Reset Value
000140h	Group 2 Waveform Generation Register 0	G2PO0	XXXXh
000141h			
000142h	Group 2 Waveform Generation Register 1	G2PO1	XXXXh
000143h			
000144h	Group 2 Waveform Generation Register 2	G2PO2	XXXXh
000145h			
000146h	Group 2 Waveform Generation Register 3	G2PO3	XXXXh
000147h			
000148h	Group 2 Waveform Generation Register 4	G2PO4	XXXXh
000149h			
00014Ah	Group 2 Waveform Generation Register 5	G2PO5	XXXXh
00014Bh			
00014Ch	Group 2 Waveform Generation Register 6	G2PO6	XXXXh
00014Dh			
00014Eh	Group 2 Waveform Generation Register 7	G2PO7	XXXXh
00014Fh			
000150h	Group 2 Waveform Generation Control Register 0	G2POCR0	0000 0000b
000151h	Group 2 Waveform Generation Control Register 1	G2POCR1	0000 0000b
000152h	Group 2 Waveform Generation Control Register 2	G2POCR2	0000 0000b
000153h	Group 2 Waveform Generation Control Register 3	G2POCR3	0000 0000b
000154h	Group 2 Waveform Generation Control Register 4	G2POCR4	0000 0000b
000155h	Group 2 Waveform Generation Control Register 5	G2POCR5	0000 0000b
000156h	Group 2 Waveform Generation Control Register 6	G2POCR6	0000 0000b
000157h	Group 2 Waveform Generation Control Register 7	G2POCR7	0000 0000b
000158h			
000159h			
00015Ah			
00015Bh			
00015Ch			
00015Dh			
00015Eh			
00015Fh			
000160h	Group 2 Base Timer Register	G2BT	XXXXh
000161h			
000162h	Group 2 Base Timer Control Register 0	G2BCR0	0000 0000b
000163h	Group 2 Base Timer Control Register 1	G2BCR1	0000 0000b
000164h	Base Timer Start Register	BTSR	XXXX 0000b
000165h			
000166h	Group 2 Function Enable Register	G2FE	00h
000167h	Group 2 RTP Output Buffer Register	G2RTP	00h
000168h			
000169h			
00016Ah	Group 2 Serial Interface Mode Register	G2MR	00XX X000b
00016Bh	Group 2 Serial Interface Control Register	G2CR	0000 X110b
00016Ch	Group 2 SI/O Transmit Buffer Register	G2TB	XXXXh
00016Dh			
00016Eh	Group 2 SI/O Receive Buffer Register	G2RB	XXXXh
00016Fh			

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.9 SFR List (9)

Address	Register	Symbol	Reset Value
0001A0h	Group 0 Base Timer Register	G0BT	XXXXh
0001A1h			
0001A2h	Group 0 Base Timer Control Register 0	G0BCR0	0000 0000b
0001A3h	Group 0 Base Timer Control Register 1	G0BCR1	0000 0000b
0001A4h	Group 0 Time Measurement Prescaler Register 6	G0TPR6	00h
0001A5h	Group 0 Time Measurement Prescaler Register 7	G0TPR7	00h
0001A6h	Group 0 Function Enable Register	G0FE	00h
0001A7h	Group 0 Function Select Register	G0FS	00h
0001A8h			
0001A9h			
0001AAh			
0001ABh			
0001ACh			
0001ADh			
0001AEh			
0001AFh			
0001B0h			
0001B1h			
0001B2h			
0001B3h			
0001B4h			
0001B5h			
0001B6h			
0001B7h			
0001B8h			
0001B9h			
0001BAh			
0001BBh			
0001BCh			
0001BDh			
0001BEh			
0001BFh			
0001C0h			
0001C1h			
0001C2h			
0001C3h			
0001C4h	UART5 Special Mode Register 4	U5SMR4	00h
0001C5h	UART5 Special Mode Register 3	U5SMR3	00h
0001C6h	UART5 Special Mode Register 2	U5SMR2	00h
0001C7h	UART5 Special Mode Register	U5SMR	00h
0001C8h	UART5 Transmit/Receive Mode Register	U5MR	00h
0001C9h	UART5 Bit Rate Register	U5BRG	XXh
0001CAh	UART5 Transmit Buffer Register	U5TB	XXXXh
0001CBh			
0001CCh	UART5 Transmit/Receive Control Register 0	U5C0	0000 1000b
0001CDh	UART5 Transmit/Receive Control Register 1	U5C1	0000 0010b
0001CEh	UART5 Receive Buffer Register	U5RB	XXXXh
0001CFh			

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.10 SFR List (10)

Address	Register	Symbol	Reset Value
0001D0h			
0001D1h			
0001D2h			
0001D3h			
0001D4h	UART6 Special Mode Register 4	U6SMR4	00h
0001D5h	UART6 Special Mode Register 3	U6SMR3	00h
0001D6h	UART6 Special Mode Register 2	U6SMR2	00h
0001D7h	UART6 Special Mode Register	U6SMR	00h
0001D8h	UART6 Transmit/Receive Mode Register	U6MR	00h
0001D9h	UART6 Bit Rate Register	U6BRG	XXh
0001DAh	UART6 Transmit Buffer Register	U6TB	XXXXh
0001DBh			
0001DCh	UART6 Transmit/Receive Control Register 0	U6C0	0000 1000b
0001DDh	UART6 Transmit/Receive Control Register 1	U6C1	0000 0010b
0001DEh	UART6 Receive Buffer Register	U6RB	XXXXh
0001DFh			
0001E0h	UART7 Transmit/Receive Mode Register	U7MR	00h
0001E1h	UART7 Bit Rate Register	U7BRG	XXh
0001E2h	UART7 Transmit Buffer Register	U7TB	XXXXh
0001E3h			
0001E4h	UART7 Transmit/Receive Control Register 0	U7C0	00X0 1000b
0001E5h	UART7 Transmit/Receive Control Register 1	U7C1	XXXX 0010b
0001E6h	UART7 Receive Buffer Register	U7RB	XXXXh
0001E7h			
0001E8h	UART8 Transmit/Receive Mode Register	U8MR	00h
0001E9h	UART8 Bit Rate Register	U8BRG	XXh
0001EAh	UART8 Transmit Buffer Register	U8TB	XXXXh
0001EBh			
0001ECh	UART8 Transmit/Receive Control Register 0	U8C0	00X0 1000b
0001EDh	UART8 Transmit/Receive Control Register 1	U8C1	XXXX 0010b
0001EEh	UART8 Receive Buffer Register	U8RB	XXXXh
0001EFh			
0001F0h	UART7, UART8 Transmit/Receive Control Register 2	U78CON	X000 0000b
0001F1h			
0001F2h			
0001F3h			
0001F4h			
0001F5h			
0001F6h			
0001F7h			
0001F8h			
0001F9h			
0001FAh			
0001FBh			
0001FCh			
0001FDh			
0001FEh			
0001FFh			

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.13 SFR List (13)

Address	Register	Symbol	Reset Value
000320h			
000321h			
000322h			
000323h			
000324h	UART3 Special Mode Register 4	U3SMR4	00h
000325h	UART3 Special Mode Register 3	U3SMR3	00h
000326h	UART3 Special Mode Register 2	U3SMR2	00h
000327h	UART3 Special Mode Register	U3SMR	00h
000328h	UART3 Transmit/Receive Mode Register	U3MR	00h
000329h	UART3 Bit Rate Register	U3BRG	XXh
00032Ah	UART3 Transmit Buffer Register	U3TB	XXXXh
00032Bh			
00032Ch	UART3 Transmit/Receive Control Register 0	U3C0	0000 1000b
00032Dh	UART3 Transmit/Receive Control Register 1	U3C1	0000 0010b
00032Eh	UART3 Receive Buffer Register	U3RB	XXXXh
00032Fh			
000330h			
000331h			
000332h			
000333h			
000334h	UART2 Special Mode Register 4	U2SMR4	00h
000335h	UART2 Special Mode Register 3	U2SMR3	00h
000336h	UART2 Special Mode Register 2	U2SMR2	00h
000337h	UART2 Special Mode Register	U2SMR	00h
000338h	UART2 Transmit/Receive Mode Register	U2MR	00h
000339h	UART2 Bit Rate Register	U2BRG	XXh
00033Ah	UART2 Transmit Buffer Register	U2TB	XXXXh
00033Bh			
00033Ch	UART2 Transmit/Receive Control Register 0	U2C0	0000 1000b
00033Dh	UART2 Transmit/Receive Control Register 1	U2C1	0000 0010b
00033Eh	UART2 Receive Buffer Register	U2RB	XXXXh
00033Fh			
000340h	Count Start Register	TABSR	0000 0000b
000341h	Clock Prescaler Reset Register	CPSRF	0XXX XXXXb
000342h	One-shot Start Register	ONSF	0000 0000b
000343h	Trigger Select Register	TRGSR	0000 0000b
000344h	Increment/Decrement Select Register	UDF	0000 0000b
000345h			
000346h	Timer A0 Register	TA0	XXXXh
000347h			
000348h	Timer A1 Register	TA1	XXXXh
000349h			
00034Ah	Timer A2 Register	TA2	XXXXh
00034Bh			
00034Ch	Timer A3 Register	TA3	XXXXh
00034Dh			
00034Eh	Timer A4 Register	TA4	XXXXh
00034Fh			

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.14 SFR List (14)

Address	Register	Symbol	Reset Value
000350h	Timer B0 Register	TB0	XXXXh
000351h			
000352h	Timer B1 Register	TB1	XXXXh
000353h			
000354h	Timer B2 Register	TB2	XXXXh
000355h			
000356h	Timer A0 Mode Register	TA0MR	0000 0000b
000357h	Timer A1 Mode Register	TA1MR	0000 0000b
000358h	Timer A2 Mode Register	TA2MR	0000 0000b
000359h	Timer A3 Mode Register	TA3MR	0000 0000b
00035Ah	Timer A4 Mode Register	TA4MR	0000 0000b
00035Bh	Timer B0 Mode Register	TB0MR	00XX 0000b
00035Ch	Timer B1 Mode Register	TB1MR	00XX 0000b
00035Dh	Timer B2 Mode Register	TB2MR	00XX 0000b
00035Eh	Timer B2 Special Mode Register	TB2SC	XXXX XXX0b
00035Fh	Count Source Prescaler Register	TCSPR	0000 0000b
000360h			
000361h			
000362h			
000363h			
000364h	UART0 Special Mode Register 4	U0SMR4	00h
000365h	UART0 Special Mode Register 3	U0SMR3	00h
000366h	UART0 Special Mode Register 2	U0SMR2	00h
000367h	UART0 Special Mode Register	U0SMR	00h
000368h	UART0 Transmit/Receive Mode Register	U0MR	00h
000369h	UART0 Bit Rate Register	U0BRG	XXh
00036Ah	UART0 Transmit Buffer Register	U0TB	XXXXh
00036Bh			
00036Ch	UART0 Transmit/Receive Control Register 0	U0C0	0000 1000b
00036Dh	UART0 Transmit/Receive Control Register 1	U0C1	0000 0010b
00036Eh	UART0 Receive Buffer Register	U0RB	XXXXh
00036Fh			
000370h			
000371h			
000372h			
000373h			
000374h			
000375h			
000376h			
000377h			
000378h			
000379h			
00037Ah			
00037Bh			
00037Ch	CRC Data Register	CRCD	XXXXh
00037Dh			
00037Eh	CRC Input Register	CRCIN	XXh
00037Fh			

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.15 SFR List (15)

Address	Register	Symbol	Reset Value
000380h	A/D0 Register 0	AD00	00XXh
000381h			
000382h	A/D0 Register 1	AD01	00XXh
000383h			
000384h	A/D0 Register 2	AD02	00XXh
000385h			
000386h	A/D0 Register 3	AD03	00XXh
000387h			
000388h	A/D0 Register 4	AD04	00XXh
000389h			
00038Ah	A/D0 Register 5	AD05	00XXh
00038Bh			
00038Ch	A/D0 Register 6	AD06	00XXh
00038Dh			
00038Eh	A/D0 Register 7	AD07	00XXh
00038Fh			
000390h			
000391h			
000392h	A/D0 Control Register 4	AD0CON4	XXXX 00XXb
000393h			
000394h	A/D0 Control Register 2	AD0CON2	XX0X X000b
000395h	A/D0 Control Register 3	AD0CON3	XXXX X000b
000396h	A/D0 Control Register 0	AD0CON0	00h
000397h	A/D0 Control Register 1	AD0CON1	00h
000398h	D/A Register 0	DA0	XXh
000399h			
00039Ah	D/A Register 1	DA1	XXh
00039Bh			
00039Ch	D/A Control Register	DACON	XXXX XX00b
00039Dh			
00039Eh			
00039Fh			
0003A0h			
0003A1h			
0003A2h			
0003A3h			
0003A4h			
0003A5h			
0003A6h			
0003A7h			
0003A8h			
0003A9h			
0003AAh			
0003ABh			
0003ACh			
0003ADh			
0003AEh			
0003AFh			

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.17 SFR List (17)

Address	Register	Symbol	Reset Value
0003E0h			
0003E1h			
0003E2h			
0003E3h			
0003E4h			
0003E5h			
0003E6h			
0003E7h			
0003E8h			
0003E9h			
0003EAh			
0003EBh			
0003ECh			
0003EDh			
0003EEh			
0003EFh			
0003F0h	Pull-up Control Register 0	PUR0	0000 0000b
0003F1h	Pull-up Control Register 1	PUR1	XXXX 0000b
0003F2h	Pull-up Control Register 2	PUR2	0000 0000b
0003F3h	Pull-up Control Register 3	PUR3	XXXX XX00b
0003F4h			
0003F5h			
0003F6h			
0003F7h			
0003F8h			
0003F9h			
0003FAh			
0003FBh			
0003FCh			
0003FDh			
0003FEh			
0003FFh	Port Control Register	PCR	XXXX XXX0b

X: Undefined

Blanks are reserved. No access is allowed.

Table 5.6 Operating Conditions (5/5)**($V_{CC1} = V_{CC2} = 3.0$ to 5.5 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted) (1)**

Symbol	Characteristic		Value			Unit
			Min.	Typ.	Max.	
$V_{r(VCC1)}$	Allowable ripple voltage	$V_{CC1} = 5.0$ V			0.5	Vp-p
		$V_{CC1} = 3.0$ V			0.3	Vp-p
$V_{r(VCC2)}$	Allowable ripple voltage	$V_{CC2} = 5.0$ V			0.5	Vp-p
		$V_{CC2} = 3.0$ V			0.3	Vp-p
$dV_{r(VCC1)}/dt$	Ripple voltage gradient	$V_{CC1} = 5.0$ V			± 0.3	V/ms
		$V_{CC1} = 3.0$ V			± 0.3	V/ms
$dV_{r(VCC2)}/dt$	Ripple voltage gradient	$V_{CC2} = 5.0$ V			± 0.3	V/ms
		$V_{CC2} = 3.0$ V			± 0.3	V/ms
$f_r(VCC1)$	Allowable ripple frequency				10	kHz
$f_r(VCC2)$	Allowable ripple frequency				10	kHz

Note:

1. The device is operationally guaranteed under these operating conditions.

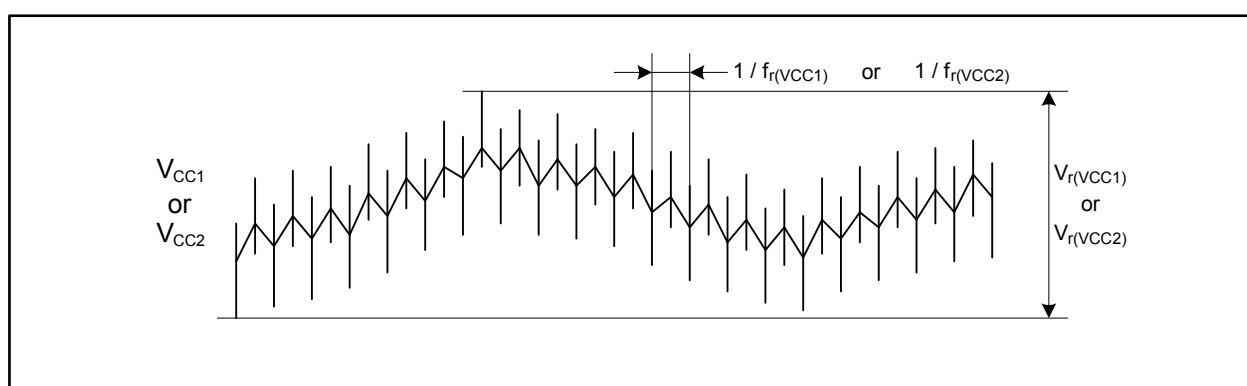
**Figure 5.2 Ripple Waveform**

Table 5.7 Electrical Characteristics of RAM**($V_{CC1} = V_{CC2} = 3.0$ to 5.5 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted)**

Symbol	Characteristic	Measurement Condition	Value			Unit
			Min.	Typ.	Max.	
V_{RDR}	RAM data retention voltage ⁽¹⁾	In stop mode	2.0			V

Note:

1. The value listed in the table is the minimum V_{CC1} to retain RAM data.

Table 5.8 Electrical Characteristics of Flash Memory**($V_{CC1} = V_{CC2} = 3.0$ to 5.5 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted)**

Symbol	Characteristic		Value			Unit
			Min.	Typ.	Max.	
—	Program/erase cycles ⁽¹⁾	Program area	1000			Cycles
		Data area	10000			Cycles
—	4-word program time	Program area		150	900	μ s
		Data area		300	1700	μ s
—	Lock bit program time	Program area		70	500	μ s
		Data area		140	1000	μ s
—	Block erasure time	4-Kbyte block		0.12	3.0	s
		32-Kbyte block		0.17	3.0	s
		64-Kbyte block		0.20	3.0	s
—	Data retention ⁽²⁾	$T_a = 55^\circ\text{C}$ ⁽³⁾	10			Years

Notes:

1. Program/erase definition
This value represents the number of erasures per block.
When the number of program/erase cycles is n, each block can be erased n times.
For example, if a 4-word write is performed in 512 different addresses in the 4-Kbyte block A and then the block is erased, this is counted as a single program/erase operation.
However, the same address cannot be written to more than once per erasure (overwrite disabled).
2. Data retention includes periods when no supply voltage is applied and no clock is provided.
3. Contact a Renesas Electronics sales office for data retention times other than the above condition.

Table 5.9 Power Supply Circuit Timing Characteristics
 ($V_{CC1} = V_{CC2} = 3.0$ to 5.5 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted)

Symbol	Characteristic	Measurement Condition	Value			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Internal power supply start-up stabilization time after the main power supply is turned on				2	ms

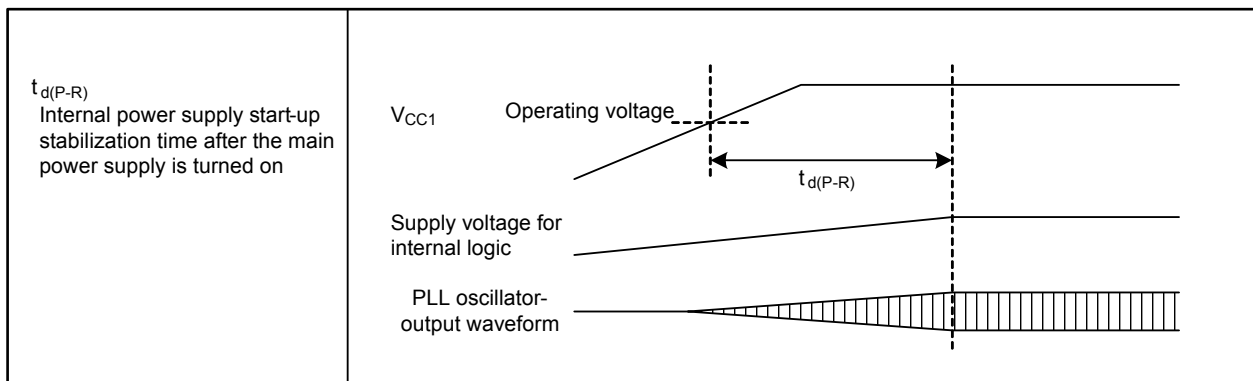


Figure 5.3 Power Supply Circuit Timing

Table 5.10 Electrical Characteristics of Voltage Regulator for Internal Logic
 ($V_{CC1} = V_{CC2} = 3.0$ to 5.5 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted)

Symbol	Characteristics	Measurement Condition	Value			Unit
			Min.	Typ.	Max.	
V_{VDC1}	Output voltage			1.5		V

Table 5.11 Electrical Characteristics of Low Voltage Detector
 ($V_{CC1} = V_{CC2} = 4.2$ to 5.5 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted)

Symbol	Characteristics	Measurement Condition	Value			Unit
			Min.	Typ.	Max.	
ΔV_{det}	Detected voltage error				± 0.3	V
$V_{det(R)} - V_{det(F)}$	Hysteresis width		0			V
—	Self-consuming current	$V_{CC1} = 5.0$ V, low voltage detector enabled		4		μA
$t_{d(E-A)}$	Operation start time of low voltage detector				150	μs

$$V_{CC1} = V_{CC2} = 5 \text{ V}$$

Timing Requirements ($V_{CC1} = V_{CC2} = 4.2$ to 5.5 V , $V_{SS} = 0 \text{ V}$, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.22 Timer A Input (counting input in event counter mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{C(TA)}$	TAiIN input clock cycle time	200		ns
$t_{W(TAH)}$	TAiIN input high level pulse width	80		ns
$t_{W(TAL)}$	TAiIN input low level pulse width	80		ns

Table 5.23 Timer A Input (gating input in timer mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{C(TA)}$	TAiIN input clock cycle time	400		ns
$t_{W(TAH)}$	TAiIN input high level pulse width	180		ns
$t_{W(TAL)}$	TAiIN input low level pulse width	180		ns

Table 5.24 Timer A Input (external trigger input in one-shot timer mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{C(TA)}$	TAiIN input clock cycle time	200		ns
$t_{W(TAH)}$	TAiIN input high level pulse width	80		ns
$t_{W(TAL)}$	TAiIN input low level pulse width	80		ns

Table 5.25 Timer A Input (external trigger input in pulse-width modulation mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{W(TAH)}$	TAiIN input high level pulse width	80		ns
$t_{W(TAL)}$	TAiIN input low level pulse width	80		ns

Table 5.26 Timer A Input (increment/decrement switching input in event counter mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{C(UP)}$	TAiOUT input clock cycle time	2000		ns
$t_{W(UPH)}$	TAiOUT input high level pulse width	1000		ns
$t_{W(UPL)}$	TAiOUT input low level pulse width	1000		ns
$t_{Su(UP-TIN)}$	TAiOUT input setup time	400		ns
$t_h(TIN-UP)$	TAiOUT input hold time	400		ns

$$V_{CC1} = V_{CC2} = 3.3 \text{ V}$$

Table 5.39 Electrical Characteristics (2/3) ($V_{CC1} = V_{CC2} = 3.0$ to 3.6 V , $V_{SS} = 0 \text{ V}$, $T_a = T_{opr}$, and $f_{CPU} = 50 \text{ MHz}$, unless otherwise noted)

Symbol	Characteristic		Measurement Condition	Value			Unit
				Min.	Typ.	Max.	
$V_{T+} - V_{T-}$	Hysteresis	HOLD, RDY, NMI, INT0 to INT5, KI0 to KI3, TA0IN to TA4IN, TA0OUT to TA4OUT, TB0IN to TB5IN, CTS0 to CTS8, CLK0 to CLK8, RXD0 to RXD8, SCL0 to SCL6, SDA0 to SDA6, SS0 to SS6, SRXD0 to SRXD6, ADTRG, IIO0_0 to IIO0_7, IIO1_0 to IIO1_7, UD0A, UD0B, UD1A, UD1B, ISCLK2, ISRXD2, IEIN ⁽¹⁾		0.2		1.0	V
		RESET		0.2		1.8	V
I_{IH}	High level input current	XIN, RESET, CNVSS, NSD, P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_1, P9_3 to P9_7, P10_0 to P10_7 ⁽²⁾	$V_I = 3.3 \text{ V}$			4.0	μA
I_{IL}	Low level input current	XIN, RESET, CNVSS, NSD, P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_1, P9_3 to P9_7, P10_0 to P10_7 ⁽²⁾	$V_I = 0 \text{ V}$			-4.0	μA
R_{PULLUP}	Pull-up resistor	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_1, P9_3 to P9_7, P10_0 to P10_7 ⁽²⁾	$V_I = 0 \text{ V}$	50	100	500	$\text{k}\Omega$
R_{fXIN}	Feedback resistor	XIN			3		$\text{M}\Omega$
R_{fXCIN}	Feedback resistor	XCIN			25		$\text{M}\Omega$

Notes:

1. Pins TB4IN, CTS4, CLK4, RXD4, SCL4, SDA4, SS4, SRXD4, and UART6, and UART7 are available in the 100-pin package only.
2. Ports P0_4 to P0_7, P1_0 to P1_4, P3_4 to P3_7, P4, P5, P9_1, and P9_4 to P9_7 are available in the 100-pin package only.

$$V_{CC1} = V_{CC2} = 3.3 \text{ V}$$

Switching Characteristics ($V_{CC1} = V_{CC2} = 3.0$ to 3.6 V , $V_{SS} = 0 \text{ V}$, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.59 Serial Interface

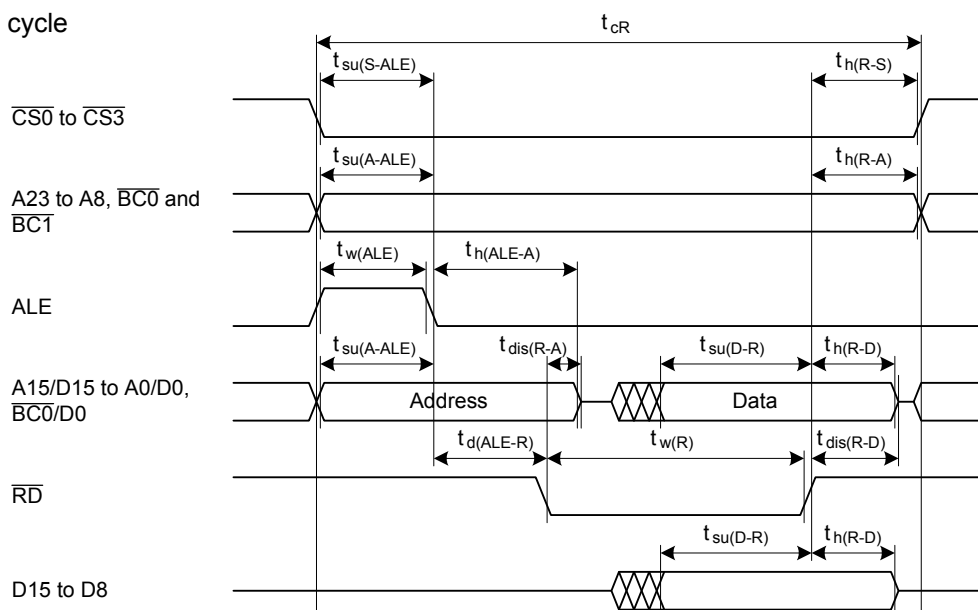
Symbol	Characteristic	Measurement Condition	Value		Unit
			Min.	Max.	
$t_{d(C-Q)}$	TXDi output delay time	Refer to Figure 5.6		80	ns
$t_{h(C-Q)}$	TXDi output hold time		0		ns

Table 5.60 Intelligent I/O

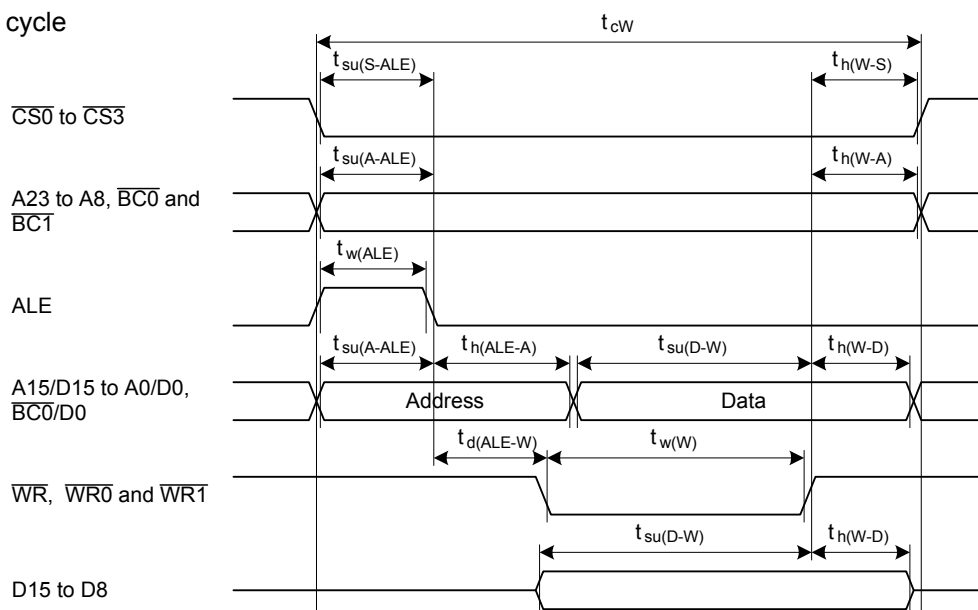
Symbol	Characteristic	Measurement Condition	Value		Unit
			Min.	Max.	
$t_{d(ISCLK2-TXD)}$	ISTXD2 output delay time	Refer to Figure 5.6		180	ns
$t_{h(ISCLK2-RXD)}$	ISTXD2 output hold time		0		ns

External bus timing (multiplexed bus)

Read cycle



Write cycle



Measurement conditions

Item		$V_{CC1} = V_{CC2} = 4.2 \text{ to } 5.5 \text{ V}$	$V_{CC1} = V_{CC2} = 3.0 \text{ to } 3.6 \text{ V}$
Criterion for input voltage	V_{IH}	2.5 V	1.5 V
	V_{IL}	0.8 V	0.5 V
Criterion for output voltage	V_{OH}	2.0 V	2.4 V
	V_{OL}	0.8 V	0.5 V

Figure 5.9 External Bus Timing for Multiplexed Bus

Revision History	R32C/111 Group Datasheet
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Rev.	Date	Description	
		Page	Summary
		15, 16	• “Interrupt table register” in Figure 2.1 and 2.1.6 changed to “Interrupt vector table base register”
		18	• Scribal error: “24 bit” in 2.2.2 corrected to “32 bit”
		Chapter 3	
		19	• Descriptions for this chapter and Figure 3.1 modified
		Chapter 4	
		20	• “(SFR)” of chapter title changed to “(SFRs)”
			• Description for initial paragraph of Chapter 4 modified
			• Reset value for CCR and PBC in Table 4.1 changed
		21, 22	• “UARTi Bus Collision Detection Interrupt Control Register” (i = 0 to 6) in Tables 4.2 and 4.3 changed to “UARTi Bus Collision, Start/Stop Condition Detection Interrupt Control Register”
			• “DMAi interrupt” in Tables 4.2 and 4.3 changed to “DMAi transfer complete interrupt”
		22	• Reset value for IIO3IR and IIO8IR to IIO11R in Table 4.3 modified
		25	• Scribal error: address “00010Fh” added to Table 4.6
		32	• “Upward/Downward Counting Select Register” in Table 4.13 changed to “Increment/Decrement Counting Select Register”
1.10	Sep 17, 2009	38	• CSOP2 for address 040056h in Table 4.19 deleted
			• Reset value for CM3 in Table 4.19 changed
		43	• “DMAi Source Select Register i” in Table 4.24 changed to “DMAi Request Source Select Register i”
		Chapter 5	
		—	• This chapter newly added
		Appendix 1	
		81	• “Package Dimension” as title changed to “Package Dimensions”
		—	Third edition released
		—	The manual in general
			• Added 100-pin plastic molded LGA and 80- and 64-pin plastic molded LQFP packages
			• When new tables/figures are added for 80-/64-pin packages, add the following description: “(for the 100-pin package)” to the title of corresponding current tables/figures
		Chapter 1. Overview	
		1	• Added description for 100-pin LGA and 80-/64-pin packages to lines 12 and 13 of 1.1 ; Added description “a maximum of” to “nine channels of serial interface”; Deleted the whole description of “Notes to users”
		2	• Changed minimum RAM size “40” in Table 1.1 , to “32”
			• Modified description for “External Bus Expansion”, to Table 1.1 ; Moved this unit below “Clock”
		3	• Added “(optional)” for IEBus mode for “Intelligent I/O” in Table 1.2
			• Modified description for “Flash memory” in Tables 1.2
			• Added “100-pin plastic molded TFLGA (PTLG0100KA-A)” to Table 1.2
		4-7	• Added Tables 1.3 to 1.6 to provide specifications for 80-/64-pin packages