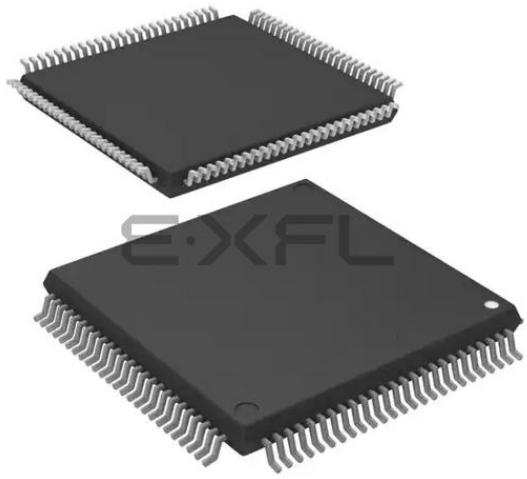

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	R32C/100
Core Size	16/32-Bit
Speed	50MHz
Connectivity	EBI/EMI, I²C, IEBus, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	82
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	40K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f64114dfb-ua

1.2 Product Information

Table 1.5 lists the product information and Figure 1.1 shows the details of the part number.

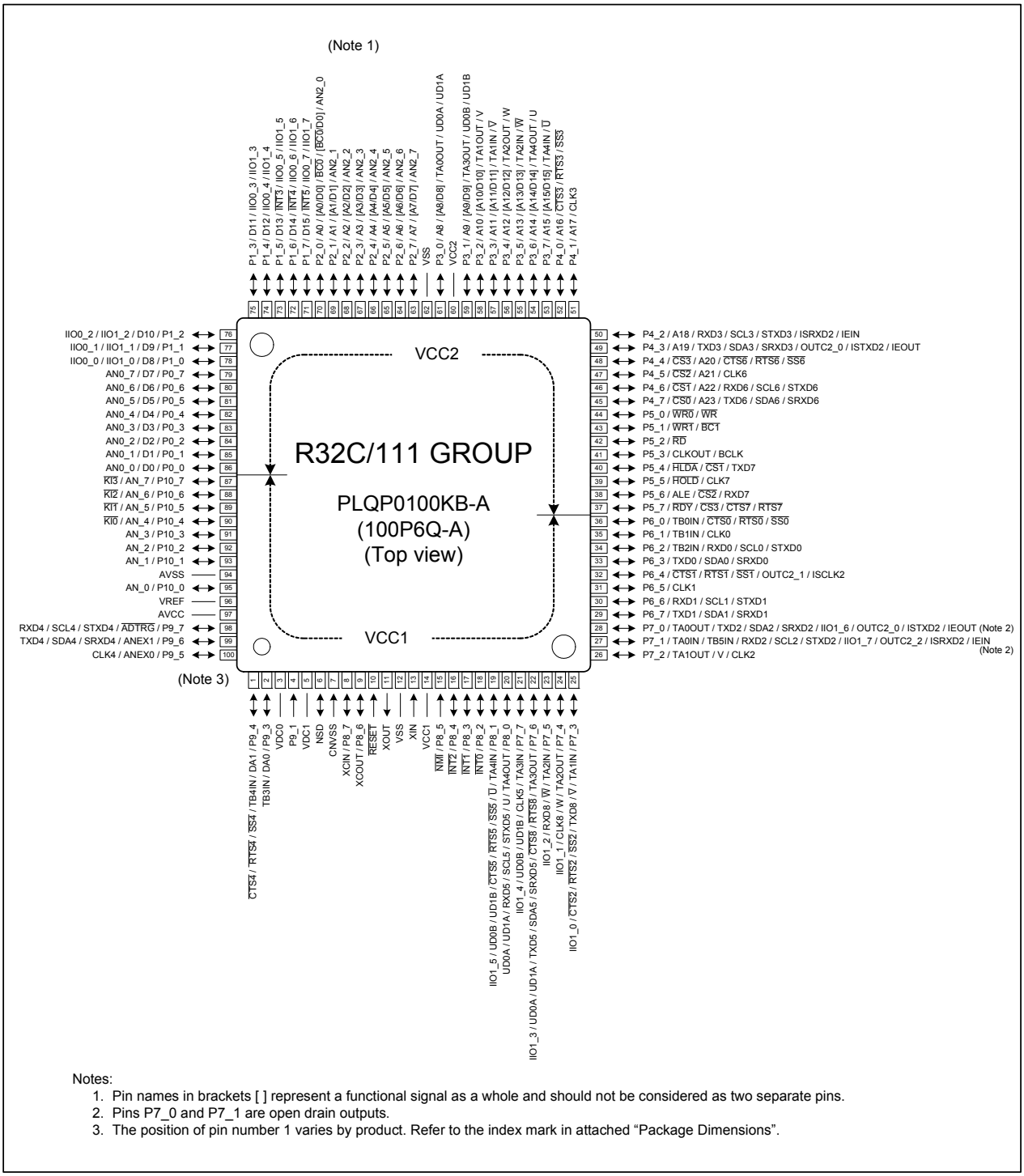
Table 1.5 R32C/111 Group Product List **As of March, 2014**

Part Number	Package Code (1)	ROM Capacity (2)	RAM Capacity	Remarks
R5F64110DFB	PLQP0100KB-A	256 Kbytes +8 Kbytes	63 Kbytes	-40°C to 85°C (D version)
R5F64111DFB		384 Kbytes +8 Kbytes		
R5F64112DFB		512 Kbytes +8 Kbytes		
R5F64114DFB		256 Kbytes +8 Kbytes	40 Kbytes	
R5F64115DFB		384 Kbytes +8 Kbytes		
R5F64116DFB		512 Kbytes +8 Kbytes		
R5F64111NLG	PTLG0100KA-A	384 Kbytes +8 Kbytes	63 Kbytes	-20°C to 85°C (N version)
R5F64112NLG		512 Kbytes +8 Kbytes		
R5F6411FNLG		256 Kbytes +8 Kbytes	32 Kbytes	
R5F6411EDFN	PLQP064KB-A	128 Kbytes +8 Kbytes	32 Kbytes	-40°C to 85°C (D version)
R5F6411FDFN		256 Kbytes +8 Kbytes		

Notes:
1. The old package codes are as follows:
   PLQP0100KB-A: 100P6Q-A
   PTLG0100KA-A: 100F0M
   PLQP0064KB-A: 64P6Q-A
2. “+ 8 Kbytes” in the ROM capacity column indicates the data flash capacity.

1.4 Pin Assignments

Figures 1.4 to 1.6 show the pin assignments (top view) and Tables 1.6 to 1.10 show the pin characteristics.



Notes:
1. Pin names in brackets [ ] represent a functional signal as a whole and should not be considered as two separate pins.
2. Pins P7_0 and P7_1 are open drain outputs.
3. The position of pin number 1 varies by product. Refer to the index mark in attached “Package Dimensions”.

Figure 1.4 Pin Assignment for the 100-pin Package (top view)

Table 1.6 Pin Characteristics for the 100-pin Package (1/3)

Pin No.		Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
QFP	LGA								
1	A1		P9_4		TB4IN	CTS4/RTS4/SS4		DA1	
2	E4		P9_3		TB3IN			DA0	
3	B1	VDC0							
4	D3		P9_1						
5	C2	VDC1							
6	C1	NSD							
7	D2	CNVSS							
8	D1	XCIN	P8_7						
9	E3	XCOUT	P8_6						
10	E2	RESET							
11	E1	XOUT							
12	F3	VSS							
13	F2	XIN							
14	F1	VCC1							
15	G2		P8_5	NMI					
16	F5		P8_4	INT2					
17	G3		P8_3	INT1					
18	G1		P8_2	INT0					
19	F4		P8_1		TA4IN/U	CTS5/RTS5/SS5	IIO1_5/UD0B/UD1B		
20	H1		P8_0		TA4OUT/U	RXD5/SCL5/STXD5	UD0A/UD1A		
21	H2		P7_7		TA3IN	CLK5	IIO1_4/UD0B/UD1B		
22	G4		P7_6		TA3OUT	TXD5/SDA5/ SRXD5/CTS8/RTS8	IIO1_3/UD0A/UD1A		
23	H3		P7_5		TA2IN/W	RXD8	IIO1_2		
24	J1		P7_4		TA2OUT/W	CLK8	IIO1_1		
25	J2		P7_3		TA1IN/V	CTS2/RTS2/SS2/ TXD8	IIO1_0		
26	K1		P7_2		TA1OUT/V	CLK2			
27	K2		P7_1		TA0IN/ TB5IN	RXD2/SCL2/STXD2	IIO1_7/OUTC2_2/ ISRXD2/IEIN		
28	J3		P7_0		TA0OUT	TXD2/SDA2/SRXD2	IIO1_6/OUTC2_0/ ISTXD2/IEOUT		
29	H4		P6_7			TXD1/SDA1/SRXD1			
30	K3		P6_6			RXD1/SCL1/STXD1			
31	G5		P6_5			CLK1			
32	J4		P6_4			CTS1/RTS1/SS1	OUTC2_1/ISCLK2		
33	K4		P6_3			TXD0/SDA0/SRXD0			
34	H5		P6_2		TB2IN	RXD0/SCL0/STXD0			
35	J5		P6_1		TB1IN	CLK0			
36	K5		P6_0		TB0IN	CTS0/RTS0/SS0			
37	G6		P5_7			CTS7/RTS7			RDY/CS3
38	H6		P5_6			RXD7			ALE/CS2
39	J6		P5_5			CLK7			HOLD

Table 1.9 Pin Characteristics for the 64-pin Package (1/2)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Intelligent I/O Pin	Analog Pin
1	VDC1						
2	NSD						
3	CNVSS						
4	XCIN	P8_7					
5	XCOUT	P8_6					
6	$\overline{\text{RESET}}$						
7	XOUT						
8	VSS						
9	XIN						
10	VCC1						
11		P8_5	$\overline{\text{NMI}}$				
12		P8_4	$\overline{\text{INT2}}$				
13		P8_3	$\overline{\text{INT1}}$				
14		P8_2	$\overline{\text{INT0}}$				
15		P8_1		TA4IN/$\overline{\text{U}}$	$\overline{\text{CTS5}}$/$\overline{\text{RTS5}}$/$\overline{\text{SS5}}$	IIO1_5/UD0B/UD1B	
16		P8_0		TA4OUT/U	RXD5/SCL5/STXD5	UD0A/UD1A	
17		P7_7		TA3IN	CLK5	IIO1_4/UD0B/UD1B	
18		P7_6		TA3OUT	TXD5/SDA5/SRXD5/ $\overline{\text{CTS8}}$/$\overline{\text{RTS8}}$	IIO1_3/UD0A/UD1A	
19		P7_5		TA2IN/$\overline{\text{W}}$	RXD8	IIO1_2	
20		P7_4		TA2OUT/W	CLK8	IIO1_1	
21		P7_3		TA1IN/$\overline{\text{V}}$	$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$/$\overline{\text{SS2}}$/TXD8	IIO1_0	
22		P7_2		TA1OUT/V	CLK2		
23		P7_1		TA0IN/ TB5IN	RXD2/SCL2/STXD2	IIO1_7/OUTC2_2/ ISRXD2/IEIN	
24		P7_0		TA0OUT	TXD2/SDA2/SRXD2	IIO1_6/OUTC2_0/ ISTXD2/IEOUT	
25		P6_7			TXD1/SDA1/SRXD1		
26		P6_6			RXD1/SCL1/STXD1		
27		P6_5			CLK1		
28		P6_4			$\overline{\text{CTS1}}$/$\overline{\text{RTS1}}$/$\overline{\text{SS1}}$	OUTC2_1/ISCLK2	
29		P3_3		TA1IN/$\overline{\text{V}}$	$\overline{\text{CTS3}}$/$\overline{\text{RTS3}}$/$\overline{\text{SS3}}$		
30		P3_2		TA1OUT/V	TXD3/SDA3/SRXD3		
31		P3_1		TA3OUT	RXD3/SCL3/STXD3	UD0B/UD1B	
32		P3_0		TA0OUT	CLK3	UD0A/UD1A	
33		P6_3			TXD0/SDA0/SRXD0		
34		P6_2		TB2IN	RXD0/SCL0/STXD0		
35		P6_1		TB1IN	CLK0		
36		P6_0		TB0IN	$\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$/$\overline{\text{SS0}}$		
37		P2_7				IIO0_7	AN2_7
38		P2_6				IIO0_6	AN2_6
39		P2_5				IIO0_5	AN2_5
40		P2_4				IIO0_4	AN2_4

Table 1.14 Pin Definitions and Functions for the 100-pin Package (4/4)

Function	Symbol	I/O	Power Supply	Description
Serial interface special functions	STXD0 to STXD6	O	VCC1 VCC2	Serial data output in slave mode. STXD2 is N-channel open drain
	SRXD0 to SRXD6	I	VCC1 VCC2	Serial data input in slave mode
	$\overline{SS0}$ to $\overline{SS6}$	I	VCC1 VCC2	Input to control serial interface special functions
A/D converter	AN_0 to AN_7	I	VCC1	Analog input for the A/D converter
	AN0_0 to AN0_7, AN2_0 to AN2_7	I	VCC2	
	$\overline{ADTRG}$	I	VCC1	External trigger input for the A/D converter
	ANEX0	I/O	VCC1	Expanded analog input for the A/D converter and output in external op-amp connection mode
	ANEX1	I	VCC1	Expanded analog input for the A/D converter
D/A converter	DA0, DA1	O	VCC1	Output for the D/A converter
Reference voltage input	VREF	I	–	Reference voltage input for the A/D converter and D/A converter
Intelligent I/O	IIO0_0 to IIO0_7	I/O	VCC1 VCC2	Input/output for Intelligent I/O group 0. Either input capture or output compare is selectable
	IIO1_0 to IIO1_7	I/O	VCC1 VCC2	Input/output for Intelligent I/O group 1. Either input capture or output compare is selectable. IIO1_6 and IIO1_7 outputs assigned for ports P7_0 and P7_1 are N-channel open drain
	UD0A, UD0B, UD1A, UD1B	I	VCC1 VCC2	Input for the two-phase encoder
	OUTC2_0 to OUTC2_2	O	VCC1 VCC2	Output for OC (output compare) of Intelligent I/O group 2. OUTC2_0 and OUTC2_2 assigned for ports P7_0 and P7_1 are N-channel open drain
	ISCLK2	I/O	VCC1 VCC2	Clock input/output for the serial interface
	ISRXD2	I		Receive data input for the serial interface
	ISTXD2	O		Transmit data output for the serial interface. ISTXD2 assigned for port P7_0 is N-channel open drain
	IEIN	I	VCC1 VCC2	Receive data input for the serial interface
	IEOUT	O		Transmit data output for the serial interface. IEOUT assigned for port P7_0 is N-channel open drain

2. Central Processing Unit (CPU)

The CPU contains the registers shown below. There are two register banks each consisting of registers R2R0, R3R1, R6R4, R7R5, A0 to A3, SB, and FB.

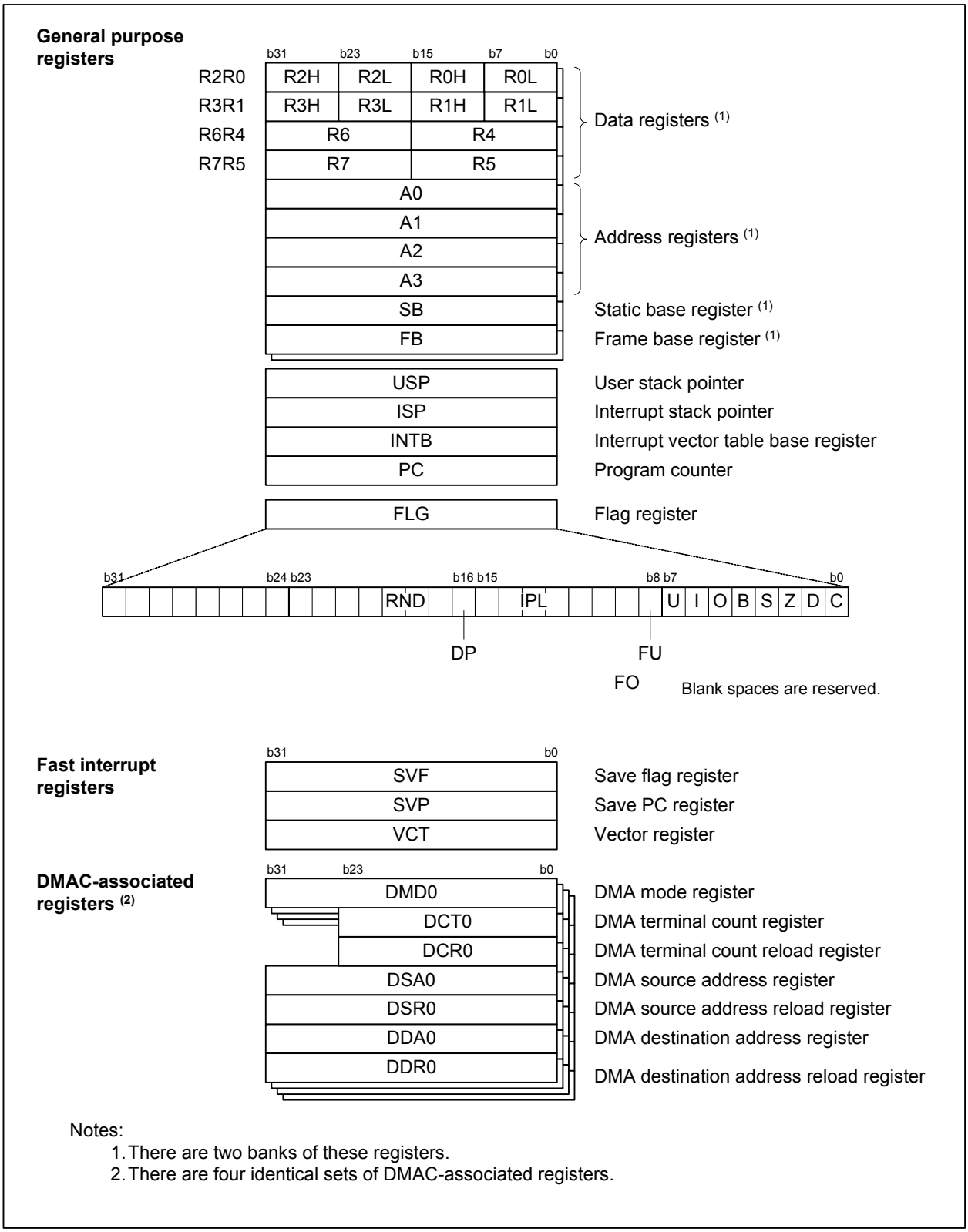


Figure 2.1 CPU Registers

Table 4.2 SFR List (2)

Address	Register	Symbol	Reset Value
000060h			
000061h	Timer B5 Interrupt Control Register	TB5IC	XXXX X000b
000062h	UART5 Transmit/NACK Interrupt Control Register	S5TIC	XXXX X000b
000063h	UART2 Receive/ACK Interrupt Control Register	S2RIC	XXXX X000b
000064h	UART6 Transmit/NACK Interrupt Control Register	S6TIC	XXXX X000b
000065h	UART3 Receive/ACK Interrupt Control Register	S3RIC	XXXX X000b
000066h	UART5/6 Bus Collision, START Condition/STOP Condition Detection Interrupt Control Register	BCN5IC/BCN6IC	XXXX X000b
000067h	UART4 Receive/ACK Interrupt Control Register	S4RIC	XXXX X000b
000068h	DMA0 Transfer Complete Interrupt Control Register	DM0IC	XXXX X000b
000069h	UART0/3 Bus Collision, START Condition/STOP Condition Detection Interrupt Control Register	BCN0IC/BCN3IC	XXXX X000b
00006Ah	DMA2 Transfer Complete Interrupt Control Register	DM2IC	XXXX X000b
00006Bh	A/D Converter 0 Convert Completion Interrupt Control Register	AD0IC	XXXX X000b
00006Ch	Timer A0 Interrupt Control Register	TA0IC	XXXX X000b
00006Dh	Intelligent I/O Interrupt Control Register 0	IIO0IC	XXXX X000b
00006Eh	Timer A2 Interrupt Control Register	TA2IC	XXXX X000b
00006Fh	Intelligent I/O Interrupt Control Register 2	IIO2IC	XXXX X000b
000070h	Timer A4 Interrupt Control Register	TA4IC	XXXX X000b
000071h	Intelligent I/O Interrupt Control Register 4	IIO4IC	XXXX X000b
000072h	UART0 Receive/ACK Interrupt Control Register	S0RIC	XXXX X000b
000073h	Intelligent I/O Interrupt Control Register 6	IIO6IC	XXXX X000b
000074h	UART1 Receive/ACK Interrupt Control Register	S1RIC	XXXX X000b
000075h	Intelligent I/O Interrupt Control Register 8	IIO8IC	XXXX X000b
000076h	Timer B1 Interrupt Control Register	TB1IC	XXXX X000b
000077h	Intelligent I/O Interrupt Control Register 10	IIO10IC	XXXX X000b
000078h	Timer B3 Interrupt Control Register	TB3IC	XXXX X000b
000079h			
00007Ah	INT5 Interrupt Control Register	INT5IC	XX00 X000b
00007Bh			
00007Ch	INT3 Interrupt Control Register	INT3IC	XX00 X000b
00007Dh			
00007Eh	INT1 Interrupt Control Register	INT1IC	XX00 X000b
00007Fh			
000080h			
000081h	UART2 Transmit/NACK Interrupt Control Register	S2TIC	XXXX X000b
000082h	UART5 Receive/ACK Interrupt Control Register	S5RIC	XXXX X000b
000083h	UART3 Transmit/NACK Interrupt Control Register	S3TIC	XXXX X000b
000084h	UART6 Receive/ACK Interrupt Control Register	S6RIC	XXXX X000b
000085h	UART4 Transmit/NACK Interrupt Control Register	S4TIC	XXXX X000b
000086h			
000087h	UART2 Bus Collision, START Condition/STOP Condition Detection Interrupt Control Register	BCN2IC	XXXX X000b

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.6 SFR List (6)

Address	Register	Symbol	Reset Value
000108h	Group 1 Time Measurement/Waveform Generation Register 4	G1TM4/G1PO4	XXXXh
000109h			
00010Ah	Group 1 Time Measurement/Waveform Generation Register 5	G1TM5/G1PO5	XXXXh
00010Bh			
00010Ch	Group 1 Time Measurement/Waveform Generation Register 6	G1TM6/G1PO6	XXXXh
00010Dh			
00010Eh	Group 1 Time Measurement/Waveform Generation Register 7	G1TM7/G1PO7	XXXXh
00010Fh			
000110h	Group 1 Waveform Generation Control Register 0	G1POCR0	0000 X000b
000111h	Group 1 Waveform Generation Control Register 1	G1POCR1	0X00 X000b
000112h	Group 1 Waveform Generation Control Register 2	G1POCR2	0X00 X000b
000113h	Group 1 Waveform Generation Control Register 3	G1POCR3	0X00 X000b
000114h	Group 1 Waveform Generation Control Register 4	G1POCR4	0X00 X000b
000115h	Group 1 Waveform Generation Control Register 5	G1POCR5	0X00 X000b
000116h	Group 1 Waveform Generation Control Register 6	G1POCR6	0X00 X000b
000117h	Group 1 Waveform Generation Control Register 7	G1POCR7	0X00 X000b
000118h	Group 1 Time Measurement Control Register 0	G1TMCR0	00h
000119h	Group 1 Time Measurement Control Register 1	G1TMCR1	00h
00011Ah	Group 1 Time Measurement Control Register 2	G1TMCR2	00h
00011Bh	Group 1 Time Measurement Control Register 3	G1TMCR3	00h
00011Ch	Group 1 Time Measurement Control Register 4	G1TMCR4	00h
00011Dh	Group 1 Time Measurement Control Register 5	G1TMCR5	00h
00011Eh	Group 1 Time Measurement Control Register 6	G1TMCR6	00h
00011Fh	Group 1 Time Measurement Control Register 7	G1TMCR7	00h
000120h	Group 1 Base Timer Register	G1BT	XXXXh
000121h			
000122h	Group 1 Base Timer Control Register 0	G1BCR0	0000 0000b
000123h	Group 1 Base Timer Control Register 1	G1BCR1	0000 0000b
000124h	Group 1 Time Measurement Prescaler Register 6	G1TPR6	00h
000125h	Group 1 Time Measurement Prescaler Register 7	G1TPR7	00h
000126h	Group 1 Function Enable Register	G1FE	00h
000127h	Group 1 Function Select Register	G1FS	00h
000128h			
000129h			
00012Ah			
00012Bh			
00012Ch			
00012Dh			
00012Eh			
00012Fh			
000130h to 00013Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.8 SFR List (8)

Address	Register	Symbol	Reset Value
000170h	Group 2 IEBus Address Register	IEAR	XXXXh
000171h			
000172h	Group 2 IEBus Control Register	IECR	00XX X000b
000173h	Group 2 IEBus Transmit Interrupt Source Detect Register	IETIF	XXX0 0000b
000174h	Group 2 IEBus Receive Interrupt Source Detect Register	IERIF	XXX0 0000b
000175h			
000176h			
000177h			
000178h			
000179h			
00017Ah			
00017Bh			
00017Ch			
00017Dh			
00017Eh			
00017Fh			
000180h	Group 0 Time Measurement/Waveform Generation Register 0	G0TM0/G0PO0	XXXXh
000181h			
000182h	Group 0 Time Measurement/Waveform Generation Register 1	G0TM1/G0PO1	XXXXh
000183h			
000184h	Group 0 Time Measurement/Waveform Generation Register 2	G0TM2/G0PO2	XXXXh
000185h			
000186h	Group 0 Time Measurement/Waveform Generation Register 3	G0TM3/G0PO3	XXXXh
000187h			
000188h	Group 0 Time Measurement/Waveform Generation Register 4	G0TM4/G0PO4	XXXXh
000189h			
00018Ah	Group 0 Time Measurement/Waveform Generation Register 5	G0TM5/G0PO5	XXXXh
00018Bh			
00018Ch	Group 0 Time Measurement/Waveform Generation Register 6	G0TM6/G0PO6	XXXXh
00018Dh			
00018Eh	Group 0 Time Measurement/Waveform Generation Register 7	G0TM7/G0PO7	XXXXh
00018Fh			
000190h	Group 0 Waveform Generation Control Register 0	G0POCR0	0000 X000b
000191h	Group 0 Waveform Generation Control Register 1	G0POCR1	0X00 X000b
000192h	Group 0 Waveform Generation Control Register 2	G0POCR2	0X00 X000b
000193h	Group 0 Waveform Generation Control Register 3	G0POCR3	0X00 X000b
000194h	Group 0 Waveform Generation Control Register 4	G0POCR4	0X00 X000b
000195h	Group 0 Waveform Generation Control Register 5	G0POCR5	0X00 X000b
000196h	Group 0 Waveform Generation Control Register 6	G0POCR6	0X00 X000b
000197h	Group 0 Waveform Generation Control Register 7	G0POCR7	0X00 X000b
000198h	Group 0 Time Measurement Control Register 0	G0TMCR0	00h
000199h	Group 0 Time Measurement Control Register 1	G0TMCR1	00h
00019Ah	Group 0 Time Measurement Control Register 2	G0TMCR2	00h
00019Bh	Group 0 Time Measurement Control Register 3	G0TMCR3	00h
00019Ch	Group 0 Time Measurement Control Register 4	G0TMCR4	00h
00019Dh	Group 0 Time Measurement Control Register 5	G0TMCR5	00h
00019Eh	Group 0 Time Measurement Control Register 6	G0TMCR6	00h
00019Fh	Group 0 Time Measurement Control Register 7	G0TMCR7	00h

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.11 SFR List (11)

Address	Register	Symbol	Reset Value
000200h to 0002BFh			
0002C0h	X0 Register/Y0 Register	X0R/Y0R	XXXXh
0002C1h			
0002C2h	X1 Register/Y1 Register	X1R/Y1R	XXXXh
0002C3h			
0002C4h	X2 Register/Y2 Register	X2R/Y2R	XXXXh
0002C5h			
0002C6h	X3 Register/Y3 Register	X3R/Y3R	XXXXh
0002C7h			
0002C8h	X4 Register/Y4 Register	X4R/Y4R	XXXXh
0002C9h			
0002CAh	X5 Register/Y5 Register	X5R/Y5R	XXXXh
0002CBh			
0002CCh	X6 Register/Y6 Register	X6R/Y6R	XXXXh
0002CDh			
0002CEh	X7 Register/Y7 Register	X7R/Y7R	XXXXh
0002CFh			
0002D0h	X8 Register/Y8 Register	X8R/Y8R	XXXXh
0002D1h			
0002D2h	X9 Register/Y9 Register	X9R/Y9R	XXXXh
0002D3h			
0002D4h	X10 Register/Y10 Register	X10R/Y10R	XXXXh
0002D5h			
0002D6h	X11 Register/Y11 Register	X11R/Y11R	XXXXh
0002D7h			
0002D8h	X12 Register/Y12 Register	X12R/Y12R	XXXXh
0002D9h			
0002DAh	X13 Register/Y13 Register	X13R/Y13R	XXXXh
0002DBh			
0002DCh	X14 Register/Y14 Register	X14R/Y14R	XXXXh
0002DDh			
0002DEh	X15 Register/Y15 Register	X15R/Y15R	XXXXh
0002DFh			
0002E0h	X-Y Control Register	XYC	XXXX XX00b
0002E1h			
0002E2h			
0002E3h			
0002E4h	UART1 Special Mode Register 4	U1SMR4	00h
0002E5h	UART1 Special Mode Register 3	U1SMR3	00h
0002E6h	UART1 Special Mode Register 2	U1SMR2	00h
0002E7h	UART1 Special Mode Register	U1SMR	00h
0002E8h	UART1 Transmit/Receive Mode Register	U1MR	00h
0002E9h	UART1 Bit Rate Register	U1BRG	XXh
0002EAh	UART1 Transmit Buffer Register	U1TB	XXXXh
0002EBh			
0002ECh	UART1 Transmit/Receive Control Register 0	U1C0	0000 1000b
0002EDh	UART1 Transmit/Receive Control Register 1	U1C1	0000 0010b
0002EEh	UART1 Receive Buffer Register	U1RB	XXXXh
0002EFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.15 SFR List (15)

Address	Register	Symbol	Reset Value
000380h	A/D0 Register 0	AD00	00XXh
000381h			
000382h	A/D0 Register 1	AD01	00XXh
000383h			
000384h	A/D0 Register 2	AD02	00XXh
000385h			
000386h	A/D0 Register 3	AD03	00XXh
000387h			
000388h	A/D0 Register 4	AD04	00XXh
000389h			
00038Ah	A/D0 Register 5	AD05	00XXh
00038Bh			
00038Ch	A/D0 Register 6	AD06	00XXh
00038Dh			
00038Eh	A/D0 Register 7	AD07	00XXh
00038Fh			
000390h			
000391h			
000392h	A/D0 Control Register 4	AD0CON4	XXXX 00XXb
000393h			
000394h	A/D0 Control Register 2	AD0CON2	XX0X X000b
000395h	A/D0 Control Register 3	AD0CON3	XXXX X000b
000396h	A/D0 Control Register 0	AD0CON0	00h
000397h	A/D0 Control Register 1	AD0CON1	00h
000398h	D/A Register 0	DA0	XXh
000399h			
00039Ah	D/A Register 1	DA1	XXh
00039Bh			
00039Ch	D/A Control Register	DACON	XXXX XX00b
00039Dh			
00039Eh			
00039Fh			
0003A0h			
0003A1h			
0003A2h			
0003A3h			
0003A4h			
0003A5h			
0003A6h			
0003A7h			
0003A8h			
0003A9h			
0003AAh			
0003ABh			
0003ACh			
0003ADh			
0003AEh			
0003AFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.16 SFR List (16)

Address	Register	Symbol	Reset Value
0003B0h			
0003B1h			
0003B2h			
0003B3h			
0003B4h			
0003B5h			
0003B6h			
0003B7h			
0003B8h			
0003B9h			
0003BAh			
0003BBh			
0003BCh			
0003BDh			
0003BEh			
0003BFh			
0003C0h	Port P0 Register	P0	XXh
0003C1h	Port P1 Register	P1	XXh
0003C2h	Port P0 Direction Register	PD0	0000 0000b
0003C3h	Port P1 Direction Register	PD1	0000 0000b
0003C4h	Port P2 Register	P2	XXh
0003C5h	Port P3 Register	P3	XXh
0003C6h	Port P2 Direction Register	PD2	0000 0000b
0003C7h	Port P3 Direction Register	PD3	0000 0000b
0003C8h	Port P4 Register	P4	XXh
0003C9h	Port P5 Register	P5	XXh
0003CAh	Port P4 Direction Register	PD4	0000 0000b
0003CBh	Port P5 Direction Register	PD5	0000 0000b
0003CCh	Port P6 Register	P6	XXh
0003CDh	Port P7 Register	P7	XXh
0003CEh	Port P6 Direction Register	PD6	0000 0000b
0003CFh	Port P7 Direction Register	PD7	0000 0000b
0003D0h	Port P8 Register	P8	XXh
0003D1h	Port P9 Register	P9	XXh
0003D2h	Port P8 Direction Register	PD8	00X0 0000b
0003D3h	Port P9 Direction Register	PD9	0000 0000b
0003D4h	Port P10 Register	P10	XXh
0003D5h			
0003D6h	Port P10 Direction Register	PD10	0000 0000b
0003D7h			
0003D8h			
0003D9h			
0003DAh			
0003DBh			
0003DCh			
0003DDh			
0003DEh			
0003DFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.24 SFR List (24)

Address	Register	Symbol	Reset Value
044060h			
044061h			
044062h			
044063h			
044064h			
044065h			
044066h			
044067h			
044068h			
044069h			
04406Ah			
04406Bh			
04406Ch			
04406Dh	External Interrupt Request Source Select Register 1	IFSR1	X0XX XXXXb
04406Eh			
04406Fh	External Interrupt Request Source Select Register 0	IFSR0	0000 0000b
044070h	DMA0 Request Source Select Register 2	DM0SL2	XX00 0000b
044071h	DMA1 Request Source Select Register 2	DM1SL2	XX00 0000b
044072h	DMA2 Request Source Select Register 2	DM2SL2	XX00 0000b
044073h	DMA3 Request Source Select Register 2	DM3SL2	XX00 0000b
044074h			
044075h			
044076h			
044077h			
044078h	DMA0 Request Source Select Register	DM0SL	XXX0 0000b
044079h	DMA1 Request Source Select Register	DM1SL	XXX0 0000b
04407Ah	DMA2 Request Source Select Register	DM2SL	XXX0 0000b
04407Bh	DMA3 Request Source Select Register	DM3SL	XXX0 0000b
04407Ch			
04407Dh	Wake-up IPL Setting Register 2	RIPL2	XX0X 0000b
04407Eh			
04407Fh	Wake-up IPL Setting Register 1	RIPL1	XX0X 0000b
044080h			
044081h			
044082h			
044083h			
044084h			
044085h			
044086h			
044087h			
044088h			
044089h			
04408Ah			
04408Bh			
04408Ch			
04408Dh			
04408Eh			
04408Fh			

X: Undefined
Blanks are reserved. No access is allowed.

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings (1)

Symbol	Characteristic		Condition	Value (2)	Unit
V_{CC1}, V_{CC2}	Supply voltage		V_{CC1} = AV_{CC}	-0.3 to 6.0	V
V_{CC2}	Supply voltage		—	-0.3 to V_{CC1}	V
AV_{CC}	Analog supply voltage		V_{CC1} = AV_{CC}	-0.3 to 6.0	V
V_I	Input voltage	XIN, $\overline{\text{RESET}}$, CNVSS, NSD, V_{REF}, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_7, P9_1, P9_3 to P9_7, P10_0 to P10_7 (3)		-0.3 to V_{CC1} + 0.3	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7 (3)		-0.3 to V_{CC2} + 0.3	V
		P7_0, P7_1		-0.3 to 6.0	V
V_O	Output voltage	XOUT, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_3 to P9_7, P10_0 to P10_7 (3)		-0.3 to V_{CC1} + 0.3	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7 (3)		-0.3 to V_{CC2} + 0.3	V
		P7_0, P7_1		-0.3 to 6.0	V
P_d	Power consumption		T_a = 25°C	500	mW
—	Operating temperature range			-40 to 85	°C
T_{stg}	Storage temperature range			-65 to 150	°C

Notes:
1. Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The V_{CC2} pin is available in the 100-pin package only. It should be considered as V_{CC1} in the 64-pin package.
3. Ports P0_4 to P0_7, P1_0 to P1_4, P3_4 to P3_7, P4, P5, P9_1, and P9_4 to P9_7 are available in the 100-pin package only.

Table 5.6 Operating Conditions (5/5)

(V_{CC1} = V_{CC2} = 3.0 to 5.5 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted) (1)

Symbol	Characteristic		Value			Unit
			Min.	Typ.	Max.	
$V_{r(VCC1)}$	Allowable ripple voltage	V_{CC1} = 5.0 V			0.5	Vp-p
		V_{CC1} = 3.0 V			0.3	Vp-p
$V_{r(VCC2)}$	Allowable ripple voltage	V_{CC2} = 5.0 V			0.5	Vp-p
		V_{CC2} = 3.0 V			0.3	Vp-p
$dV_{r(VCC1)}/dt$	Ripple voltage gradient	V_{CC1} = 5.0 V			±0.3	V/ms
		V_{CC1} = 3.0 V			±0.3	V/ms
$dV_{r(VCC2)}/dt$	Ripple voltage gradient	V_{CC2} = 5.0 V			±0.3	V/ms
		V_{CC2} = 3.0 V			±0.3	V/ms
$f_{r(VCC1)}$	Allowable ripple frequency				10	kHz
$f_{r(VCC2)}$	Allowable ripple frequency				10	kHz

Note:
1. The device is operationally guaranteed under these operating conditions.

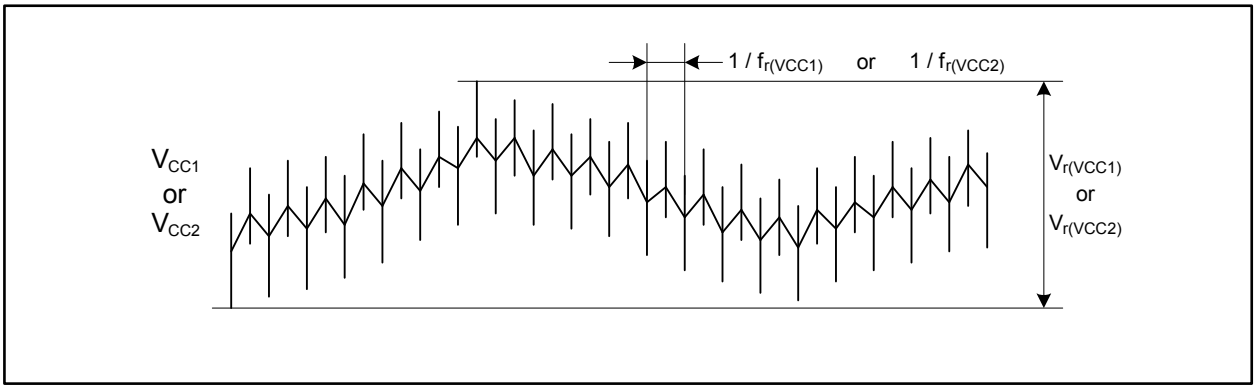


Figure 5.2 Ripple Waveform

$V_{CC1} = V_{CC2} = 5\ V$

Timing Requirements ($V_{CC1} = V_{CC2} = 4.2$ to 5.5 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.27 Timer B Input (counting input in event counter mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input clock cycle time (one edge counting)	200		ns
$t_{w(TBH)}$	TBiIN input high level pulse width (one edge counting)	80		ns
$t_{w(TBL)}$	TBiIN input low level pulse width (one edge counting)	80		ns
$t_{c(TB)}$	TBiIN input clock cycle time (both edges counting)	200		ns
$t_{w(TBH)}$	TBiIN input high level pulse width (both edges counting)	80		ns
$t_{w(TBL)}$	TBiIN input low level pulse width (both edges counting)	80		ns

Table 5.28 Timer B Input (pulse period measure mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input clock cycle time	400		ns
$t_{w(TBH)}$	TBiIN input high level pulse width	180		ns
$t_{w(TBL)}$	TBiIN input low level pulse width	180		ns

Table 5.29 Timer B Input (pulse-width measure mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input clock cycle time	400		ns
$t_{w(TBH)}$	TBiIN input high level pulse width	180		ns
$t_{w(TBL)}$	TBiIN input low level pulse width	180		ns

$V_{CC1} = V_{CC2} = 3.3$ V

Switching Characteristics ($V_{CC1} = V_{CC2} = 3.0$ to 3.6 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.59 Serial Interface

Symbol	Characteristic	Measurement Condition	Value		Unit
			Min.	Max.	
$t_{d(C-Q)}$	TXDi output delay time	Refer to Figure 5.6		80	ns
$t_{h(C-Q)}$	TXDi output hold time		0		ns

Table 5.60 Intelligent I/O

Symbol	Characteristic	Measurement Condition	Value		Unit
			Min.	Max.	
$t_{d(ISCLK2-TXD)}$	ISTXD2 output delay time	Refer to Figure 5.6		180	ns
$t_{h(ISCLK2-RXD)}$	ISTXD2 output hold time		0		ns

Rev.	Date	Description	
		Page	Summary
		37, 38	• Changed register names associated with “Start/Stop Condition” for BCNiIC in **Tables 4.2 and 4.3**, to “Start Condition/Stop Condition”
		45	• Modified reset values “XXXX XXXXb” and “XXXX 000Xb” for registers U7RB and U8RB in **Table 4.10**, to “XXXXh”
		46	• Changed expression of register name “Xi Register Yi Register” (i = 0 to 15) and register symbol “XiR, YiR” in **Table 4.11**, to “Xi Register/Yi Register” and “XiR/YiR”, respectively
		51	• Changed hexadecimal format of reset values for PDi in **Table 4.16**, to binary
		54	• Modified Note 1 in **Table 4.19**
		55	• Merged addresses 40090h to 40093h in **Table 4.20**, into previous page • Modified reset values for IFS0 and IFS2 in **Table 4.20**; Added Notes 1 to 3 for 80-/64-pin packages and IFS7 register
		55-57	• Modified the following register name in **Tables 4.20 to 4.22**: “Port Pi_j Port Function Select Register”, to “Port Pi_j Function Select Register”
		59	• Modified register name “DMAi Request Source Select Register 1” in **Table 4.24**, to “DMAi Request Source Select Register” • Changed register names “Wake-up Interrupt Priority Level Control Register 2” and “Wake-up Interrupt Priority Level Control Register 1” in **Table 4.24**, to “Wake-up IPL Setting Register 2” and “Wake-up IPL Setting Register 1”, respectively
			Chapter 5. Electrical Characteristics
		60	• Added Notes 2 and 3 for 80-/64-pin packages to **Table 5.1**
		61	• Added specification of “dV_{CC1}/dt” to **Table 5.2**; Added Notes 2, 4, and 5 for 80-/64-pin packages
		62	• Added Note 2 for **Table 5.3**
		63	• Added Note 3 for 80-/64-pin packages to **Table 5.4**
		65	• Modified description “V_{CC}”s in **Table 5.6**, to “V_{CC1}”s and “V_{CC2}”s
		66	• Added **Table 5.7** to provide RAM electrical characteristics • Deleted specification of “t_{PS}” from **Table 5.8**
		67	• Deleted measurement condition for power supply circuit timing characteristics in **Table 5.9** • Added “Supply voltage for internal logic” to **Figure 5.3** and deleted “CPU clock” from the figure • Changed voltage condition for **Table 5.11**, from “V_{CC1} = V_{CC2} = 3.3 to 5.5 V” to “V_{CC1} = V_{CC2} = 4.2 to 5.5 V”; Clarified maximum value for “ΔVdet” in **Table 5.11**; Modified self-consuming current “V_{CC}”, to “V_{CC1}”
		68	• Changed typical value and maximum value for $f_{SO(PLL)}$ in **Table 5.12**, to “55” and “80” respectively • Changed the following expressions: “PLL frequency synthesizer stabilization time” in **Table 5.12**, to “PLL lock time” and “$t_{OSC(PLL)}$”, to “$t_{LOCK(PLL)}$” • Modified description for Note1 of **Table 5.13**

Rev.	Date	Description	
		Page	Summary
		70, 82	• Added Notes 1 and 2 for 80-/64-pin packages to **Tables 5.15 and 5.38**
		71, 83	• Deleted ports P7_0, P7_1, and P8_5 for R_{PULLUP} from **Tables 5.16 and 5.39**; Added Notes 1 and 2 for 80-/64-pin packages
		72, 84	• Added "XIN" as "Active" to first, third, and sixth rows of **Tables 5.17 and 5.40** • Deleted specification of ICC under condition "Ta = 85°C" from **Tables 5.17 and 5.40**
		73, 85	• Modified minimum value "0.125" for ϕ_{AD} in **Tables 5.18 and 5.41**, to "0.25"; Added Note 1 for 80-/64-pin packages
		75, 87	• Clarified three "TBD"s for external bus timing in **Tables 5.21 and 5.44**
		78	• Corrected a typo "$t_{h(C-Q)}$" in **Table 5.30**, to "$t_{h(C-D)}$"
		78, 90	• Modified maximum value for $t_{h(C-D)}$ "30" in **Tables 5.30 and 5.53**, to "80" • Modified minimum value for $t_{w(ADH)}$ in **Tables 5.31 and 5.54**, to "$\frac{3}{\phi_{AD}}$" • Added **Tables 5.33 and 5.56** to provide intelligent I/O timing requirements
		79, 91	• Changed the third formula of Note 1 in **Tables 5.34 and 5.57**
		80, 92	• Modified minimum value of $t_{h(W-D)}$ "0" in **Tables 5.35 and 5.58**, to "0.5 x $t_{c(Base)}$"; Changed the first formula of Note 1
		81, 93	• Modified "Characteristic" for $t_{h(C-Q)}$ in **Tables 5.36 and 5.59**, from "TXDi hold time" to "TXDi output hold time" • Added **Tables 5.37 and 5.60** to provide intelligent switching characteristics
		83	• Changed measurement condition for "High level input current" in **Table 5.39**, from "V_I = 3 V" to "V_I = 3.3 V"
		85	• Added a skipped word "error" after "Differential non-linearity" in **Table 5.41**
		87	• Corrected typos "$t_{w(H)}$," "$t_{w(L)}$", "t_r", and "t_f" in **Table 5.43**, to "$t_{w(XH)}$", "$t_{w(XL)}$", "$t_{r(X)}$", and "$t_{f(X)}$", respectively
		95	• Changed D15 to D0 output period of write cycle in **Figures 5.8**
		96	• Changed D15 to D8 output period of write cycle in **Figures 5.9**
			Appendix 1
		98, 99	• Added figures for 100-pin plastic molded LGA, and 80-/64-pin plastic molded LQFP packages
1.20	Sep 26, 2011	—	Fourth edition released
		—	The manual in general • Applied new Renesas templates and formats to the manual • Changed company name to "Renesas Electronics Corporation" and changed related descriptions due to business merger of Renesas Technology Corporation and NEC Electronics Corporation • Modified expressions "version N" and "version D" to "N version" and "D version", respectively (under Chapters 1 and 5)
			Chapter 1. Overview
		—	• Modified wording and enhanced description in this chapter

Revision History	R32C/111 Group Datasheet

Rev.	Date	Description	
		Page	Summary
		66	• Changed expression “Programming and erasure endurance” in **Table 5.8** to “Program and erase cycles”; Changed its unit “times” in the table and Note 1 to “Cycles”
		68	• Changed order of descriptions of “$t_{rec(STOP)}$” and “$t_{rec(WAIT)}$” in **Table 5.13 and Figure 5.4**
		69	• Changed expressions “$\overline{CS0}$” and “A23 to A0, $\overline{BC0}$ to $\overline{BC3}$” in **Figure 5.5** to “Chip select” and “Address”, respectively
		78, 90	• Corrected “INTi” in title of **Tables 5.32 and 5.55** to “$\overline{INTi}$”
		81, 93	• Added measurement condition to **Tables 5.37 and 5.60**
			Appendix 1. Package Dimensions
		98-99	• Added a seating plane to the drawing of package dimension
1.30	Mar 3, 2014	—	Fifth edition released
		—	• Deleted description for the 80-pin package
			Chapter 1. Overview
		—	• Modified wording and enhanced description in this chapter
		1	• Modified expression “I^2C” in line 9 of **1.1** to “I^2C-bus interface”
		2, 4	• Modified expressions “calculation transfer” and “chained transfer” in **Tables 1.1 and 1.3** to “calculation result transfer” and “chain transfer”, respectively
		5	• Deleted N version from the Operating Temperature row in **Table 1.4**
		6	• Deleted products on planning phase from **Table 1.5**
		20, 23	• Modified expression “I^2C bus” in **Tables 1.13 and 1.16** to “I^2C-bus”
			Chapter 2. CPU
		—	• Modified wording and enhanced description in this chapter
			Chapter 5. Electrical Characteristics
		—	• Modified wording and enhanced description in this chapter
		65, 77	• Deleted TXD4, STXD4, and $\overline{RTS4}$ from **Tables 5.16 and 5.39**
		66, 78	• Modified description “Drive power” in **Tables 5.17 and 5.40** to “Drive strength”