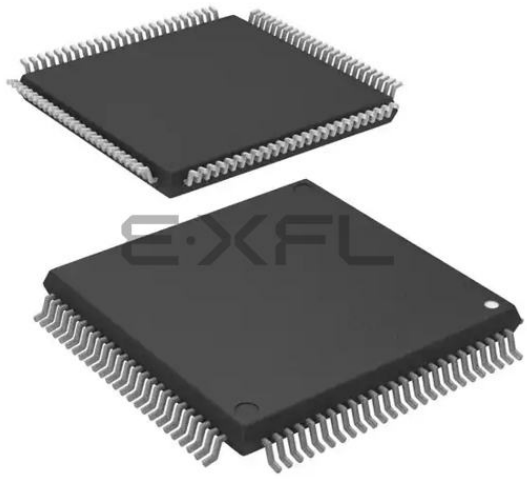
Renesas Electronics America Inc - R5F64115DFB#U0 Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	R32C/100
Core Size	16/32-Bit
Speed	50MHz
Connectivity	EBI/EMI, I²C, IEBus, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	82
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	40K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f64115dfb-u0

1.1.2 Performance Overview

Tables 1.1 to 1.4 show the performance overview of the R32C/111 Group.

Table 1.1 Performance Overview for the 100-pin Package (1/2)

Unit	Function	Explanation
CPU	Central processing unit	R32C/100 Series CPU Core • Basic instructions: 108 • Minimum instruction execution time: 20 ns (f(CPU) = 50 MHz) • Multiplier: 32-bit × 32-bit → 64-bit • Multiply-accumulate unit: 32-bit × 32-bit + 64-bit → 64-bit • IEEE-754 compatible FPU: Single precision • 32-bit barrel shifter • Operating mode: Single-chip mode, memory expansion mode, microprocessor mode (optional (1))
Memory		Flash memory: 256 to 512 Kbytes RAM: 32 to 63 Kbytes Data flash: 4 Kbytes × 2 blocks Refer to Table 1.5 for memory size of each product group
Voltage Detector	Low voltage detector	Optional (1) Low voltage detection interrupt
Clock	Clock generator	• 4 circuits (main clock, sub clock, PLL, on-chip oscillator) • Oscillation stop detector: Main clock oscillator stop/restart detection • Frequency divide circuit: Divide-by-2 to divide-by-24 selectable • Low power modes: Wait mode, stop mode
External Bus Expansion	Bus and memory expansion	• Address space: 4 Gbytes (of which up to 64 Mbytes is user accessible) • External bus Interface: Support for wait-state insertion, 4 chip select outputs, 3V/5V interface • Bus format: Separate bus/Multiplexed bus selectable, data bus width selectable (8/16 bits)
Interrupts		Interrupt vectors: 261 External interrupt inputs: $\overline{\text{NMI}}$, $\overline{\text{INT}}$ × 6, key input × 4 Interrupt priority levels: 7
Watchdog Timer		15 bits × 1 (selectable input frequency from prescaler output)
DMA	DMAC	4 channels • Cycle-steal transfer mode • Request sources: 51 • 2 transfer modes: Single transfer, repeat transfer
	DMAC II	• Triggered by an interrupt request of any peripheral • 3 characteristic transfer functions: Immediate data transfer, calculation result transfer, chain transfer
I/O Ports	Programmable I/O ports	• 2 input-only ports • 82 CMOS I/O ports • 2 N-channel open drain ports • A pull-up resistor is selectable for every 4 input ports

Note:
1. Contact a Renesas Electronics sales office to use the optional features.

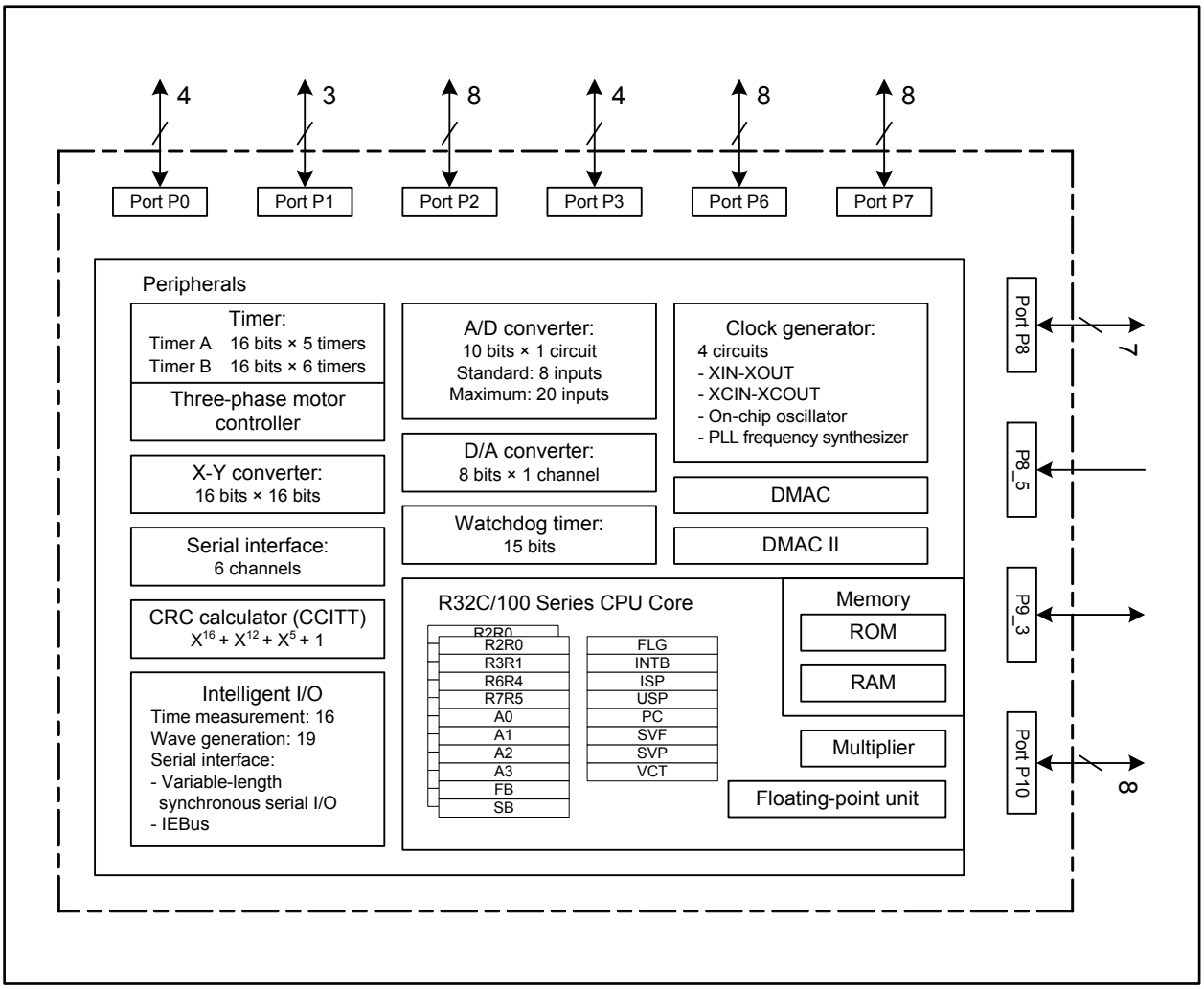
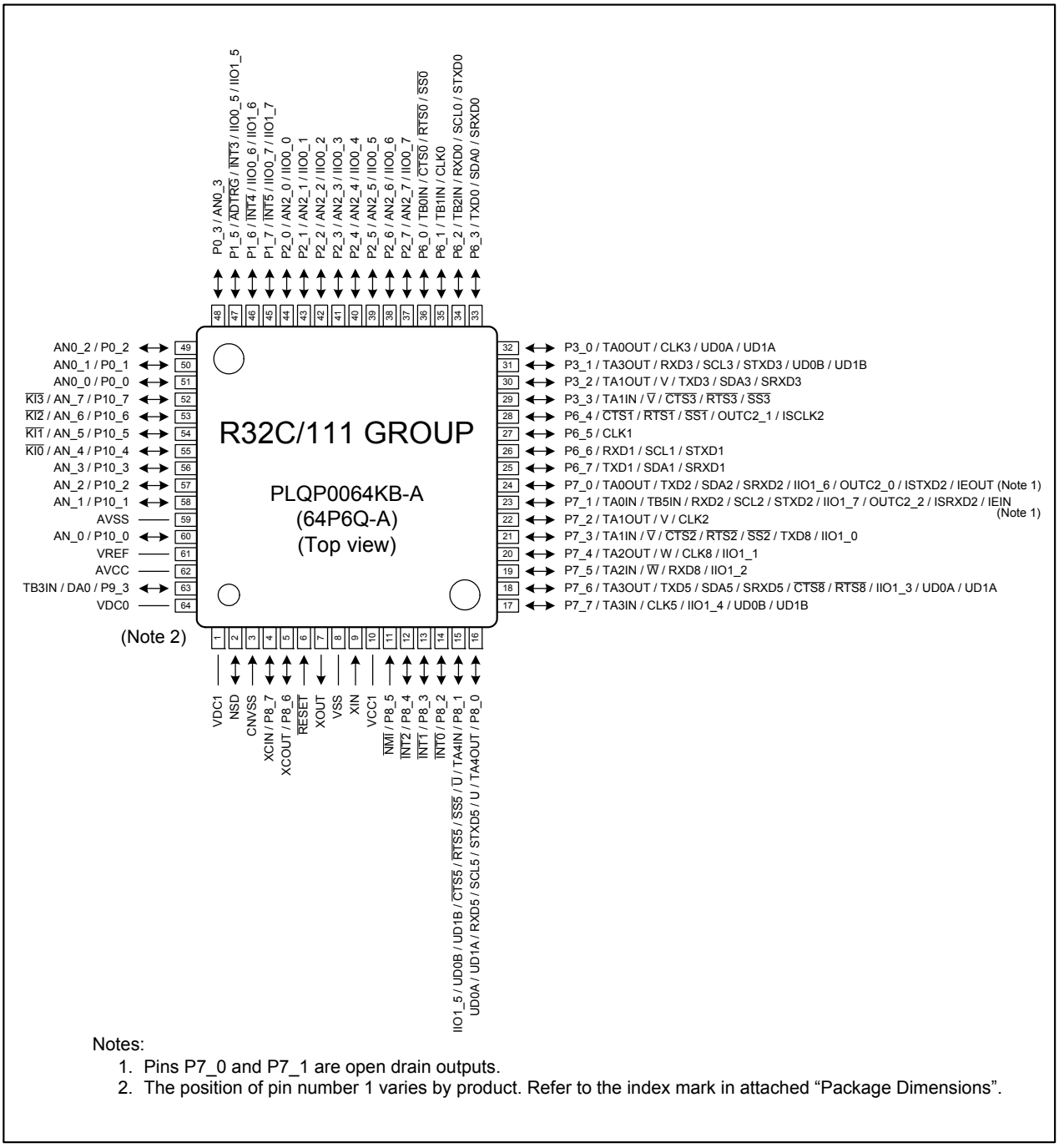


Figure 1.3 R32C/111 Group Block Diagram for the 64-pin Package

Table 1.6 Pin Characteristics for the 100-pin Package (1/3)

Pin No.		Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
QFP	LGA								
1	A1		P9_4		TB4IN	CTS4/RTS4/SS4		DA1	
2	E4		P9_3		TB3IN			DA0	
3	B1	VDC0							
4	D3		P9_1						
5	C2	VDC1							
6	C1	NSD							
7	D2	CNVSS							
8	D1	XCIN	P8_7						
9	E3	XCOUT	P8_6						
10	E2	RESET							
11	E1	XOUT							
12	F3	VSS							
13	F2	XIN							
14	F1	VCC1							
15	G2		P8_5	NMI					
16	F5		P8_4	INT2					
17	G3		P8_3	INT1					
18	G1		P8_2	INT0					
19	F4		P8_1		TA4IN/U	CTS5/RTS5/SS5	IIO1_5/UD0B/UD1B		
20	H1		P8_0		TA4OUT/U	RXD5/SCL5/STXD5	UD0A/UD1A		
21	H2		P7_7		TA3IN	CLK5	IIO1_4/UD0B/UD1B		
22	G4		P7_6		TA3OUT	TXD5/SDA5/ SRXD5/CTS8/RTS8	IIO1_3/UD0A/UD1A		
23	H3		P7_5		TA2IN/W	RXD8	IIO1_2		
24	J1		P7_4		TA2OUT/W	CLK8	IIO1_1		
25	J2		P7_3		TA1IN/V	CTS2/RTS2/SS2/ TXD8	IIO1_0		
26	K1		P7_2		TA1OUT/V	CLK2			
27	K2		P7_1		TA0IN/ TB5IN	RXD2/SCL2/STXD2	IIO1_7/OUTC2_2/ ISRXD2/IEIN		
28	J3		P7_0		TA0OUT	TXD2/SDA2/SRXD2	IIO1_6/OUTC2_0/ ISTXD2/IEOUT		
29	H4		P6_7			TXD1/SDA1/SRXD1			
30	K3		P6_6			RXD1/SCL1/STXD1			
31	G5		P6_5			CLK1			
32	J4		P6_4			CTS1/RTS1/SS1	OUTC2_1/ISCLK2		
33	K4		P6_3			TXD0/SDA0/SRXD0			
34	H5		P6_2		TB2IN	RXD0/SCL0/STXD0			
35	J5		P6_1		TB1IN	CLK0			
36	K5		P6_0		TB0IN	CTS0/RTS0/SS0			
37	G6		P5_7			CTS7/RTS7			RDY/CS3
38	H6		P5_6			RXD7			ALE/CS2
39	J6		P5_5			CLK7			HOLD



Notes:
1. Pins P7_0 and P7_1 are open drain outputs.
2. The position of pin number 1 varies by product. Refer to the index mark in attached “Package Dimensions”.

Figure 1.6 Pin Assignment for the 64-pin Package (top view)

2.1.8.5 Register Bank Select Flag (B flag)

This flag selects a register bank. It indicates 0 when register bank 0 is selected, and 1 when register bank 1 is selected.

2.1.8.6 Overflow Flag (O flag)

This flag becomes 1 when the result of an operation overflows; otherwise it is 0.

2.1.8.7 Interrupt Enable Flag (I flag)

This flag enables maskable interrupts. To disable maskable interrupts, set this flag to 0. To enable them, set this flag to 1. When an interrupt is accepted, the flag becomes 0.

2.1.8.8 Stack Pointer Select Flag (U flag)

To select the interrupt stack pointer (ISP), set this flag to 0. To select the user stack pointer (USP), set this flag to 1.
It becomes 0 when a hardware interrupt is accepted or when an INT instruction designated by a software interrupt number from 0 to 127 is executed.

2.1.8.9 Floating-point Underflow Flag (FU flag)

This flag becomes 1 when an underflow occurs in a floating-point operation; otherwise it is 0. It also becomes 1 when the operand contains invalid numbers (subnormal numbers).

2.1.8.10 Floating-point Overflow Flag (FO flag)

This flag becomes 1 when an overflow occurs in a floating-point operation; otherwise it is 0. It also becomes 1 when the operand contains invalid numbers (subnormal numbers).

2.1.8.11 Processor Interrupt Priority Level (IPL)

The processor interrupt priority level (IPL), consisting of 3 bits, selects a processor interrupt priority level from level 0 to 7. An interrupt is enabled when the interrupt request level is higher than the selected IPL.
When the processor interrupt priority level (IPL) is set to 111b (level 7), all interrupts are disabled.

2.1.8.12 Fixed-point Radix Point Designation Bit (DP bit)

This bit designates the radix point. It also specifies which portion of the fixed-point multiplication result to extract. It is used for the MULX instruction.

2.1.8.13 Floating-point Rounding Mode (RND)

The 2-bit floating-point rounding mode selects a rounding mode for floating-point calculation results.

2.1.8.14 Reserved

Only set this bit to 0. The read value is undefined.

3. Memory

Figure 3.1 shows the memory map of the R32C/111 Group.
The R32C/111 Group provides a 4-Gbyte address space from 00000000h to FFFFFFFFh.

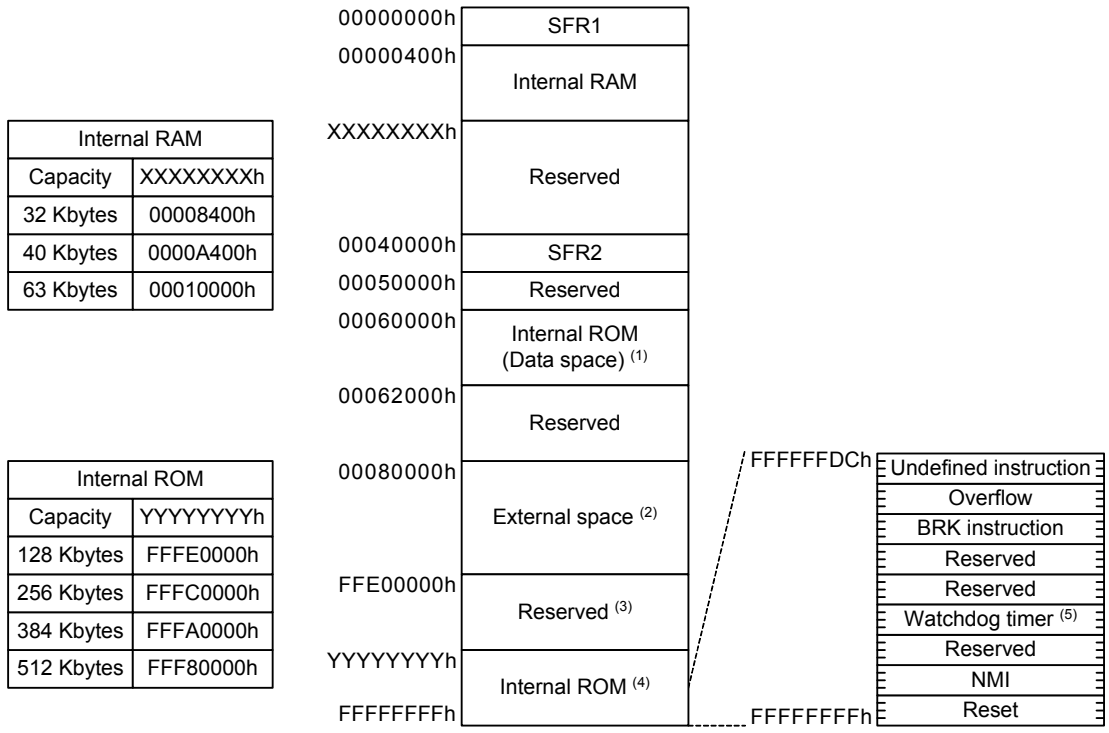
The internal ROM is mapped from address FFFFFFFFh in the inferior direction. For example, the 512-Kbyte internal ROM is mapped from FFF80000h to FFFFFFFFh.
The fixed interrupt vector table contains the start address of interrupt handlers and is mapped from FFFFFFDCh to FFFFFFFFh.
The internal RAM is mapped from address 00000400h in the superior direction. For example, the 63-Kbyte internal RAM is mapped from 00000400h to 0000FFFFh. Besides being used for data storage, the internal RAM functions as a stack(s) for subroutine calls and/or interrupt handlers.

Special function registers (SFRs), which are control registers for peripheral functions, are mapped from 00000000h to 000003FFh, and from 00040000h to 0004FFFFh. Unoccupied SFR locations are reserved, and no access is allowed.

In memory expansion mode or microprocessor mode, some spaces are reserved for internal use and should not be accessed.

Internal RAM	
Capacity	XXXXXXXXh
32 Kbytes	00008400h
40 Kbytes	0000A400h
63 Kbytes	00010000h

Internal ROM	
Capacity	YYYYYYYYh
128 Kbytes	FFFE0000h
256 Kbytes	FFFC0000h
384 Kbytes	FFFA0000h
512 Kbytes	FFF80000h



Notes:
1. The flash memory version provides two additional 4-Kbyte spaces (blocks A and B) for storing data.
2. This space can be used in memory expansion mode or microprocessor mode. Addresses from 02000000h to FDFFFFFFh are inaccessible.
3. This space is reserved in memory expansion mode. It becomes an external space in microprocessor mode.
4. This space can be used in single-chip mode or memory expansion mode. It becomes an external space in microprocessor mode.
5. The watchdog timer interrupt shares a vector with the oscillator stop detection interrupt and low voltage detection interrupt.

Figure 3.1 Memory Map

Table 4.4 SFR List (4)

Address	Register	Symbol	Reset Value
0000B0h	Intelligent I/O Interrupt Enable Register 0	IIO0IE	00h
0000B1h	Intelligent I/O Interrupt Enable Register 1	IIO1IE	00h
0000B2h	Intelligent I/O Interrupt Enable Register 2	IIO2IE	00h
0000B3h	Intelligent I/O Interrupt Enable Register 3	IIO3IE	00h
0000B4h	Intelligent I/O Interrupt Enable Register 4	IIO4IE	00h
0000B5h	Intelligent I/O Interrupt Enable Register 5	IIO5IE	00h
0000B6h	Intelligent I/O Interrupt Enable Register 6	IIO6IE	00h
0000B7h	Intelligent I/O Interrupt Enable Register 7	IIO7IE	00h
0000B8h	Intelligent I/O Interrupt Enable Register 8	IIO8IE	00h
0000B9h	Intelligent I/O Interrupt Enable Register 9	IIO9IE	00h
0000BAh	Intelligent I/O Interrupt Enable Register 10	IIO10IE	00h
0000BBh	Intelligent I/O Interrupt Enable Register 11	IIO11IE	00h
0000BCh			
0000BDh			
0000BEh			
0000BFh			
0000C0h			
0000C1h			
0000C2h			
0000C3h			
0000C4h			
0000C5h			
0000C6h			
0000C7h			
0000C8h			
0000C9h			
0000CAh			
0000CBh			
0000CCh			
0000CDh			
0000CEh			
0000CFh			
0000D0h			
0000D1h			
0000D2h			
0000D3h			
0000D4h			
0000D5h			
0000D6h			
0000D7h			
0000D8h			
0000D9h			
0000DAh			
0000DBh			
0000DCh			
0000DDh	UART7 Transmit Interrupt Control Register	S7TIC	XXXX X000b
0000DEh			
0000DFh	UART8 Transmit Interrupt Control Register	S8TIC	XXXX X000b

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.17 SFR List (17)

Address	Register	Symbol	Reset Value
0003E0h			
0003E1h			
0003E2h			
0003E3h			
0003E4h			
0003E5h			
0003E6h			
0003E7h			
0003E8h			
0003E9h			
0003EAh			
0003EBh			
0003ECh			
0003EDh			
0003EEh			
0003EFh			
0003F0h	Pull-up Control Register 0	PUR0	0000 0000b
0003F1h	Pull-up Control Register 1	PUR1	XXXX 0000b
0003F2h	Pull-up Control Register 2	PUR2	0000 0000b
0003F3h	Pull-up Control Register 3	PUR3	XXXX XX00b
0003F4h			
0003F5h			
0003F6h			
0003F7h			
0003F8h			
0003F9h			
0003FAh			
0003FBh			
0003FCh			
0003FDh			
0003FEh			
0003FFh	Port Control Register	PCR	XXXX XXX0b

X: Undefined
Blanks are reserved. No access is allowed.

Table 5.12 Electrical Characteristics of Oscillator
(V_{CC1} = V_{CC2} = 3.0 to 5.5 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Symbol	Characteristics	Measurement Condition	Value			Unit
			Min.	Typ.	Max.	
$f_{SO(PLL)}$	PLL clock self-oscillation frequency		35	55	80	MHz
$t_{LOCK(PLL)}$	PLL lock time (1)				1	ms
$t_{jitter(p-p)}$	PLL jitter period (p-p)				2.0	ns
$f_{(OCO)}$	On-chip oscillator frequency		62.5	125	250	kHz

Note:
1. This value is applicable only when the main clock oscillation is stable.

Table 5.13 Electrical Characteristics of Clock Circuitry
(V_{CC1} = V_{CC2} = 3.0 to 5.5 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Symbol	Characteristics	Measurement Condition	Value			Unit
			Min.	Typ.	Max.	
$t_{rec(WAIT)}$	Recovery time from wait mode to low power mode				225	µs
$t_{rec(STOP)}$	Recovery time from stop mode (1)				225	µs

Note:
1. The recovery time from stop mode does not include the main clock oscillation stabilization time. The CPU starts operating before the oscillator is stabilized.

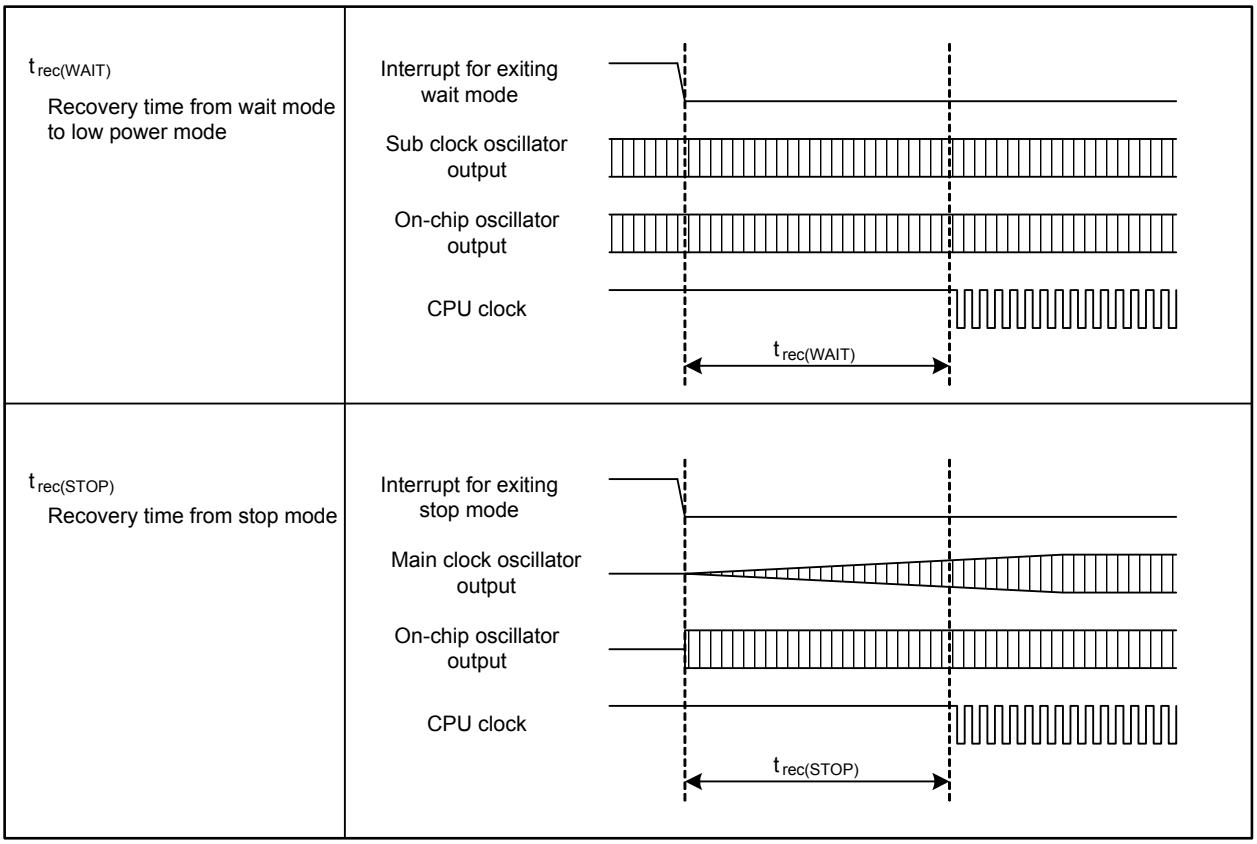


Figure 5.4 Clock Circuit Timing

$V_{CC1} = V_{CC2} = 5\ V$

Table 5.16 Electrical Characteristics (2/3)
($V_{CC1} = V_{CC2} = 4.2$ to 5.5 V, $V_{SS} = 0$ V, $T_a = T_{opr}$, and $f_{(CPU)} = 50$ MHz, unless otherwise noted)

Symbol	Characteristic		Measurement Condition	Value			Unit
				Min.	Typ.	Max.	
$V_{T+} - V_{T-}$	Hysteresis	HOLD, RDY, NMI, INT0 to INT5, KI0 to KI3, TA0IN to TA4IN, TA0OUT to TA4OUT, TB0IN to TB5IN, CTS0 to CTS8, CLK0 to CLK8, RXD0 to RXD8, SCL0 to SCL6, SDA0 to SDA6, SS0 to SS6, SRXD0 to SRXD6, ADTRG, IIO0_0 to IIO0_7, IIO1_0 to IIO1_7, UD0A, UD0B, UD1A, UD1B, ISCLK2, ISRXD2, IEIN (1)		0.2		1.0	V
		RESET		0.2		1.8	V
I_{IH}	High level input current	XIN, RESET, CNVSS, NSD, P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_1, P9_3 to P9_7, P10_0 to P10_7 (2)	$V_I = 5$ V			5.0	µA
I_{IL}	Low level input current	XIN, RESET, CNVSS, NSD, P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_1, P9_3 to P9_7, P10_0 to P10_7 (2)	$V_I = 0$ V			-5.0	µA
R_{PULLUP}	Pull-up resistor	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_1, P9_3 to P9_7, P10_0 to P10_7 (2)	$V_I = 0$ V	30	50	170	kΩ
R_{fXIN}	Feedback resistor	XIN			1.5		MΩ
R_{fXCIN}	Feedback resistor	XCIN			15		MΩ

Notes:
1. Pins TB4IN, CTS4, CLK4, RXD4, SCL4, SDA4, SS4, SRXD4, and UART6, and UART7 are available in the 100-pin package only.
2. Ports P0_4 to P0_7, P1_0 to P1_4, P3_4 to P3_7, P4, P5, P9_1, and P9_4 to P9_7 are available in the 100-pin package only.

$V_{CC1} = V_{CC2} = 5$ V

Timing Requirements ($V_{CC1} = V_{CC2} = 4.2$ to 5.5 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.30 Serial Interface

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input clock cycle time	200		ns
$t_{w(CKH)}$	CLKi input high level pulse width	80		ns
$t_{w(CKL)}$	CLKi input low level pulse width	80		ns
$t_{su(D-C)}$	RXDi input setup time	80		ns
$t_{h(C-D)}$	RXDi input hold time	90		ns

Table 5.31 A/D Trigger Input

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{w(ADH)}$	$\overline{\text{ADTRG}}$ input high level pulse width Hardware trigger input high level pulse width	$\frac{3}{\phi_{AD}}$		ns
$t_{w(ADL)}$	$\overline{\text{ADTRG}}$ input low level pulse width Hardware trigger input high level pulse width	125		ns

Table 5.32 External Interrupt $\overline{\text{INTi}}$ Input

Symbol	Characteristic		Value		Unit
			Min.	Max.	
$t_{w(INH)}$	$\overline{\text{INTi}}$ input high level pulse width	Edge sensitive	250		ns
		Level sensitive	$t_{c(CPU)}$ + 200		ns
$t_{w(INL)}$	$\overline{\text{INTi}}$ input low level pulse width	Edge sensitive	250		ns
		Level sensitive	$t_{c(CPU)}$ + 200		ns

Table 5.33 Intelligent I/O

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(ISCLK2)}$	ISCLK2 input clock cycle time	600		ns
$t_{w(ISCLK2H)}$	ISCLK2 input high level pulse width	270		ns
$t_{w(ISCLK2L)}$	ISCLK2 input low level pulse width	270		ns
$t_{su(RXD-ISCLK2)}$	ISRXD2 input setup time	150		ns
$t_{h(ISCLK2-RXD)}$	ISRXD2 input hold time	100		ns

$V_{CC1} = V_{CC2} = 3.3$ V

Table 5.41 A/D Conversion Characteristics ($V_{CC1} = V_{CC2} = AV_{CC} = V_{REF} = 3.0$ to 3.6 V, $V_{SS} = AV_{SS} = 0$ V, $T_a = T_{opr}$, and $f_{(BCLK)} = 25$ MHz, unless otherwise noted)

Symbol	Characteristic	Measurement Condition		Value			Unit
				Min.	Typ.	Max.	
—	Resolution	$V_{REF} = V_{CC1}$				10	Bits
—	Absolute error	$V_{REF} = V_{CC1} = V_{CC2} = 3.3$ V	AN_0 to AN_7, AN0_0 to AN0_7, AN2_0 to AN2_7, ANEX0, ANEX1 (1)			±5	LSB
			External op-amp connection mode			±7	LSB
INL	Integral non-linearity error	$V_{REF} = V_{CC1} = V_{CC2} = 3.3$ V	AN_0 to AN_7, AN0_0 to AN0_7, AN2_0 to AN2_7, ANEX0, ANEX1 (1)			±5	LSB
			External op-amp connection mode			±7	LSB
DNL	Differential non-linearity error	$V_{REF} = V_{CC1} = V_{CC2} = 3.3$ V				±1	LSB
—	Offset error					±3	LSB
—	Gain error					±3	LSB
R_{LADDER}	Resistor ladder	$V_{REF} = V_{CC1}$		4		20	kΩ
t_{CONV}	Conversion time (10 bits)	ϕ_{AD} = 10 MHz, with sample and hold function		3.3			µs
t_{CONV}	Conversion time (8 bits)	ϕ_{AD} = 10 MHz, with sample and hold function		2.8			µs
t_{SAMP}	Sampling time	ϕ_{AD} = 10 MHz		0.3			µs
V_{IA}	Analog input voltage			0		V_{REF}	V
ϕ_{AD}	Operating clock frequency	Without sample and hold function		0.25		10	MHz
		With sample and hold function		1		10	MHz

Note:
1. Pins AN0_4 to AN0_7, ANEX0, and ANEX1 are available in the 100-pin package only.

$V_{CC1} = V_{CC2} = 3.3$ V

Timing Requirements ($V_{CC1} = V_{CC2} = 3.0$ to 3.6 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.43 External Clock Input

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(X)}$	External clock input period	62.5	250	ns
$t_{w(XH)}$	External clock input high level pulse width	25		ns
$t_{w(XL)}$	External clock input low level pulse width	25		ns
$t_{r(X)}$	External clock input rise time		5	ns
$t_{f(X)}$	External clock input fall time		5	ns
t_w / t_c	External clock input duty	40	60	%

Table 5.44 External Bus Timing

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{su(D-R)}$	Data setup time before read	40		ns
$t_{h(R-D)}$	Data hold time after read	0		ns
$t_{dis(R-D)}$	Data disable time after read		$0.5 \times t_{c(Base)} + 10$	ns

V_{CC1} = V_{CC2} = 3.3 V

Switching Characteristics (V_{CC1} = V_{CC2} = 3.0 to 3.6 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Table 5.57 External Bus Timing (separate bus)

Symbol	Characteristic	Measurement Condition	Value		Unit
			Min.	Max.	
$t_{su(S-R)}$	Chip-select setup time before read	Refer to Figure 5.6	(1)		ns
$t_{h(R-S)}$	Chip-select hold time after read		$t_{c(Base)}$ - 10		ns
$t_{su(A-R)}$	Address setup time before read		(1)		ns
$t_{h(R-A)}$	Address hold time after read		$t_{c(Base)}$ - 10		ns
$t_{w(R)}$	Read pulse width		(1)		ns
$t_{su(S-W)}$	Chip-select setup time before write		(1)		ns
$t_{h(W-S)}$	Chip-select hold time after write		1.5 × $t_{c(Base)}$ - 10		ns
$t_{su(A-W)}$	Address setup time before write		(1)		ns
$t_{h(W-A)}$	Address hold time after write		1.5 × $t_{c(Base)}$ - 10		ns
$t_{w(W)}$	Write pulse width		(1)		ns
$t_{su(D-W)}$	Data setup time before write		(1)		ns
$t_{h(W-D)}$	Data hold time after write		0		ns

Note:

1. The value is calculated using the formulas below based on the base clock cycles ($t_{c(Base)}$) and respective cycles of Tsu(A-R), Tw(R), Tsu(A-W), and Tw(W) set by registers EBC0 to EBC3. If the calculation results in a negative value, modify the value to be set. For details on how to set values, refer to the User's manual.

   $t_{su(S-R)}$ = $t_{su(A-R)}$ = Tsu(A-R) × $t_{c(Base)}$ - 15 [ns]

   $t_{w(R)}$ = Tw(R) × $t_{c(Base)}$ - 10 [ns]

   $t_{su(S-W)}$ = $t_{su(A-W)}$ = Tsu(A-W) × $t_{c(Base)}$ - 15 [ns]

   $t_{w(W)}$ = $t_{su(D-W)}$ = Tw(W) × $t_{c(Base)}$ - 10 [ns]

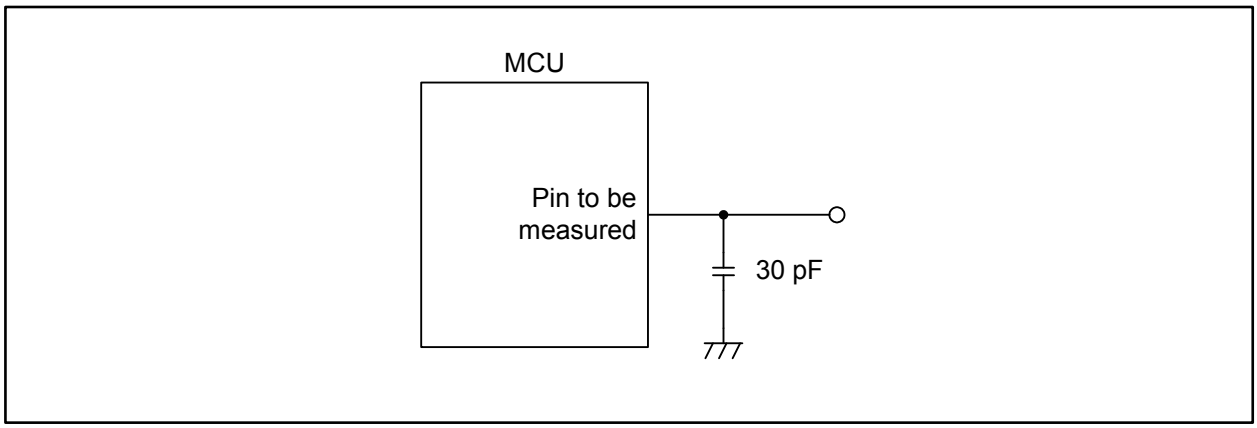


Figure 5.6 Switching Characteristic Measurement Circuit

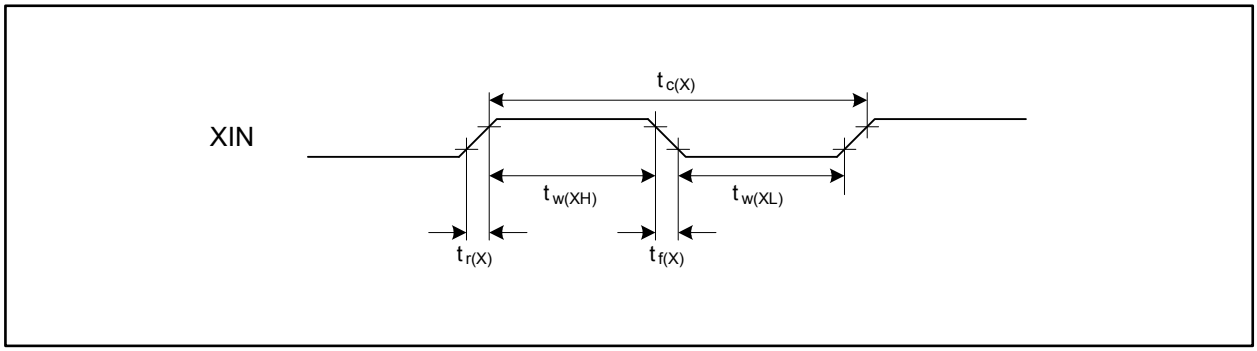
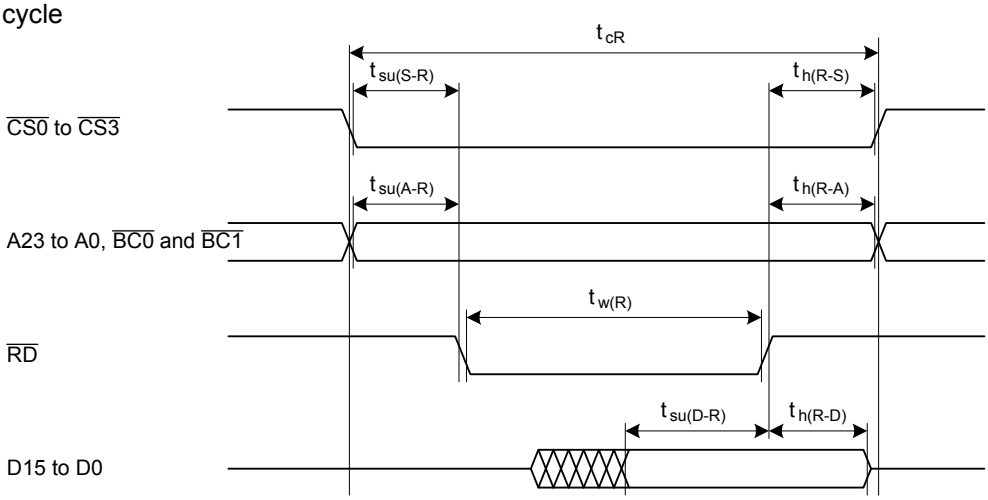


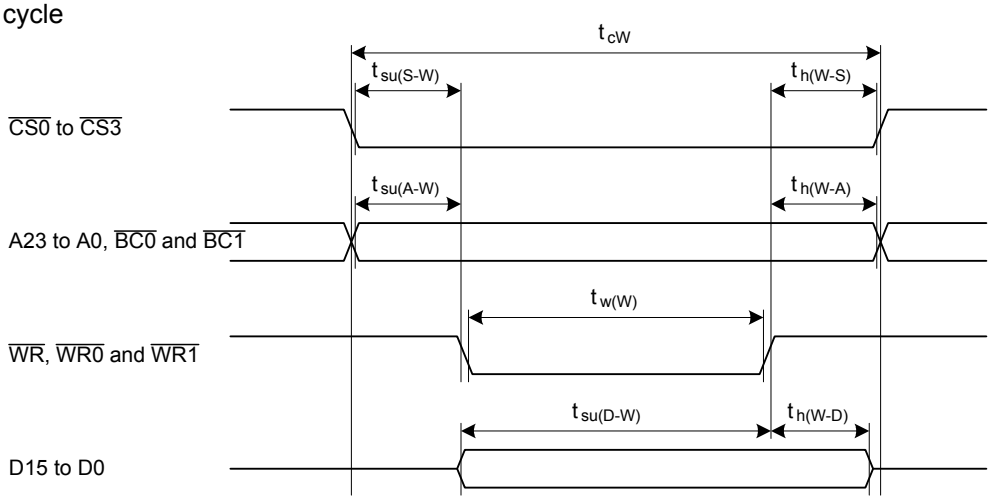
Figure 5.7 External Clock Input Timing

External bus timing (separate bus)

Read cycle



Write cycle



Measurement conditions

Item		$V_{CC1} = V_{CC2} = 4.2$ to 5.5 V	$V_{CC1} = V_{CC2} = 3.0$ to 3.6 V
Criterion for input voltage	V_{IH}	2.5 V	1.5 V
	V_{IL}	0.8 V	0.5 V
Criterion for output voltage	V_{OH}	2.0 V	2.4 V
	V_{OL}	0.8 V	0.5 V

Figure 5.8 External Bus Timing for Separate Bus

Rev.	Date	Description	
		Page	Summary
		15, 16	• "Interrupt table register" in **Figure 2.1** and **2.1.6** changed to "Interrupt vector table base register"
		18	• Scribal error: "24 bit" in **2.2.2** corrected to "32 bit"
			Chapter 3
		19	• Descriptions for this chapter and **Figure 3.1** modified
			Chapter 4
		20	• "(SFR)" of chapter title changed to "(SFRs)" • Description for initial paragraph of **Chapter 4** modified • Reset value for CCR and PBC in **Table 4.1** changed
		21, 22	• "UARTi Bus Collision Detection Interrupt Control Register" (i = 0 to 6) in **Tables 4.2 and 4.3** changed to "UARTi Bus Collision, Start/Stop Condition Detection Interrupt Control Register" • "DMAi interrupt" in **Tables 4.2 and 4.3** changed to "DMAi transfer complete interrupt"
		22	• Reset value for IIO3IR and IIO8IR to IIO11R in **Table 4.3** modified
		25	• Scribal error: address "00010Fh" added to **Table 4.6**
		32	• "Upward/Downward Counting Select Register" in **Table 4.13** changed to "Increment/Decrement Counting Select Register"
		38	• CSOP2 for address 040056h in **Table 4.19** deleted • Reset value for CM3 in **Table 4.19** changed
		43	• "DMAi Source Select Register i" in **Table 4.24** changed to "DMAi Request Source Select Register i"
			Chapter 5
		—	• This chapter newly added
			Appendix 1
		81	• "Package Dimension" as title changed to "Package Dimensions"
1.10	Sep 17, 2009	—	Third edition released
		—	The manual in general • Added 100-pin plastic molded LGA and 80- and 64-pin plastic molded LQFP packages • When new tables/figures are added for 80-/64-pin packages, add the following description: "(for the 100-pin package)" to the title of corresponding current tables/figures
			Chapter 1. Overview
		1	• Added description for 100-pin LGA and 80-/64-pin packages to lines 12 and 13 of **1.1**; Added description "a maximum of" to "nine channels of serial interface"; Deleted the whole description of "Notes to users"
		2	• Changed minimum RAM size "40" in **Table 1.1**, to "32" • Modified description for "External Bus Expansion", to **Table 1.1**; Moved this unit below "Clock"
		3	• Added "(optional)" for IEBus mode for "Intelligent I/O" in **Table 1.2** • Modified description for "Flash memory" in **Tables 1.2** • Added "100-pin plastic molded TFLGA (PTLG0100KA-A)" to **Table 1.2**
		4-7	• Added **Tables 1.3 to 1.6** to provide specifications for 80-/64-pin packages

Revision History	R32C/111 Group Datasheet

Rev.	Date	Description	
		Page	Summary
		66	• Changed expression “Programming and erasure endurance” in **Table 5.8** to “Program and erase cycles”; Changed its unit “times” in the table and Note 1 to “Cycles”
		68	• Changed order of descriptions of “$t_{rec(STOP)}$” and “$t_{rec(WAIT)}$” in **Table 5.13 and Figure 5.4**
		69	• Changed expressions “$\overline{CS0}$” and “A23 to A0, $\overline{BC0}$ to $\overline{BC3}$” in **Figure 5.5** to “Chip select” and “Address”, respectively
		78, 90	• Corrected “INTi” in title of **Tables 5.32 and 5.55** to “$\overline{INTi}$”
		81, 93	• Added measurement condition to **Tables 5.37 and 5.60**
			Appendix 1. Package Dimensions
		98-99	• Added a seating plane to the drawing of package dimension
1.30	Mar 3, 2014	—	Fifth edition released
		—	• Deleted description for the 80-pin package
			Chapter 1. Overview
		—	• Modified wording and enhanced description in this chapter
		1	• Modified expression “I^2C” in line 9 of **1.1** to “I^2C-bus interface”
		2, 4	• Modified expressions “calculation transfer” and “chained transfer” in **Tables 1.1 and 1.3** to “calculation result transfer” and “chain transfer”, respectively
		5	• Deleted N version from the Operating Temperature row in **Table 1.4**
		6	• Deleted products on planning phase from **Table 1.5**
		20, 23	• Modified expression “I^2C bus” in **Tables 1.13 and 1.16** to “I^2C-bus”
			Chapter 2. CPU
		—	• Modified wording and enhanced description in this chapter
			Chapter 5. Electrical Characteristics
		—	• Modified wording and enhanced description in this chapter
		65, 77	• Deleted TXD4, STXD4, and $\overline{RTS4}$ from **Tables 5.16 and 5.39**
		66, 78	• Modified description “Drive power” in **Tables 5.17 and 5.40** to “Drive strength”

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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