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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | R32C/100 |
| Core Size | 16/32-Bit |
| Speed | 50MHz |
| Connectivity | EBI/EMI, I²C, IEBus, UART/USART |
| Peripherals | DMA, LVD, PWM, WDT |
| Number of I/O | 49 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 8K x 8 |
| RAM Size | 32K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 5.5V |
| Data Converters | A/D 26x10b; D/A 2x8b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | 64-LFQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f6411edfn-ua |

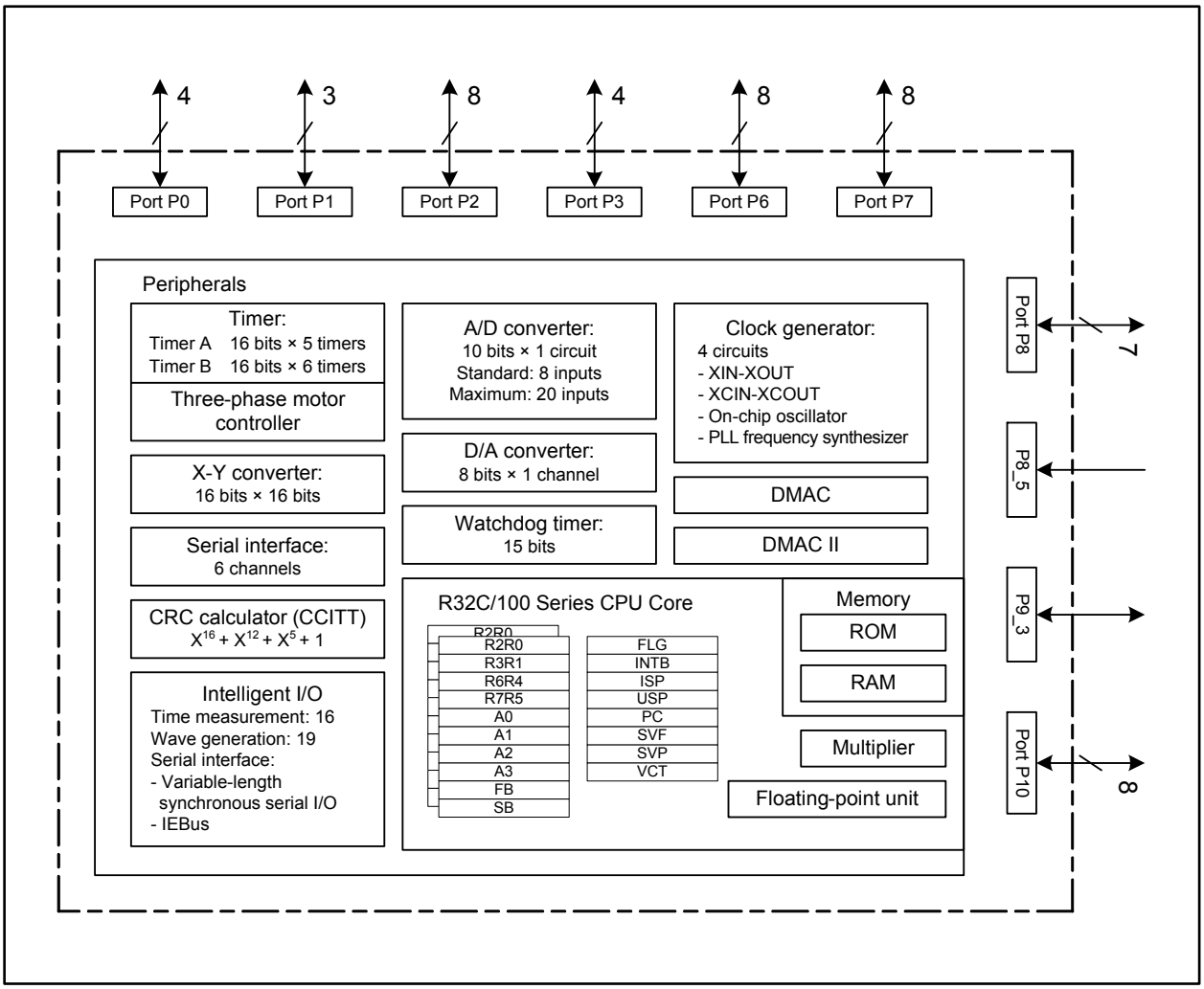
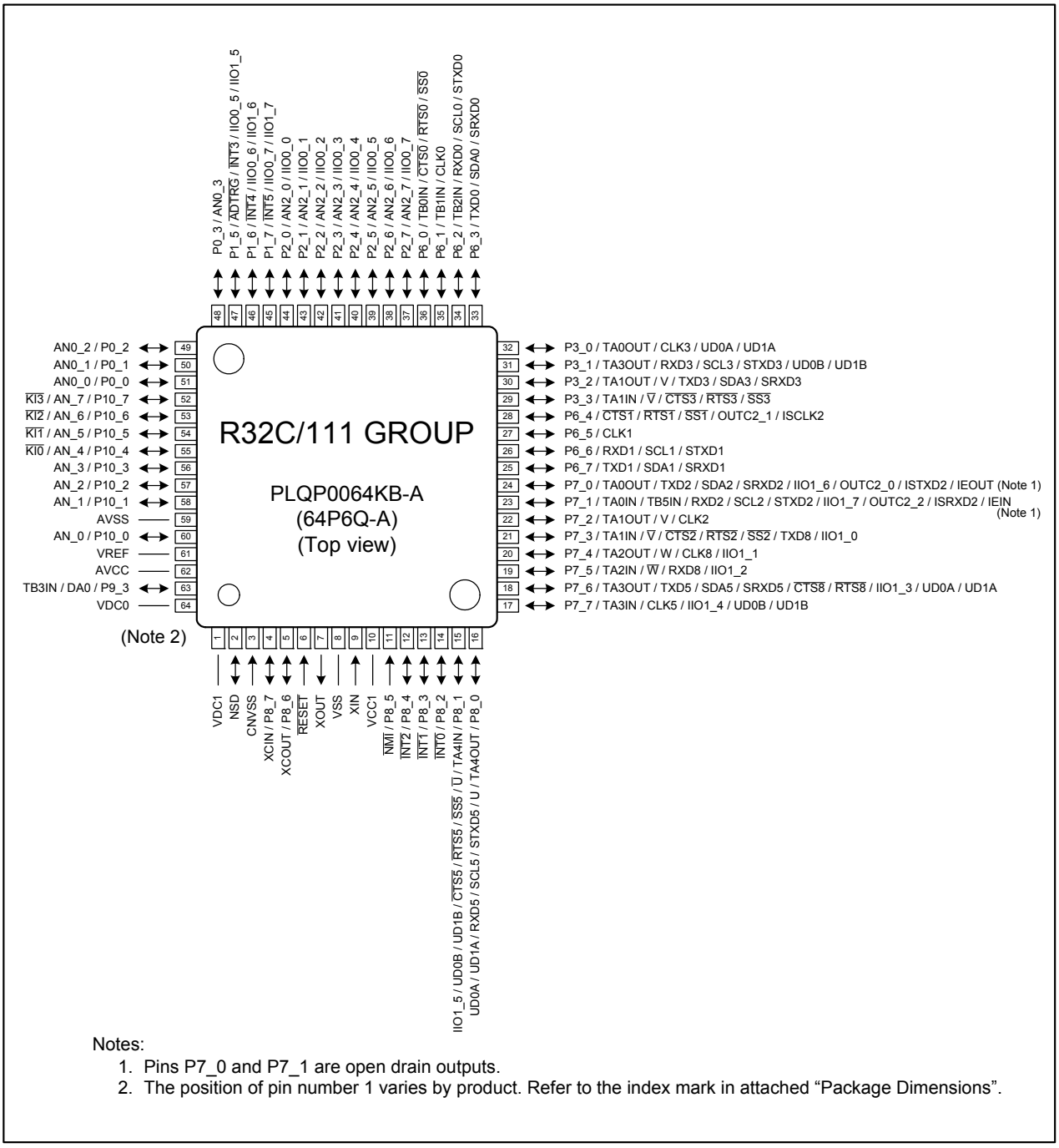



**Figure 1.3 R32C/111 Group Block Diagram for the 64-pin Package**




Notes:
1. Pins P7_0 and P7_1 are open drain outputs.
2. The position of pin number 1 varies by product. Refer to the index mark in attached “Package Dimensions”.

**Figure 1.6 Pin Assignment for the 64-pin Package (top view)**

#### 2.1.8.5 Register Bank Select Flag (B flag)

This flag selects a register bank. It indicates 0 when register bank 0 is selected, and 1 when register bank 1 is selected.

#### 2.1.8.6 Overflow Flag (O flag)

This flag becomes 1 when the result of an operation overflows; otherwise it is 0.

#### 2.1.8.7 Interrupt Enable Flag (I flag)

This flag enables maskable interrupts. To disable maskable interrupts, set this flag to 0. To enable them, set this flag to 1. When an interrupt is accepted, the flag becomes 0.

#### 2.1.8.8 Stack Pointer Select Flag (U flag)

To select the interrupt stack pointer (ISP), set this flag to 0. To select the user stack pointer (USP), set this flag to 1.
It becomes 0 when a hardware interrupt is accepted or when an INT instruction designated by a software interrupt number from 0 to 127 is executed.

#### 2.1.8.9 Floating-point Underflow Flag (FU flag)

This flag becomes 1 when an underflow occurs in a floating-point operation; otherwise it is 0. It also becomes 1 when the operand contains invalid numbers (subnormal numbers).

#### 2.1.8.10 Floating-point Overflow Flag (FO flag)

This flag becomes 1 when an overflow occurs in a floating-point operation; otherwise it is 0. It also becomes 1 when the operand contains invalid numbers (subnormal numbers).

#### 2.1.8.11 Processor Interrupt Priority Level (IPL)

The processor interrupt priority level (IPL), consisting of 3 bits, selects a processor interrupt priority level from level 0 to 7. An interrupt is enabled when the interrupt request level is higher than the selected IPL.
When the processor interrupt priority level (IPL) is set to 111b (level 7), all interrupts are disabled.

#### 2.1.8.12 Fixed-point Radix Point Designation Bit (DP bit)

This bit designates the radix point. It also specifies which portion of the fixed-point multiplication result to extract. It is used for the MULX instruction.

#### 2.1.8.13 Floating-point Rounding Mode (RND)

The 2-bit floating-point rounding mode selects a rounding mode for floating-point calculation results.

#### 2.1.8.14 Reserved

Only set this bit to 0. The read value is undefined.

# 3. Memory

Figure 3.1 shows the memory map of the R32C/111 Group.
The R32C/111 Group provides a 4-Gbyte address space from 00000000h to FFFFFFFFh.

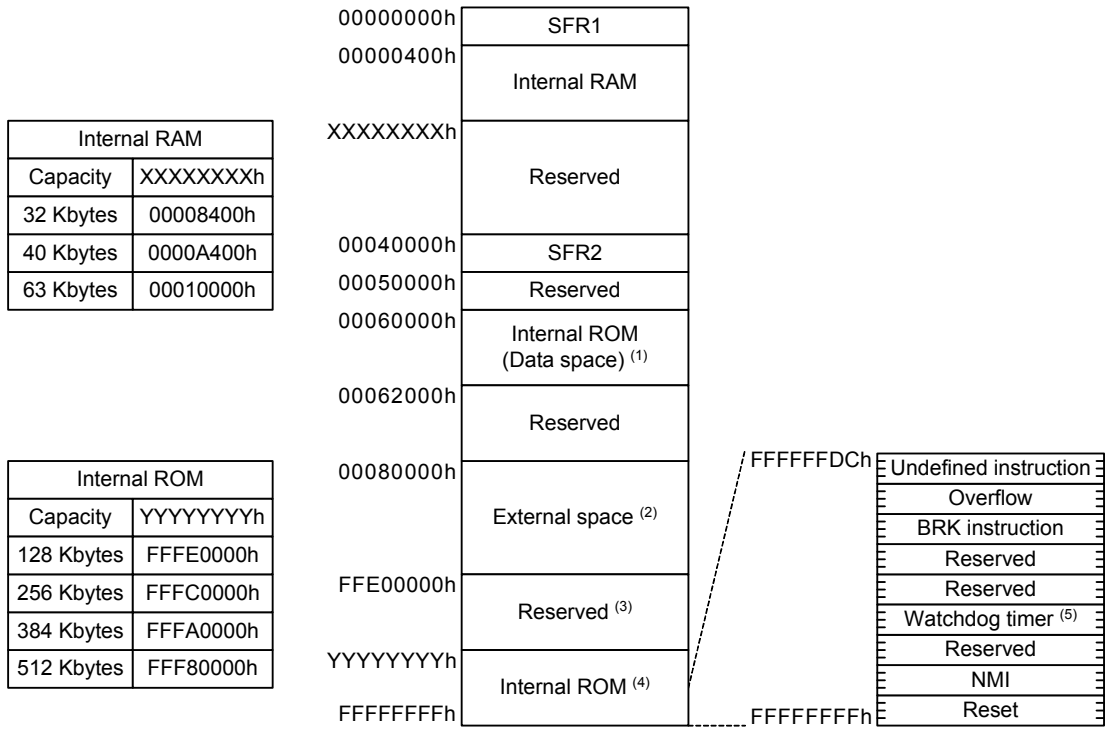
The internal ROM is mapped from address FFFFFFFFh in the inferior direction. For example, the 512-Kbyte internal ROM is mapped from FFF80000h to FFFFFFFFh.
The fixed interrupt vector table contains the start address of interrupt handlers and is mapped from FFFFFFDCh to FFFFFFFFh.
The internal RAM is mapped from address 00000400h in the superior direction. For example, the 63-Kbyte internal RAM is mapped from 00000400h to 0000FFFFh. Besides being used for data storage, the internal RAM functions as a stack(s) for subroutine calls and/or interrupt handlers.

Special function registers (SFRs), which are control registers for peripheral functions, are mapped from 00000000h to 000003FFh, and from 00040000h to 0004FFFFh. Unoccupied SFR locations are reserved, and no access is allowed.

In memory expansion mode or microprocessor mode, some spaces are reserved for internal use and should not be accessed.

| Internal RAM | |
|---|---|
| Capacity | XXXXXXXXh |
| 32 Kbytes | 00008400h |
| 40 Kbytes | 0000A400h |
| 63 Kbytes | 00010000h |

| Internal ROM | |
|---|---|
| Capacity | YYYYYYYYh |
| 128 Kbytes | FFFE0000h |
| 256 Kbytes | FFFC0000h |
| 384 Kbytes | FFFA0000h |
| 512 Kbytes | FFF80000h |




Notes:
1. The flash memory version provides two additional 4-Kbyte spaces (blocks A and B) for storing data.
2. This space can be used in memory expansion mode or microprocessor mode. Addresses from 02000000h to FDFFFFFFh are inaccessible.
3. This space is reserved in memory expansion mode. It becomes an external space in microprocessor mode.
4. This space can be used in single-chip mode or memory expansion mode. It becomes an external space in microprocessor mode.
5. The watchdog timer interrupt shares a vector with the oscillator stop detection interrupt and low voltage detection interrupt.

**Figure 3.1 Memory Map**

**Table 4.19 SFR List (19)**

| Address | Register | Symbol | Reset Value |
|---|---|---|---|
| 040030h to 04003Fh | | | |
| 040040h | | | |
| 040041h | | | |
| 040042h | | | |
| 040043h | | | |
| 040044h | Processor Mode Register 0 (1) | PM0 | 1000 0000b (CNVSS pin = Low)<br>0000 0011b (CNVSS pin = High) |
| 040045h | | | |
| 040046h | System Clock Control Register 0 | CM0 | 0000 1000b |
| 040047h | System Clock Control Register 1 | CM1 | 0010 0000b |
| 040048h | Processor Mode Register 3 | PM3 | 00h |
| 040049h | | | |
| 04004Ah | Protect Register | PRCR | XXXX X000b |
| 04004Bh | | | |
| 04004Ch | Protect Register 3 | PRCR3 | 0000 0000b |
| 04004Dh | Oscillator Stop Detection Register | CM2 | 00h |
| 04004Eh | | | |
| 04004Fh | | | |
| 040050h | | | |
| 040051h | | | |
| 040052h | | | |
| 040053h | Processor Mode Register 2 | PM2 | 00h |
| 040054h | Chip Select Output Pin Setting Register 0 | CSOP0 | 1000 XXXXb |
| 040055h | Chip Select Output Pin Setting Register 1 | CSOP1 | 01X0 XXXXb |
| 040056h | | | |
| 040057h | | | |
| 040058h | | | |
| 040059h | | | |
| 04005Ah | Low Speed Mode Clock Control Register | CM3 | XXXX XX00b |
| 04005Bh | | | |
| 04005Ch | | | |
| 04005Dh | | | |
| 04005Eh | | | |
| 04005Fh | | | |
| 040060h | Voltage Regulator Control Register | VRCR | 0000 0000b |
| 040061h | | | |
| 040062h | Low Voltage Detector Control Register | LVDC | 0000 XX00b |
| 040063h | | | |
| 040064h | Detection Voltage Configuration Register | DVCR | 0000 XXXXb |
| 040065h | | | |
| 040066h | | | |
| 040067h | | | |
| 040068h to 040093h | | | |

X: Undefined
Blanks are reserved. No access is allowed.

Note:
1. The value in the PM0 register is retained even after a software reset or watchdog timer reset.

**Table 4.20 SFR List (20)**

| Address | Register | Symbol | Reset Value |
|---|---|---|---|
| 040094h | | | |
| 040095h | | | |
| 040096h | | | |
| 040097h | Three-phase Output Buffer Control Register | IOBC | 0XXX XXXXb |
| 040098h | Input Function Select Register 0 | IFS0 | X000 0000b (1) |
| 040099h | | | |
| 04009Ah | Input Function Select Register 2 | IFS2 | 0000 00X0b (2) |
| 04009Bh | Input Function Select Register 3 | IFS3 | XXXX XX00b |
| 04009Ch | | | |
| 04009Dh | | | |
| 04009Eh | | | |
| 04009Fh | Input Function Select Register 7 (3) | IFS7 | XXXX XX0Xb |
| 0400A0h | Port P0_0 Function Select Register | P0_0S | 0XXX X000b |
| 0400A1h | Port P1_0 Function Select Register | P1_0S | XXXX X000b |
| 0400A2h | Port P0_1 Function Select Register | P0_1S | 0XXX X000b |
| 0400A3h | Port P1_1 Function Select Register | P1_1S | XXXX X000b |
| 0400A4h | Port P0_2 Function Select Register | P0_2S | 0XXX X000b |
| 0400A5h | Port P1_2 Function Select Register | P1_2S | XXXX X000b |
| 0400A6h | Port P0_3 Function Select Register | P0_3S | 0XXX X000b |
| 0400A7h | Port P1_3 Function Select Register | P1_3S | XXXX X000b |
| 0400A8h | Port P0_4 Function Select Register | P0_4S | 0XXX X000b |
| 0400A9h | Port P1_4 Function Select Register | P1_4S | XXXX X000b |
| 0400AAh | Port P0_5 Function Select Register | P0_5S | 0XXX X000b |
| 0400ABh | Port P1_5 Function Select Register | P1_5S | XXXX X000b |
| 0400ACh | Port P0_6 Function Select Register | P0_6S | 0XXX X000b |
| 0400ADh | Port P1_6 Function Select Register | P1_6S | XXXX X000b |
| 0400AEh | Port P0_7 Function Select Register | P0_7S | 0XXX X000b |
| 0400AFh | Port P1_7 Function Select Register | P1_7S | XXXX X000b |
| 0400B0h | Port P2_0 Function Select Register | P2_0S | 0XXX X000b |
| 0400B1h | Port P3_0 Function Select Register | P3_0S | XXXX X000b |
| 0400B2h | Port P2_1 Function Select Register | P2_1S | 0XXX X000b |
| 0400B3h | Port P3_1 Function Select Register | P3_1S | XXXX X000b |
| 0400B4h | Port P2_2 Function Select Register | P2_2S | 0XXX X000b |
| 0400B5h | Port P3_2 Function Select Register | P3_2S | XXXX X000b |
| 0400B6h | Port P2_3 Function Select Register | P2_3S | 0XXX X000b |
| 0400B7h | Port P3_3 Function Select Register | P3_3S | XXXX X000b |
| 0400B8h | Port P2_4 Function Select Register | P2_4S | 0XXX X000b |
| 0400B9h | Port P3_4 Function Select Register | P3_4S | XXXX X000b |
| 0400BAh | Port P2_5 Function Select Register | P2_5S | 0XXX X000b |
| 0400BBh | Port P3_5 Function Select Register | P3_5S | XXXX X000b |
| 0400BCh | Port P2_6 Function Select Register | P2_6S | 0XXX X000b |
| 0400BDh | Port P3_6 Function Select Register | P3_6S | XXXX X000b |
| 0400BEh | Port P2_7 Function Select Register | P2_7S | 0XXX X000b |
| 0400BFh | Port P3_7 Function Select Register | P3_7S | XXXX X000b |

X: Undefined
Blanks are reserved. No access is allowed.

Notes:
1. The reset value is 0000 0000b in the 64-pin package.
2. The reset value is 0000 000Xb in the 64-pin package.
3. This register is provided for the 64-pin package only. No access is allowed in the 100-pin package.

# 5. Electrical Characteristics

**Table 5.1 Absolute Maximum Ratings (1)**

| Symbol | Characteristic | | Condition | Value (2) | Unit |
|---|---|---|---|---|---|
| $V_{CC1}$, $V_{CC2}$ | Supply voltage | | $V_{CC1}$ = $AV_{CC}$ | -0.3 to 6.0 | V |
| $V_{CC2}$ | Supply voltage | | — | -0.3 to $V_{CC1}$ | V |
| $AV_{CC}$ | Analog supply voltage | | $V_{CC1}$ = $AV_{CC}$ | -0.3 to 6.0 | V |
| $V_I$ | Input voltage | XIN, $\overline{\text{RESET}}$, CNVSS, NSD, $V_{REF}$, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_7, P9_1, P9_3 to P9_7, P10_0 to P10_7 (3) | | -0.3 to $V_{CC1}$ + 0.3 | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7 (3) | | -0.3 to $V_{CC2}$ + 0.3 | V |
| | | P7_0, P7_1 | | -0.3 to 6.0 | V |
| $V_O$ | Output voltage | XOUT, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_3 to P9_7, P10_0 to P10_7 (3) | | -0.3 to $V_{CC1}$ + 0.3 | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7 (3) | | -0.3 to $V_{CC2}$ + 0.3 | V |
| | | P7_0, P7_1 | | -0.3 to 6.0 | V |
| $P_d$ | Power consumption | | $T_a$ = 25°C | 500 | mW |
| — | Operating temperature range | | | -40 to 85 | °C |
| $T_{stg}$ | Storage temperature range | | | -65 to 150 | °C |

Notes:
1. Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The $V_{CC2}$ pin is available in the 100-pin package only. It should be considered as $V_{CC1}$ in the 64-pin package.
3. Ports P0_4 to P0_7, P1_0 to P1_4, P3_4 to P3_7, P4, P5, P9_1, and P9_4 to P9_7 are available in the 100-pin package only.

**Table 5.2 Operating Conditions (1/5) (1)**

| Symbol | Characteristic | | | Value (2) | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| $V_{CC1}$, $V_{CC2}$ | Digital supply voltage ($V_{CC1} \geq V_{CC2}$) | | | 3.0 | 5.0 | 5.5 | V |
| $AV_{CC}$ | Analog supply voltage | | | | $V_{CC1}$ | | V |
| $V_{REF}$ | Reference voltage | | | 3.0 | | $V_{CC1}$ | V |
| $V_{SS}$ | Digital ground voltage | | | | 0 | | V |
| $AV_{SS}$ | Analog ground voltage | | | | 0 | | V |
| $dV_{CC1}$/dt | $V_{CC1}$ ramp up rate ($V_{CC1}$ < 2.0 V) | | | 0.05 | | | V/ms |
| $V_{IH}$ | High level input voltage | P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7 (4) | | 0.8 × $V_{CC2}$ | | $V_{CC2}$ | V |
| | | XIN, $\overline{\text{RESET}}$, CNVSS, NSD, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_7 (3), P9_1, P9_3 to P9_7, P10_0 to P10_7 (4) | | 0.8 × $V_{CC1}$ | | $V_{CC1}$ | V |
| | | P7_0, P7_1 | | 0.8 × $V_{CC1}$ | | 6.0 | V |
| | | P0_0 to P0_7, P1_0 to P1_7 (4) | in single-chip mode | 0.8 × $V_{CC2}$ | | $V_{CC2}$ | V |
| | | | in memory expansion mode or microprocessor mode (5) | 0.5 × $V_{CC2}$ | | $V_{CC2}$ | V |
| $V_{IL}$ | Low level input voltage | P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7 (4) | | 0 | | 0.2 × $V_{CC2}$ | V |
| | | XIN, $\overline{\text{RESET}}$, CNVSS, NSD, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7 (3), P9_1, P9_3 to P9_7, P10_0 to P10_7 (4) | | 0 | | 0.2 × $V_{CC1}$ | V |
| | | P0_0 to P0_7, P1_0 to P1_7 (4) | in single-chip mode | 0 | | 0.2 × $V_{CC2}$ | V |
| | | | in memory expansion mode or microprocessor mode (5) | 0 | | 0.16 × $V_{CC2}$ | V |
| $T_{opr}$ | Operating temperature range | N version | | -20 | | 85 | °C |
| | | D version | | -40 | | 85 | °C |

Notes:
1. The device is operationally guaranteed under these operating conditions.
2. The $V_{CC2}$ pin is available in the 100-pin package only. It should be considered as $V_{CC1}$ in the 64-pin package.
3. $V_{IH}$ and $V_{IL}$ for P8_7 are specified for P8_7 as a programmable port. These values are not applicable for P8_7 as XCIN.
4. Ports P0_4 to P0_7, P1_0 to P1_4, P3_4 to P3_7, P4, P5, P9_1, and P9_4 to P9_7 are available in the 100-pin package only.
5. Memory expansion mode and microprocessor mode are available in the 100-pin package only.

**Table 5.4 Operating Conditions (3/5)**

**($V_{CC1}$ = $V_{CC2}$ = 3.0 to 5.5 V, $V_{SS}$ = 0 V, and $T_a$ = $T_{opr}$, unless otherwise noted) (1)**

| Symbol | Characteristic | | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $I_{OH(peak)}$ | High level peak output current (2) | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_3 to P9_7, P10_0 to P10_7 (3) | | | -10.0 | mA |
| $I_{OH(avg)}$ | High level average output current (4) | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_3 to P9_7, P10_0 to P10_7 (3) | | | -5.0 | mA |
| $I_{OL(peak)}$ | Low level peak output current (2) | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_3 to P9_7, P10_0 to P10_7 (3) | | | 10.0 | mA |
| $I_{OL(avg)}$ | Low level average output current (4) | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_3 to P9_7, P10_0 to P10_7 (3) | | | 5.0 | mA |

Notes:

1. The device is operationally guaranteed under these operating conditions.
2. The following conditions should be satisfied:
   - The sum of $I_{OL(peak)}$ of ports P0, P1, P2, P8_6, P8_7, P9, and P10 is 80 mA or less.
   - The sum of $I_{OL(peak)}$ of ports P3, P4, P5, P6, P7, and P8_0 to P8_4 is 80 mA or less.
   - The sum of $I_{OH(peak)}$ of ports P0, P1, and P2 is -40 mA or less.
   - The sum of $I_{OH(peak)}$ of ports P8_6, P8_7, P9, and P10 is -40 mA or less.
   - The sum of $I_{OH(peak)}$ of ports P3, P4, and P5 is -40 mA or less.
   - The sum of $I_{OH(peak)}$ of ports P6, P7, and P8_0 to P8_4 is -40 mA or less.
3. Ports P0_4 to P0_7, P1_0 to P1_4, P3_4 to P3_7, P4, P5, and P9_4 to P9_7 are available in the 100-pin package only.
4. Average value within 100 ms.

**Table 5.6 Operating Conditions (5/5)**

**($V_{CC1}$ = $V_{CC2}$ = 3.0 to 5.5 V, $V_{SS}$ = 0 V, and $T_a$ = $T_{opr}$, unless otherwise noted) (1)**

| Symbol | Characteristic | | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{r(VCC1)}$ | Allowable ripple voltage | $V_{CC1}$ = 5.0 V | | | 0.5 | Vp-p |
| | | $V_{CC1}$ = 3.0 V | | | 0.3 | Vp-p |
| $V_{r(VCC2)}$ | Allowable ripple voltage | $V_{CC2}$ = 5.0 V | | | 0.5 | Vp-p |
| | | $V_{CC2}$ = 3.0 V | | | 0.3 | Vp-p |
| $dV_{r(VCC1)}/dt$ | Ripple voltage gradient | $V_{CC1}$ = 5.0 V | | | ±0.3 | V/ms |
| | | $V_{CC1}$ = 3.0 V | | | ±0.3 | V/ms |
| $dV_{r(VCC2)}/dt$ | Ripple voltage gradient | $V_{CC2}$ = 5.0 V | | | ±0.3 | V/ms |
| | | $V_{CC2}$ = 3.0 V | | | ±0.3 | V/ms |
| $f_{r(VCC1)}$ | Allowable ripple frequency | | | | 10 | kHz |
| $f_{r(VCC2)}$ | Allowable ripple frequency | | | | 10 | kHz |

Note:
1. The device is operationally guaranteed under these operating conditions.

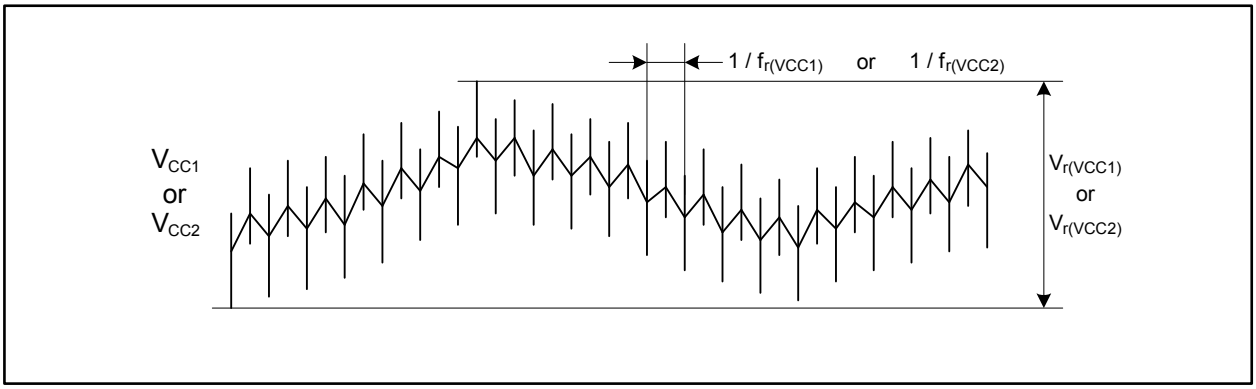



**Figure 5.2 Ripple Waveform**

**Table 5.7 Electrical Characteristics of RAM**
**($V_{CC1}$ = $V_{CC2}$ = 3.0 to 5.5 V, $V_{SS}$ = 0 V, and Ta = $T_{opr}$, unless otherwise noted)**

| Symbol | Characteristic | Measurement Condition | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{RDR}$ | RAM data retention voltage (1) | In stop mode | 2.0 | | | V |

Note:
1. The value listed in the table is the minimum $V_{CC1}$ to retain RAM data.

**Table 5.8 Electrical Characteristics of Flash Memory**
**($V_{CC1}$ = $V_{CC2}$ = 3.0 to 5.5 V, $V_{SS}$ = 0 V, and Ta = $T_{opr}$, unless otherwise noted)**

| Symbol | Characteristic | | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| — | Program/erase cycles (1) | Program area | 1000 | | | Cycles |
| | | Data area | 10000 | | | Cycles |
| — | 4-word program time | Program area | | 150 | 900 | µs |
| | | Data area | | 300 | 1700 | µs |
| — | Lock bit program time | Program area | | 70 | 500 | µs |
| | | Data area | | 140 | 1000 | µs |
| — | Block erasure time | 4-Kbyte block | | 0.12 | 3.0 | s |
| | | 32-Kbyte block | | 0.17 | 3.0 | s |
| | | 64-Kbyte block | | 0.20 | 3.0 | s |
| — | Data retention (2) | $T_a$ = 55°C (3) | 10 | | | Years |

Notes:
1. Program/erase definition
   This value represents the number of erasures per block.
   When the number of program/erase cycles is n, each block can be erased n times.
   For example, if a 4-word write is performed in 512 different addresses in the 4-Kbyte block A and then the block is erased, this is counted as a single program/erase operation.
   However, the same address cannot be written to more than once per erasure (overwrite disabled).
2. Data retention includes periods when no supply voltage is applied and no clock is provided.
3. Contact a Renesas Electronics sales office for data retention times other than the above condition.

$V_{CC1} = V_{CC2} = 5\ V$

**Table 5.15 Electrical Characteristics (1/3)**
**($V_{CC1} = V_{CC2} = 4.2$ to 5.5 V, $V_{SS} = 0$ V, $T_a = T_{opr}$, and $f_{(CPU)} = 50$ MHz, unless otherwise noted)**

| Symbol | Characteristic | | Measurement Condition | Value (2) | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| $V_{OH}$ | High level output voltage | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7 (1) | $I_{OH}$ = -5 mA | $V_{CC2}$ -2.0 | | $V_{CC2}$ | V |
| | | P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_3 to P9_7, P10_0 to P10_7 (1) | $I_{OH}$ = -5 mA | $V_{CC1}$ -2.0 | | $V_{CC1}$ | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7 (1) | $I_{OH}$ = -200 µA | $V_{CC2}$ -0.3 | | $V_{CC2}$ | V |
| | | P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_3 to P9_7, P10_0 to P10_7 (1) | $I_{OH}$ = -200 µA | $V_{CC1}$ -0.3 | | $V_{CC1}$ | V |
| $V_{OL}$ | Low level output voltage | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_3 to P9_7, P10_0 to P10_7 (1) | $I_{OL}$ = 5 mA | | | 2.0 | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_3 to P9_7, P10_0 to P10_7 (1) | $I_{OL}$ = 200 µA | | | 0.45 | V |

Notes:
1. Ports P0_4 to P0_7, P1_0 to P1_4, P3_4 to P3_7, P4, P5, and P9_4 to P9_7 are available in the 100-pin package only.
2. The $V_{CC2}$ pin is available in the 100-pin package only. It should be considered as $V_{CC1}$ in the 64-pin package.

$V_{CC1} = V_{CC2} = 5\ V$

**Table 5.19 D/A Conversion Characteristics ($V_{CC1} = V_{CC2} = AV_{CC} = V_{REF}$ = 4.2 to 5.5 V, $V_{SS} = AV_{SS}$ = 0 V, and $T_a = T_{opr}$, unless otherwise noted)**

| Symbol | Characteristic | Measurement Condition | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| — | Resolution | | | | 8 | Bits |
| — | Absolute precision | | | | 1.0 | % |
| $t_S$ | Settling time | | | | 3 | µs |
| $R_O$ | Output resistance | | 4 | 10 | 20 | kΩ |
| $I_{VREF}$ | Reference input current | See Note 1 | | | 1.5 | mA |

Note:
1. One D/A converter is used. The DAi register (i = 0, 1) of the other unused converter is set to 00h. The resistor ladder for the A/D converter is not considered.
Even when the VCUT bit in the AD0CON1 register is set to 0 ($V_{REF}$ disconnected), $I_{VREF}$ is supplied.

$V_{CC1} = V_{CC2} = 5\ V$

**Timing Requirements ($V_{CC1} = V_{CC2} = 4.2$ to 5.5 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted)**

**Table 5.27 Timer B Input (counting input in event counter mode)**

| Symbol | Characteristic | Value | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TB)}$ | TBiIN input clock cycle time (one edge counting) | 200 | | ns |
| $t_{w(TBH)}$ | TBiIN input high level pulse width (one edge counting) | 80 | | ns |
| $t_{w(TBL)}$ | TBiIN input low level pulse width (one edge counting) | 80 | | ns |
| $t_{c(TB)}$ | TBiIN input clock cycle time (both edges counting) | 200 | | ns |
| $t_{w(TBH)}$ | TBiIN input high level pulse width (both edges counting) | 80 | | ns |
| $t_{w(TBL)}$ | TBiIN input low level pulse width (both edges counting) | 80 | | ns |

**Table 5.28 Timer B Input (pulse period measure mode)**

| Symbol | Characteristic | Value | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TB)}$ | TBiIN input clock cycle time | 400 | | ns |
| $t_{w(TBH)}$ | TBiIN input high level pulse width | 180 | | ns |
| $t_{w(TBL)}$ | TBiIN input low level pulse width | 180 | | ns |

**Table 5.29 Timer B Input (pulse-width measure mode)**

| Symbol | Characteristic | Value | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TB)}$ | TBiIN input clock cycle time | 400 | | ns |
| $t_{w(TBH)}$ | TBiIN input high level pulse width | 180 | | ns |
| $t_{w(TBL)}$ | TBiIN input low level pulse width | 180 | | ns |

## $V_{CC1} = V_{CC2} = 5$ V

**Switching Characteristics ($V_{CC1} = V_{CC2} = 4.2$ to 5.5 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted)**

**Table 5.36 Serial Interface**

| Symbol | Characteristic | Measurement Condition | Value | | Unit |
|---|---|---|---|---|---|
| | | | Min. | Max. | |
| $t_{d(C-Q)}$ | TXDi output delay time | Refer to Figure 5.6 | | 80 | ns |
| $t_{h(C-Q)}$ | TXDi output hold time | | 0 | | ns |

**Table 5.37 Intelligent I/O**

| Symbol | Characteristic | Measurement Condition | Value | | Unit |
|---|---|---|---|---|---|
| | | | Min. | Max. | |
| $t_{d(ISCLK2-TXD)}$ | ISTXD2 output delay time | Refer to Figure 5.6 | | 180 | ns |
| $t_{h(ISCLK2-RXD)}$ | ISTXD2 output hold time | | 0 | | ns |

$V_{CC1} = V_{CC2} = 3.3$ V

**Table 5.40 Electrical Characteristics (3/3)**
**($V_{CC1} = V_{CC2} = 3.0$ to 3.6 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted)**

| Symbol | Characteristic | Measurement Condition | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| $I_{CC}$ | Power supply current | In single-chip mode, output pins are left open and others are connected to $V_{SS}$<br><br>XIN-XOUT<br>Drive strength: low<br><br>XCIN-XCOUT<br>Drive strength: low | $f_{(CPU)}$ = 50 MHz, $f_{(BCLK)}$ = 25 MHz,<br>$f_{(XIN)}$ = 8 MHz,<br>Active: XIN, PLL,<br>Stopped: XCIN, OCO | | 28 | 40 | mA |
| | | | $f_{(CPU)} = f_{SO(PLL)}/24$ MHz,<br>Active: PLL (self-oscillation),<br>Stopped: XIN, XCIN, OCO | | 7 | | mA |
| | | | $f_{(CPU)} = f_{(BCLK)} = f_{(XIN)}/256$ MHz,<br>$f_{(XIN)}$ = 8 MHz,<br>Active: XIN,<br>Stopped: PLL, XCIN, OCO | | 670 | | µA |
| | | | $f_{(CPU)} = f_{(BCLK)}$ = 32.768 kHz,<br>Active: XCIN,<br>Stopped: XIN, PLL, OCO,<br>Main regulator: shutdown | | 180 | | µA |
| | | | $f_{(CPU)} = f_{(BCLK)} = f_{(OCO)}/4$ kHz,<br>Active: OCO,<br>Stopped: XIN, PLL, XCIN,<br>Main regulator: shutdown | | 190 | | µA |
| | | | $f_{(CPU)} = f_{(BCLK)} = f_{(XIN)}/256$ MHz,<br>$f_{(XIN)}$ = 8 MHz,<br>Active: XIN,<br>Stopped: PLL, XCIN, OCO,<br>$T_a$ = 25°C, Wait mode | | 500 | 900 | µA |
| | | | $f_{(CPU)} = f_{(BCLK)}$ = 32.768 kHz,<br>Active: XCIN,<br>Stopped: XIN, PLL, OCO,<br>Main regulator: shutdown,<br>$T_a$ = 25°C, Wait mode | | 8 | 140 | µA |
| | | | $f_{(CPU)} = f_{(BCLK)} = f_{(OCO)}/4$ kHz,<br>Active: OCO,<br>Stopped: XIN, PLL, XCIN,<br>Main regulator: shutdown,<br>$T_a$ = 25°C, Wait mode | | 10 | 150 | µA |
| | | | Stopped: all clocks,<br>Main regulator: shutdown,<br>$T_a$ = 25°C | | 5 | 70 | µA |

## $V_{CC1} = V_{CC2} = 3.3$ V

**Switching Characteristics ($V_{CC1} = V_{CC2} = 3.0$ to 3.6 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted)**

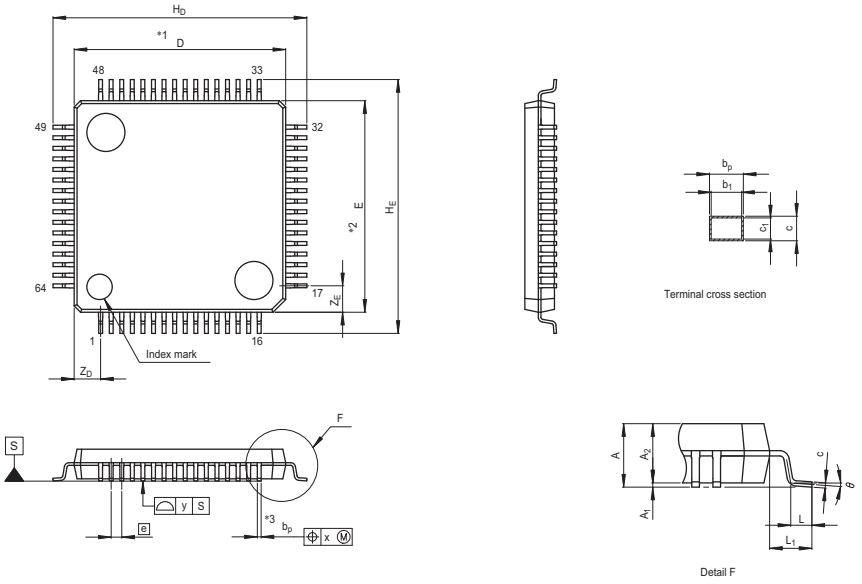
**Table 5.59 Serial Interface**

| Symbol | Characteristic | Measurement Condition | Value | | Unit |
|---|---|---|---|---|---|
| | | | Min. | Max. | |
| $t_{d(C-Q)}$ | TXDi output delay time | Refer to Figure 5.6 | | 80 | ns |
| $t_{h(C-Q)}$ | TXDi output hold time | | 0 | | ns |

**Table 5.60 Intelligent I/O**

| Symbol | Characteristic | Measurement Condition | Value | | Unit |
|---|---|---|---|---|---|
| | | | Min. | Max. | |
| $t_{d(ISCLK2-TXD)}$ | ISTXD2 output delay time | Refer to Figure 5.6 | | 180 | ns |
| $t_{h(ISCLK2-RXD)}$ | ISTXD2 output hold time | | 0 | | ns |

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-LQFP64-10x10-0.50 | PLQP0064KB-A | 64P6Q-A / FP-64K / FP-64KV | 0.3g |




NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 9.9 | 10.0 | 10.1 |
| E | 9.9 | 10.0 | 10.1 |
| $A_2$ | — | 1.4 | — |
| $H_D$ | 11.8 | 12.0 | 12.2 |
| $H_E$ | 11.8 | 12.0 | 12.2 |
| A | — | — | 1.7 |
| $A_1$ | 0.05 | 0.1 | 0.15 |
| $b_p$ | 0.15 | 0.20 | 0.25 |
| $b_1$ | — | 0.18 | — |
| c | 0.09 | 0.145 | 0.20 |
| $c_1$ | — | 0.125 | — |
| $\theta$ | 0° | — | 8° |
| e | — | 0.5 | — |
| x | — | — | 0.08 |
| y | — | — | 0.08 |
| $Z_D$ | — | 1.25 | — |
| $Z_E$ | — | 1.25 | — |
| L | 0.35 | 0.5 | 0.65 |
| $L_1$ | — | 1.0 | — |

| Revision History | R32C/111 Group Datasheet |
|---|---|

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 0.03 | Oct 17, 2007 | — | Initial release |
| 0.30 | Aug 19, 2008 | — | Second edition released |
| | | — | The manual in general<br>• Maximum operating frequency changed from 48 MHz to 50 MHz<br>• Specification of on-chip oscillator disclosed<br>• Microprocessor mode becomes optional<br>• “memory-expanded mode” changed to “memory expansion mode” |
| | | | Chapter 1 |
| | | 1 | • “(MCUs)” added to line 1 of **1.1**<br>• Applications in **1.1.1** revised and modified<br>• “Attention Users” below **1.1.1** modified to “Notes to users”; “The specification” in this box changed to “Specifications” |
| | | 2 | • “instructions” in “CPU” of **Table 1.1** deleted<br>• Minimum instruction execution time in “CPU” of **Table 1.1** changed<br>• Microprocessor mode in CPU” of **Table 1.1** changed to optional<br>• “TBD” for “Voltage Detection” in **Table 1.1** deleted<br>• “3 circuits” for “Clock” in **Table 1.1** changed to “4 circuits”<br>• “Total interrupt vectors” in **Table 1.1** changed to “Interrupt vectors”<br>• Trigger sources” for DMA in **Table 1.1** modified to “Request sources”; Request sources for “DMA” defined as 51<br>• Scribal error: “peripheral interrupt sources” for “DMACII” in **Table 1.1** corrected to “peripheral interrupt source” |
| | | 3 | • Unit names in **Table 1.2** sorted in chapter order<br>• Description for “A/D Converter” in **Table 1.2** changed<br>• “Operating frequency” in **Table 1.2** changed from “48 MHz” to “50 MHz”<br>• “version N” and “version D” added to “Operating Temperature” in **Table 1.2**; “optional” deleted<br>• Values for “Current Consumption” in **Table 1.2** added |
| | | 4 | • “version N” and “version D” added to **Table 1.3**<br>• All “version N”s in **Table 1.3** become on planning phase |
| | | 6 | • **Figure 1.2** modified |
| | | 7 | • Note 2 for **Figure 1.3** modified |
| | | 8 | • Scribal error: “CLK5/” (pin No. 21) in **Table 1.4** corrected to “CLK5” |
| | | 11 | • Description for “Connecting pins for decoupling capacitor”, “CNVSS”, and “Debug port” in **Table 1.7** modified |
| | | 12 | • Some descriptions for “$\overline{\text{WR0}}$/$\overline{\text{WR1}}$/$\overline{\text{WR}}$/$\overline{\text{BC0}}$/$\overline{\text{BC1}}$/$\overline{\text{RD}}$” of “Bus control pins” in **Table 1.8** modified |
| | | 13, 14 | • Functional category items in **Tables 1.9 and 1.10** sorted in chapter order; Descriptions modified |
| | | | Chapter 2 |
| | | — | • Descriptions for this chapter modified; Expression “DMAC-related registers”s modified to “DMAC-associated registers”s |
| | | 15 | • “Data register” and “Address register” in **Figure 2.1** pluralized; Explanation in Notes 1 and 2 for this figure revised |

## General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.