Renesas Electronics America Inc - R5F6411FDFN#UA Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	R32C/100
Core Size	16/32-Bit
Speed	50MHz
Connectivity	EBI/EMI, I²C, IEBus, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	49
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f6411fdfn-ua

Table 1.12 Pin Definitions and Functions for the 100-pin Package (2/4)

Function	Symbol	I/O	Power Supply	Description
Bus control pins	A0/D0 to A7/D7	I/O	VCC2	Output of address bits (A0 to A7) and input/output of data (D0 to D7) by time-division while accessing an external memory space with multiplexed bus
	A8/D8 to A15/D15	I/O	VCC2	Output of address bits (A8 to A15) and input/output of data (D8 to D15) by time-division while accessing an external memory space with 16-bit multiplexed bus
	$\overline{BC0}$/D0	I/O	VCC2	Output of byte control ($\overline{BC0}$) and input/output of data (D0) by time-division while accessing an external memory space with multiplexed bus
	$\overline{CS0}$ to $\overline{CS3}$	O	VCC2	Chip select output
	$\overline{WR0}$/$\overline{WR1}$/$\overline{WR}$/ $\overline{BC0}$/$\overline{BC1}$/$\overline{RD}$	O	VCC2	Output of write, byte control, and read signals. Either $\overline{WRx}$ or $\overline{WR}$ and $\overline{BCx}$ can be selected by a program. Data is read when $\overline{RD}$ is low. • When $\overline{WR0}$, $\overline{WR1}$, and $\overline{RD}$ are selected, data is written to the following address: an even address, when $\overline{WR0}$ is low an odd address, when $\overline{WR1}$ is low on 16-bit external data bus • When $\overline{WR}$, $\overline{BC0}$, $\overline{BC1}$, and $\overline{RD}$ are selected, data is written, when $\overline{WR}$ is low and the following address is accessed: an even address, when $\overline{BC0}$ is low an odd address, when $\overline{BC1}$ is low on 16-bit external data bus
	ALE	O	VCC2	Latch enable signal in multiplexed bus format
	$\overline{HOLD}$	I	VCC2	The MCU is in a hold state while this pin is held low
	$\overline{HLDA}$	O	VCC2	This pin is driven low while the MCU is held in a hold state
	$\overline{RDY}$	I	VCC2	Bus cycle is extended by the CPU if this pin is low on the falling edge of BCLK

2.1.8.5 Register Bank Select Flag (B flag)

This flag selects a register bank. It indicates 0 when register bank 0 is selected, and 1 when register bank 1 is selected.

2.1.8.6 Overflow Flag (O flag)

This flag becomes 1 when the result of an operation overflows; otherwise it is 0.

2.1.8.7 Interrupt Enable Flag (I flag)

This flag enables maskable interrupts. To disable maskable interrupts, set this flag to 0. To enable them, set this flag to 1. When an interrupt is accepted, the flag becomes 0.

2.1.8.8 Stack Pointer Select Flag (U flag)

To select the interrupt stack pointer (ISP), set this flag to 0. To select the user stack pointer (USP), set this flag to 1.
It becomes 0 when a hardware interrupt is accepted or when an INT instruction designated by a software interrupt number from 0 to 127 is executed.

2.1.8.9 Floating-point Underflow Flag (FU flag)

This flag becomes 1 when an underflow occurs in a floating-point operation; otherwise it is 0. It also becomes 1 when the operand contains invalid numbers (subnormal numbers).

2.1.8.10 Floating-point Overflow Flag (FO flag)

This flag becomes 1 when an overflow occurs in a floating-point operation; otherwise it is 0. It also becomes 1 when the operand contains invalid numbers (subnormal numbers).

2.1.8.11 Processor Interrupt Priority Level (IPL)

The processor interrupt priority level (IPL), consisting of 3 bits, selects a processor interrupt priority level from level 0 to 7. An interrupt is enabled when the interrupt request level is higher than the selected IPL.
When the processor interrupt priority level (IPL) is set to 111b (level 7), all interrupts are disabled.

2.1.8.12 Fixed-point Radix Point Designation Bit (DP bit)

This bit designates the radix point. It also specifies which portion of the fixed-point multiplication result to extract. It is used for the MULX instruction.

2.1.8.13 Floating-point Rounding Mode (RND)

The 2-bit floating-point rounding mode selects a rounding mode for floating-point calculation results.

2.1.8.14 Reserved

Only set this bit to 0. The read value is undefined.

3. Memory

Figure 3.1 shows the memory map of the R32C/111 Group.
The R32C/111 Group provides a 4-Gbyte address space from 00000000h to FFFFFFFFh.

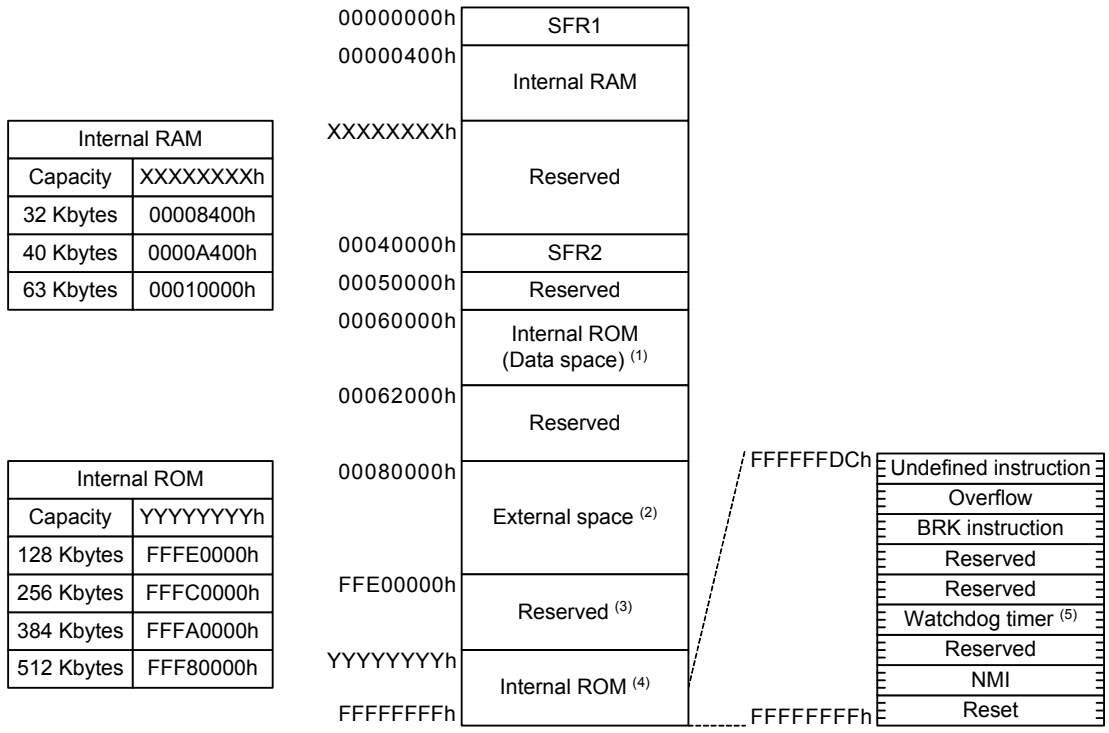
The internal ROM is mapped from address FFFFFFFFh in the inferior direction. For example, the 512-Kbyte internal ROM is mapped from FFF80000h to FFFFFFFFh.
The fixed interrupt vector table contains the start address of interrupt handlers and is mapped from FFFFFFDCh to FFFFFFFFh.
The internal RAM is mapped from address 00000400h in the superior direction. For example, the 63-Kbyte internal RAM is mapped from 00000400h to 0000FFFFh. Besides being used for data storage, the internal RAM functions as a stack(s) for subroutine calls and/or interrupt handlers.

Special function registers (SFRs), which are control registers for peripheral functions, are mapped from 00000000h to 000003FFh, and from 00040000h to 0004FFFFh. Unoccupied SFR locations are reserved, and no access is allowed.

In memory expansion mode or microprocessor mode, some spaces are reserved for internal use and should not be accessed.

Internal RAM	
Capacity	XXXXXXXXh
32 Kbytes	00008400h
40 Kbytes	0000A400h
63 Kbytes	00010000h

Internal ROM	
Capacity	YYYYYYYYh
128 Kbytes	FFFE0000h
256 Kbytes	FFFC0000h
384 Kbytes	FFFA0000h
512 Kbytes	FFF80000h



Notes:
1. The flash memory version provides two additional 4-Kbyte spaces (blocks A and B) for storing data.
2. This space can be used in memory expansion mode or microprocessor mode. Addresses from 02000000h to FDFFFFFFh are inaccessible.
3. This space is reserved in memory expansion mode. It becomes an external space in microprocessor mode.
4. This space can be used in single-chip mode or memory expansion mode. It becomes an external space in microprocessor mode.
5. The watchdog timer interrupt shares a vector with the oscillator stop detection interrupt and low voltage detection interrupt.

Figure 3.1 Memory Map

Table 4.2 SFR List (2)

Address	Register	Symbol	Reset Value
000060h			
000061h	Timer B5 Interrupt Control Register	TB5IC	XXXX X000b
000062h	UART5 Transmit/NACK Interrupt Control Register	S5TIC	XXXX X000b
000063h	UART2 Receive/ACK Interrupt Control Register	S2RIC	XXXX X000b
000064h	UART6 Transmit/NACK Interrupt Control Register	S6TIC	XXXX X000b
000065h	UART3 Receive/ACK Interrupt Control Register	S3RIC	XXXX X000b
000066h	UART5/6 Bus Collision, START Condition/STOP Condition Detection Interrupt Control Register	BCN5IC/BCN6IC	XXXX X000b
000067h	UART4 Receive/ACK Interrupt Control Register	S4RIC	XXXX X000b
000068h	DMA0 Transfer Complete Interrupt Control Register	DM0IC	XXXX X000b
000069h	UART0/3 Bus Collision, START Condition/STOP Condition Detection Interrupt Control Register	BCN0IC/BCN3IC	XXXX X000b
00006Ah	DMA2 Transfer Complete Interrupt Control Register	DM2IC	XXXX X000b
00006Bh	A/D Converter 0 Convert Completion Interrupt Control Register	AD0IC	XXXX X000b
00006Ch	Timer A0 Interrupt Control Register	TA0IC	XXXX X000b
00006Dh	Intelligent I/O Interrupt Control Register 0	IIO0IC	XXXX X000b
00006Eh	Timer A2 Interrupt Control Register	TA2IC	XXXX X000b
00006Fh	Intelligent I/O Interrupt Control Register 2	IIO2IC	XXXX X000b
000070h	Timer A4 Interrupt Control Register	TA4IC	XXXX X000b
000071h	Intelligent I/O Interrupt Control Register 4	IIO4IC	XXXX X000b
000072h	UART0 Receive/ACK Interrupt Control Register	S0RIC	XXXX X000b
000073h	Intelligent I/O Interrupt Control Register 6	IIO6IC	XXXX X000b
000074h	UART1 Receive/ACK Interrupt Control Register	S1RIC	XXXX X000b
000075h	Intelligent I/O Interrupt Control Register 8	IIO8IC	XXXX X000b
000076h	Timer B1 Interrupt Control Register	TB1IC	XXXX X000b
000077h	Intelligent I/O Interrupt Control Register 10	IIO10IC	XXXX X000b
000078h	Timer B3 Interrupt Control Register	TB3IC	XXXX X000b
000079h			
00007Ah	INT5 Interrupt Control Register	INT5IC	XX00 X000b
00007Bh			
00007Ch	INT3 Interrupt Control Register	INT3IC	XX00 X000b
00007Dh			
00007Eh	INT1 Interrupt Control Register	INT1IC	XX00 X000b
00007Fh			
000080h			
000081h	UART2 Transmit/NACK Interrupt Control Register	S2TIC	XXXX X000b
000082h	UART5 Receive/ACK Interrupt Control Register	S5RIC	XXXX X000b
000083h	UART3 Transmit/NACK Interrupt Control Register	S3TIC	XXXX X000b
000084h	UART6 Receive/ACK Interrupt Control Register	S6RIC	XXXX X000b
000085h	UART4 Transmit/NACK Interrupt Control Register	S4TIC	XXXX X000b
000086h			
000087h	UART2 Bus Collision, START Condition/STOP Condition Detection Interrupt Control Register	BCN2IC	XXXX X000b

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.7 SFR List (7)

Address	Register	Symbol	Reset Value
000140h	Group 2 Waveform Generation Register 0	G2PO0	XXXXh
000141h			
000142h	Group 2 Waveform Generation Register 1	G2PO1	XXXXh
000143h			
000144h	Group 2 Waveform Generation Register 2	G2PO2	XXXXh
000145h			
000146h	Group 2 Waveform Generation Register 3	G2PO3	XXXXh
000147h			
000148h	Group 2 Waveform Generation Register 4	G2PO4	XXXXh
000149h			
00014Ah	Group 2 Waveform Generation Register 5	G2PO5	XXXXh
00014Bh			
00014Ch	Group 2 Waveform Generation Register 6	G2PO6	XXXXh
00014Dh			
00014Eh	Group 2 Waveform Generation Register 7	G2PO7	XXXXh
00014Fh			
000150h	Group 2 Waveform Generation Control Register 0	G2POCR0	0000 0000b
000151h	Group 2 Waveform Generation Control Register 1	G2POCR1	0000 0000b
000152h	Group 2 Waveform Generation Control Register 2	G2POCR2	0000 0000b
000153h	Group 2 Waveform Generation Control Register 3	G2POCR3	0000 0000b
000154h	Group 2 Waveform Generation Control Register 4	G2POCR4	0000 0000b
000155h	Group 2 Waveform Generation Control Register 5	G2POCR5	0000 0000b
000156h	Group 2 Waveform Generation Control Register 6	G2POCR6	0000 0000b
000157h	Group 2 Waveform Generation Control Register 7	G2POCR7	0000 0000b
000158h			
000159h			
00015Ah			
00015Bh			
00015Ch			
00015Dh			
00015Eh			
00015Fh			
000160h	Group 2 Base Timer Register	G2BT	XXXXh
000161h			
000162h	Group 2 Base Timer Control Register 0	G2BCR0	0000 0000b
000163h	Group 2 Base Timer Control Register 1	G2BCR1	0000 0000b
000164h	Base Timer Start Register	BTSR	XXXX 0000b
000165h			
000166h	Group 2 Function Enable Register	G2FE	00h
000167h	Group 2 RTP Output Buffer Register	G2RTP	00h
000168h			
000169h			
00016Ah	Group 2 Serial Interface Mode Register	G2MR	00XX X000b
00016Bh	Group 2 Serial Interface Control Register	G2CR	0000 X110b
00016Ch	Group 2 SI/O Transmit Buffer Register	G2TB	XXXXh
00016Dh			
00016Eh	Group 2 SI/O Receive Buffer Register	G2RB	XXXXh
00016Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.14 SFR List (14)

Address	Register	Symbol	Reset Value
000350h	Timer B0 Register	TB0	XXXXh
000351h			
000352h	Timer B1 Register	TB1	XXXXh
000353h			
000354h	Timer B2 Register	TB2	XXXXh
000355h			
000356h	Timer A0 Mode Register	TA0MR	0000 0000b
000357h	Timer A1 Mode Register	TA1MR	0000 0000b
000358h	Timer A2 Mode Register	TA2MR	0000 0000b
000359h	Timer A3 Mode Register	TA3MR	0000 0000b
00035Ah	Timer A4 Mode Register	TA4MR	0000 0000b
00035Bh	Timer B0 Mode Register	TB0MR	00XX 0000b
00035Ch	Timer B1 Mode Register	TB1MR	00XX 0000b
00035Dh	Timer B2 Mode Register	TB2MR	00XX 0000b
00035Eh	Timer B2 Special Mode Register	TB2SC	XXXX XXX0b
00035Fh	Count Source Prescaler Register	TCSPR	0000 0000b
000360h			
000361h			
000362h			
000363h			
000364h	UART0 Special Mode Register 4	U0SMR4	00h
000365h	UART0 Special Mode Register 3	U0SMR3	00h
000366h	UART0 Special Mode Register 2	U0SMR2	00h
000367h	UART0 Special Mode Register	U0SMR	00h
000368h	UART0 Transmit/Receive Mode Register	U0MR	00h
000369h	UART0 Bit Rate Register	U0BRG	XXh
00036Ah	UART0 Transmit Buffer Register	U0TB	XXXXh
00036Bh			
00036Ch	UART0 Transmit/Receive Control Register 0	U0C0	0000 1000b
00036Dh	UART0 Transmit/Receive Control Register 1	U0C1	0000 0010b
00036Eh	UART0 Receive Buffer Register	U0RB	XXXXh
00036Fh			
000370h			
000371h			
000372h			
000373h			
000374h			
000375h			
000376h			
000377h			
000378h			
000379h			
00037Ah			
00037Bh			
00037Ch	CRC Data Register	CRCD	XXXXh
00037Dh			
00037Eh	CRC Input Register	CRCIN	XXh
00037Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.15 SFR List (15)

Address	Register	Symbol	Reset Value
000380h	A/D0 Register 0	AD00	00XXh
000381h			
000382h	A/D0 Register 1	AD01	00XXh
000383h			
000384h	A/D0 Register 2	AD02	00XXh
000385h			
000386h	A/D0 Register 3	AD03	00XXh
000387h			
000388h	A/D0 Register 4	AD04	00XXh
000389h			
00038Ah	A/D0 Register 5	AD05	00XXh
00038Bh			
00038Ch	A/D0 Register 6	AD06	00XXh
00038Dh			
00038Eh	A/D0 Register 7	AD07	00XXh
00038Fh			
000390h			
000391h			
000392h	A/D0 Control Register 4	AD0CON4	XXXX 00XXb
000393h			
000394h	A/D0 Control Register 2	AD0CON2	XX0X X000b
000395h	A/D0 Control Register 3	AD0CON3	XXXX X000b
000396h	A/D0 Control Register 0	AD0CON0	00h
000397h	A/D0 Control Register 1	AD0CON1	00h
000398h	D/A Register 0	DA0	XXh
000399h			
00039Ah	D/A Register 1	DA1	XXh
00039Bh			
00039Ch	D/A Control Register	DACON	XXXX XX00b
00039Dh			
00039Eh			
00039Fh			
0003A0h			
0003A1h			
0003A2h			
0003A3h			
0003A4h			
0003A5h			
0003A6h			
0003A7h			
0003A8h			
0003A9h			
0003AAh			
0003ABh			
0003ACh			
0003ADh			
0003AEh			
0003AFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.22 SFR List (22)

Address	Register	Symbol	Reset Value
0400F0h	Port P10_0 Function Select Register	P10_0S	0XXX X000b
0400F1h			
0400F2h	Port P10_1 Function Select Register	P10_1S	0XXX X000b
0400F3h			
0400F4h	Port P10_2 Function Select Register	P10_2S	0XXX X000b
0400F5h			
0400F6h	Port P10_3 Function Select Register	P10_3S	0XXX X000b
0400F7h			
0400F8h	Port P10_4 Function Select Register	P10_4S	0XXX X000b
0400F9h			
0400FAh	Port P10_5 Function Select Register	P10_5S	0XXX X000b
0400FBh			
0400FCh	Port P10_6 Function Select Register	P10_6S	0XXX X000b
0400FDh			
0400FEh	Port P10_7 Function Select Register	P10_7S	0XXX X000b
0400FFh			
040100h			
040101h			
040102h			
040103h			
040104h			
040105h			
040106h			
040107h			
040108h			
040109h			
04010Ah			
04010Bh			
04010Ch			
04010Dh			
04010Eh			
04010Fh			
040110h			
040111h			
040112h			
040113h			
040114h			
040115h			
040116h			
040117h			
040118h			
040119h			
04011Ah			
04011Bh			
04011Ch			
04011Dh			
04011Eh			
04011Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 5.3 Operating Conditions (2/5)
(V_{CC1} = V_{CC2} = 3.0 to 5.5 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted) (1)

Symbol	Characteristic		Value (2)			Unit
			Min.	Typ.	Max.	
C_{VDC}	Decoupling capacitance for voltage regulator	Inter-pin voltage: 1.5 V	2.4		10.0	µF

Notes:
1. The device is operationally guaranteed under these operating conditions.
2. This value should be met with due consideration to the following conditions: operating temperature, DC bias, aging, etc.

Table 5.7 Electrical Characteristics of RAM
(V_{CC1} = V_{CC2} = 3.0 to 5.5 V, V_{SS} = 0 V, and Ta = T_{opr}, unless otherwise noted)

Symbol	Characteristic	Measurement Condition	Value			Unit
			Min.	Typ.	Max.	
V_{RDR}	RAM data retention voltage (1)	In stop mode	2.0			V

Note:
1. The value listed in the table is the minimum V_{CC1} to retain RAM data.

Table 5.8 Electrical Characteristics of Flash Memory
(V_{CC1} = V_{CC2} = 3.0 to 5.5 V, V_{SS} = 0 V, and Ta = T_{opr}, unless otherwise noted)

Symbol	Characteristic		Value			Unit
			Min.	Typ.	Max.	
—	Program/erase cycles (1)	Program area	1000			Cycles
		Data area	10000			Cycles
—	4-word program time	Program area		150	900	µs
		Data area		300	1700	µs
—	Lock bit program time	Program area		70	500	µs
		Data area		140	1000	µs
—	Block erasure time	4-Kbyte block		0.12	3.0	s
		32-Kbyte block		0.17	3.0	s
		64-Kbyte block		0.20	3.0	s
—	Data retention (2)	T_a = 55°C (3)	10			Years

Notes:
1. Program/erase definition
   This value represents the number of erasures per block.
   When the number of program/erase cycles is n, each block can be erased n times.
   For example, if a 4-word write is performed in 512 different addresses in the 4-Kbyte block A and then the block is erased, this is counted as a single program/erase operation.
   However, the same address cannot be written to more than once per erasure (overwrite disabled).
2. Data retention includes periods when no supply voltage is applied and no clock is provided.
3. Contact a Renesas Electronics sales office for data retention times other than the above condition.

Table 5.12 Electrical Characteristics of Oscillator
(V_{CC1} = V_{CC2} = 3.0 to 5.5 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Symbol	Characteristics	Measurement Condition	Value			Unit
			Min.	Typ.	Max.	
$f_{SO(PLL)}$	PLL clock self-oscillation frequency		35	55	80	MHz
$t_{LOCK(PLL)}$	PLL lock time (1)				1	ms
$t_{jitter(p-p)}$	PLL jitter period (p-p)				2.0	ns
$f_{(OCO)}$	On-chip oscillator frequency		62.5	125	250	kHz

Note:
1. This value is applicable only when the main clock oscillation is stable.

Table 5.13 Electrical Characteristics of Clock Circuitry
(V_{CC1} = V_{CC2} = 3.0 to 5.5 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Symbol	Characteristics	Measurement Condition	Value			Unit
			Min.	Typ.	Max.	
$t_{rec(WAIT)}$	Recovery time from wait mode to low power mode				225	µs
$t_{rec(STOP)}$	Recovery time from stop mode (1)				225	µs

Note:
1. The recovery time from stop mode does not include the main clock oscillation stabilization time. The CPU starts operating before the oscillator is stabilized.

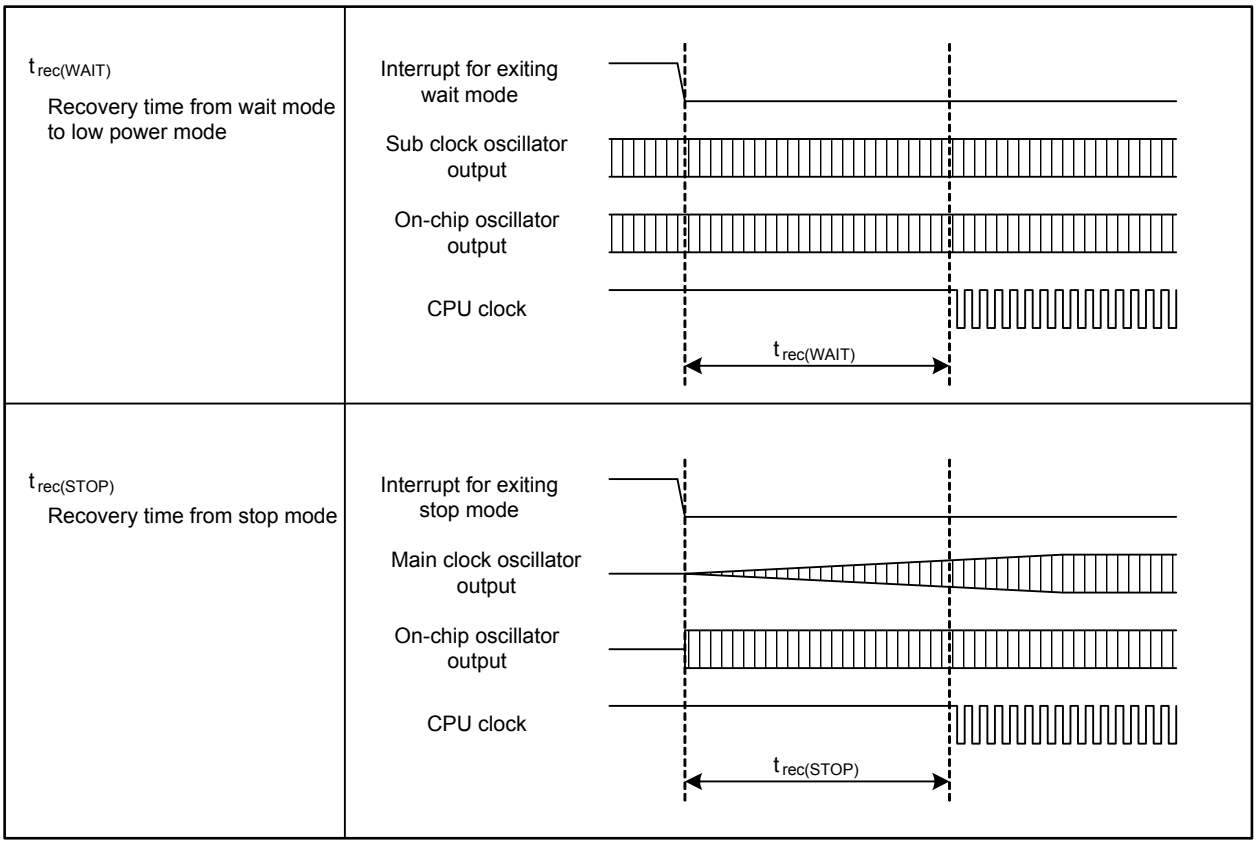


Figure 5.4 Clock Circuit Timing

$V_{CC1} = V_{CC2} = 5\ V$

Table 5.15 Electrical Characteristics (1/3)
($V_{CC1} = V_{CC2} = 4.2$ to 5.5 V, $V_{SS} = 0$ V, $T_a = T_{opr}$, and $f_{(CPU)} = 50$ MHz, unless otherwise noted)

Symbol	Characteristic		Measurement Condition	Value (2)			Unit
				Min.	Typ.	Max.	
V_{OH}	High level output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7 (1)	I_{OH} = -5 mA	V_{CC2} -2.0		V_{CC2}	V
		P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_3 to P9_7, P10_0 to P10_7 (1)	I_{OH} = -5 mA	V_{CC1} -2.0		V_{CC1}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7 (1)	I_{OH} = -200 µA	V_{CC2} -0.3		V_{CC2}	V
		P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_3 to P9_7, P10_0 to P10_7 (1)	I_{OH} = -200 µA	V_{CC1} -0.3		V_{CC1}	V
V_{OL}	Low level output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_3 to P9_7, P10_0 to P10_7 (1)	I_{OL} = 5 mA			2.0	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_3 to P9_7, P10_0 to P10_7 (1)	I_{OL} = 200 µA			0.45	V

Notes:
1. Ports P0_4 to P0_7, P1_0 to P1_4, P3_4 to P3_7, P4, P5, and P9_4 to P9_7 are available in the 100-pin package only.
2. The V_{CC2} pin is available in the 100-pin package only. It should be considered as V_{CC1} in the 64-pin package.

$V_{CC1} = V_{CC2} = 5\ V$

Table 5.18 A/D Conversion Characteristics ($V_{CC1} = V_{CC2} = AV_{CC} = V_{REF} = 4.2$ to 5.5 V, $V_{SS} = AV_{SS} = 0$ V, $T_a = T_{opr}$, and $f_{(BCLK)} = 25$ MHz, unless otherwise noted)

Symbol	Characteristic	Measurement Condition		Value			Unit
				Min.	Typ.	Max.	
—	Resolution	$V_{REF} = V_{CC1}$				10	Bits
—	Absolute error	$V_{REF} = V_{CC1} = V_{CC2} = 5$ V	AN_0 to AN_7, AN0_0 to AN0_7, AN2_0 to AN2_7, ANEX0, ANEX1 (1)			±3	LSB
			External op-amp connection mode			±7	LSB
INL	Integral non-linearity error	$V_{REF} = V_{CC1} = V_{CC2} = 5$ V	AN_0 to AN_7, AN0_0 to AN0_7, AN2_0 to AN2_7, ANEX0, ANEX1 (1)			±3	LSB
			External op-amp connection mode			±7	LSB
DNL	Differential non-linearity error					±1	LSB
—	Offset error					±3	LSB
—	Gain error					±3	LSB
R_{LADDER}	Resistor ladder	$V_{REF} = V_{CC1}$		4		20	kΩ
t_{CONV}	Conversion time (10 bits)	ϕ_{AD} = 16 MHz, with sample and hold function		2.06			µs
		ϕ_{AD} = 16 MHz, without sample and hold function		3.69			µs
t_{CONV}	Conversion time (8 bits)	ϕ_{AD} = 16 MHz, with sample and hold function		1.75			µs
		ϕ_{AD} = 16 MHz, without sample and hold function		3.06			µs
t_{SAMP}	Sampling time	ϕ_{AD} = 16 MHz		0.188			µs
V_{IA}	Analog input voltage			0		V_{REF}	V
ϕ_{AD}	Operating clock frequency	Without sample and hold function		0.25		16	MHz
		With sample and hold function		1		16	MHz

Note:
1. Pins AN0_4 to AN0_7, ANEX0, and ANEX1 are available in the 100-pin package only.

$V_{CC1} = V_{CC2} = 3.3$ V

Table 5.42 D/A Conversion Characteristics ($V_{CC1} = V_{CC2} = AV_{CC} = V_{REF}$ = 3.0 to 3.6 V, $V_{SS} = AV_{SS}$ = 0 V, and $T_a = T_{opr}$, unless otherwise noted)

Symbol	Characteristic	Measurement Condition	Value			Unit
			Min.	Typ.	Max.	
—	Resolution				8	Bits
—	Absolute precision				1.0	%
t_S	Settling time				3	µs
R_O	Output resistance		4	10	20	kΩ
I_{VREF}	Reference input current	See Note 1			1.0	mA

Note:
1. One D/A converter is used. The DAi register (i = 0, 1) of the other unused converter is set to 00h. The resistor ladder for the A/D converter is not considered.
Even when the VCUT bit in the AD0CON1 register is set to 0 (V_{REF} disconnected), I_{VREF} is supplied.

$V_{CC1} = V_{CC2} = 3.3$ V

Timing Requirements ($V_{CC1} = V_{CC2} = 3.0$ to 3.6 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.43 External Clock Input

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(X)}$	External clock input period	62.5	250	ns
$t_{w(XH)}$	External clock input high level pulse width	25		ns
$t_{w(XL)}$	External clock input low level pulse width	25		ns
$t_{r(X)}$	External clock input rise time		5	ns
$t_{f(X)}$	External clock input fall time		5	ns
t_w / t_c	External clock input duty	40	60	%

Table 5.44 External Bus Timing

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{su(D-R)}$	Data setup time before read	40		ns
$t_{h(R-D)}$	Data hold time after read	0		ns
$t_{dis(R-D)}$	Data disable time after read		$0.5 \times t_{c(Base)} + 10$	ns

V_{CC1} = V_{CC2} = 3.3 V

Switching Characteristics (V_{CC1} = V_{CC2} = 3.0 to 3.6 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Table 5.58 External Bus Timing (multiplexed bus)

Symbol	Characteristic	Measurement Condition	Value		Unit
			Min.	Max.	
$t_{su(S-ALE)}$	Chip-select setup time before ALE	Refer to Figure 5.6	(1)		ns
$t_{h(R-S)}$	Chip-select hold time after read		1.5 × $t_{c(Base)}$ - 10		ns
$t_{su(A-ALE)}$	Address setup time before ALE		(1)		ns
$t_{h(ALE-A)}$	Address hold time after ALE		0.5 × $t_{c(Base)}$ - 5		ns
$t_{h(R-A)}$	Address hold time after read		1.5 × $t_{c(Base)}$ - 10		ns
$t_{d(ALE-R)}$	ALE-read delay time		0.5 × $t_{c(Base)}$ - 5	0.5 × $t_{c(Base)}$ + 10	ns
$t_{w(ALE)}$	ALE pulse width		(1)		ns
$t_{dis(R-A)}$	Address disable time after read			8	ns
$t_{w(R)}$	Read pulse width		(1)		ns
$t_{h(W-S)}$	Chip-select hold time after write		1.5 × $t_{c(Base)}$ - 10		ns
$t_{h(W-A)}$	Address hold time after write		1.5 × $t_{c(Base)}$ - 10		ns
$t_{d(ALE-W)}$	ALE-write delay time		0.5 × $t_{c(Base)}$ - 5	0.5 × $t_{c(Base)}$ + 10	ns
$t_{w(W)}$	Write pulse width		(1)		ns
$t_{su(D-W)}$	Data setup time before write		(1)		ns
$t_{h(W-D)}$	Data hold time after write		0.5 × $t_{c(Base)}$		ns

Note:

1. The value is calculated using the formulas below based on the base clock cycles ($t_{c(Base)}$) and respective cycles of Tsu(A-R), Tw(R), Tsu(A-W), and Tw(W) set by registers EBC0 to EBC3. If the calculation results in a negative value, modify the value to be set. For details on how to set values, refer to the User's manual.

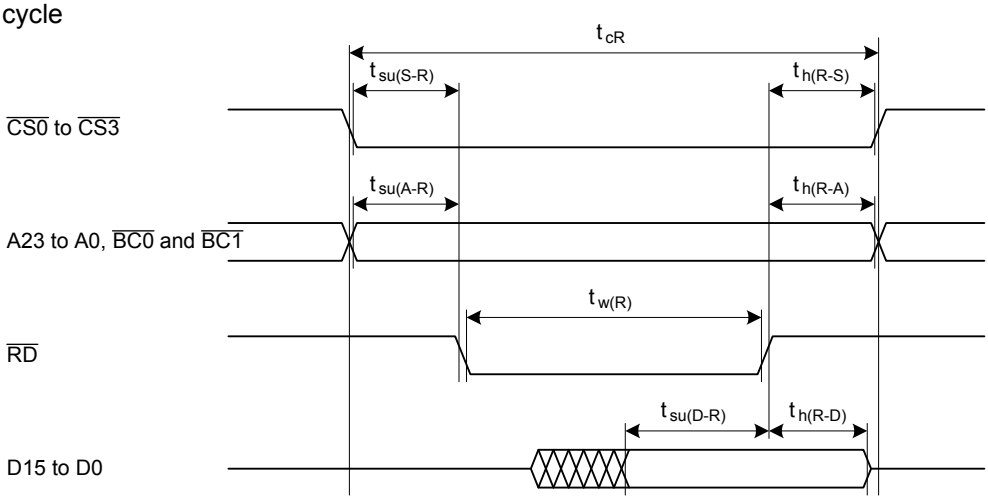
   $t_{su(S-ALE)}$ = $t_{su(A-ALE)}$ = $t_{w(ALE)}$ = (Tsu(A-R) - 0.5) × $t_{c(Base)}$ -15 [ns]

   $t_{w(R)}$ = Tw(R) × $t_{c(Base)}$ -10 [ns]

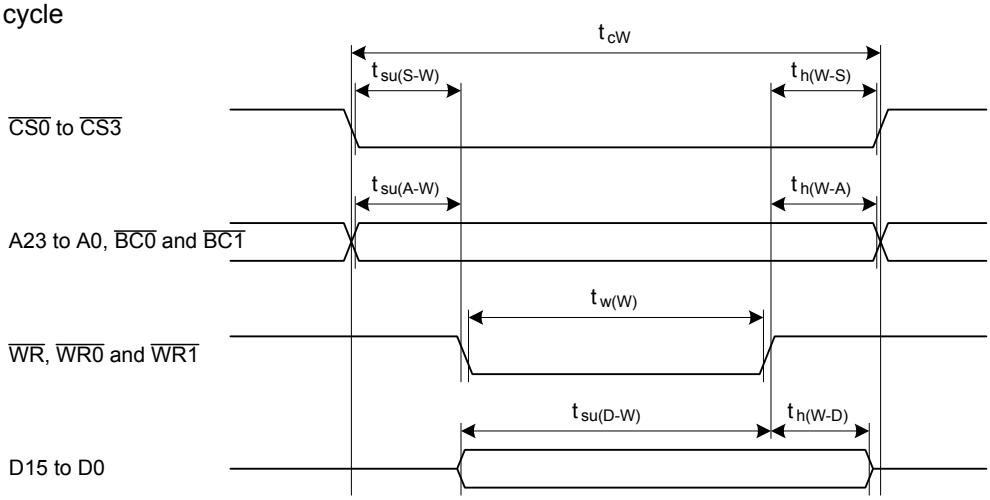
   $t_{w(W)}$ = $t_{su(D-W)}$ = Tw(W) × $t_{c(Base)}$ -10 [ns]

External bus timing (separate bus)

Read cycle



Write cycle



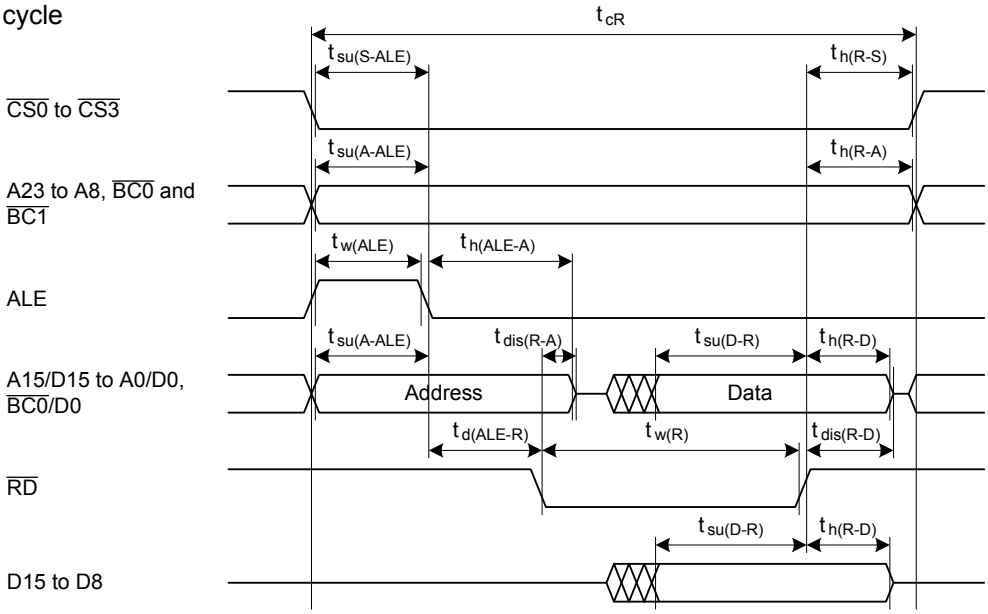
Measurement conditions

Item		$V_{CC1} = V_{CC2} = 4.2$ to 5.5 V	$V_{CC1} = V_{CC2} = 3.0$ to 3.6 V
Criterion for input voltage	V_{IH}	2.5 V	1.5 V
	V_{IL}	0.8 V	0.5 V
Criterion for output voltage	V_{OH}	2.0 V	2.4 V
	V_{OL}	0.8 V	0.5 V

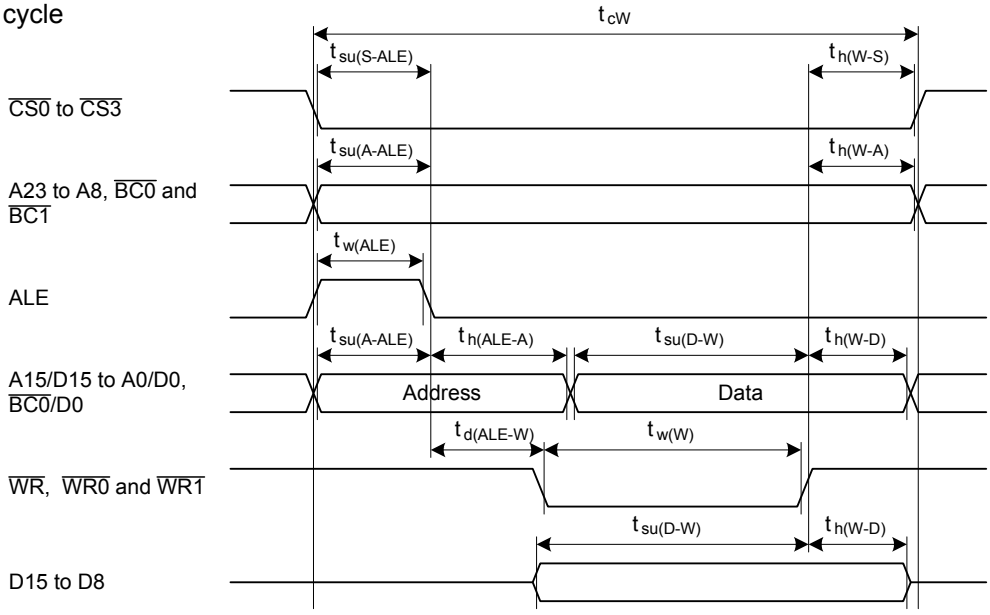
Figure 5.8 External Bus Timing for Separate Bus

External bus timing (multiplexed bus)

Read cycle



Write cycle



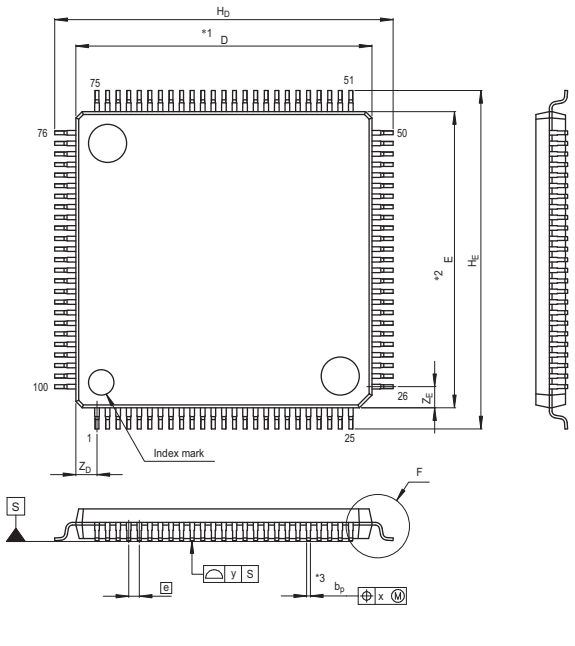
Measurement conditions

Item		$V_{CC1} = V_{CC2} = 4.2$ to 5.5 V	$V_{CC1} = V_{CC2} = 3.0$ to 3.6 V
Criterion for input voltage	V_{IH}	2.5 V	1.5 V
	V_{IL}	0.8 V	0.5 V
Criterion for output voltage	V_{OH}	2.0 V	2.4 V
	V_{OL}	0.8 V	0.5 V

Figure 5.9 External Bus Timing for Multiplexed Bus

Appendix 1. Package Dimensions

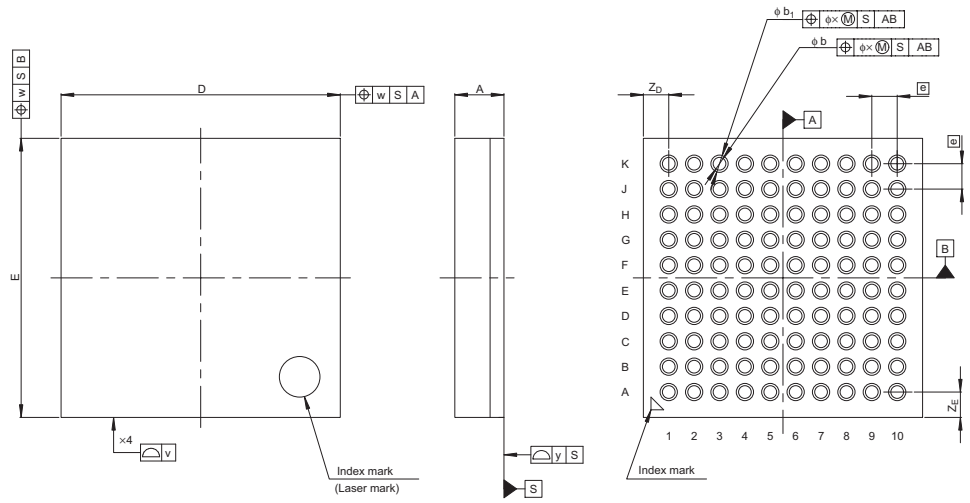
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP100-14x14-0.50	PLQP0100KB-A	100P6Q-A / FP-100U / FP-100UV	0.6g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.35	0.5	0.65
L_1	—	1.0	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TFLGA100-5.5x5.5-0.50	PTLG0100KA-A	100F0M	0.1g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	5.5	—
E	—	5.5	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.05
e	—	0.5	—
b	0.21	0.25	0.29
b_1	0.29	0.34	0.39
x	—	—	0.08
y	—	—	0.10
Z_D	—	0.5	—
Z_E	—	0.5	—

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