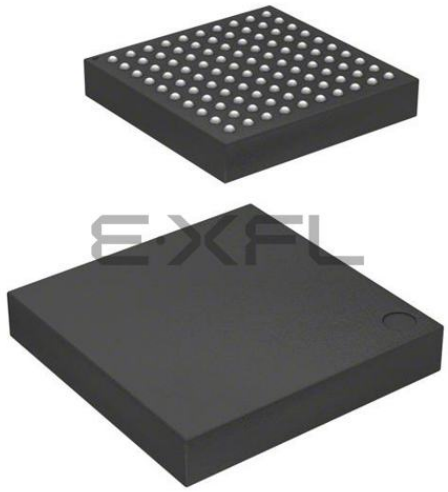

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	R32C/100
Core Size	16/32-Bit
Speed	50MHz
Connectivity	EBI/EMI, I²C, IEBus, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	82
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFLGA
Supplier Device Package	100-TFLGA (5.5x5.5)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f6411fnlg-u0

Table 1.2 Performance Overview for the 100-pin Package (2/2)

Unit	Function	Explanation
Timer	Timer A	16-bit timer × 5 Timer mode, event counter mode, one-shot timer mode, pulse-width modulation (PWM) mode Two-phase pulse signal processing in event counter mode (two-phase encoder input) × 3
	Timer B	16-bit timer × 6 Timer mode, event counter mode, pulse frequency measurement mode, pulse-width measurement mode
	Three-phase motor control timer	Three-phase motor control timer × 1 (timers A1, A2, A4, and B2 used) 8-bit programmable dead time timer
Serial Interface	UART0 to UART8	Asynchronous/synchronous serial interface × 9 channels • I^2C-bus (UART0 to UART6) • Special mode 2 (UART0 to UART6) • IEBus (optional (1)) (UART0 to UART6)
A/D Converter		10-bit resolution × 26 channels Sample and hold functionality integrated
D/A Converter		8-bit resolution × 2
CRC Calculator		CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$)
X-Y Converter		16 bits × 16 bits
Intelligent I/O		Time measurement (input capture): 16 bits × 16 Waveform generation (output compare): 16 bits × 19 Serial interface: Variable-length synchronous serial I/O mode, IEBus mode (optional (1))
Flash Memory		Programming and erasure supply voltage: VCC1 = VCC2 = 3.0 to 5.5 V Minimum endurance: 1,000 program/erase cycles Security protection: ROM code protect, ID code protect Debugging: On-chip debug, on-board flash programming
Operating Frequency/Supply Voltage		50 MHz/VCC1 = 3.0 to 5.5 V, VCC2 = 3.0 V to VCC1
Operating Temperature		-20°C to 85°C (N version) -40°C to 85°C (D version)
Current Consumption		32 mA (VCC1 = VCC2 = 5.0 V, f(CPU) = 50 MHz) 8 µA (VCC1 = VCC2 = 3.3 V, f(XCIN) = 32.768 kHz, in wait mode)
Package		100-pin plastic molded LQFP (PLQP0100KB-A) 100-pin plastic molded TFLGA (PTLG0100KA-A)

Note:
1. Contact a Renesas Electronics sales office to use the optional features.

1.3 Block Diagram

Figures 1.2 and 1.3 show block diagram of the R32C/111 Group.

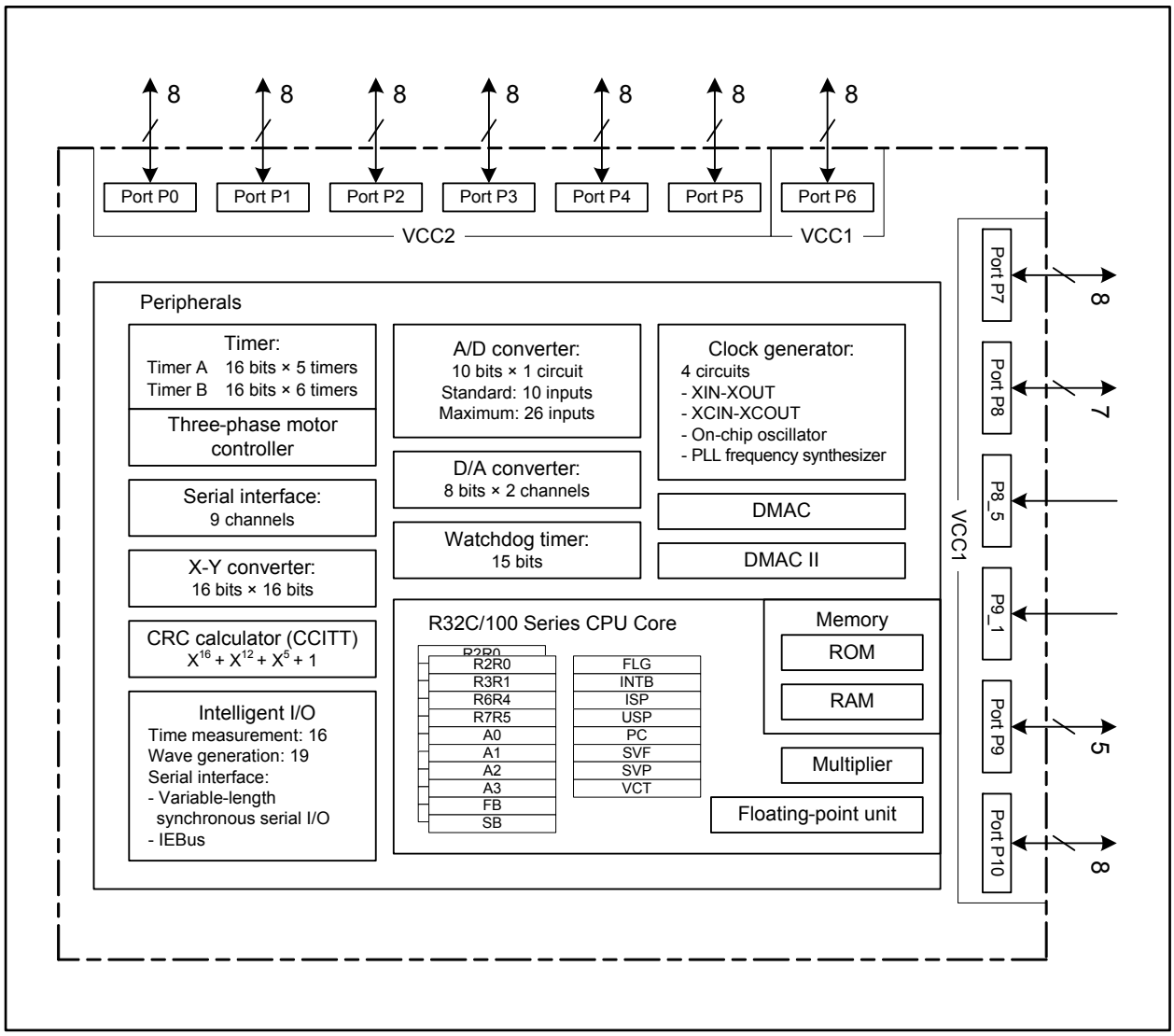


Figure 1.2 R32C/111 Group Block Diagram for the 100-pin Package

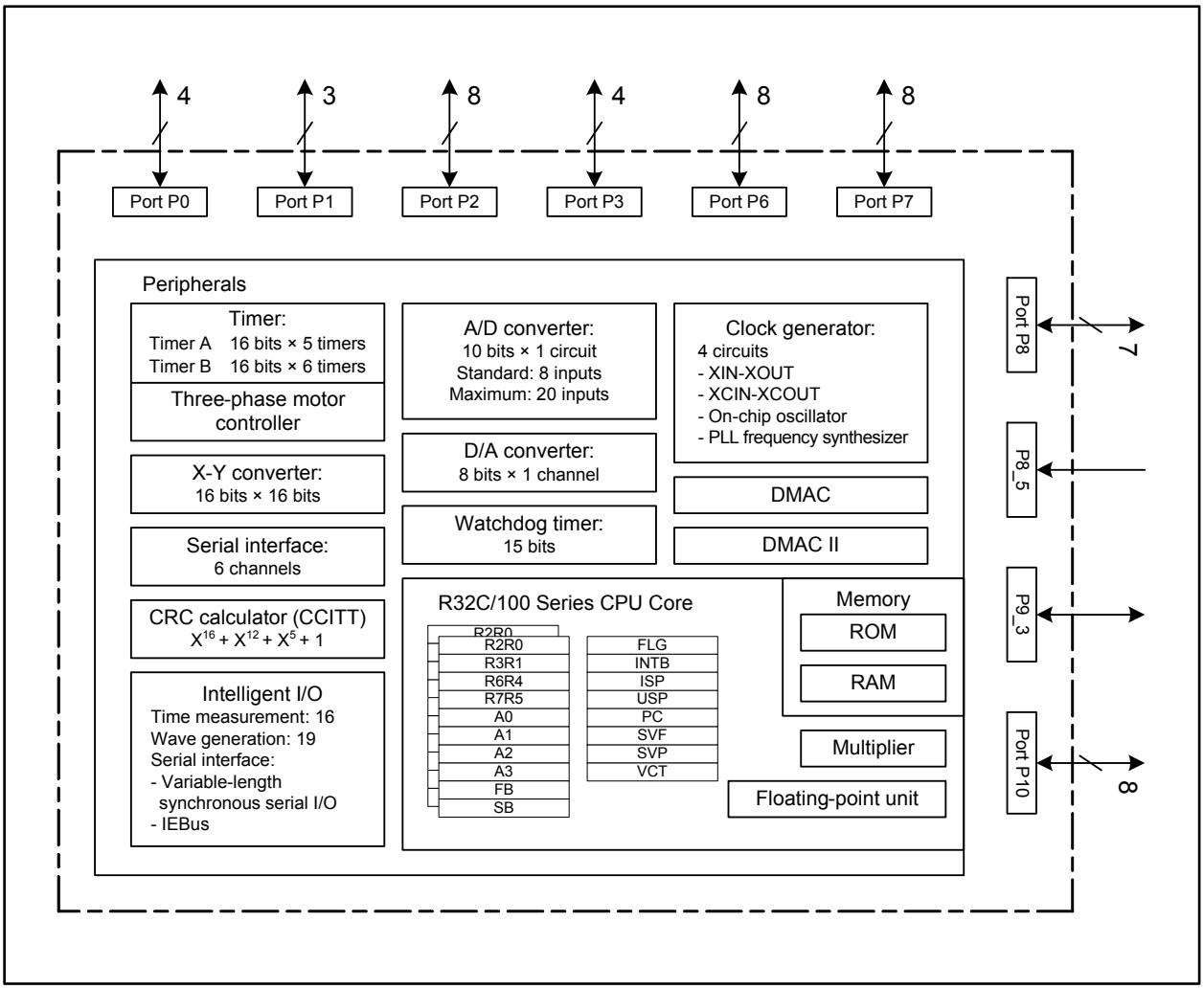
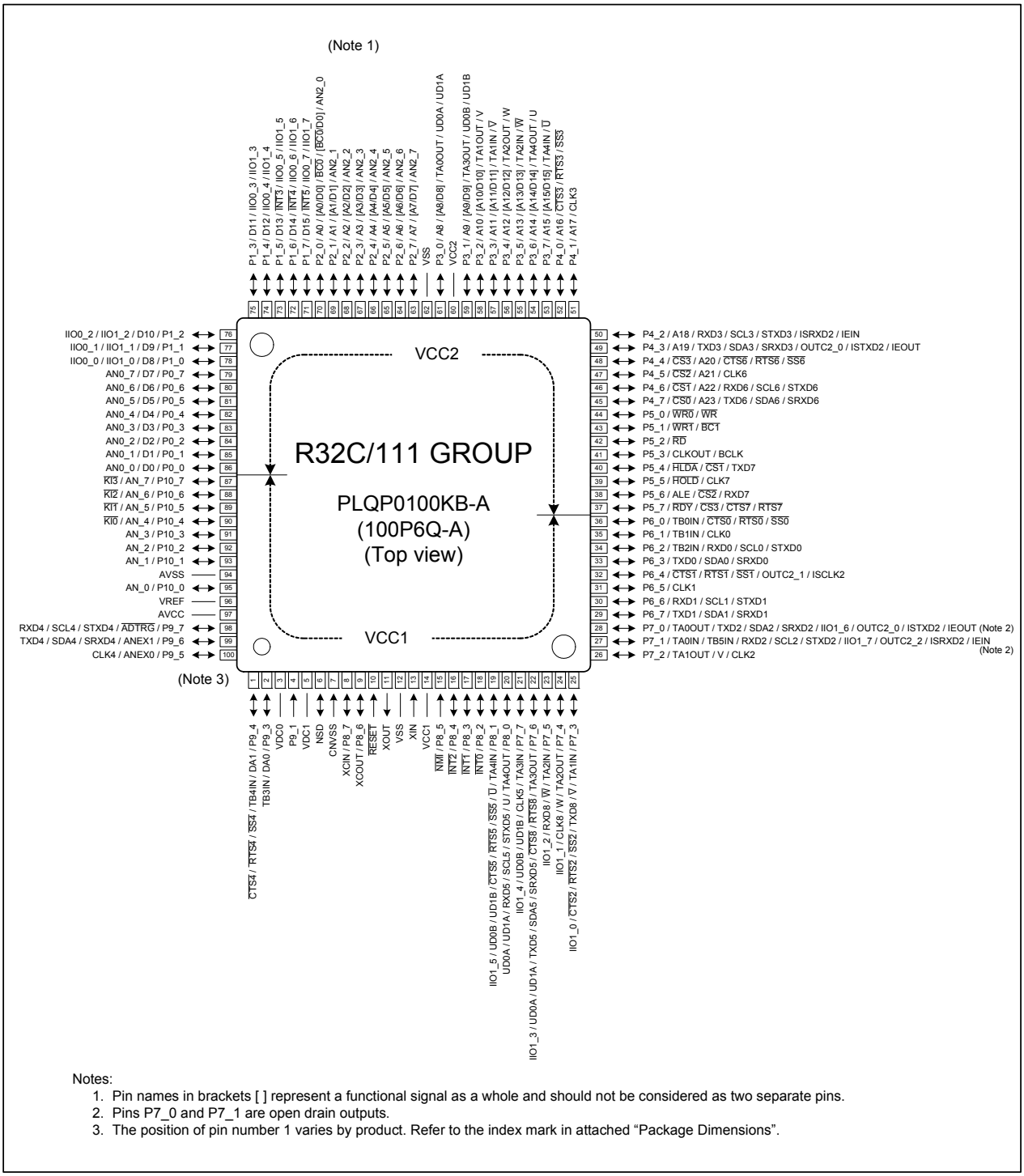


Figure 1.3 R32C/111 Group Block Diagram for the 64-pin Package

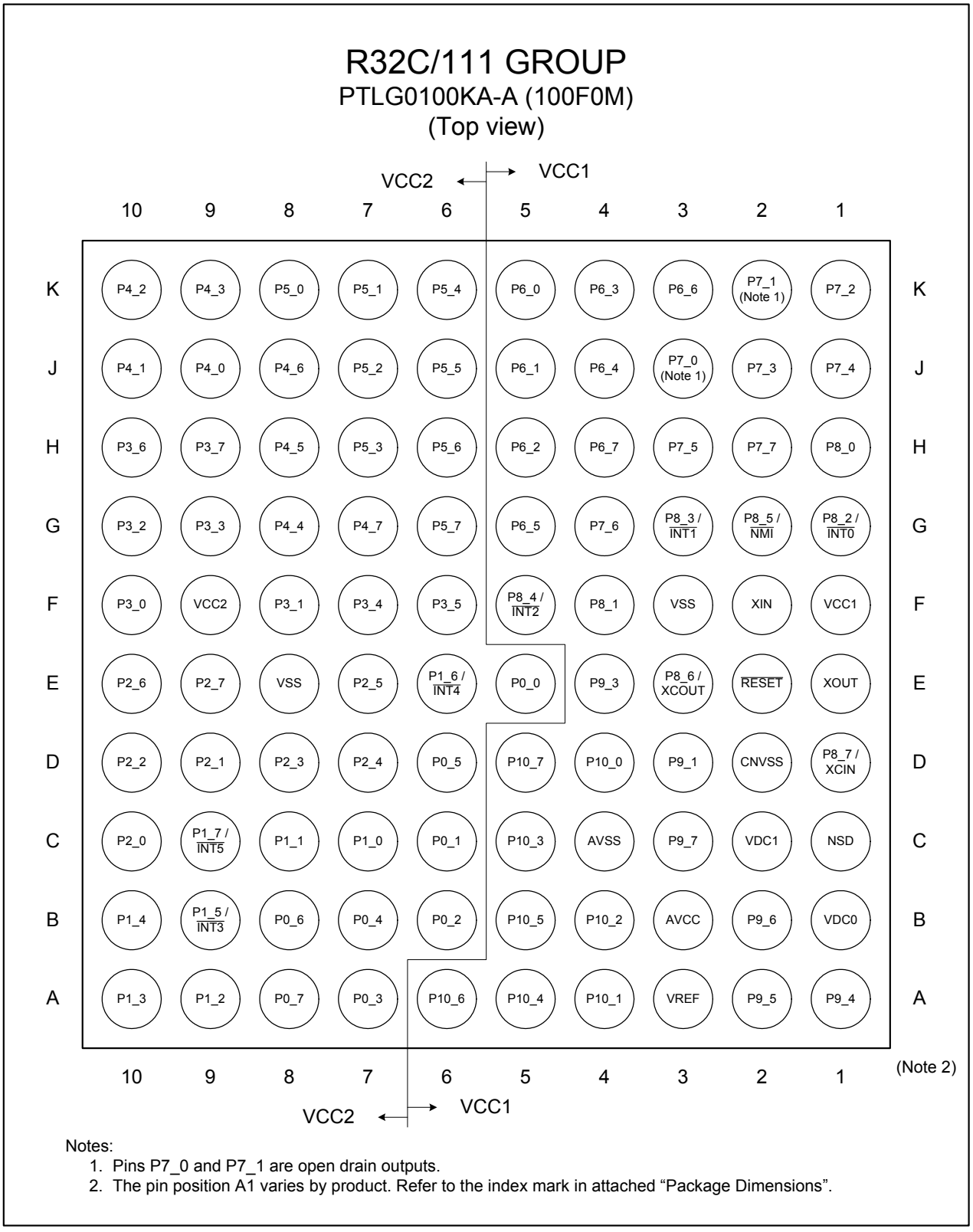
1.4 Pin Assignments

Figures 1.4 to 1.6 show the pin assignments (top view) and Tables 1.6 to 1.10 show the pin characteristics.



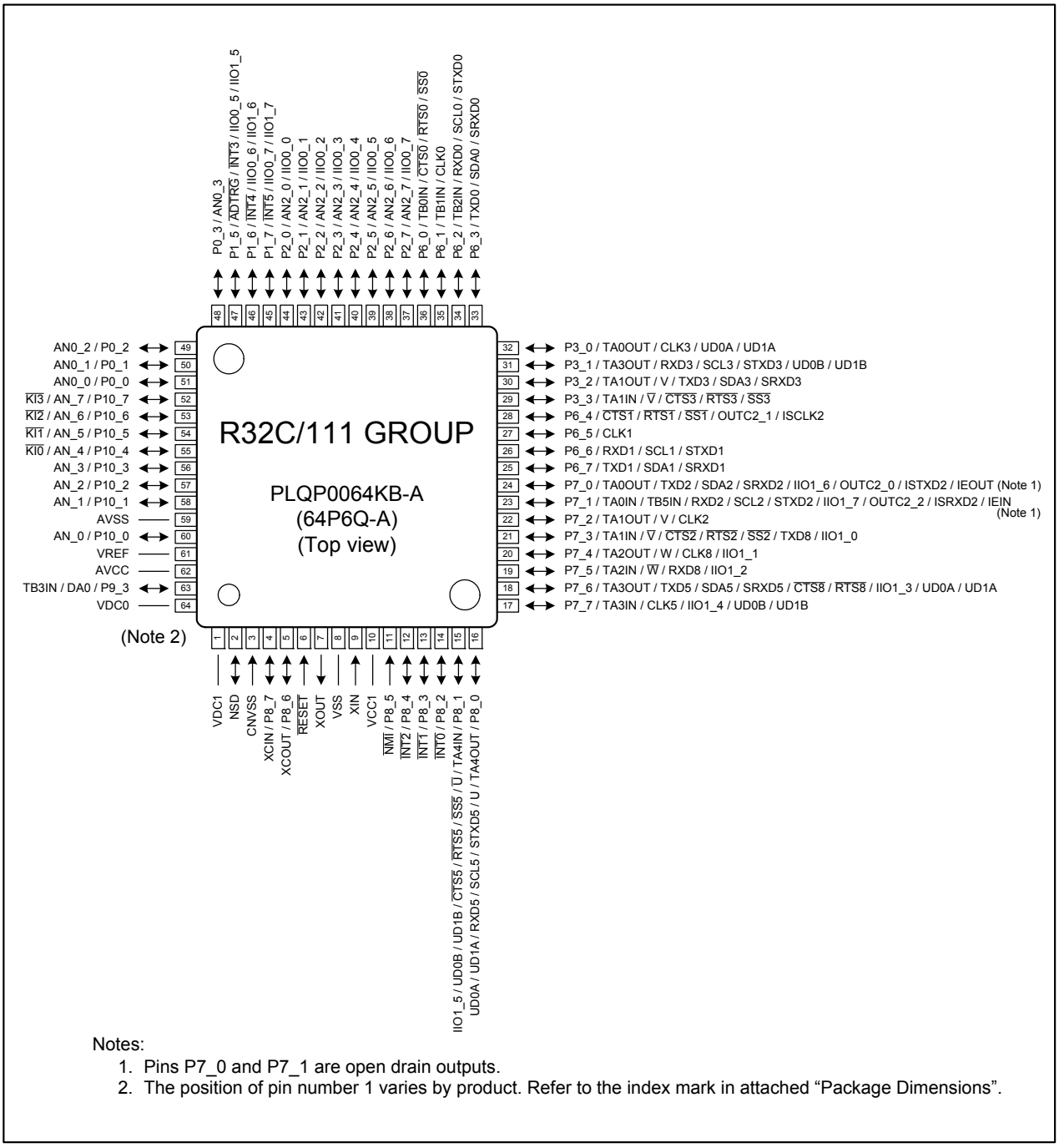
Notes:
1. Pin names in brackets [ ] represent a functional signal as a whole and should not be considered as two separate pins.
2. Pins P7_0 and P7_1 are open drain outputs.
3. The position of pin number 1 varies by product. Refer to the index mark in attached “Package Dimensions”.

Figure 1.4 Pin Assignment for the 100-pin Package (top view)



Notes:
1. Pins P7_0 and P7_1 are open drain outputs.
2. The pin position A1 varies by product. Refer to the index mark in attached “Package Dimensions”.

Figure 1.5 Pin Assignment for the 100-pin LGA Package (top view)



Notes:
1. Pins P7_0 and P7_1 are open drain outputs.
2. The position of pin number 1 varies by product. Refer to the index mark in attached “Package Dimensions”.

Figure 1.6 Pin Assignment for the 64-pin Package (top view)

Table 1.12 Pin Definitions and Functions for the 100-pin Package (2/4)

Function	Symbol	I/O	Power Supply	Description
Bus control pins	A0/D0 to A7/D7	I/O	VCC2	Output of address bits (A0 to A7) and input/output of data (D0 to D7) by time-division while accessing an external memory space with multiplexed bus
	A8/D8 to A15/D15	I/O	VCC2	Output of address bits (A8 to A15) and input/output of data (D8 to D15) by time-division while accessing an external memory space with 16-bit multiplexed bus
	$\overline{BC0}$/D0	I/O	VCC2	Output of byte control ($\overline{BC0}$) and input/output of data (D0) by time-division while accessing an external memory space with multiplexed bus
	$\overline{CS0}$ to $\overline{CS3}$	O	VCC2	Chip select output
	$\overline{WR0}$/$\overline{WR1}$/$\overline{WR}$/ $\overline{BC0}$/$\overline{BC1}$/$\overline{RD}$	O	VCC2	Output of write, byte control, and read signals. Either $\overline{WRx}$ or $\overline{WR}$ and $\overline{BCx}$ can be selected by a program. Data is read when $\overline{RD}$ is low. • When $\overline{WR0}$, $\overline{WR1}$, and $\overline{RD}$ are selected, data is written to the following address: an even address, when $\overline{WR0}$ is low an odd address, when $\overline{WR1}$ is low on 16-bit external data bus • When $\overline{WR}$, $\overline{BC0}$, $\overline{BC1}$, and $\overline{RD}$ are selected, data is written, when $\overline{WR}$ is low and the following address is accessed: an even address, when $\overline{BC0}$ is low an odd address, when $\overline{BC1}$ is low on 16-bit external data bus
	ALE	O	VCC2	Latch enable signal in multiplexed bus format
	$\overline{HOLD}$	I	VCC2	The MCU is in a hold state while this pin is held low
	$\overline{HLDA}$	O	VCC2	This pin is driven low while the MCU is held in a hold state
	$\overline{RDY}$	I	VCC2	Bus cycle is extended by the CPU if this pin is low on the falling edge of BCLK

2.1.8.5 Register Bank Select Flag (B flag)

This flag selects a register bank. It indicates 0 when register bank 0 is selected, and 1 when register bank 1 is selected.

2.1.8.6 Overflow Flag (O flag)

This flag becomes 1 when the result of an operation overflows; otherwise it is 0.

2.1.8.7 Interrupt Enable Flag (I flag)

This flag enables maskable interrupts. To disable maskable interrupts, set this flag to 0. To enable them, set this flag to 1. When an interrupt is accepted, the flag becomes 0.

2.1.8.8 Stack Pointer Select Flag (U flag)

To select the interrupt stack pointer (ISP), set this flag to 0. To select the user stack pointer (USP), set this flag to 1.
It becomes 0 when a hardware interrupt is accepted or when an INT instruction designated by a software interrupt number from 0 to 127 is executed.

2.1.8.9 Floating-point Underflow Flag (FU flag)

This flag becomes 1 when an underflow occurs in a floating-point operation; otherwise it is 0. It also becomes 1 when the operand contains invalid numbers (subnormal numbers).

2.1.8.10 Floating-point Overflow Flag (FO flag)

This flag becomes 1 when an overflow occurs in a floating-point operation; otherwise it is 0. It also becomes 1 when the operand contains invalid numbers (subnormal numbers).

2.1.8.11 Processor Interrupt Priority Level (IPL)

The processor interrupt priority level (IPL), consisting of 3 bits, selects a processor interrupt priority level from level 0 to 7. An interrupt is enabled when the interrupt request level is higher than the selected IPL.
When the processor interrupt priority level (IPL) is set to 111b (level 7), all interrupts are disabled.

2.1.8.12 Fixed-point Radix Point Designation Bit (DP bit)

This bit designates the radix point. It also specifies which portion of the fixed-point multiplication result to extract. It is used for the MULX instruction.

2.1.8.13 Floating-point Rounding Mode (RND)

The 2-bit floating-point rounding mode selects a rounding mode for floating-point calculation results.

2.1.8.14 Reserved

Only set this bit to 0. The read value is undefined.

Table 4.5 SFR List (5)

Address	Register	Symbol	Reset Value
0000E0h			
0000E1h			
0000E2h			
0000E3h			
0000E4h			
0000E5h			
0000E6h			
0000E7h			
0000E8h			
0000E9h			
0000EAh			
0000EBh			
0000ECh			
0000EDh			
0000EEh			
0000EFh			
0000F0h			
0000F1h			
0000F2h			
0000F3h			
0000F4h			
0000F5h			
0000F6h			
0000F7h			
0000F8h			
0000F9h			
0000FAh			
0000FBh			
0000FCh			
0000FDh	UART7 Receive Interrupt Control Register	S7RIC	XXXX X000b
0000FEh			
0000FFh	UART8 Receive Interrupt Control Register	S8RIC	XXXX X000b
000100h	Group 1 Time Measurement/Waveform Generation Register 0	G1TM0/G1PO0	XXXXh
000101h			
000102h	Group 1 Time Measurement/Waveform Generation Register 1	G1TM1/G1PO1	XXXXh
000103h			
000104h	Group 1 Time Measurement/Waveform Generation Register 2	G1TM2/G1PO2	XXXXh
000105h			
000106h	Group 1 Time Measurement/Waveform Generation Register 3	G1TM3/G1PO3	XXXXh
000107h			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.10 SFR List (10)

Address	Register	Symbol	Reset Value
0001D0h			
0001D1h			
0001D2h			
0001D3h			
0001D4h	UART6 Special Mode Register 4	U6SMR4	00h
0001D5h	UART6 Special Mode Register 3	U6SMR3	00h
0001D6h	UART6 Special Mode Register 2	U6SMR2	00h
0001D7h	UART6 Special Mode Register	U6SMR	00h
0001D8h	UART6 Transmit/Receive Mode Register	U6MR	00h
0001D9h	UART6 Bit Rate Register	U6BRG	XXh
0001DAh	UART6 Transmit Buffer Register	U6TB	XXXXh
0001DBh			
0001DCh	UART6 Transmit/Receive Control Register 0	U6C0	0000 1000b
0001DDh	UART6 Transmit/Receive Control Register 1	U6C1	0000 0010b
0001DEh	UART6 Receive Buffer Register	U6RB	XXXXh
0001DFh			
0001E0h	UART7 Transmit/Receive Mode Register	U7MR	00h
0001E1h	UART7 Bit Rate Register	U7BRG	XXh
0001E2h	UART7 Transmit Buffer Register	U7TB	XXXXh
0001E3h			
0001E4h	UART7 Transmit/Receive Control Register 0	U7C0	00X0 1000b
0001E5h	UART7 Transmit/Receive Control Register 1	U7C1	XXXX 0010b
0001E6h	UART7 Receive Buffer Register	U7RB	XXXXh
0001E7h			
0001E8h	UART8 Transmit/Receive Mode Register	U8MR	00h
0001E9h	UART8 Bit Rate Register	U8BRG	XXh
0001EAh	UART8 Transmit Buffer Register	U8TB	XXXXh
0001EBh			
0001ECh	UART8 Transmit/Receive Control Register 0	U8C0	00X0 1000b
0001EDh	UART8 Transmit/Receive Control Register 1	U8C1	XXXX 0010b
0001EEh	UART8 Receive Buffer Register	U8RB	XXXXh
0001EFh			
0001F0h	UART7, UART8 Transmit/Receive Control Register 2	U78CON	X000 0000b
0001F1h			
0001F2h			
0001F3h			
0001F4h			
0001F5h			
0001F6h			
0001F7h			
0001F8h			
0001F9h			
0001FAh			
0001FBh			
0001FCh			
0001FDh			
0001FEh			
0001FFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.11 SFR List (11)

Address	Register	Symbol	Reset Value
000200h to 0002BFh			
0002C0h	X0 Register/Y0 Register	X0R/Y0R	XXXXh
0002C1h			
0002C2h	X1 Register/Y1 Register	X1R/Y1R	XXXXh
0002C3h			
0002C4h	X2 Register/Y2 Register	X2R/Y2R	XXXXh
0002C5h			
0002C6h	X3 Register/Y3 Register	X3R/Y3R	XXXXh
0002C7h			
0002C8h	X4 Register/Y4 Register	X4R/Y4R	XXXXh
0002C9h			
0002CAh	X5 Register/Y5 Register	X5R/Y5R	XXXXh
0002CBh			
0002CCh	X6 Register/Y6 Register	X6R/Y6R	XXXXh
0002CDh			
0002CEh	X7 Register/Y7 Register	X7R/Y7R	XXXXh
0002CFh			
0002D0h	X8 Register/Y8 Register	X8R/Y8R	XXXXh
0002D1h			
0002D2h	X9 Register/Y9 Register	X9R/Y9R	XXXXh
0002D3h			
0002D4h	X10 Register/Y10 Register	X10R/Y10R	XXXXh
0002D5h			
0002D6h	X11 Register/Y11 Register	X11R/Y11R	XXXXh
0002D7h			
0002D8h	X12 Register/Y12 Register	X12R/Y12R	XXXXh
0002D9h			
0002DAh	X13 Register/Y13 Register	X13R/Y13R	XXXXh
0002DBh			
0002DCh	X14 Register/Y14 Register	X14R/Y14R	XXXXh
0002DDh			
0002DEh	X15 Register/Y15 Register	X15R/Y15R	XXXXh
0002DFh			
0002E0h	X-Y Control Register	XYC	XXXX XX00b
0002E1h			
0002E2h			
0002E3h			
0002E4h	UART1 Special Mode Register 4	U1SMR4	00h
0002E5h	UART1 Special Mode Register 3	U1SMR3	00h
0002E6h	UART1 Special Mode Register 2	U1SMR2	00h
0002E7h	UART1 Special Mode Register	U1SMR	00h
0002E8h	UART1 Transmit/Receive Mode Register	U1MR	00h
0002E9h	UART1 Bit Rate Register	U1BRG	XXh
0002EAh	UART1 Transmit Buffer Register	U1TB	XXXXh
0002EBh			
0002ECh	UART1 Transmit/Receive Control Register 0	U1C0	0000 1000b
0002EDh	UART1 Transmit/Receive Control Register 1	U1C1	0000 0010b
0002EEh	UART1 Receive Buffer Register	U1RB	XXXXh
0002EFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.13 SFR List (13)

Address	Register	Symbol	Reset Value
000320h			
000321h			
000322h			
000323h			
000324h	UART3 Special Mode Register 4	U3SMR4	00h
000325h	UART3 Special Mode Register 3	U3SMR3	00h
000326h	UART3 Special Mode Register 2	U3SMR2	00h
000327h	UART3 Special Mode Register	U3SMR	00h
000328h	UART3 Transmit/Receive Mode Register	U3MR	00h
000329h	UART3 Bit Rate Register	U3BRG	XXh
00032Ah	UART3 Transmit Buffer Register	U3TB	XXXXh
00032Bh			
00032Ch	UART3 Transmit/Receive Control Register 0	U3C0	0000 1000b
00032Dh	UART3 Transmit/Receive Control Register 1	U3C1	0000 0010b
00032Eh	UART3 Receive Buffer Register	U3RB	XXXXh
00032Fh			
000330h			
000331h			
000332h			
000333h			
000334h	UART2 Special Mode Register 4	U2SMR4	00h
000335h	UART2 Special Mode Register 3	U2SMR3	00h
000336h	UART2 Special Mode Register 2	U2SMR2	00h
000337h	UART2 Special Mode Register	U2SMR	00h
000338h	UART2 Transmit/Receive Mode Register	U2MR	00h
000339h	UART2 Bit Rate Register	U2BRG	XXh
00033Ah	UART2 Transmit Buffer Register	U2TB	XXXXh
00033Bh			
00033Ch	UART2 Transmit/Receive Control Register 0	U2C0	0000 1000b
00033Dh	UART2 Transmit/Receive Control Register 1	U2C1	0000 0010b
00033Eh	UART2 Receive Buffer Register	U2RB	XXXXh
00033Fh			
000340h	Count Start Register	TABSR	0000 0000b
000341h	Clock Prescaler Reset Register	CPSRF	0XXX XXXXb
000342h	One-shot Start Register	ONSF	0000 0000b
000343h	Trigger Select Register	TRGSR	0000 0000b
000344h	Increment/Decrement Select Register	UDF	0000 0000b
000345h			
000346h	Timer A0 Register	TA0	XXXXh
000347h			
000348h	Timer A1 Register	TA1	XXXXh
000349h			
00034Ah	Timer A2 Register	TA2	XXXXh
00034Bh			
00034Ch	Timer A3 Register	TA3	XXXXh
00034Dh			
00034Eh	Timer A4 Register	TA4	XXXXh
00034Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.15 SFR List (15)

Address	Register	Symbol	Reset Value
000380h	A/D0 Register 0	AD00	00XXh
000381h			
000382h	A/D0 Register 1	AD01	00XXh
000383h			
000384h	A/D0 Register 2	AD02	00XXh
000385h			
000386h	A/D0 Register 3	AD03	00XXh
000387h			
000388h	A/D0 Register 4	AD04	00XXh
000389h			
00038Ah	A/D0 Register 5	AD05	00XXh
00038Bh			
00038Ch	A/D0 Register 6	AD06	00XXh
00038Dh			
00038Eh	A/D0 Register 7	AD07	00XXh
00038Fh			
000390h			
000391h			
000392h	A/D0 Control Register 4	AD0CON4	XXXX 00XXb
000393h			
000394h	A/D0 Control Register 2	AD0CON2	XX0X X000b
000395h	A/D0 Control Register 3	AD0CON3	XXXX X000b
000396h	A/D0 Control Register 0	AD0CON0	00h
000397h	A/D0 Control Register 1	AD0CON1	00h
000398h	D/A Register 0	DA0	XXh
000399h			
00039Ah	D/A Register 1	DA1	XXh
00039Bh			
00039Ch	D/A Control Register	DACON	XXXX XX00b
00039Dh			
00039Eh			
00039Fh			
0003A0h			
0003A1h			
0003A2h			
0003A3h			
0003A4h			
0003A5h			
0003A6h			
0003A7h			
0003A8h			
0003A9h			
0003AAh			
0003ABh			
0003ACh			
0003ADh			
0003AEh			
0003AFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.17 SFR List (17)

Address	Register	Symbol	Reset Value
0003E0h			
0003E1h			
0003E2h			
0003E3h			
0003E4h			
0003E5h			
0003E6h			
0003E7h			
0003E8h			
0003E9h			
0003EAh			
0003EBh			
0003ECh			
0003EDh			
0003EEh			
0003EFh			
0003F0h	Pull-up Control Register 0	PUR0	0000 0000b
0003F1h	Pull-up Control Register 1	PUR1	XXXX 0000b
0003F2h	Pull-up Control Register 2	PUR2	0000 0000b
0003F3h	Pull-up Control Register 3	PUR3	XXXX XX00b
0003F4h			
0003F5h			
0003F6h			
0003F7h			
0003F8h			
0003F9h			
0003FAh			
0003FBh			
0003FCh			
0003FDh			
0003FEh			
0003FFh	Port Control Register	PCR	XXXX XXX0b

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.23 SFR List (23)

Address	Register	Symbol	Reset Value
040120h to 04403Fh			
044040h			
044041h			
044042h			
044043h			
044044h			
044045h			
044046h			
044047h			
044048h			
044049h			
04404Ah			
04404Bh			
04404Ch			
04404Dh			
04404Eh	Watchdog Timer Start Register	WDTS	XXXX XXXXb
04404Fh	Watchdog Timer Control Register	WDC	000X XXXXb
044050h			
044051h			
044052h			
044053h			
044054h			
044055h			
044056h			
044057h			
044058h			
044059h			
04405Ah			
04405Bh			
04405Ch			
04405Dh			
04405Eh			
04405Fh	Protect Register 2	PRCR2	0XXX XXXXb

X: Undefined
Blanks are reserved. No access is allowed.

Table 5.3 Operating Conditions (2/5)
(V_{CC1} = V_{CC2} = 3.0 to 5.5 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted) (1)

Symbol	Characteristic		Value (2)			Unit
			Min.	Typ.	Max.	
C_{VDC}	Decoupling capacitance for voltage regulator	Inter-pin voltage: 1.5 V	2.4		10.0	µF

Notes:
1. The device is operationally guaranteed under these operating conditions.
2. This value should be met with due consideration to the following conditions: operating temperature, DC bias, aging, etc.

Table 5.5 Operating Conditions (4/5)

(V_{CC1} = V_{CC2} = 3.0 to 5.5 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted) (1)

Symbol	Characteristic	Value			Unit
		Min.	Typ.	Max.	
$f_{(XIN)}$	Main clock oscillator frequency	4		16	MHz
$f_{(XRef)}$	Reference clock frequency	2		4	MHz
$f_{(PLL)}$	PLL clock oscillator frequency	96		128	MHz
$f_{(Base)}$	Base clock frequency			50	MHz
$t_{c(Base)}$	Base clock cycle time	20			ns
$f_{(CPU)}$	CPU operating frequency			50	MHz
$t_{c(CPU)}$	CPU clock cycle time	20			ns
$f_{(BCLK)}$	Peripheral bus clock operating frequency			25	MHz
$t_{c(BCLK)}$	Peripheral bus clock cycle time	40			ns
$f_{(PER)}$	Peripheral clock source frequency			32	MHz
$f_{(XCIN)}$	Sub clock oscillator frequency		32.768	62.5	kHz

Note:
1. The device is operationally guaranteed under these operating conditions.

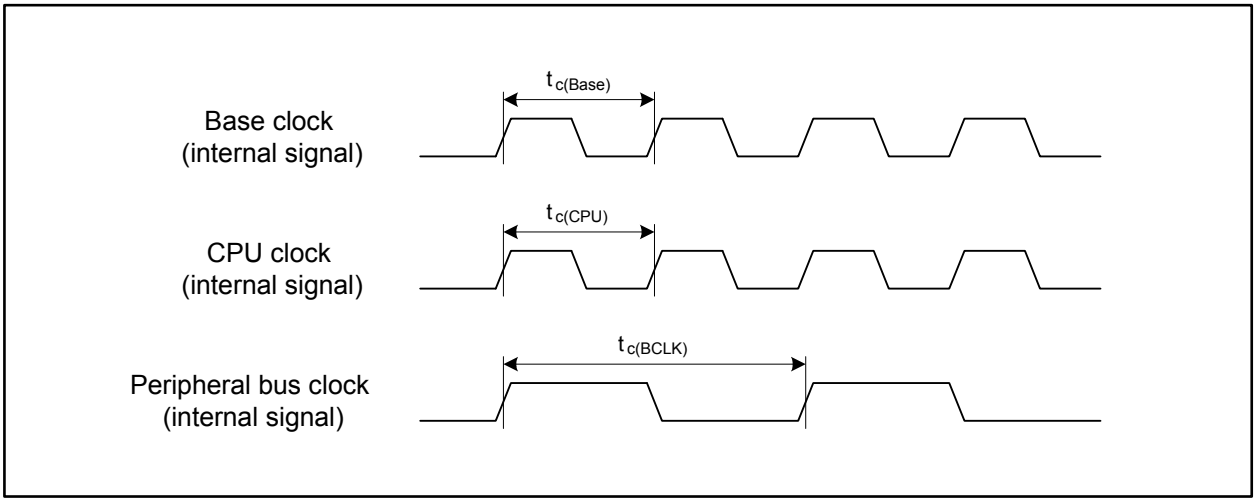


Figure 5.1 Clock Cycle Time

$V_{CC1} = V_{CC2} = 3.3$ V

Table 5.40 Electrical Characteristics (3/3)
($V_{CC1} = V_{CC2} = 3.0$ to 3.6 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted)

Symbol	Characteristic	Measurement Condition		Value			Unit
				Min.	Typ.	Max.	
I_{CC}	Power supply current	In single-chip mode, output pins are left open and others are connected to V_{SS} XIN-XOUT Drive strength: low XCIN-XCOUT Drive strength: low	$f_{(CPU)}$ = 50 MHz, $f_{(BCLK)}$ = 25 MHz, $f_{(XIN)}$ = 8 MHz, Active: XIN, PLL, Stopped: XCIN, OCO		28	40	mA
			$f_{(CPU)} = f_{SO(PLL)}/24$ MHz, Active: PLL (self-oscillation), Stopped: XIN, XCIN, OCO		7		mA
			$f_{(CPU)} = f_{(BCLK)} = f_{(XIN)}/256$ MHz, $f_{(XIN)}$ = 8 MHz, Active: XIN, Stopped: PLL, XCIN, OCO		670		µA
			$f_{(CPU)} = f_{(BCLK)}$ = 32.768 kHz, Active: XCIN, Stopped: XIN, PLL, OCO, Main regulator: shutdown		180		µA
			$f_{(CPU)} = f_{(BCLK)} = f_{(OCO)}/4$ kHz, Active: OCO, Stopped: XIN, PLL, XCIN, Main regulator: shutdown		190		µA
			$f_{(CPU)} = f_{(BCLK)} = f_{(XIN)}/256$ MHz, $f_{(XIN)}$ = 8 MHz, Active: XIN, Stopped: PLL, XCIN, OCO, T_a = 25°C, Wait mode		500	900	µA
			$f_{(CPU)} = f_{(BCLK)}$ = 32.768 kHz, Active: XCIN, Stopped: XIN, PLL, OCO, Main regulator: shutdown, T_a = 25°C, Wait mode		8	140	µA
			$f_{(CPU)} = f_{(BCLK)} = f_{(OCO)}/4$ kHz, Active: OCO, Stopped: XIN, PLL, XCIN, Main regulator: shutdown, T_a = 25°C, Wait mode		10	150	µA
			Stopped: all clocks, Main regulator: shutdown, T_a = 25°C		5	70	µA

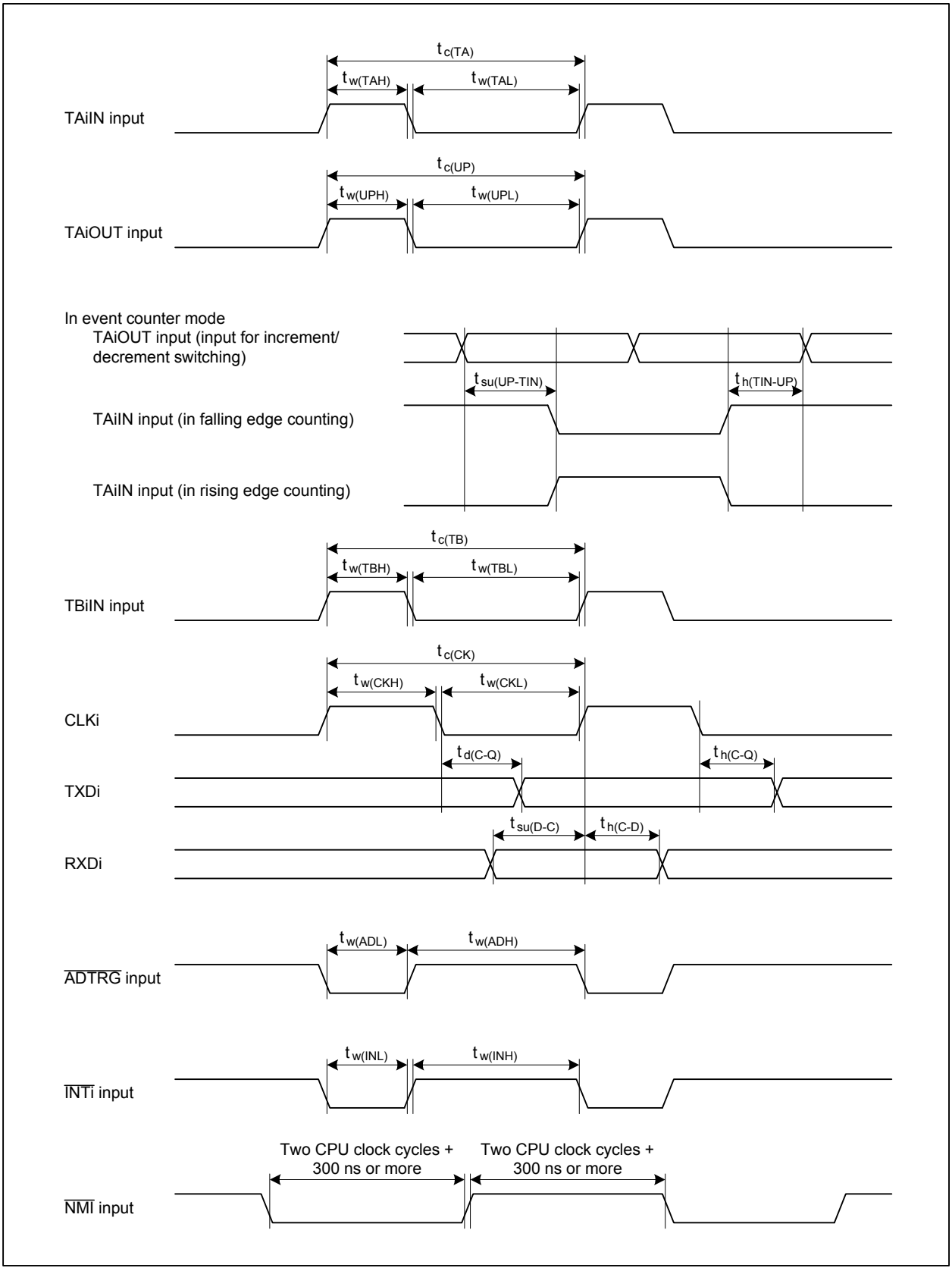


Figure 5.10 Timing of Peripherals

Revision History	R32C/111 Group Datasheet

Rev.	Date	Description	
		Page	Summary
		8	• Completed “under development” phase of part numbers R5F64110DFB, R5F64111DFB, R5F64112DFB, R5F64114DFB, R5F64115DFB, and R5F64116DFB in **Table 1.7** • Added product information for 100-pin LGA and 80-/64-pin packages to **Table 1.7**
		9	• Added product information for 100-pin LGA and 80-/64-pin packages, and 32-Kbyte RAM to **Figure 1.1** • Deleted hyphenation for part number in **Figure 1.1**
		11, 12, 14, 18, 21	• Added **Figures 1.3, 1.4, and 1.6 to 1.8** to provide block diagrams and pin assignment for 100-pin LGA and 80-/64-pin packages
		13	• Changed the order of Notes in **Figures 1.5**
		15-17	• Added pin No. for 100-pin LGA package to **Tables 1.8 to 1.10**
		19, 20, 22, 23	• Added **Tables 1.11 to 1.14** to provide pin characteristics for 80-/64-pin packages.
		24	• Changed the following expression: “A ceramic resonator or a crystal oscillator” for “Main clock input/output” in **Table 1.15**, to “A crystal, or a ceramic resonator”
		25	• Modified descriptions for $\overline{\text{HLDA}}$ and $\overline{\text{RDY}}$ of “Bus control pins” in **Table 1.16**
		26	• Changed the following expression: “selected” for “Input port” in **Table 1.17**, to “selectable” • Modified description “TXD2” for TXD0 to TXD8 of “Serial interface” in **Table 1.17**, to “TXD2 output”
		28-30	• Added **Tables 1.19 to 1.21** to provide pin definitions and functions for 80-/64-pin packages
			Chapter 2. CPU
		—	• Made major text modifications to this chapter
		33	• Changed the following expression: “a requested interrupt’s priority level” in line 2 of **2.1.8.11**, to “the interrupt request level”
			Chapter 3. Memory
		35	• Made major text modifications to this chapter • Changed RAM size “40” in line 7 of this chapter, to “63”, and address “0000A3FFh” in line 8, to “0000FFFFh” • Added descriptions for 32-Kbyte RAM and 128-Kbyte ROM to **Figure 3.1** • Changed two “can be”s in Notes 3 and 4 of **Figure 3.1**, to “becomes”s
			Chapter 4. SFRs
		36	• Changed hexadecimal format of reset values for registers CCR and FMCR in **Table 4.1**, to binary • Added FEBC3 register to addresses 000010h-000011h in **Table 4.1** • Changed FEBC register for addresses 00001Ch-00001Dh, to FEBC0 in **Table 4.1** • Modified the following register name in **Table 4.1**: “Chip-select Boundary (between n and n + 1) Setting Register”, to “Chip-select n and n + 1 Boundary Setting Register”