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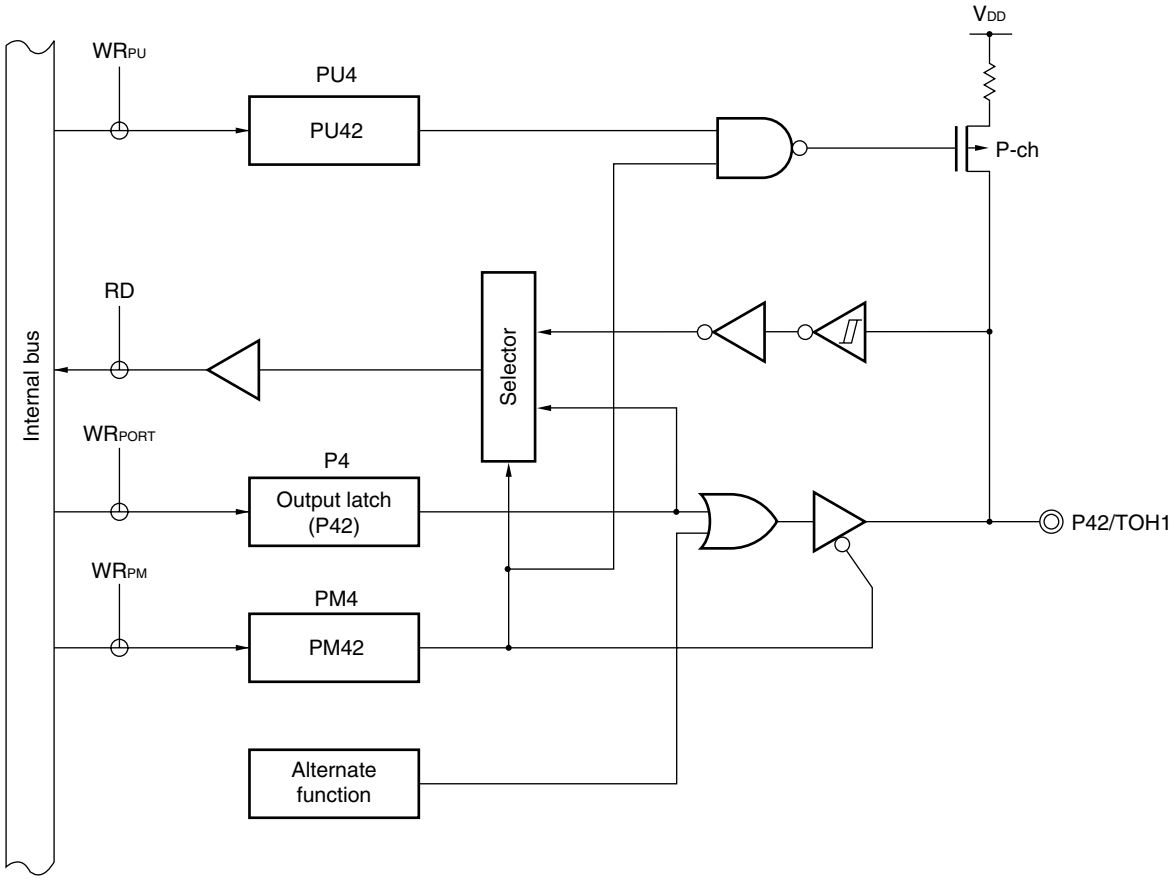
Program Memory Type	-
EEPROM Size	-
RAM Size	-
Voltage - Supply (Vcc/Vdd)	-
Data Converters	-
Oscillator Type	-
Operating Temperature	-
Mounting Type	-
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f9232mc-5a4-a

Figure 4-10. Block Diagram of P42



PU4: Pull-up resistor option register 4
P4: Port register 4
PM4: Port mode register 4
RD: Read signal
WR××: Write signal

5.4 System Clock Oscillators

The following three types of system clock oscillators are available.

- High-speed internal oscillator: Internally oscillates a clock of 8 MHz (TYP.).
- Crystal/ceramic oscillator: Oscillates a clock of 2 to 10 MHz.
- External clock input circuit: Supplies a clock of 2 to 10 MHz to the X1 pin.

5.4.1 High-speed internal oscillator

The 78K0S/KB1+ includes a high-speed internal oscillator (8 MHz (TYP.)).

If the high-speed internal oscillation is selected by the option byte as the clock source, the X1 and X2 pins can be used as I/O port pins.

For details of the option byte, refer to **CHAPTER 18 OPTION BYTE**. For details of I/O ports, refer to **CHAPTER 4 PORT FUNCTIONS**.

5.4.2 Crystal/ceramic oscillator

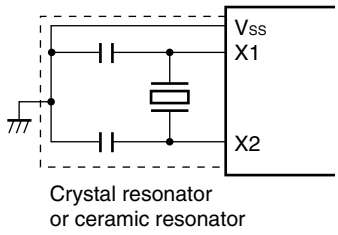
The crystal/ceramic oscillator oscillates using a crystal or ceramic resonator connected between the X1 and X2 pins.

If the crystal/ceramic oscillator is selected by the option byte as the system clock source, the X1 and X2 pins are used as crystal or ceramic resonator connection pins.

For details of the option byte, refer to **CHAPTER 18 OPTION BYTE**. For details of I/O ports, refer to **CHAPTER 4 PORT FUNCTIONS**.

Figure 5-6 shows the external circuit of the crystal/ceramic oscillator.

Figure 5-6. External Circuit of Crystal/Ceramic Oscillator



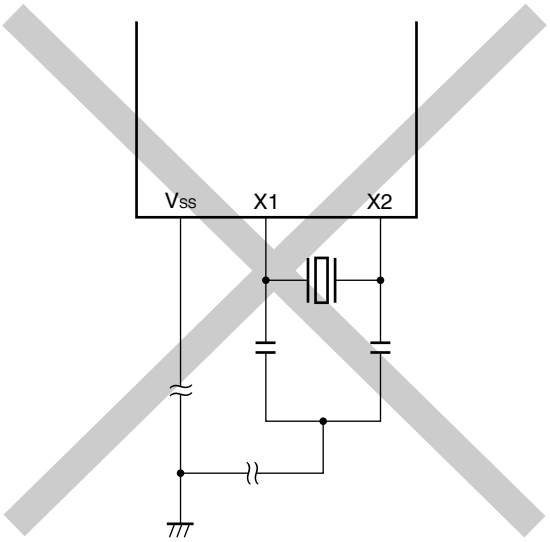
Caution When using the crystal/ceramic oscillator, wire as follows in the area enclosed by the broken lines in Figure 5-6 to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines. Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}. Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

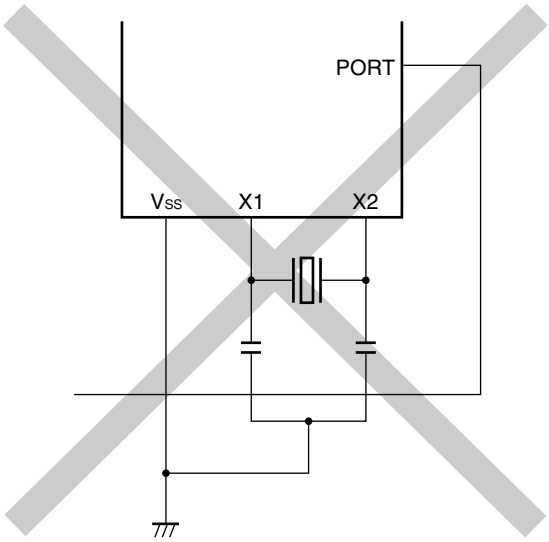
Figure 5-7 shows examples of incorrect resonator connection.

Figure 5-7. Examples of Incorrect Resonator Connection (1/2)

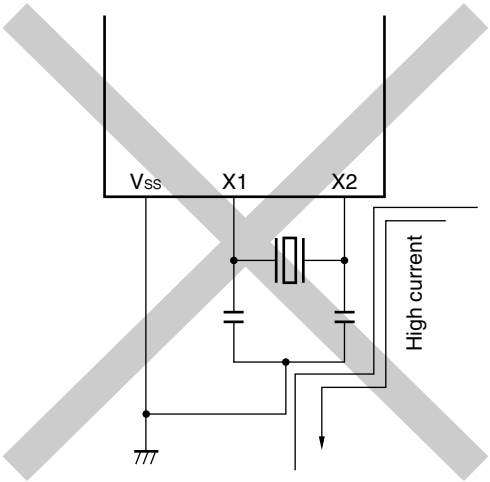
(a) Too long wiring of connected circuit



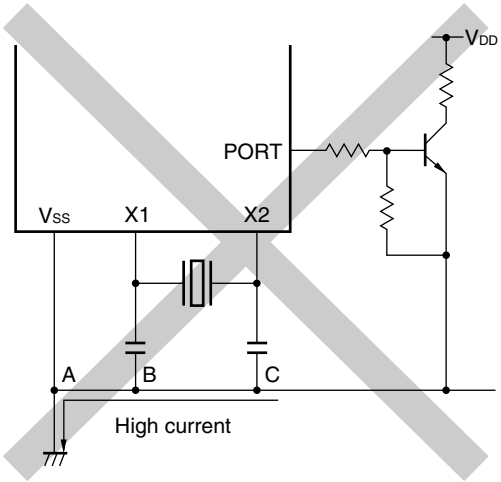
(b) Crossed signal lines



(c) Wiring near high fluctuating current



(d) Current flowing through ground line of oscillator
(Potential at points A, B, and C fluctuates.)



6.2 Configuration of 16-bit Timer/Event Counter 00

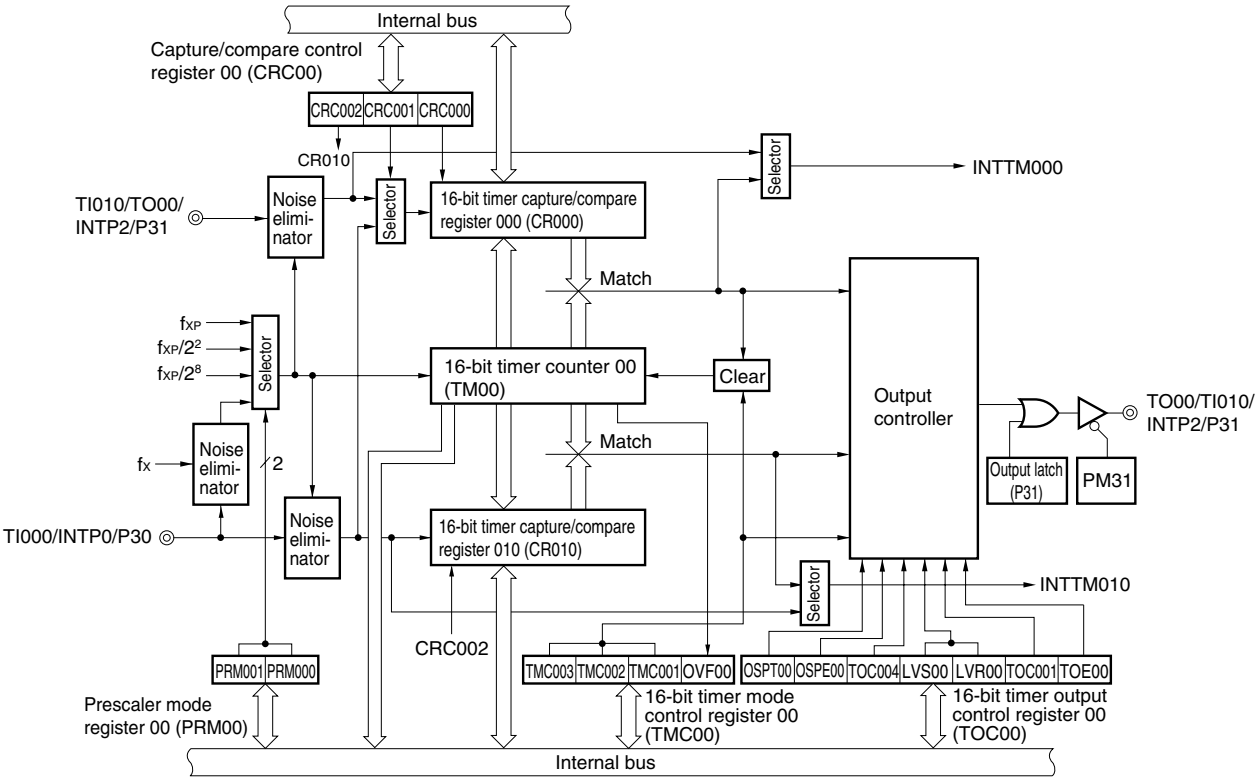
16-bit timer/event counter 00 consists of the following hardware.

Table 6-1. Configuration of 16-bit Timer/Event Counter 00

Item	Configuration
Timer counter	16-bit timer counter 00 (TM00)
Register	16-bit timer capture/compare registers 000, 010 (CR000, CR010)
Timer input	TI000, TI010
Timer output	TO00, output controller
Control registers	16-bit timer mode control register 00 (TMC00) Capture/compare control register 00 (CRC00) 16-bit timer output control register 00 (TOC00) Prescaler mode register 00 (PRM00) Port mode register 3 (PM3) Port register 3 (P3)

Figure 6-1 shows a block diagram of these counters.

Figure 6-1. Block Diagram of 16-bit Timer/Event Counter 00



(3) 16-bit timer output control register 00 (TOC00)

This register controls the operation of the 16-bit timer/event counter output controller. It sets timer output F/F set/reset, output inversion enable/disable, 16-bit timer/event counter 00 timer output enable/disable, one-shot pulse output operation enable/disable, and output trigger of one-shot pulse by software.

TOC00 is set by a 1-bit or 8-bit memory manipulation instruction.

Generation of reset signal sets the value of TOC00 to 00H.

Figure 6-7. Format of 16-bit Timer Output Control Register 00 (TOC00)

Address: FF63H After reset: 00H R/W

Symbol	7	<6>	<5>	4	<3>	<2>	1	<0>
TOC00	0	OSPT00	OSPE00	TOC004	LVS00	LVR00	TOC001	TOE00

OSPT00	One-shot pulse output trigger control via software
0	No one-shot pulse output trigger
1	One-shot pulse output trigger

OSPE00	One-shot pulse output operation control
0	Successive pulse output mode
1	One-shot pulse output mode[Note]

TOC004	Timer output F/F control using match of CR010 and TM00
0	Disables inversion operation
1	Enables inversion operation

LVS00	LVR00	Timer output F/F status setting
0	0	No change
0	1	Timer output F/F reset (0)
1	0	Timer output F/F set (1)
1	1	Setting prohibited

TOC001	Timer output F/F control using match of CR000 and TM00
0	Disables inversion operation
1	Enables inversion operation

TOE00	Timer output control
0	Disables output (output fixed to level 0)
1	Enables output

Note The one-shot pulse output mode operates correctly only in the free-running mode and the mode in which clear & start occurs at the TI000 pin valid edge. In the mode in which clear & start occurs on a match between TM00 and CR000, one-shot pulse output is not possible because an overflow does not occur.

Cautions 1. The timer operation must be stopped before setting other than OSPT00.

2. If LVS00 and LVR00 are read, 0 is read.

3. OSPT00 is automatically cleared after data is set, so 0 is read.

4. Do not set OSPT00 to 1 other than in one-shot pulse output mode.

5. A write interval of two cycles or more of the count clock selected by prescaler mode register 00 (PRM00) is required, when OSPT00 is set to 1 successively.

6. When TOE00 is 0, set TOE00, LVS00, and LVR00 at the same time with the 8-bit memory manipulation instruction. When TOE00 is 1, LVS00 and LVR00 can be set with the 1-bit memory manipulation instruction.

The external event counter counts the number of external clock pulses to be input to the TI000 pin with using 16-bit timer counter 00 (TM00).

TM00 is incremented each time the valid edge specified by prescaler mode register 00 (PRM00) is input.

When the TM00 count value matches the 16-bit timer capture/compare register 000 (CR000) value, TM00 is cleared to 0 and the interrupt request signal (INTTM000) is generated.

Input a value other than 0000H to CR000. (A count operation with a pulse cannot be carried out.)

The rising edge, the falling edge, or both edges can be selected using bits 4 and 5 (ES000 and ES010) of prescaler mode register 00 (PRM00).

Because an operation is carried out only when the valid edge of the TI000 pin is detected twice after sampling with the internal clock (f_{XP}), noise with a short pulse width can be removed.

Figure 6-14. Control Register Settings in External Event Counter Mode (with Rising Edge Specified)

(a) Capture/compare control register 00 (CRC00)

	7	6	5	4	3	CRC002	CRC001	CRC000
CRC00	0	0	0	0	0	0/1	0/1	0

CR000 used as compare register

(b) Prescaler mode register 00 (PRM00)

	ES110	ES100	ES010	ES000	3	2	PRM001	PRM000
PRM00	0/1	0/1	0	1	0	0	1	1

Selects external clock.

Specifies rising edge for pulse width detection.

Setting invalid (setting “10” is prohibited.)

(c) 16-bit timer mode control register 00 (TMC00)

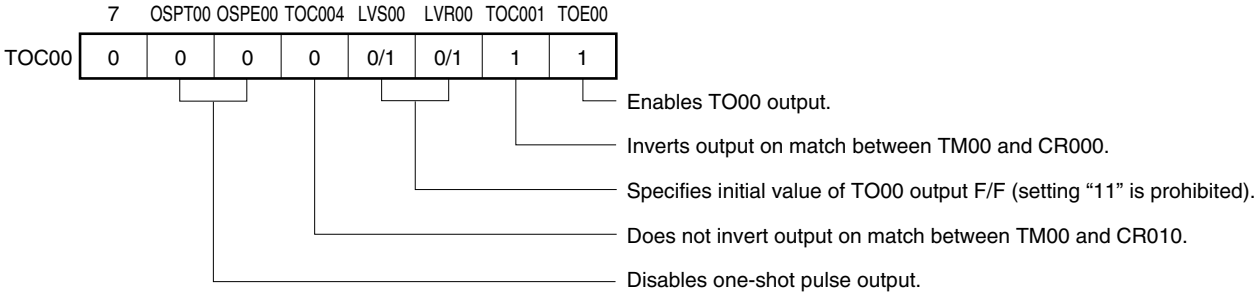
	7	6	5	4	TMC003	TMC002	TMC001	OVF00
TMC00	0	0	0	0	1	1	0/1	0

Clears and starts on match between TM00 and CR000.

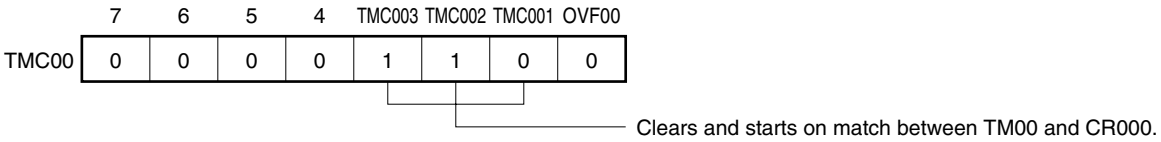
Remark 0/1: Setting 0 or 1 allows another function to be used simultaneously with the external event counter. See the description of the respective control registers for details.

Figure 6-27. Control Register Settings in Square-Wave Output Mode (2/2)

(c) 16-bit timer output control register 00 (TOC00)

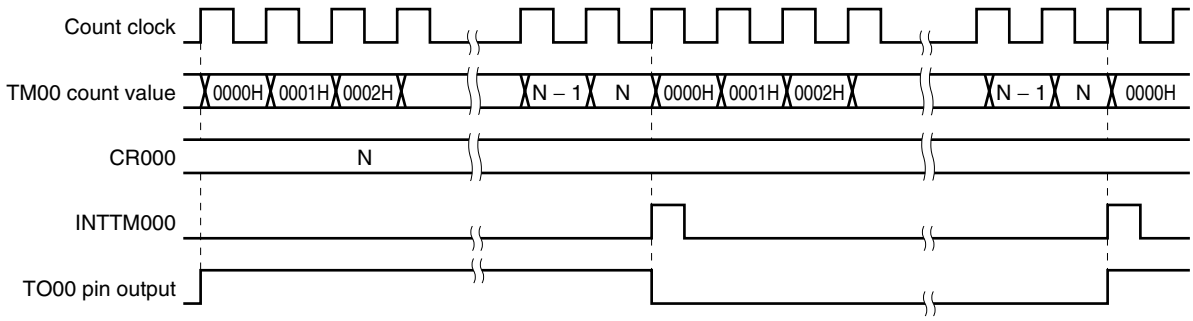


(d) 16-bit timer mode control register 00 (TMC00)



Remark 0/1: Setting 0 or 1 allows another function to be used simultaneously with square-wave output. See the description of the respective control registers for details.

Figure 6-28. Square-Wave Output Operation Timing



6.4.5 PPG output operations

Setting 16-bit timer mode control register 00 (TMC00) and capture/compare control register 00 (CRC00) as shown in Figure 6-29 allows operation as PPG (Programmable Pulse Generator) output.

Setting

The basic operation setting procedure is as follows.

<1> Set the CRC00 register (see **Figure 6-29** for the set value).
<2> Set any value to the CR000 register as the cycle.
<3> Set any value to the CR010 register as the duty factor.
<4> Set the TOC00 register (see **Figure 6-29** for the set value).
<5> Set the count clock by using the PRM00 register.
<6> Set the TMC00 register to start the operation (see **Figure 6-29** for the set value).

Caution Changing the CRC0n0 setting during TM00 operation may cause a malfunction. To change the setting, refer to 6.5 Cautions Related to 16-bit Timer/Event Counter 00 (17) Changing compare register during timer operation.

Remarks 1. For the setting of the TO00 pin, see **6.3 (5) Port mode register 3 (PM3)**.
2. For how to enable the INTTM000 interrupt, see **CHAPTER 13 INTERRUPT FUNCTIONS**.
3. n = 0 or 1

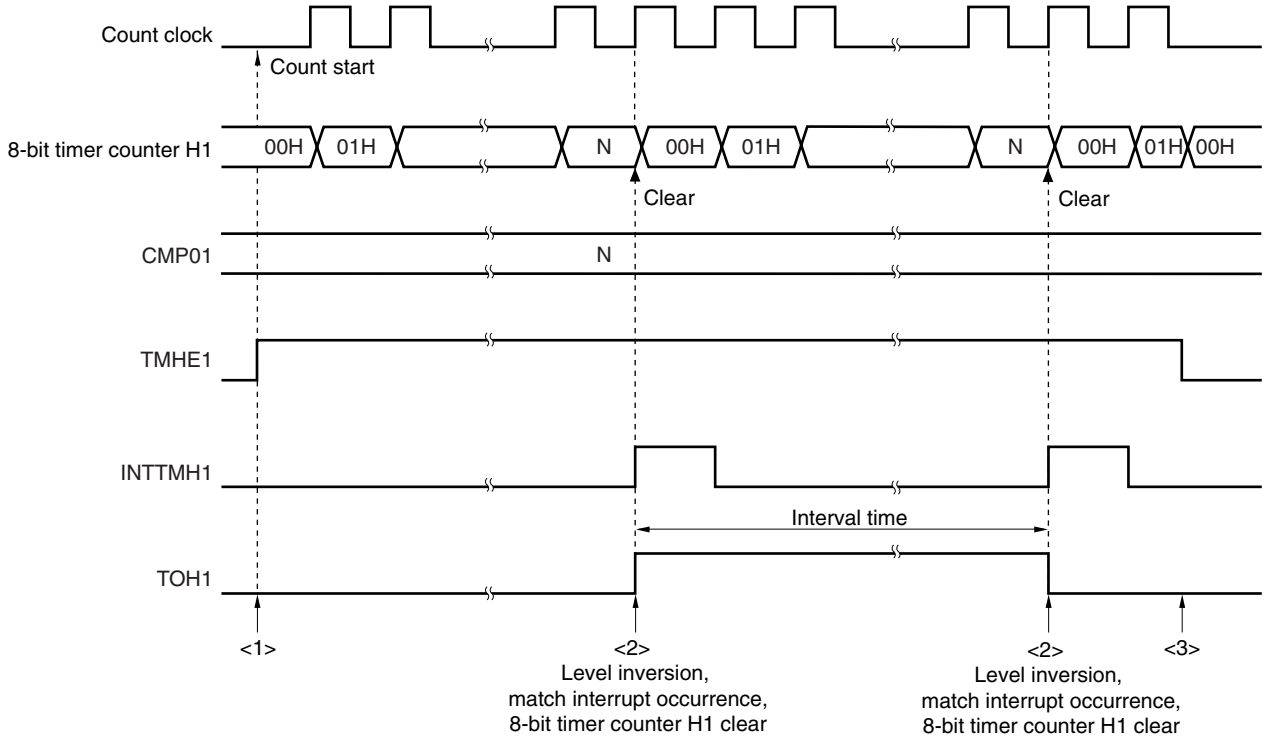
In the PPG output operation, rectangular waves are output from the TO00 pin with the pulse width and the cycle that correspond to the count values preset in 16-bit timer capture/compare register 010 (CR010) and in 16-bit timer capture/compare register 000 (CR000), respectively.

(2) Timing chart

The timing of the interval timer/square-wave output operation is shown below.

Figure 8-7. Timing of Interval Timer/Square-Wave Output Operation (1/2)

(a) Basic operation (01H ≤ CMP01 ≤ FEH)



<1> The count operation is enabled by setting the TMHE1 bit to 1. The count clock starts counting no more than 1 clock after the operation is enabled.

<2> When the values of 8-bit timer counter H1 and the CMP01 register match, the value of 8-bit timer counter H1 is cleared, the TOH1 output level is inverted, and the INTTMH1 signal is output.

<3> The INTTMH1 signal and TOH1 output become inactive by clearing the TMHE1 bit to 0 during timer H1 operation. If these are inactive from the first, the level is retained.

Remark 01H ≤ N ≤ FEH

14.1.2 Registers used during standby

The oscillation stabilization time after the standby mode is released is controlled by the oscillation stabilization time select register (OSTS).

Remark For the registers that start, stop, or select the clock, see **CHAPTER 5 CLOCK GENERATORS**.

(1) Oscillation stabilization time select register (OSTS)

This register is used to select oscillation stabilization time of the clock supplied from the oscillator when the STOP mode is released. The wait time set by OSTS is valid only when the crystal/ceramic oscillation clock is selected as the system clock and after the STOP mode is released. If the high-speed internal oscillation or external clock input is selected as the system clock source, no wait time elapses.

The system clock oscillator and the oscillation stabilization time that elapses after power application or release of reset are selected by the option byte. For details, refer to **CHAPTER 18 OPTION BYTE**.

OSTS is set by using the 8-bit memory manipulation instruction.

Figure 14-1. Format of Oscillation Stabilization Time Select Register (OSTS)

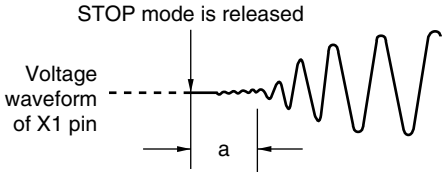
Address: FFF4H After reset: Undefined R/W

Symbol	7	6	5	4	3	2	1	0
OSTS	0	0	0	0	0	0	OSTS1	OSTS0

OSTS1	OSTS0	Selection of oscillation stabilization time
0	0	2^{10}/fx (102.4 μs)
0	1	2^{12}/fx (409.6 μs)
1	0	2^{15}/fx (3.27 ms)
1	1	2^{17}/fx (13.1 ms)

Cautions 1. To set and then release the STOP mode, set the oscillation stabilization time as follows. Expected oscillation stabilization time of resonator ≤ Oscillation stabilization time set by OSTS

2. The wait time after the STOP mode is released does not include the time from the release of the STOP mode to the start of clock oscillation (“a” in the figure below), regardless of whether STOP mode was released by reset signal generation or interrupt generation.



3. The oscillation stabilization time that elapses on power application or after release of reset is selected by the option byte. For details, refer to CHAPTER 18 OPTION BYTE.

Remarks 1. ( ): fx = 10 MHz

2. Determine the oscillation stabilization time of the resonator by checking the characteristics of the resonator to be used.

14.2.2 STOP mode

(1) STOP mode setting and operating statuses

The STOP mode is set by executing the STOP instruction.

Caution Because an interrupt request signal is used to clear the standby mode, if there is an interrupt source with the interrupt request flag set and the interrupt mask flag reset, the standby mode is immediately cleared if set. Thus, in the STOP mode, the normal operation mode is restored after the STOP instruction is executed and then the operation is stopped for 34 μs (TYP.) (after an additional wait time for stabilizing the oscillation set by the oscillation stabilization time select register (OSTS) has elapsed when crystal/ceramic oscillation is used).

The operating statuses in the STOP mode are shown below.

Table 14-4. Operating Statuses in STOP Mode

Item \ Setting of HALT Mode		Low-Speed Internal Oscillator Cannot Be Stopped[Note]	Low-Speed Internal Oscillator Can Be Stopped[Note]	
			When Low-Speed Internal Oscillation Continues	When Low-Speed Internal Oscillation Stops
System clock		Oscillation stops.		
CPU		Operation stops.		
Port (latch)		Holds status before STOP mode is set.		
16-bit timer/event counter 00		Operation stops.		
8-bit timer 80		Operation stops.		
8-bit timer H1	Sets count clock to f_{XP} to $f_{XP}/2^{12}$	Operation stops.		
	Sets count clock to $f_{RL}/2^{7}$	Operable	Operable	Operation stops.
Watchdog timer	“Clock to peripheral hardware” selected as operating clock	Setting prohibited	Operation stops.	
	“Low-speed internal oscillation clock” selected as operating clock	Operable (Operation continues.)	Operation stops.	
A/D converter		Operation stops.		
Serial interface UART6		Operation stops.		
Power-on-clear circuit		Always operates.		
Low-voltage detector		Operable		
External interrupt		Operable		

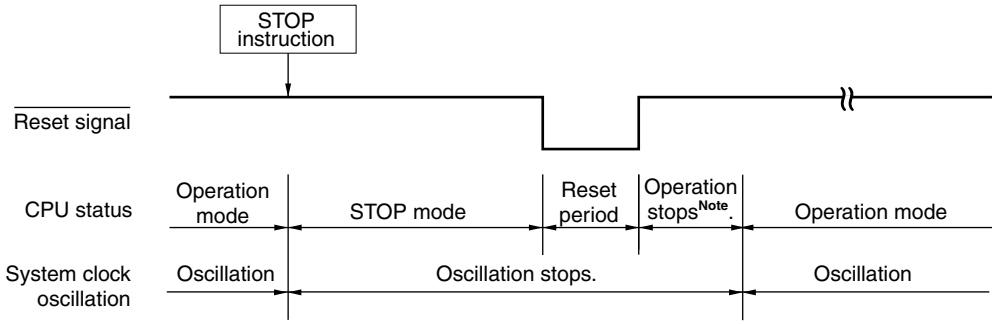
Note “Cannot be stopped” or “Stopped by software” is selected for low-speed internal oscillator by the option byte (for the option byte, see **CHAPTER 18 OPTION BYTE**).

(b) Release by reset signal generation

When the reset signal is generated, STOP mode is released and a reset operation is performed after the oscillation stabilization time has elapsed.

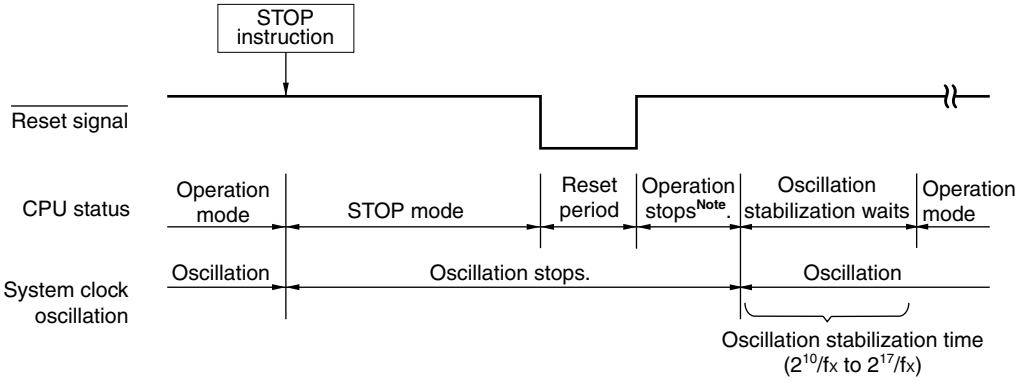
Figure 14-6. STOP Mode Release by Reset Signal Generation

(1) If CPU clock is high-speed internal oscillation clock or external input clock



Note Operation is stopped (277 μs (MIN.), 544 μs (TYP.), 1.075 ms (MAX.)) because the option byte is referenced.

(2) If CPU clock is crystal/ceramic oscillation clock



Note Operation is stopped (276 μs (MIN.), 544 μs (TYP.), 1.074 ms (MAX.)) because the option byte is referenced.

Remark fx: System clock oscillation frequency

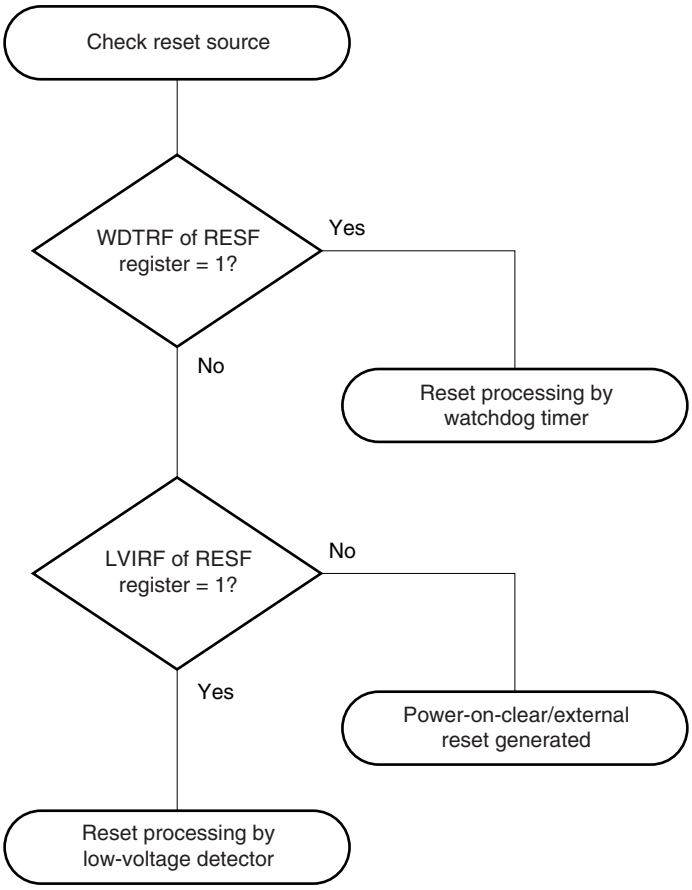
Table 14-5. Operation in Response to Interrupt Request in STOP Mode

Release Source	MK××	IE	Operation
Maskable interrupt request	0	0	Next address instruction execution
	0	1	Interrupt servicing execution
	1	×	STOP mode held
Reset signal generation	–	×	Reset processing

×: don't care

Figure 17-6. Example of Software Processing After Release of Reset (2/2)

• Checking reset source



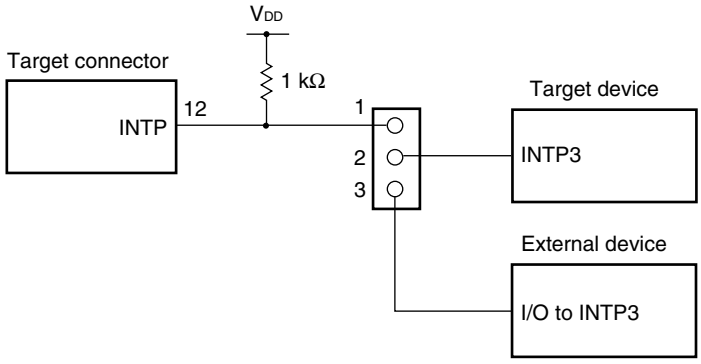
```
;-------------------------------------------------------------------
StatusError:

;-------------------------------------------------------------------
;END (normal termination processing)
;-------------------------------------------------------------------
StatusNormal:

;-------------------------------------------------------------------
; Data to be written
;-------------------------------------------------------------------
DataAdrTop:
        DB      XXH
        DB      XXH
        DB      XXH
        DB      XXH
         :
         :
        DB      XXH
DataAdrBtm:
;-------------------------------------------------------------------
```

Remark Internal verify 2 is used in the above program example. Use internal verify 1 to verify a whole block.

Figure 20-4. Circuit Connection for the Case Where QB-MINI2 Is Used for Debugging and Debugging of INTP3 Pin Is Performed Only with Real Machine



* Jumper setting

When debugging with QB-MINI2 connected: 1-2 shorted

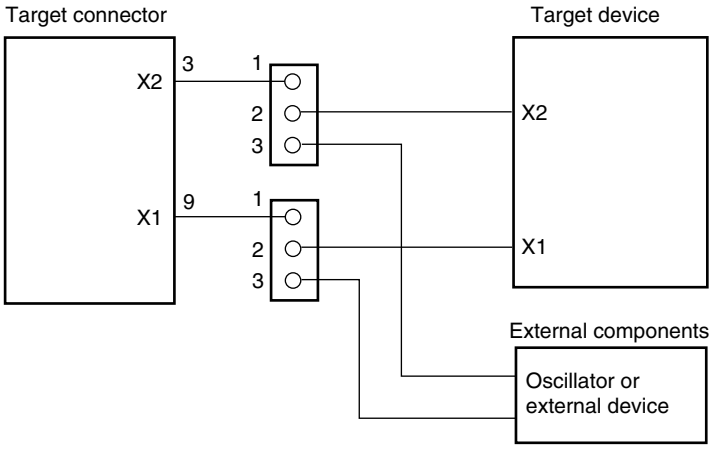
Other than above: 2-3 shorted

Caution If debugging is performed with a real machine running, without using QB-MINI2, write the user program using the QB-Programmer. Programs downloaded by the debugger include the monitor program, and such a program malfunctions if it is not controlled via QB-MINI2.

20.1.2 Connection of X1 and X2 pins

The X1 and X2 pins are used when the debugger is started for the first time (when downloading the monitor program) and when programming is performed with the QB-Programmer.

Figure 20-5. Circuit Connection for the Case Where X1 and X2 Pins Are Used in Target System



* Jumper setting

When debugger is started for the first time (downloading the monitor program) or when programming is performed with QB-Programmer: 1-2 shorted

Other than above: 2-3 shorted

(2/20)

Chapter	Classification	Function	Details of Function	Cautions	Page
Chapter 5	Soft	Main clock	OSTS: Oscillation stabilization time select register	To set and then release the STOP mode, set the oscillation stabilization time as follows. Expected oscillation stabilization time of resonator ≤ Oscillation stabilization time set by OSTS	p.77 ☐
				The wait time after the STOP mode is released does not include the time from the release of the STOP mode to the start of clock oscillation (“a” in the figure below), regardless of whether STOP mode was released by reset signal generation or interrupt generation.	p.77 ☐
				The oscillation stabilization time that elapses on power application or after release of reset is selected by the option byte. For details, refer to CHAPTER 18 OPTION BYTE.	p.77 ☐
	Hard	Crystal/ ceramic oscillator	–	When using the crystal/ceramic oscillator, wire as follows in the area enclosed by the broken lines in Figure 5-6 to avoid an adverse effect from wiring capacitance. • Keep the wiring length as short as possible. • Do not cross the wiring with the other signal lines. Do not route the wiring near a signal line through which a high fluctuating current flows. • Always make the ground point of the oscillator capacitor the same potential as V_{SS}. Do not ground the capacitor to a ground pattern through which a high current flows. • Do not fetch signals from the oscillator.	p.78 ☐
Chapter 6	Hard	16-bit timer/event counter 00	TM00: 16-bit timer counter 00	Even if TM00 is read, the value is not captured by CR010.	pp. ☐ 90, 122
				When TM00 is read, count misses do not occur, since the input of the count clock is temporarily stopped and then resumed after the read.	pp. ☐ 90, 122
	Soft		CR000: 16-bit timer capture/ compare register 000	Set CR000 to other than 0000H in the clear & start mode entered on match between TM00 and CR000. This means a 1-pulse count operation cannot be performed when this register is used as an external event counter.	pp. ☐ 91, 122
				In the free-running mode and in the clear & start mode using the valid edge of TI000 pin, if CR000 is set to 0000H, an interrupt request (INTTM000) is generated when CR000 changes from 0000H to 0001H following overflow (FFFFH).	pp. ☐ 91, 122
				If the new value of CR000 is less than the value of 16-bit timer counter 0 (TM00), TM00 continues counting, overflows, and then starts counting from 0 again. If the new value of CR000 is less than the old value, therefore, the timer must be reset to be restarted after the value of CR000 is changed.	pp. ☐ 91, 122
				The value of CR000 after 16-bit timer/event counter 00 has stopped is not guaranteed.	pp. ☐ 91, 123
	Hard			The capture operation may not be performed for CR000 set in compare mode even if a capture trigger is input.	pp. ☐ 91, 126
				When using P31 as the input pin (TI010) of the valid edge, it cannot be used as a timer output pin (TO00). When using P31 as the timer output pin (TO00), it cannot be used as the input pin (TI010) of the valid edge.	pp. ☐ 91, 127

(6/20)

Chapter	Classification	Function	Details of Function	Cautions	Page
Chapter 6	Hard	16-bit timer/event counter 00	One-shot pulse output with external trigger	Do not input the external trigger again while the one-shot pulse is being output. To output the one-shot pulse again, wait until the current one-shot pulse output is completed.	pp. ☐ 119, 124
	Soft			Do not set 0000H to the CR000 and CR010 registers.	pp. ☐ 120, 124
				16-bit timer counter 00 starts operating as soon as a value other than 00 (operation stop mode) is set to the TMC003 and TMC002 bits.	pp. ☐ 121, 122
	Hard		Timer start errors	An error of up to one clock may occur in the time required for a match signal to be generated after timer start. This is because 16-bit timer counter 00 (TM00) is started asynchronously to the count clock.	p.122 ☐
	Soft		One-shot pulse output	One-shot pulse output normally operates only in the free-running mode or in the clear & start mode at the valid edge of the TI000 pin. Because an overflow does not occur in the clear & start mode on a match between TM00 and CR000, one-shot pulse output is not possible.	p.123 ☐
			Capture operation	If both the rising and falling edges are selected as the valid edges of the TI000 pin, capture is not performed.	p.125 ☐
				When the CRC001 bit value is 1, the TM00 count value is not captured in the CR000 register when a valid edge of the TI010 pin is detected, but the input from the TI010 pin can be used as an external interrupt source because INTTM000 is generated at that timing.	p.125 ☐
			Changing compare register during timer operation	With the 16-bit timer capture/compare register 0n0 (CR0n0) used as a compare register, when changing CR0n0 around the timing of a match between 16-bit timer counter 00 (TM00) and 16-bit timer capture/compare register 0n0 (CR0n0) during timer counting, the change timing may conflict with the timing of the match, so the operation is not guaranteed in such cases. To change CR0n0 during timer counting, follow the procedure below using an INTTM000 interrupt.	p.126 ☐
				If CR010 is changed during timer counting without performing processing <1> above, the value in CR010 may be rewritten twice or more, causing an inversion of the output level of the TO00 pin at each rewrite.	p.126 ☐
			External event counter	The timing of the count start is after two valid edge detections.	p.127 ☐
	Hard		External clock limitation	When using an input pulse of the TI000 pin as a count clock (external trigger), be sure to input the pulse width which satisfies the AC characteristics. For the AC characteristics, refer to CHAPTER 22 and CHAPTER 23 ELECTRICAL SPECIFICATIONS.	p.128 ☐
				When an external waveform is input to 16-bit timer/event counter 00, it is sampled by the noise limiter circuit and thus an error occurs on the timing to become valid inside the device.	p.128 ☐
Chapter 7	Soft	8-bit timer 80	CR80: 8-bit compare register 80	When changing the value of CR80, be sure to stop the timer operation. If the value of CR80 is changed with the timer operation enabled, a match interrupt request signal is generated immediately and the timer may be cleared.	p.131 ☐
			TMC80: 8-bit timer mode control register 80	Be sure to set TMC80 after stopping the timer operation.	p.132 ☐
				Be sure to clear bits 0 and 6 to 0.	p.132 ☐

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Chapter	Classification	Function	Details of Function	Cautions	Page
Chapter 9	Soft	Watchdog timer	WDTM: Watchdog timer mode register	WDTM cannot be set by a 1-bit memory manipulation instruction.	p.155 ☐
				When using the flash memory programming by self programming, set the overflow time for the watchdog timer so that enough overflow time is secured (Example 1-byte writing: 200 μs MIN., 1-block deletion: 10 ms MIN.).	p.155 ☐
			WDTE: Watchdog timer enable register	If a value other than ACH is written to WDTE, an internal reset signal is generated.	p.155 ☐
				If a 1-bit memory manipulation instruction is executed for WDTE, an internal reset signal is generated.	p.155 ☐
				The value read from WDTE is 9AH (this differs from the written value (ACH)).	p.155 ☐
	Hard		When "low-speed internal oscillator cannot be stopped" is selected by option byte	In this mode, operation of the watchdog timer cannot be stopped even during STOP instruction execution. For 8-bit timer H1 (TMH1), a division of the low-speed internal oscillation clock can be selected as the count source, so clear the watchdog timer using the interrupt request of TMH1 before the watchdog timer overflows after STOP instruction execution. If this processing is not performed, an internal reset signal is generated when the watchdog timer overflows after STOP instruction execution.	p.156 ☐
			When "low-speed internal oscillator can be stopped by software" is selected by option byte	In this mode, watchdog timer operation is stopped during HALT/STOP instruction execution. After HALT/STOP mode is released, counting is started again using the operation clock of the watchdog timer set before HALT/STOP instruction execution by WDTM. At this time, the counter is not cleared to 0 but holds its value.	p.158 ☐
Chapter 10	Soft	A/D converter	Sampling time and conversion time	The above sampling time and conversion time do not include the clock frequency error. Select the sampling time and conversion time such that Notes 2 and 3 above are satisfied, while taking the clock frequency error into consideration (an error margin maximum of ±5% when using the high-speed internal oscillator).	p.164 ☐
			ADM: A/D converter mode register	The above sampling time and conversion time do not include the clock frequency error. Select the sampling time and conversion time such that Notes 3 and 4 above are satisfied, while taking the clock frequency error into consideration (an error margin maximum of ±5% when using the high-speed internal oscillator).	p.169 ☐
				If a bit other than ADCS of ADM is manipulated while A/D conversion is stopped (ADCS = 0) and then A/D conversion is started, execute two NOP instructions or an instruction equivalent to two machine cycles, and set ADCS to 1.	p.170 ☐
				A/D conversion must be stopped (ADCS = 0) before rewriting bits FR0 to FR2.	p.170 ☐
				Be sure to clear bits 6, 2, and 1 to 0.	p.170 ☐
			ADS: Analog input channel specification register	Be sure to clear bits 2 to 7 of ADS to 0.	p.170 ☐
			ADCR: 10-bit A/D conversion result register	When writing to the A/D converter mode register (ADM) and analog input channel specification register (ADS), the contents of ADCR may become undefined. Read the conversion result following conversion completion before writing to ADM and ADS. Using timing other than the above may cause an incorrect conversion result to be read.	p.170 ☐

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Chapter	Classification	Function	Details of Function	Cautions	Page
Chapter 10	Hard	A/D converter	Input impedance of ANI0 to ANI3 pins	In this A/D converter, the internal sampling capacitor is charged and sampling is performed during sampling time. Since only the leakage current flows other than during sampling and the current for charging the capacitor also flows during sampling, the input impedance fluctuates both during sampling and otherwise. If the shortest conversion time of the reference voltage is used, to perform sufficient sampling, it is recommended to make the output impedance of the analog input source 1 kΩ or lower, or attach a capacitor of around 0.01 μF to 0.1 μF to the ANI0 to ANI3 pins (see Figure 10-19).	p.180 □
	Soft		ADIF: Interrupt request flag	The interrupt request flag (ADIF) is not cleared even if the analog input channel specification register (ADS) is changed. Therefore, if an analog input pin is changed during A/D conversion, the A/D conversion result and ADIF for the pre-change analog input may be set just before the ADS rewrite. Caution is therefore required since, at this time, when ADIF is read immediately after the ADS rewrite, ADIF is set despite the fact A/D conversion for the post-change analog input has not ended. When A/D conversion is stopped and then resumed, clear ADIF before the A/D conversion operation is resumed.	p.180 □
			Conversion results just after A/D conversion start	The first A/D conversion value immediately after A/D conversion starts may not fall within the rating range if the ADCS bit is set to 1 within 1 μs after the ADCE bit was set to 1, or if the ADCS bit is set to 1 with the ADCE bit = 0. Take measures such as polling the A/D conversion end interrupt request (INTAD) and removing the first conversion result.	p.181 □
			A/D conversion result register (ADCR, ADCRH) read operation	When a write operation is performed to the A/D converter mode register (ADM) and analog input channel specification register (ADS), the contents of ADCR and ADCRH may become undefined. Read the conversion result following conversion completion before writing to ADM and ADS. Using a timing other than the above may cause an incorrect conversion result to be read.	p.181 □
	Hard		Operating current at conversion waiting mode	The DC characteristic of the operating current during the STOP mode is not satisfied due to the conversion waiting mode (only the comparator consumes power), when bit 7 (ADCS) and bit 0 (ADCE) of the A/D converter mode register (ADM) are set to 0 and 1 respectively.	p.181 □
Chapter 11	Hard	Serial interface UART6	UART mode	The TxD6 output inversion function inverts only the transmission side and not the reception side. To use this function, the reception side must be ready for reception of inverted data.	p.182 □
	Soft			If clock supply to serial interface UART6 is not stopped (e.g., in the HALT mode), normal operation continues. If clock supply to serial interface UART6 is stopped (e.g., in the STOP mode), each register stops operating, and holds the value immediately before clock supply was stopped. The TxD6 pin also holds the value immediately before clock supply was stopped and outputs it. However, the operation is not guaranteed after clock supply is resumed. Therefore, reset the circuit so that POWER6 = 0, RXE6 = 0, and TXE6 = 0.	p.182 □
				If data is continuously transmitted, the communication timing from the stop bit to the next start bit is extended two operating clocks of the macro. However, this does not affect the result of communication because the reception side initializes the timing when it has detected a start bit. Do not use the continuous transmission function if the interface used in LIN communication operation.	p.182 □

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Chapter	Classification	Function	Details of Function	Cautions	Page
Chapter 23	Hard	Electrical specifications ((A2) grade product)	Absolute maximum ratings	Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.	p.356 ☐
			X1 oscillator	When using the X1 oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance. • Keep the wiring length as short as possible. • Do not cross the wiring with the other signal lines. • Do not route the wiring near a signal line through which a high fluctuating current flows. • Always make the ground point of the oscillator capacitor the same potential as V_{SS}. • Do not ground the capacitor to a ground pattern through which a high current flows. • Do not fetch signals from the oscillator.	p.358 ☐
			A/D converter	The conversion accuracy may be degraded if the analog input pin is used as an alternate I/O port or if a port is changed during A/D conversion.	p.365 ☐
Chapter 25	Hard	Recommended soldering conditions	Lead-free products	Products with –A or –AX at the end of the part number are lead-free products.	p.373 ☐
			–	For soldering methods and conditions other than those recommended below, contact an NEC Electronics sales representative.	p.373 ☐
				Do not use different soldering methods together (except for partial heating).	pp. ☐ 373, 374
				Only the pins of the THD are heated when performing wave soldering. Make sure that flow solder does not come in contact with the package.	p.374 ☐