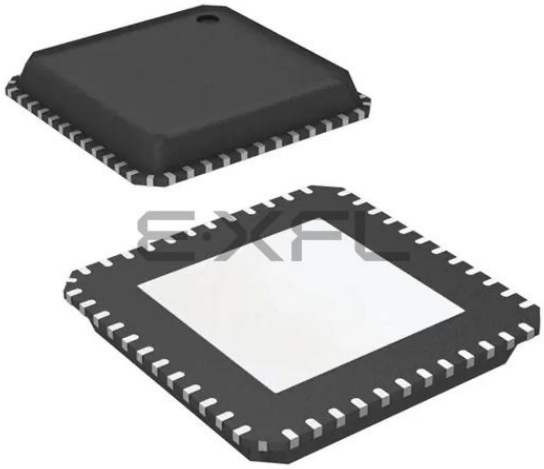

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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	Automotive
Core Processor	ARM® Cortex®-M3
Program Memory Type	FLASH (64kB)
Controller Series	-
RAM Size	6K x 8
Interface	LIN, SSI, UART
Number of I/O	10
Voltage - Supply	5.5V ~ 28V
Operating Temperature	-40°C ~ 175°C
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	PG-VQFN-48-29
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/tle9877qxw40xuma1

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Number	Type	Reset State[1)]	Function
P2				**Port 2** Port 2 is a 5-bit general purpose input-only port. Alternate functions can be assigned and are listed in the Port description. Main function is listed below.
P2.0/XTAL1	29	I/I	I	AN0 ADC analog input 0 Alternate function mapping see **Table 10**
P2.2/XTAL2	30	I/O	I	AN2 ADC analog input 2 Alternate function mapping see **Table 10**
P2.3	35	I	I	AN3 ADC analog input 3 Alternate function mapping see **Table 10**
P2.4	32	I	I	AN4 ADC analog input 4 Alternate function mapping see **Table 10**
P2.5	31	I	I	AN5 ADC analog input 5 Alternate function mapping see **Table 10**
Power Supply				
VS	45	P	–	Battery supply input
VDDP	40	P	–	[2)]I/O port supply (5.0 V). Connect external buffer capacitor.
VDDC	38	P	–	[3)]Core supply (1.5 V during Active Mode). Do not connect external loads, connect external buffer capacitor.
VDDEXT	41	P	–	External voltage supply output (5.0 V, 20 mA)
GND	19	P	–	GND digital
GND	28	P	–	GND digital
GND	39	P	–	GND analog
Monitor Input				
MON	14	I	–	High Voltage Monitor Input
LIN Interface				
LIN	43	I/O	–	LIN bus interface input/output
GND_LIN	42	P	–	LIN ground
Charge Pump				
CP1H	48	P	–	Charge Pump Capacity 1 High, connect external C
CP1L	1	P	–	Charge Pump Capacity 1 Low, connect external C
CP2H	3	P	–	Charge Pump Capacity 2 High, connect external C
CP2L	4	P	–	Charge Pump Capacity 2 Low, connect external C
VCP	2	P	–	Charge Pump Capacity
VSD	47	P	–	Battery supply input for Charge Pump
MOSFET Driver				
VDH	44	P	–	Voltage Drain High Side MOSFET Driver
SH3	46	P	–	Source High Side FET 3
SH2	6	P	–	Source High Side FET 2

4 Modes of Operation

This highly integrated circuit contains analog and digital functional blocks. An embedded 32-bit microcontroller is available for system and interface control. On-chip, low-dropout regulators are provided for internal and external power supply. An internal oscillator provides a cost effective clock that is particularly well suited for LIN communications. A LIN transceiver is available as a communication interface. Driver stages for a Motor Bridge or BLDC Motor Bridge with external MOSFET are integrated, featuring PWM capability, protection features and a charge pump for operation at low supply voltage. A 10-bit SAR ADC is implemented for high precision sensor measurement. An 8-bit ADC is used for diagnostic measurements.

The Micro Controller Unit supervision and system protection (including a reset feature) is complemented by a programmable window watchdog. A cyclic wake-up circuit, supply voltage supervision and integrated temperature sensors are available on-chip.

All relevant modules offer power saving modes in order to support automotive applications connected to terminal 30. A wake-up from power-save mode is possible via a LIN bus message, via the monitoring input or using a programmable time period (cyclic wake-up).

Featuring LTI, the integrated circuit is available in a VQFN-48-29 package with 0.5 mm pitch, and is designed to withstand the severe conditions of automotive applications.

The TLE9877QXW40 has several operation modes mainly to support low power consumption requirements.

Reset Mode

The Reset Mode is a transition mode used e.g. during power-up of the device after a power-on reset, or after wake-up from Sleep Mode. In this mode, the on-chip power supplies are enabled and all other modules are initialized. Once the core supply VDDC is stable, the device enters Active Mode. If the watchdog timer WDT1 fails more than four times, the device performs a fail-safe transition to Sleep Mode.

Active Mode

In Active Mode, all modules are activated and the TLE9877QXW40 is fully operational.

Stop Mode

Stop Mode is one of two major low power modes. The transition to the low power modes is performed by setting the corresponding bits in the mode control register. In Stop Mode the embedded microcontroller is still powered, allowing faster wake-up response times. Wake-up from this mode is possible through LIN bus activity, by using the high-voltage monitoring pin or the corresponding 5V GPIOs.

Stop Mode with Cyclic Wake-Up

The Cyclic Wake-Up Mode is a special operating mode of the Stop Mode. The transition to the Cyclic Wake-Up Mode is done by first setting the corresponding bits in the mode control register followed by the Stop Mode command. In addition to the cyclic wake-up behavior (wake-up after a programmable time period), asynchronous wake events via the activated sources (LIN and/or MON) are available, as in normal Stop Mode.

Sleep Mode

The Sleep Mode is a low-power mode. The transition to the low-power mode is done by setting the corresponding bits in the MCU mode control register or in case of failure, see below. In Sleep Mode the embedded microcontroller power supply is deactivated allowing the lowest system power consumption. A wake-up from this mode is possible by LIN bus activity, the High Voltage Monitor Input pin or Cyclic Wake-up.

Sleep Mode in Case of Failure

5.2.2 PMU Modes Overview

The following state diagram shows the available modes of the device.

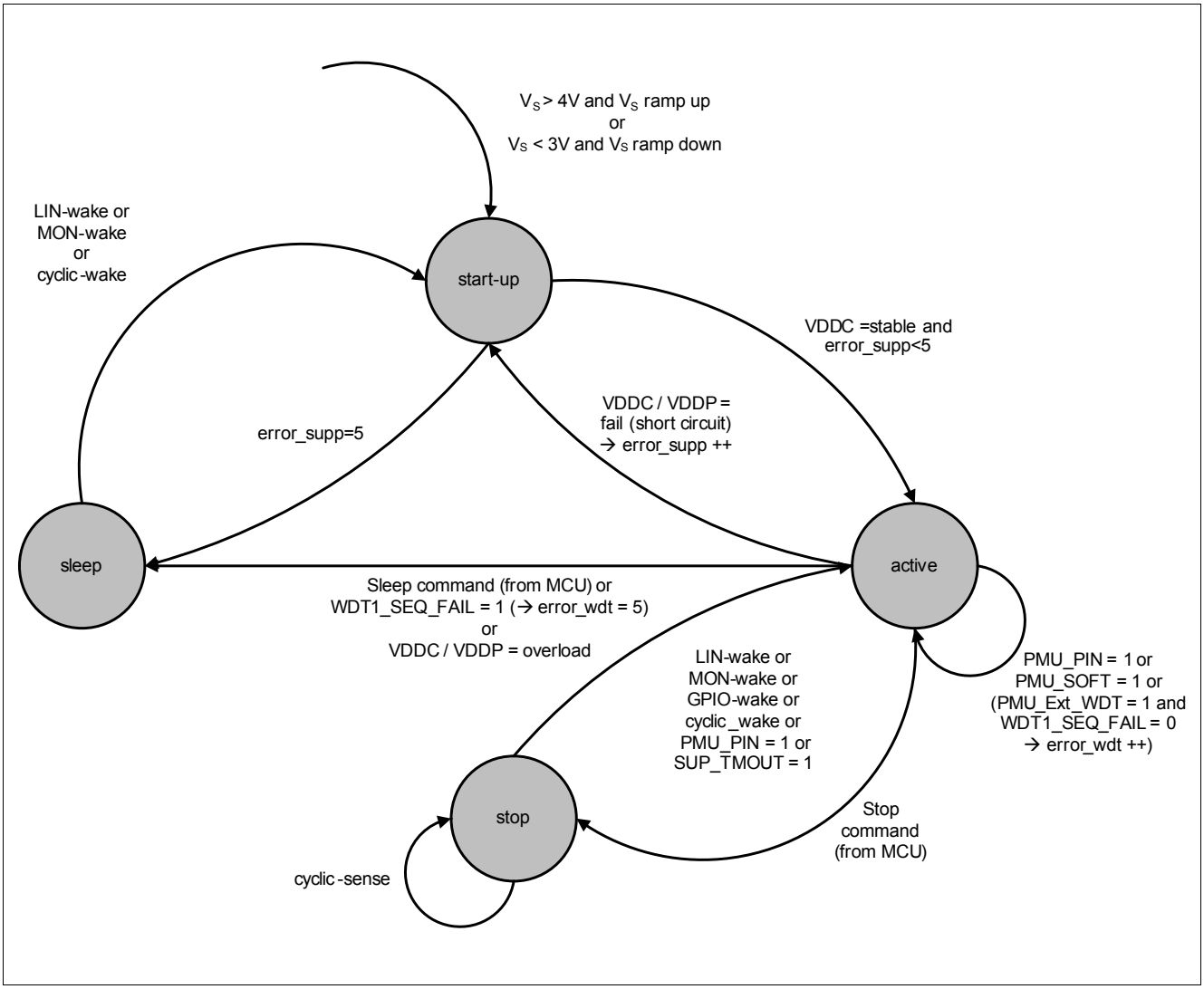

Figure 4 Power Management Unit System Modes

5.3.2 Voltage Regulator 1.5V (VDDC)

This module represents the 1.5 V voltage regulator, which provides the supply for the microcontroller core, the digital peripherals and other internal analog 1.5 V functions (e.g. ADC2) of the chip. To further reduce the current consumption of the MCU during Stop Mode the output voltage can be lowered to 1.1 V.

Features

- 1.5 V low-drop voltage regulator
- Overcurrent monitoring and shutdown with MCU signaling (interrupt)
- Overvoltage monitoring with MCU signaling (interrupt)
- Undervoltage monitoring with MCU signaling (interrupt)
- Undervoltage monitoring with reset
- Pull Down Current Source at the output for Sleep Mode only (typ. 100 A)

The output capacitor C_{VDDC} is mandatory to ensure a proper regulator functionality.

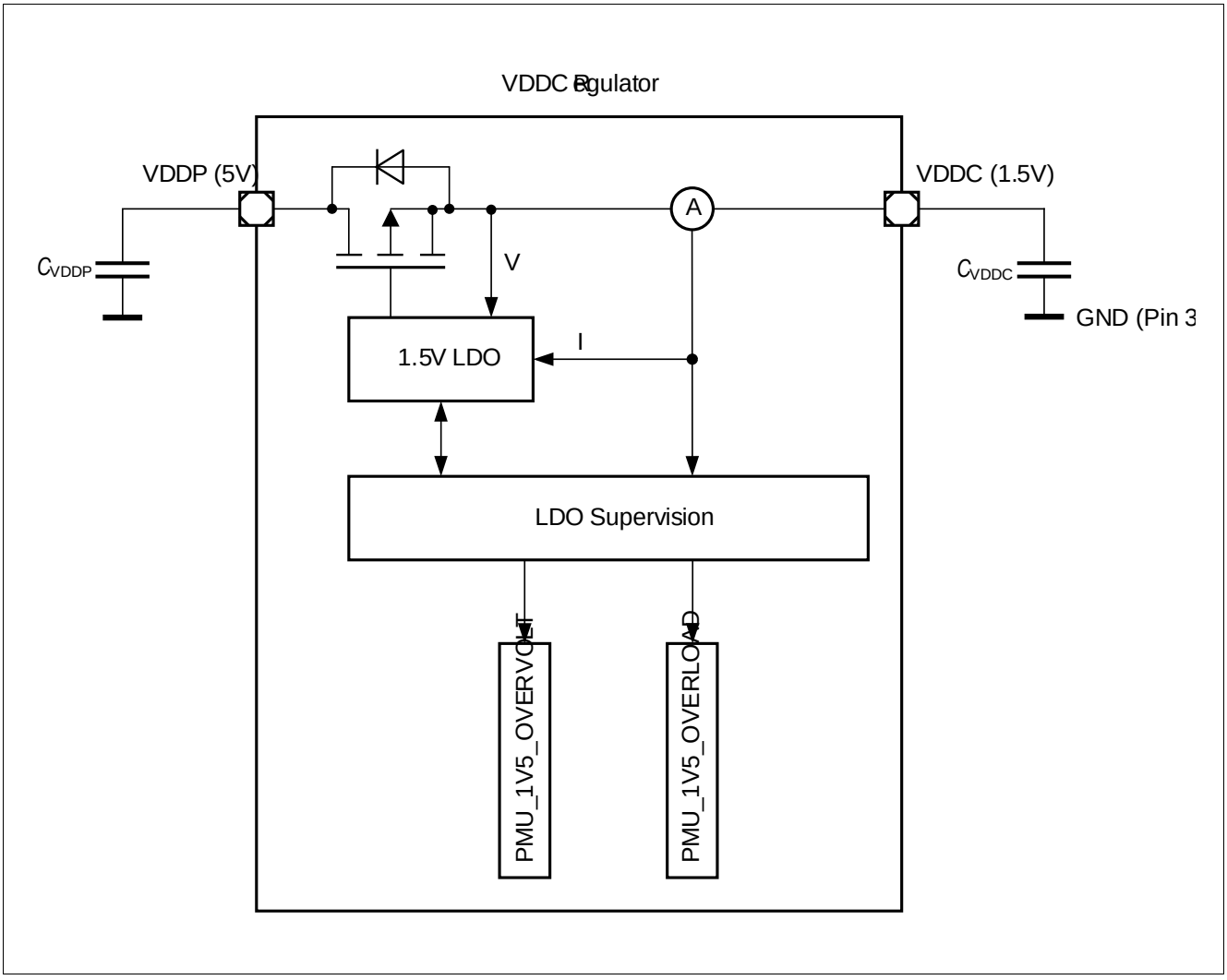

Figure 6 Module Block Diagram of VDDC Voltage Regulator

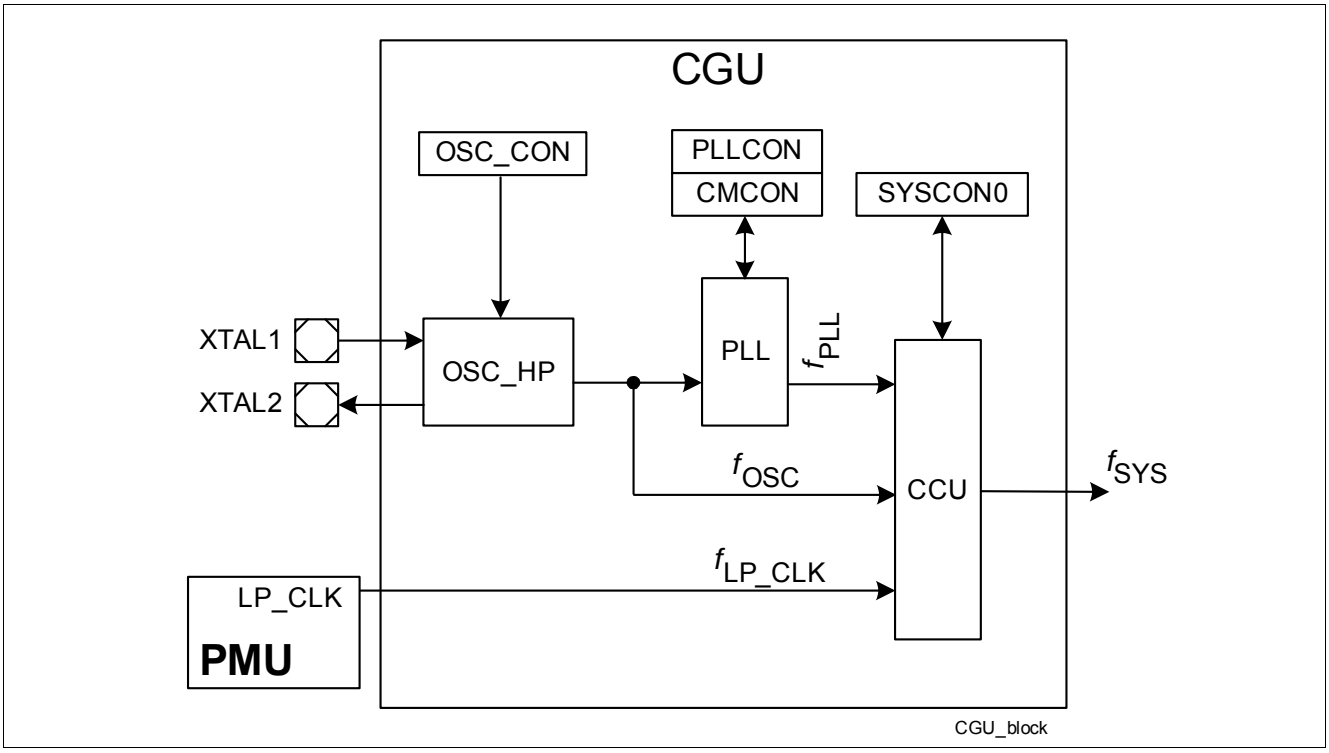

Figure 9 Clock Generation Unit Block Diagram

The following sections describe the different parts of the CGU.

6.3.1 Low Precision Clock

The clock source LP_CLK is a low-precision RC oscillator (LP-OSC) with a nominal frequency of 18 MHz that is enabled by hardware as an independent clock source for the TLE9877QXW40 startup after reset and during the power-down wake-up sequence. f_{LP_CLK} is not user configurable.

6.3.2 High Precision Oscillator Circuit (OSC_HP)

The high precision oscillator circuit, designed to work with both an external crystal oscillator or an external stable clock source, consists of an inverting amplifier with XTAL1 as the input, and XTAL2 as the output.

Figure 10 shows the recommended external circuitry for both operating modes, External Crystal Mode and External Input Clock Mode.

6.3.2.1 External Input Clock Mode

When supplying the clock signal directly, not using an external crystal and bypassing the oscillator, the input frequency needs to be equal or greater than 4 MHz if the PLL VCO part is used.

When using an external clock signal it must be connected to XTAL1. XTAL2 is left open (unconnected).

6.3.2.2 External Crystal Mode

When using an external crystal, its frequency can be within the range of 4 MHz to 25 MHz. An external oscillator load circuitry must be used, connected to both pins, XTAL1 and XTAL2. It normally consists of the two load capacitances C1 and C2. A series damping resistor could be required for some crystals. The exact values and the corresponding operating ranges depend on the crystal and have to be determined and optimized in cooperation with the crystal vendor using the negative resistance method. The following load cap values can be used as starting point for the evaluation:

7 System Control Unit - Power Modules (SCU-PM)

7.1 Features

- Clock Watchdog Unit (CWU): supervision of all clocks with NMI signaling relevant to power modules
- Interrupt Control Unit (ICU): all interrupt flags and status flags with system relevance
- Power Control Unit (PCU): takes over control when device enters and exits Sleep and Stop Mode
- External Watchdog (WDT1): independent system watchdog for monitoring system activity

7.2 Introduction

7.2.1 Block Diagram

The System Control Unit of the power modules consists of the sub-modules in the figure shown below:

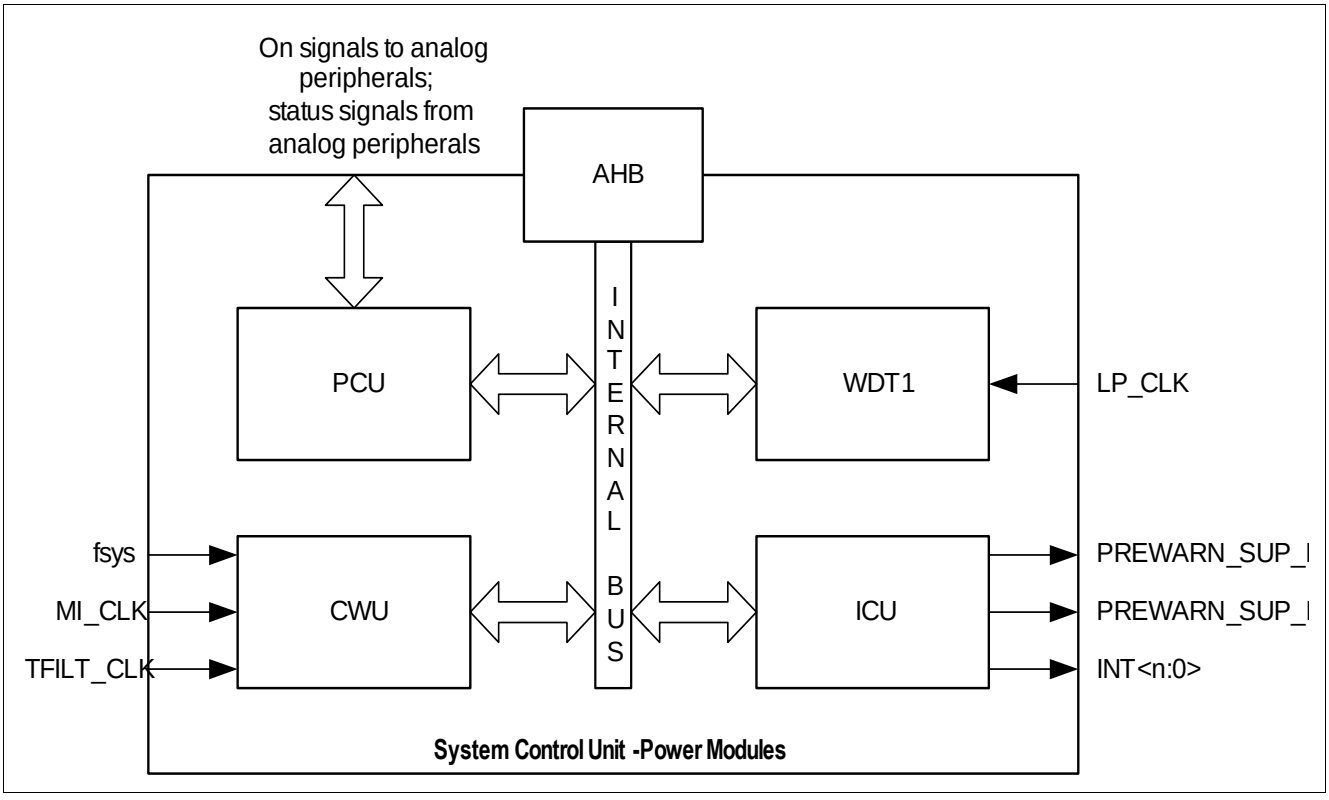

Figure 11 Block diagram of System Control Unit - Power Modules

AHB (Advanced High-Performance Bus)

CWU (Clock Watchdog Unit)

- f_{sys} system frequency: PLL output
- MI_CLK measurement interface clock (analog clock): derived from fsys using division factors 1/2/3/4
- TFILT_CLK clock used for digital filters: derived from fsys using configurable division factors

10 Address Space Organization

The TLE9877QXW40 manipulates operands in the following memory spaces:

- 64 KByte of Flash memory in code space
- 32 KByte Boot ROM memory in code space (used for boot code and IP storage)
- 6 KByte RAM memory in code space and data space (RAM can be read/written as program memory or external data memory)
- Special function registers (SFRs) in peripheral space

The figure below shows the detailed address alignment of TLE9877QXW40:

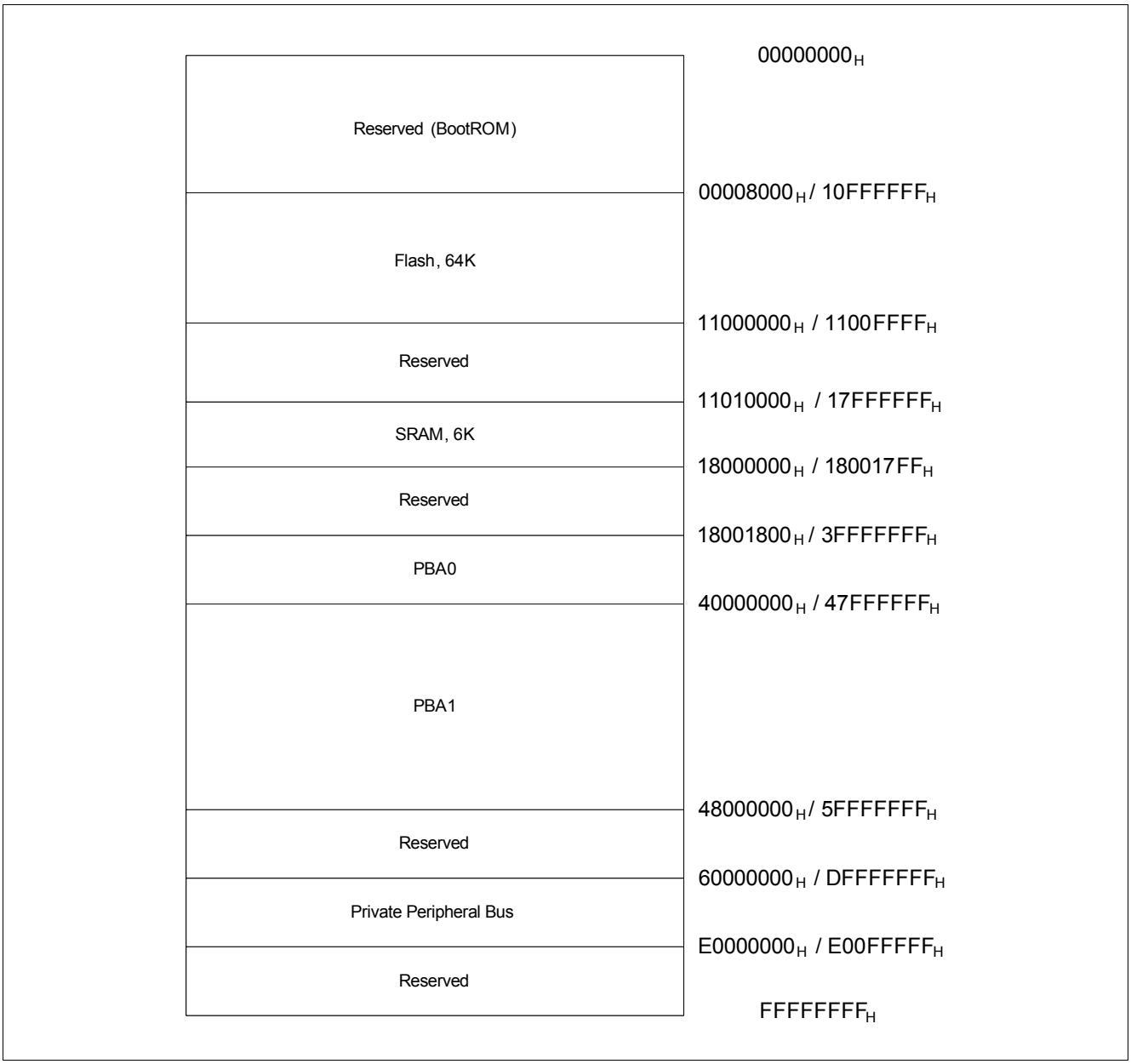

Figure 14 TLE9877QXW40 Memory Map

14.3 TLE9877QXW40 Port Module

14.3.1 Port 0

14.3.1.1 Port 0 Functions

Table 8 Port 0 Input/Output Functions

Port Pin	Input/Output	Select	Connected Signal(s)	From/to Module
P0.0	Input	GPI	P0_DATA.P0	
		INP1	SWCLK / TCK_0	SW
		INP2	T12HR_0	CCU6
		INP3	T4INA	GPT12T4
		INP4	T2_0	Timer 2
		INP5	–	–
		INP6	EXINT2_3	SCU
	Output	GPO	P0_DATA.P0	
		ALT1	T3OUT	GPT12T3
		ALT2	EXF21_0	Timer 21
		ALT3	RXDO_2	UART2
P0.1	Input	GPI	P0_DATA.P1	
		INP2	T13HR_0	CCU6
		INP3	TxD1	LIN_TxD
		INP4	CAPINA	GPT12CAP
		INP5	T21_0	Timer 21
		INP6	T4INC	GPT12T4
		INP7	MRST_1_2	SSC1
		INP8	EXINT0_2	SCU
	Output	GPO	P0_DATA.P1	
		ALT1	TxD1	UART1 / LIN_TxD
		ALT2	–	–
		ALT3	T6OUT	GPT12T6

16 Timer2 and Timer21

16.1 Features

- 16-bit auto-reload mode
  - selectable up or down counting
- One channel 16-bit capture mode

16.2 Introduction

The timer modules are general-purpose 16-bit timers. Timer 2/21 can function as a timer or counter in each of its modes. As a timer, it counts with an input clock of $f_{PCLK}/12$ (if prescaler is disabled). As a counter, Timer 2 counts 1-to-0 transitions on pin T2. In the counter mode, the maximum resolution for the count is $f_{PCLK}/24$ (if prescaler is disabled).

16.2.1 Timer2 and Timer21 Modes Overview

Table 11 Timer2 and Timer21 Modes

Mode	Description
Auto-reload	**Up/Down Count Disabled** • Count up only • Start counting from 16-bit reload value, overflow at $FFFF_H$ • Reload event configurable for trigger by overflow condition only, or by negative/positive edge at input pin T2EX as well • Programmable reload value in register RC2 • Interrupt is generated with reload events.
Auto-reload	**Up/Down Count Enabled** • Count up or down, direction determined by level at input pin T2EX • No interrupt is generated • Count up – Start counting from 16-bit reload value, overflow at $FFFF_H$ – Reload event triggered by overflow condition – Programmable reload value in register RC2 • Count down – Start counting from $FFFF_H$, underflow at value defined in register RC2 – Reload event triggered by underflow condition – Reload value fixed at $FFFF_H$
Channel capture	• Count up only • Start counting from 0000_H, overflow at $FFFF_H$ • Reload event triggered by overflow condition • Reload value fixed at 0000_H • Capture event triggered by falling/rising edge at pin T2EX • Captured timer value stored in register RC2 • Interrupt is generated by reload or capture events

Table 12 Timer3 Modes (cont'd)

Mode	Sub-Mode	Operation
2	**No Sub-Mode**	**8-bit Timer with auto-reload** The timer register TL3 is reloaded with a user-defined 8-bit value in TH3 upon overflow.
3	**a**	**Timer3 operates as two 8-bit timers** The timer registers TL3 and TH3, operate as two separate 8-bit counters.
3	**b**	**Timer3 operates as Two 8-bit timers for clock measurement** The timer registers, TL3 and TH3 operate as two separate 8-bit counters. In this mode the LP_CLK2 Low Power Clock can be measured. TL3 acts as an edge counter for the clock edges and TH3 as a counter which counts the time between the edges.

28 Application Information

28.1 BLDC Driver

Figure 32 shows the TLE9877QXW40 in an electric drive application setup controlling a BLDC motor.

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

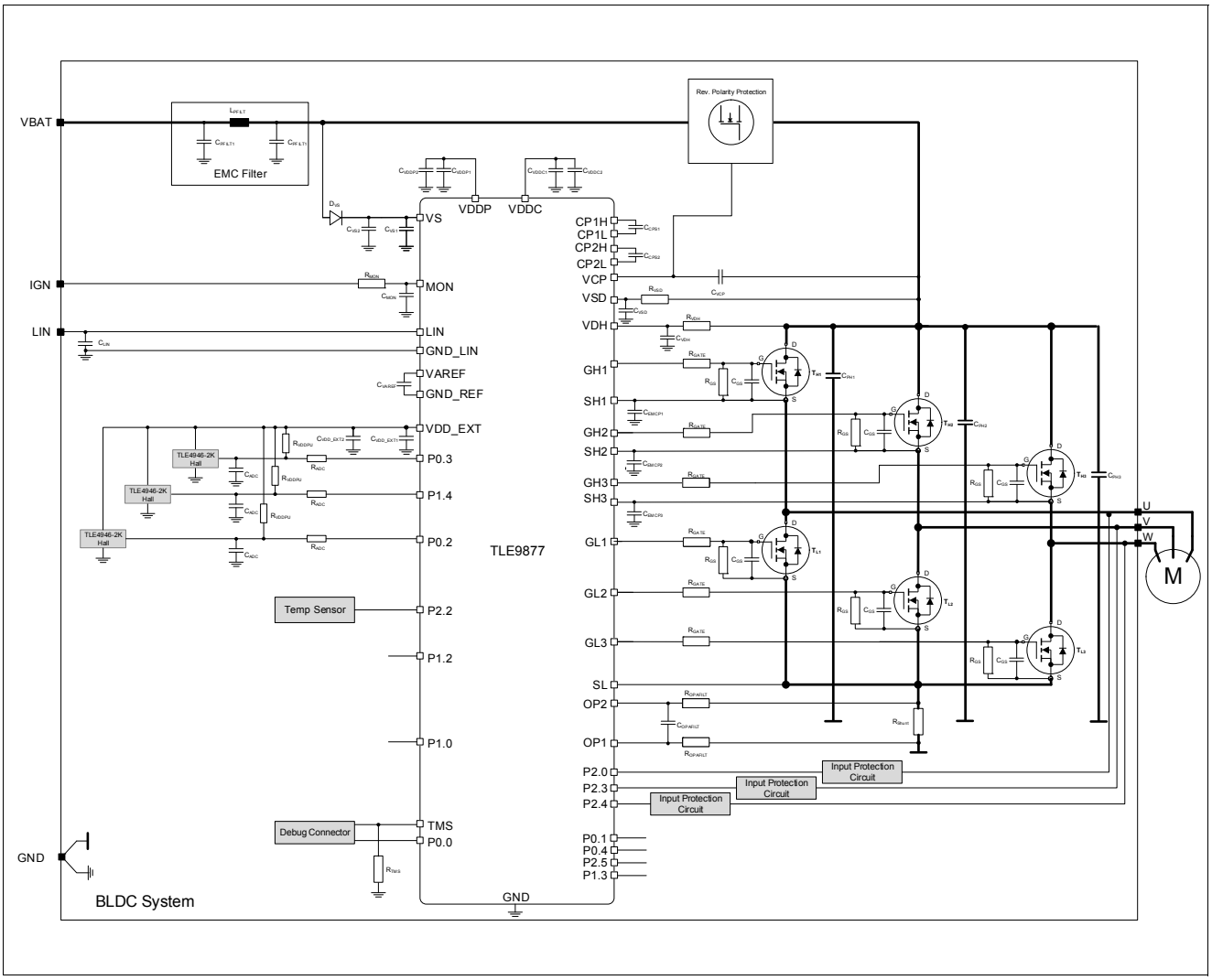

Figure 32 Simplified Application Diagram Example

Note: This is a very simplified example of an application circuit and bill of materials. The function must be verified in the actual application.

4) Min voltage -2.8V with external 1k series resistor only.
5) To achieve max. ratings on this pin, Parameter P_1.1.44 has to be taken into account resulting in the following dependency: $V_{GH} < V_{SH} + V_{GHvsSH\_min}$ and additionally $V_{SH} < V_{GH} + 0.3V$.
6) To achieve max. ratings on this pin, Parameter P_1.1.45 has to be taken into account resulting in the following dependency: $V_{GL} < V_{SL} + V_{GLvsSL\_min}$ and additionally $V_{SL} < V_{GL} + 0.3V$.
7) These limits can be kept if max current drawn out of pin does not exceed limit of 200 µA.
8) See XTAL parameter specification, when GPIOs (Port Pin P2.0 and P2.2) are used as XTAL.
9) Includes TMS and RESET.
10) Maximum rating for injection current of GPIO with V_{IN} respected.
11) ESD susceptibility HBM according to ANSI/ESDA/JEDEC JS-001 (1.5k , 100pF)
12) MON with external circuitry of a series resistor of 3.9k and 10nF (at connector); VS with an external ceramic capacitor of 100nF; VSD with an external capacitor of 470nF; VDH with external circuitry of a series resistor of 1k and 3.3nF (at pin).
13) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JESD22-C101F

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

29.4 Flash Memory

This chapter includes the parameters for the 64 kByte embedded flash module.

29.4.1 Flash Parameters

Table 29 Flash Characteristics[1)]

V_S = 3.0 V to 28 V, T_j = -40 °C to +175 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Programming time per 128 byte page	t_{PR}	–	3[2)]	3.5	ms	3V < V_S < 28V	P_4.1.1
Erase time per sector/page	t_{ER}	–	4[2)]	4.5	ms	3V < V_S < 28V	P_4.1.2
Data retention time	t_{RET}	20	–	–	years	1,000 erase / program cycles	P_4.1.3
Data retention time	t_{RET}	50	–	–	years	1,000 erase / program cycles T_j = 30°C[3)]	P_4.1.9
Flash erase endurance for user sectors	N_{ER}	30	–	–	kcycles	Data retention time 5 years	P_4.1.4
Flash erase endurance for security pages	N_{SEC}	10	–	–	cycles	[4)]Data retention time 20 years	P_4.1.5
Drain disturb limit	N_{DD}	32	–	–	kcycles	[5)]	P_4.1.6
Junction temperature range 1	$T_{j\_extend\_1}$	-40	–	150	°C		P_4.1.10
Junction temperature range 2	$T_{j\_extend\_2}$	-40	–	165	°C	[1)]incl. Flash erase/write/read	P_4.1.11
Junction temperature range 3	$T_{j\_extend\_3}$	165	–	175	°C	[1)]incl. Flash read	P_4.1.12

1) Not subject for production test, specified by design.

2) Programming and erase times depend on the internal Flash clock source. The control state machine needs a few system clock cycles. The requirement is only relevant for extremely low system frequencies.

3) Derived by extrapolation of lifetime tests.

4) T_j = 25 °C.

5) This parameter limits the number of subsequent programming operations within a physical sector without a given page in this sector being (re-)programmed. The drain disturb limit is applicable if wordline erase is used repeatedly. For normal sector erase/program cycles this limit will not be violated. For data sectors the integrated EEPROM emulation firmware routines handle this limit automatically, for wordline erases in code sectors (without EEPROM emulation) it is recommended to execute a software based refresh, which may make use of the integrated random number generator NVMBRNG to statistically start a refresh.

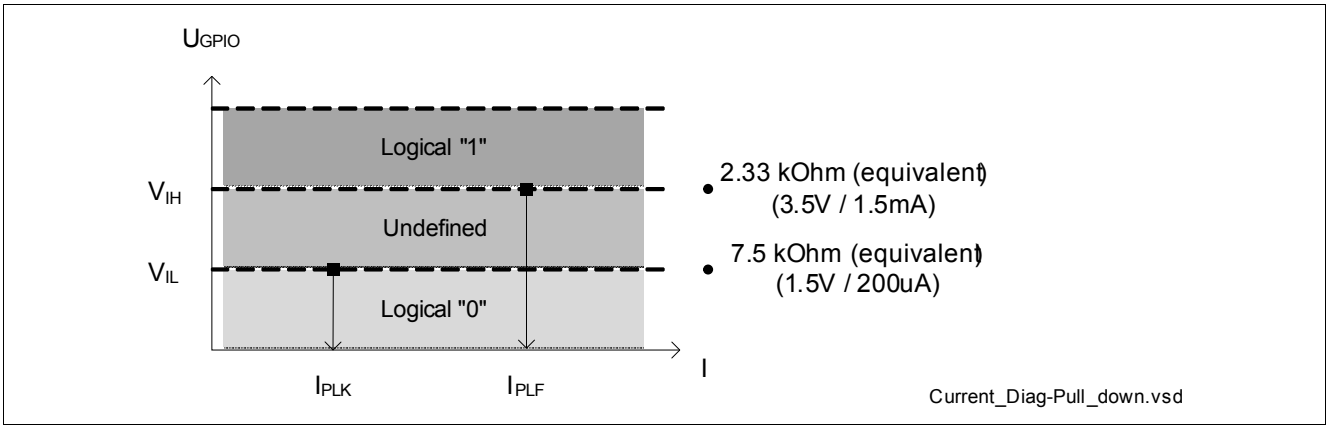

Figure 36 Pull-Down Keep and Force Current

29.5.2 DC Parameters of Port 0, Port 1, TMS and Reset

Note: Operating Conditions apply.
Keeping signal levels within the limits specified in this table ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the maximum allowed ocurrent which can be taken out of VDDP.

Table 30 Current Limits for Port Output Drivers[1)]

Port Output Driver Mode	Maximum Output Current (I_{OLmax} , - I_{OHmax})		Maximum Output Current (I_{OLnom} , - I_{OHnom})		Number
	V_{DDP} 4.5V	2.6V < V_{DDP} < 4.5V	V_{DDP} 4.5V	2.6V < V_{DDP} < 4.5V	
Strong driver[2)]	5 mA	3 mA	1.6 mA	1.0 mA	P_5.1.15
Medium driver[3)]	3 mA	1.8 mA	1.0 mA	0.8 mA	P_5.1.1
Weak driver[3)]	0.5 mA	0.3 mA	0.25 mA	0.15 mA	P_5.1.2

1) Not subject to production test, specified by design.
2) Not available for port pins P0.4, P1.0, P1.1 and P1.2
3) All P0.x and P1.x

Table 31 DC Characteristics Port0, Port1

V_S = 5.5 V to 28 V, T_j = -40 °C to +175 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input hysteresis	HYS_{P0_P1}	0.11 x V_{DDP}	–	–	V	[1)] Series resistance = 0 ; 4.5V V_{DDP} 5.5V	P_5.1.5
Input hysteresis	$HYS_{P0\_P1\_exend}$	–	0.09 x V_{DDP}	–	V	[1)] Series resistance = 0 ; 2.6V V_{DDP} 4.5V	P_5.1.16

Table 31 DC Characteristics Port0, Port1 (cont'd)

V_S = 5.5 V to 28 V, T_j = -40 °C to +175 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input low voltage	V_{IL}	-0.3	–	0.3 x V_{DDP}	V	2)4.5V V_{DDP} 5.5V	P_5.1.3
Input low voltage	V_{IL_extend}	-0.3	0.42 x V_{DDP}	–	V	1)2.6V V_{DDP} 4.5V	P_5.1.17
Input high voltage	V_{IH}	0.7 x V_{DDP}	–	V_{DDP} + 0.3	V	2)4.5V V_{DDP} 5.5V	P_5.1.4
Input high voltage	V_{IH_extend}	–	0.52 x V_{DDP}	V_{DDP} + 0.3	V	1)2.6V V_{DDP} 4.5V	P_5.1.18
Output low voltage	V_{OL}	–	–	1.0	V	3) 4) I_{OL} I_{OLmax}	P_5.1.6
Output low voltage	V_{OL}	–	–	0.4	V	3) 5) I_{OL} I_{OLnom}	P_5.1.7
Output high voltage	V_{OH}	V_{DDP} - 1.0	–	–	V	3) 4) I_{OH} I_{OHmax}	P_5.1.8
Output high voltage	V_{OH}	V_{DDP} - 0.4	–	–	V	3) 5) I_{OH} I_{OHnom}	P_5.1.9
Input leakage current	$I_{OZ\_extend1}$	-500	–	+500	nA	-40°C T_J 25°C, 0.45 V < V_{IN} < V_{DDP}	P_5.1.20
Input leakage current	I_{OZ1}	-5	–	+5	µA	6) 25°C < T_J 85°C, 0.45 V < V_{IN} < V_{DDP}	P_5.1.10
Input leakage current	$I_{OZ\_extend2}$	-15	–	+15	µA	85°C < T_J 150°C, 0.45 V < V_{IN} < V_{DDP}	P_5.1.21
Input leakage current	$I_{OZ\_extend3}$	-20	–	+20	µA	85°C < T_J 175°C, 0.45 V < V_{IN} < V_{DDP}	P_5.1.11
Pull level keep current	I_{PLK}	-200	–	+200	µA	7) V_{PIN} V_{IH} (up) V_{PIN} V_{IL} (dn)	P_5.1.12
Pull level force current	I_{PLF}	-1.5	–	+1.5	mA	7) V_{PIN} V_{IL} (up) V_{PIN} V_{IH} (dn)	P_5.1.13
Pin capacitance	C_{IO}	–	–	10	pF	1)	P_5.1.14
Reset Pin Timing							
Reset Pin Input Filter Time	t_{filt_RESET}	–	5	–	µs	1)	P_5.1.19

1) Not subject to production test, specified by design.

2) Tested at V_{DDP} = 5V, specified for 4.5V < V_{DDP} < 5.5V.

3) The maximum deliverable output current of a port driver depends on the selected output driver mode. The limit for pin groups must be respected.

4) Tested at 4.9V < V_{DDP} < 5.1V, I_{OL} = 4mA, I_{OH} = -4mA, specified for 4.5V < V_{DDP} < 5.5V.

Table 35 Supply Voltage Signal Conditioning (cont'd)

V_S = 5.5 V to 28 V, T_j = -40 °C to +175 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Accuracy of V_{VDH}-10-bit ADC -measurement without calibration, ATT_{VDH_2}	$\delta V_{VDHADC10B}$	-400	–	400	mV	V_{DH}= 5.5V to 17.5V, -40°C Tj 150°C	P_8.1.71
Accuracy of V_{VDH}-10-bit ADC -measurement without calibration, ATT_{VDH_2} - Extended temperature range	$\delta V_{VDHADC10B}$	-1.5	–	1.5	V	V_{DH}= 5.5V to 17.5V, -40°C Tj 175°C	P_8.1.78
10-Bit ADC measurement-input resistance for VDH	$R_{in\_VDH,measure}$	200	390	470	k	PD_N=1 (on-state)	P_8.1.3
Measurement input leakage current for V_{VDH}	$I_{leak\_VDH,\ measure}$	-0.05	–	2.0	µA	PD_N=0 (off-state), T_j = -40..150°C	P_8.1.10
Measurement input leakage current for V_{VDH}-Extended temperature range	$I_{leak\_VDH,\ measure\_HT}$	-0.05	–	4.0	µA	PD_N=0 (off-state), T_j = 150..175°C	P_8.1.79

1) Not subject to production test, specified by design.

2) Accuracy is valid for a calibrated device.

29.8.2 Central Temperature Sensor Parameters

Table 36 Electrical Characteristics Temperature Sensor Module

V_S = 5.5 V to 28 V, T_j = -40 °C to +175 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Output voltage V_{TEMP} at T_0=273 K (0°C)	a	–	0.666	–	V	1) T_0=273 K (0°C)	P_8.2.2
Temperature sensitivity b	b	–	2.31	–	mV/K	1)	P_8.2.4
Accuracy_1	Acc_1	-10	–	10	°C	2)1) -40°C < Tj < 85°C	P_8.2.5
Accuracy_2	Acc_2	-10	–	10	°C	2)1) 125°C < Tj < 150°C	P_8.2.6
Accuracy_3	Acc_3	-5	–	5	°C	2)1) 85°C < Tj < 125°C	P_8.2.7

1) Not subject to production test, specified by design

2) Accuracy with reference to on-chip temperature calibration measurement, valid for Mode1