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Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Automotive Mirror Control
Core Processor	HC08
Program Memory Type	FLASH (16kB)
Controller Series	908E
RAM Size	512 x 8
Interface	SCI, SPI
Number of I/O	12
Voltage - Supply	9V ~ 16V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	54-SSOP (0.295", 7.50mm Width) Exposed Pad
Supplier Device Package	54-SOIC-EP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mm908e621acdwb

PIN CONNECTIONS

Transparent Top View of Package

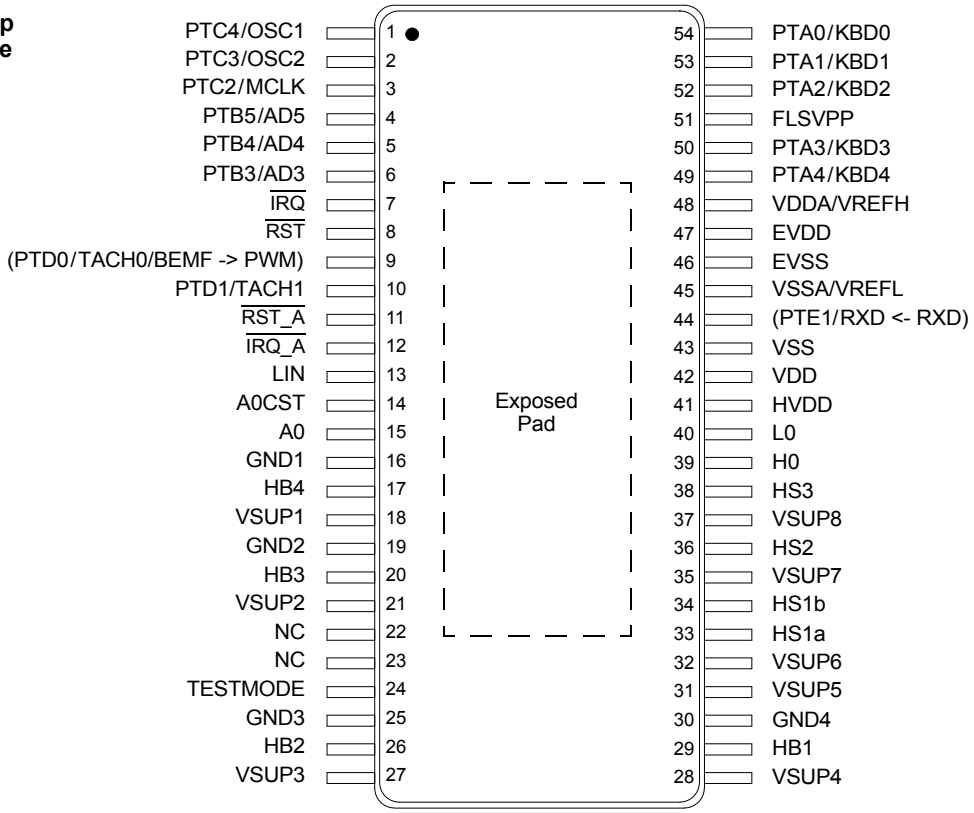


Figure 3. Pin Connections

Table 1. Pin Definitions

A functional description of each pin can be found in the Functional Pin Description section beginning on page 19.

Die	Pin	Pin Name	Formal Name	Definition
MCU	1 2 3	PTC4/OSC1 PTC3/OSC2 PTC2/MCLK	Port C I/Os	These pins are special function, bidirectional I/O port pins that are shared with other functional modules in the MCU.
MCU	4 5 6	PTB5/AD5 PTB4/AD4 PTB3/AD3	Port B I/Os	These pins are special function, bidirectional I/O port pins that are shared with other functional modules in the MCU.
MCU	7	$\overline{\text{IRQ}}$	External Interrupt Input	This pin is an asynchronous external interrupt input pin.
MCU	8	$\overline{\text{RST}}$	External Reset	This pin is bidirectional, allowing a reset of the entire system. It is driven low when any internal reset source is asserted.
MCU / Analog	9	(PTD0/TACH0/BEMF -> PWM)	PWM signal	This pin is the PWM signal test pin. It internally connects the MCU PTD0/TACH0 pin with the Analog die PWM input. Note: Do not connect in the application.
MCU	10	PTD1/TACH1	Port D I/Os	This pin is a special function, bidirectional I/O port pin that is shared with other functional modules in the MCU.
MCU / Analog	44	(PTE1/RXD <- RXD)	LIN Transceiver Output	This pin is the LIN Transceiver output test pin. It internally connects the MCU PTE1/RXD pin with the Analog die LIN transceiver output pin RXD. Note: Do not connect in the application.

Table 1. Pin Definitions (continued)

A functional description of each pin can be found in the Functional Pin Description section beginning on page 19.

Die	Pin	Pin Name	Formal Name	Definition
MCU	45 48	VSSA/VREFL VDDA/VREFH	ADC Supply and Reference Pins	These pins are the power supply and voltage reference pins for the analog-to-digital converter (ADC).
MCU	46 47	EVSS EVDD	MCU Power Supply Pins	These pins are the ground and power supply pins, respectively. The MCU operates from a single power supply.
MCU	49 50 52 53 54	PTA4/KBD4 PTA3/KBD3 PTA2/KBD2 PTA1/KBD1 PTA0/KBD0	Port A I/Os	These pins are special function, bidirectional I/O port pins that are shared with other functional modules in the MCU.
MCU	51	FLSVPP	Test Pin	For test purposes only. Do not connect in the application.
Analog	11	$\overline{\text{RST\_A}}$	Internal Reset	This pin is the bidirectional reset pin of the analog die.
Analog	12	$\overline{\text{IRQ\_A}}$	Internal Interrupt Output	This pin is the interrupt output pin of the analog die indicating errors or wake-up events.
Analog	13	LIN	LIN Bus	This pin represents the single wire bus transmitter and receiver.
Analog	14	A0CST	Analog Input Trim Pin	This is the analog input trim pin for the A0 input. This is to connect a known fixed resistor value to trim the current source measurement.
Analog	15	A0	Analog Input Pin	This pin is an analog input port with selectable source values.
Analog	16 19 25 30	GND1 GND2 GND3 GND4	Power Ground Pins	These pins are device power ground connections.
Analog	29 26 20 17	HB1 HB2 HB3 HB4	Half-bridge Outputs	This device includes power MOSFETs configured as four half-bridge driver outputs. These outputs may be configured for DC motor drivers, or as high side and low side switches. Note: The HB3 and HB4 have a lower $R_{DS(ON)}$ then HB1 and HB2.
Analog	18 21 27 28 31 32 35	VSUP1 VSUP2 VSUP3 VSUP4 VSUP5 VSUP6 VSUP7	Power Supply Pins	These pins are device power supply pins.
–	22 23	NC NC	No Connect	These pins are not connected.
Analog	24	TESTMODE	TESTMODE Input	Pin for test purpose only. In application this pin needs to be tied GND.
Analog	34 35	HS1a HS1b	High Side HS1 Output	This output pin is a low $R_{DS(ON)}$ high side switch.
Analog	36 38	HS2 HS3	High Side HS2 Output High Side HS3 Output	These output pins are low $R_{DS(ON)}$ high side switches.
Analog	39	H0	Hall-Effect Sensor / General Purpose Input	This pin provides an input for a Hall-effect sensor or general purpose input.
Analog	40	L0	Wake-up Input	This pin provides an high voltage input, which is wake-up capable.
Analog	41	HVDD	Switchable V_{DD} Output	This pin is a switchable V_{DD} output for driving resistive loads requiring a regulated 5.0 V supply; e.g. potentiometers.
Analog	42	VDD	Voltage Regulator Output	The +5. V voltage regulator output pin is intended to supply the embedded microcontroller.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground, unless otherwise noted. Exceeding limits on any pin may cause permanent damage to the device.

Rating	Symbol	Value	Unit
ELECTRICAL RATINGS			
Supply Voltage Analog Chip Supply Voltage under Normal Operation (Steady-state) Analog Chip Supply Voltage under Transient Conditions(1) MCU Chip Supply Voltage	 $V_{SUP(SS)}$ $V_{SUP(PK)}$ V_{DD}	 -0.3 to 28 -0.3 to 40 -0.3 to 5.5	V
Input Pin Voltage Analog Chip Microcontroller Chip	 $V_{IN(ANALOG)}$ $V_{IN(MCU)}$	 -0.3 to 5.5 V_{SS}-0.3 to V_{DD}+0.3	V
Maximum Microcontroller Current per Pin All Pins except VDD, VSS, PTA0:PTA4 PTA0:PTA4	 $I_{PIN(1)}$ $I_{PIN(2)}$	 ±15 ±25	mA
Maximum Microcontroller VSS Output Current	I_{MVSS}	100	mA
Maximum Microcontroller VDD Input Current	I_{MVDD}	100	mA
LIN Supply Voltage Normal Operation (Steady-state) Transient Input Voltage (per ISO7637 Specification) and with External Components (Figure 4, page 16)	 $V_{BUS(SS)}$ $V_{BUS(PK)}$	 -18 to 40 -150 to 100	V
ESD Voltage(2) Human Body Model H0 pin Human Body Model all other pins Machine Model Charge Device Model	 V_{ESD1-1} V_{ESD1-2} V_{ESD2} V_{ESD3}	 ±1000 ±2000 ±200 ±750	V

Notes
1. Transient capability for pulses with a time of t < 0.5 sec.
2. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), the Machine Model (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω) and the Charge Device Model, Robotic (C_{ZAP} = 4.0 pF).

Table 3. Static Electrical Characteristics (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 datasheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40 °C ≤ T_J ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
HALF-BRIDGE OUTPUTS HB3 AND HB4					
Switch On Resistance	$R_{DS(ON)-HB34}$				mΩ
High Side, T_J = 25 °C, I_{LOAD} = 1.0 A		–	275	325	
Low Side, T_J = 25 °C, I_{LOAD} = 1.0 A		–	275	325	
Over-current Shutdown	I_{HBOC34}				A
High Side		4.8	–	7.2	
Low Side		4.8	–	7.2	
Over-current Shutdown blanking time(21)	t_{OCB}	–	4-8	–	µs
Switching Frequency(21)	f_{PWM}	–	–	25	kHz
Freewheeling Diode Forward Voltage					V
High Side, T_J = 25 °C, I_{LOAD} = 1.0 A	V_{HSF}	–	0.9	–	
Low Side, T_J = 25 °C, I_{LOAD} = 1.0 A	V_{LSF}	–	0.9	–	
Leakage Current	I_{LEAKHB}	–	<0.2	10	µA
Low Side Current to Voltage Ratio(22)	$CR_{RATIOHB34}$				V/A
V_{ADOUT} [V] / I_{HB} [A], CSA = 1, (measured and trimmed I_{HB} = 500 mA)		3.5	5.0	6.5	
V_{ADOUT} [V] / I_{HB} [A], CSA = 0, (measured and trimmed I_{HB} = 2.0 A)		0.7	1.0	1.3	
SWITCHABLE V_{DD} OUTPUT HVDD					
Over-current Shutdown	I_{HVDDOC}	25	35	50	mA
Over-current Shutdown Blanking Time(23)	$t_{HVDDOCB}$				µs
HVDDT1:0 = 00		–	950	–	
HVDDT1:0 = 01		–	536	–	
HVDDT1:0 = 10		–	234	–	
HVDDT1:0 = 11		–	78	–	
Over-current Flag Delay(23)	$t_{HVDDOCFD}$	–	0.5	–	ms
Dropout Voltage @ I_{LOAD} = 20 mA	$V_{HVDDDROP}$	–	110	300	mV
V_{SUP} DOWN SCALER(24)					
Voltage Ratio (RATIO $_{VSUP}$ = V_{SUP} / V_{ADOUT})	$RATIO_{VSUP}$	4.75	5.0	5.25	–
INTERNAL DIE TEMPERATURE SENSOR(24)					
Voltage / Temperature Slope(23)	S_{TTOV}	–	26	–	mV/°C
Output Voltage @25°C	V_{T25}	1.7	1.9	2.1	V

Notes
21. This parameter is guaranteed by process monitoring but is not production tested.
22. This parameter is guaranteed only if correct trimming was applied
23. This parameter is guaranteed by process monitoring but is not production tested.
24. This parameter is guaranteed only if correct trimming was applied

Table 3. Static Electrical Characteristics (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 datasheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40 °C ≤ T_J ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
HALL-EFFECT SENSOR INPUT H0 - GENERAL PURPOSE INPUT MODE (H0MS = 0)					
Input Voltage Low Threshold	V_{LT}	–	–	1.5	V
Input Voltage High Threshold	V_{HT}	3.5	–	–	V
Input Voltage Hysteresis	V_{HH}	100	–	500	mV
Pull-up resistor	R_{PH}	7.0	10	13	kΩ
HALL-EFFECT SENSOR INPUT H0 - 2PIN HALL SENSOR INPUT MODE (H0MS = 1)					
Output Voltage V_{SUP} < 17 V V_{SUP} >17 V	 V_{HALL1} V_{HALL2}	 – –	 V_{SUP}-1.2 –	 – 15.8	V
Output Drop @ I_{OUT} = 15 mA	V_{H0D}	–	–	2.5	V
Sense Current Threshold	I_{HSCT}	6.0	7.9	10	mA
Sense Current Hysteresis	I_{HSCH}	650	–	1650	µA
Sense Current Limitation	V_{HSCLIM}	20	40	70	mA
ANALOG INPUT A0, A0CST					
Current Source A0, A0CST[25], [26] CSSEL1:0 = 00 CSSEL1:0 = 01 CSSEL1:0 = 10 CSSEL1:0 = 11	 I_{CS1} I_{CS2} I_{CS3} I_{CS4}	 – – – –	 40 120 320 800	 – – – –	µA
WAKE-UP INPUT L0					
Input Voltage Threshold Low	V_{LT}	–	–	1.5	V
Input Voltage Threshold High	V_{HT}	3.5	–	–	V
Input Voltage Hysteresis	V_{LH}	0.5	–	–	V
Input Current	I_N	-10	–	10	µA
Wake-up Filter Time[27]	t_{WUP}	–	20	–	µs

Notes
25. This parameter is guaranteed only if correct trimming was applied
26. The current values are optimized to read a NTC temperature sensor, e.g. EPCOS type B57861 (R25 = 3000Ω, R/T characteristic 8016)
27. This parameter is guaranteed by process monitoring but is not production tested.

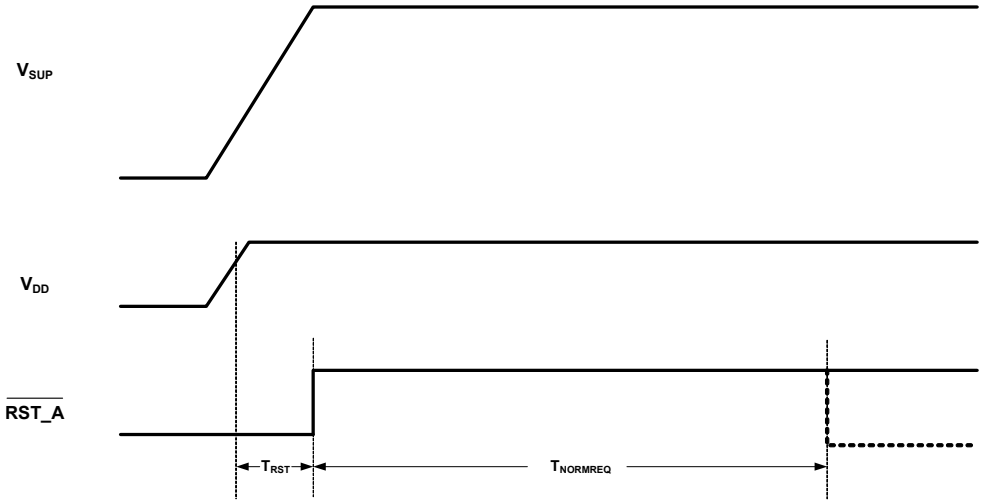


Figure 10. Power On Reset and Normal Request Timeout Timing

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 908E621 was designed and developed as a highly integrated and cost-effective solution for automotive and industrial applications. For automotive body electronics, the 908E621 is well suited to perform complete mirror control via a three wire LIN bus.

This device combines an HC908EY16 MCU core with flash memory together with a *SMARTMOS* IC chip. The *SMARTMOS* IC chip combines power and control in one chip. Power switches are provided on the *SMARTMOS* IC configured as half-bridge outputs and three high side switches. Other ports are also provided, which include one Hall-effect sensor input port, one analog input port with a switched current source, one wake-up pin, and a selectable HVDD pin. An internal voltage regulator provides power to the MCU chip.

Also included in this device is a LIN physical layer, which communicates using a single wire. This enables this device to be compatible with three wire bus systems, where one wire is used for communication, one for battery, and one for ground.

FUNCTIONAL PIN DESCRIPTION

See Figure 2, 908E621 Simplified Internal Block Diagram, page 2, for a graphic representation of the various pins referred to in the following paragraphs. Also, see the pin diagram on page 3 for a depiction of the pin locations on the package.

PORT A I/O PINS

These pins are special function, bidirectional I/O port pins that are shared with other functional modules in the MCU. PTA0:PTA4 are shared with the keyboard interrupt pins, KBD0:KBD4.

The PTA5/SPSCK pin is not accessible in this device and is internally connected to the SPI clock pin of the analog die.

The PTA6/$\overline{SS}$ pin is not accessible in this device and is internally connected to the SPI slave select input of the analog die.

For details refer to the 68HC908EY16 datasheet.

PORT B I/O PINS

These pins are special function, bidirectional I/O port pins that are shared with other functional modules in the MCU. All pins are shared with the ADC module.

PTB0/AD0 is internally connected to the ADOUT pin of the analog die, allowing diagnostic measurements to be calculated (e.g., current recopy, V_{SUP}, etc.).

The PTB1/AD1, PTB2/AD2, PTB6/AD6/TBCH0, PTB7/AD7/TBCH1 pins are not accessible in this device.

For details refer to the 68HC908EY16 datasheet.

PORT C I/O PINS

These pins are special function, bidirectional I/O port pins that are shared with other functional modules in the MCU. For example, PTC2:PTC4 are shared with the ICG module.

PTC0/MISO and PTC1/MOSI are not accessible in this device and are internally connected to the MISO and MOSI SPI pins of the analog die.

For details refer to the 68HC908EY16 datasheet.

PORT D I/O PINS

PTD0/TACH0/BEMF and PTD1/TACH1 are special function, bi-directional I/O port pins that can also be programmed to be timer pins.

PTD0/TACH0 pin is internally connected to the PWM input of the analog die and only accessible for test purposes (can not be used in the application).

For details refer to the 68HC908EY16 datasheet.

PORT E I/O PIN

PTE0/TXD and PTE1/RXD are special function, bidirectional I/O port pins that can also be programmed to be enhanced serial communication.

PTE0/TXD is internally connected to the TXD pin of the analog die. The connection for the receiver must be done externally.

PTE1/RXD is internally connected to the RXD pin of the analog die and only accessible for test purposes (can not be used in the application).

For details refer to the 68HC908EY16 datasheet.

EXTERNAL INTERRUPT PIN ($\overline{IRQ}$)

The $\overline{IRQ}$ pin is an asynchronous external interrupt pin. This pin contains an internal pull-up resistor that is always activated, even when the $\overline{IRQ}$ pin is pulled LOW.

For details refer to the 68HC908EY16 datasheet.

EXTERNAL RESET PIN ($\overline{\text{RST}}$)

A logic [0] on the $\overline{\text{RST}}$ pin forces the MCU to a known startup state. $\overline{\text{RST}}$ is bidirectional, allowing a reset of the entire system. It is driven LOW when any internal reset source is asserted.

This pin contains an internal pull-up resistor that is always activated, even when the reset pin is pulled LOW.

For details refer to the 68HC908EY16 datasheet.

POWER SUPPLY PINS (VSUP1:VSUP8)

VSUP1:VSUP8 are device power supply pins. The nominal input voltage is designed for operation from 12 V systems. Owing to the low ON-resistance and current requirements of the half-bridge driver outputs and high side output drivers, multiple VSUP pins are provided.

All VSUP pins must be connected to get full chip functionality.

POWER GROUND PINS (GND1:GND4)

GND1:GND4 are device power ground connections. Owing to the low ON-resistance and current requirements of the half-bridge driver outputs and high side output drivers, multiple pins are provided.

GND1 and GND2 pins must be connected to get full chip functionality.

HALF-BRIDGE OUTPUT PINS (HB1:HB4)

The 908E621 device includes power MOSFETs configured as four half-bridge driver outputs. The HB3:HB4 have a lower $R_{DS(ON)}$, to run higher currents (e.g. fold motor), than the HB1:B2 outputs.

The HB1:HB4 outputs are short-circuit and over-temperature protected, and they feature current recopy. Over-current protection is done on both high side and low side FET's. The current recopy are done on the low side MOSFETs.

HIGH SIDE OUTPUT PINS (HS1:HS3)

The HS output pins are a low $R_{DS(ON)}$ high side switches. Each HS switch is protected against over-temperature and over-current. The output is capable of limiting the inrush current with an automatic PWM or feature a real PWM capability using the PWM input.

The HS1 has a lower $R_{DS(ON)}$, to run higher currents (e.g. heater), than the HS2 and HS3 outputs.

For the HS1 two pins (HS1a:HS1b) are necessary for the current capability and have to be connected externally.

Important: The HS3 can be only used to drive resistive loads.

HALL-EFFECT SENSOR INPUT PIN (H0)

The Hall-effect sensor input pin H0 provides an input for Hall-effect sensors (2-pin or 3-pin) or a switch.

ANALOG INPUT PINS (A0, A0CST)

These pins are analog inputs with selectable current source values. The A0CST intent is to trim the A0 input.

WAKE-UP INPUT PIN (L0)

This pin is 40 V rated input. It can be used as wake-up source for a system wake-up. The input is falling or rising edge sensitive.

Important: If unused this pin should be connected to VSUP or GND to avoid parasitic transitions. In Low Power mode this could lead to random wake-up events.

SWITCHABLE V_{DD} OUTPUT PIN (HVDD)

The HVDD pin is a switchable V_{DD} output for driving resistive loads requiring a regulated 5.0 V supply (e.g., 3 pin Hall-effect sensors or potentiometers). The output is short-circuit protected.

LIN BUS PIN (LIN)

The LIN pin represents the single wire bus transmitter and receiver. It is suited for automotive bus systems and is based on the LIN bus specification.

+5.0 V VOLTAGE REGULATOR OUTPUT PIN (VDD)

The VDD pin is needed to place an external capacitor to stabilize the regulated output voltage. The VDD pin is intended to supply the embedded microcontroller.

Important: The VDD pin should not be used to supply other loads; use the HVDD pin for this purpose. The VDD, EVDD and VDDA/VREFH pins must be connected together.

VOLTAGE REGULATOR GROUND PIN (VSS)

The VSS pin is the ground pin for the connection of all non-power ground connections (microcontroller and sensors). **Important**: VSS, EVSS and VSSA/VREFL pins must be connected together.

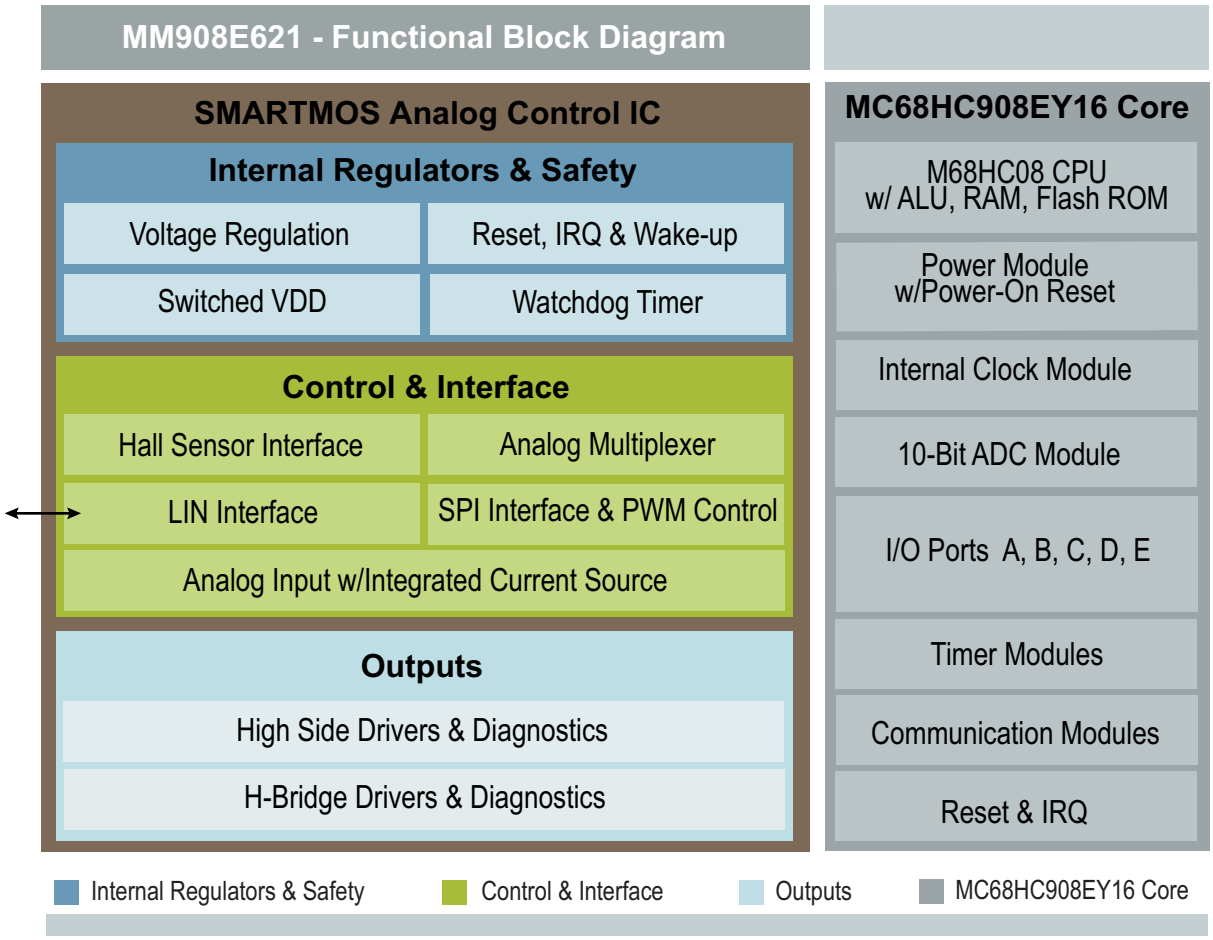
RESET PIN ($\overline{\text{RST\_A}}$)

$\overline{\text{RST\_A}}$ is the bidirectional reset pin of the analog die. It is an open drain with pullup resistor and must be connected to the $\overline{\text{RST}}$ pin of the MCU.

INTERRUPT PIN ($\overline{\text{IRQ\_A}}$)

$\overline{\text{IRQ\_A}}$ is the interrupt output pin of the analog die indicating errors or wake-up events. It is an open drain with pullup resistor and must be connected to the $\overline{\text{IRQ}}$ pin of the MCU.

FUNCTIONAL INTERNAL BLOCK DESCRIPTION



SMARTMOS ANALOG CONTROL IC

INTERNAL REGULATORS & SAFETY:

VOLTAGE REGULATION

The voltage regulator circuitry provides the regulated voltage for the Analog IC as well as the VDD/VSS rails for the core IC. The on-chip regulator consists of two elements, the main regulator, and the low voltage reset circuit. The V_{DD} regulator accepts an unregulated input supply, and provides a regulated V_{DD} supply to all digital sections of the device. The output of the regulator is also connected to the VDD pin, to provide the 5.0 V to the microcontroller.

SWITCHED VDD

This function provides a switchable +5.0 V V_{DD} rail for an external load.

WATCHDOG TIMER

The watchdog timer module generates a reset, in case of a watchdog timeout or wrong watchdog timer reset. A watchdog reset event will reset all registers in the SPI, excluding the RSR.

RESET, IRQ & WAKE-UP

There are several functions on the Analog IC that can generate a reset or wake-up signal to the core IC. There is a pin that is used to detect an external wake-up event. The Reset signal has many possible sources in the Analog IC circuitry. The IRQ function on the Analog IC, will notify the core IC of pending system critical conditions.

CONTROL & INTERFACE:

HALL SENSOR INTERFACE

This interface can be configured to support an input pin as a general purpose input, or as a hall-effect sensor input, to be able to read 3-pin / 2-pin hall sensors or switches.

microcontroller could not control it during system power-up or power-down.

RXD Pin

The RXD transceiver pin is the MCU interface, which reports the state of the LIN bus voltage. LIN HIGH (recessive state) is reported by a high level on RXD, LIN LOW (dominant state) by a low level on RXD.

STOP Mode and Wake-up Feature

During STOP mode operation the transmitter of the physical layer is disabled and the internal pull-up resistor is disconnected from VSUP and a small current source keeps the LIN pin in recessive state. The receiver is still active and able to detect wake-up events on the LIN bus line.

If the LIN interrupt is enabled (LINIE bit in the Interrupt Mask register is set), a dominant level longer than T_{PROPWL} followed by an rising edge will set the LINIF flag and generate an interrupt which causes a system wake-up (see Figure 8, page 17)

SLEEP Mode and Wake-up Feature

During SLEEP mode operation the transmitter of the physical layer is disabled, the internal pull-up resistor is disconnected from VSUP, and a small current source keeps the LIN pin in the recessive state. The receiver is still active to be able to detect wake-up events on the LIN bus line.

A dominant level longer than T_{PROPWL} followed by an rising edge will generate a system wake-up (reset) and set the LINWF flag in the Reset Status register (RSR). Also see Figure 9, page 17).

A0 INPUT AND ANALOG MULTIPLEXER

A0 - Analog Input

Input A0 is an analog input used for reading switches, or as analog inputs for potentiometers, NTC, etc.

A0 is internally connected to the analog multiplexer. This pin offers a switchable current source. To read the Analog Input, the pin has to be selected with the SS[3:0] bits in the A0MUCTL register.

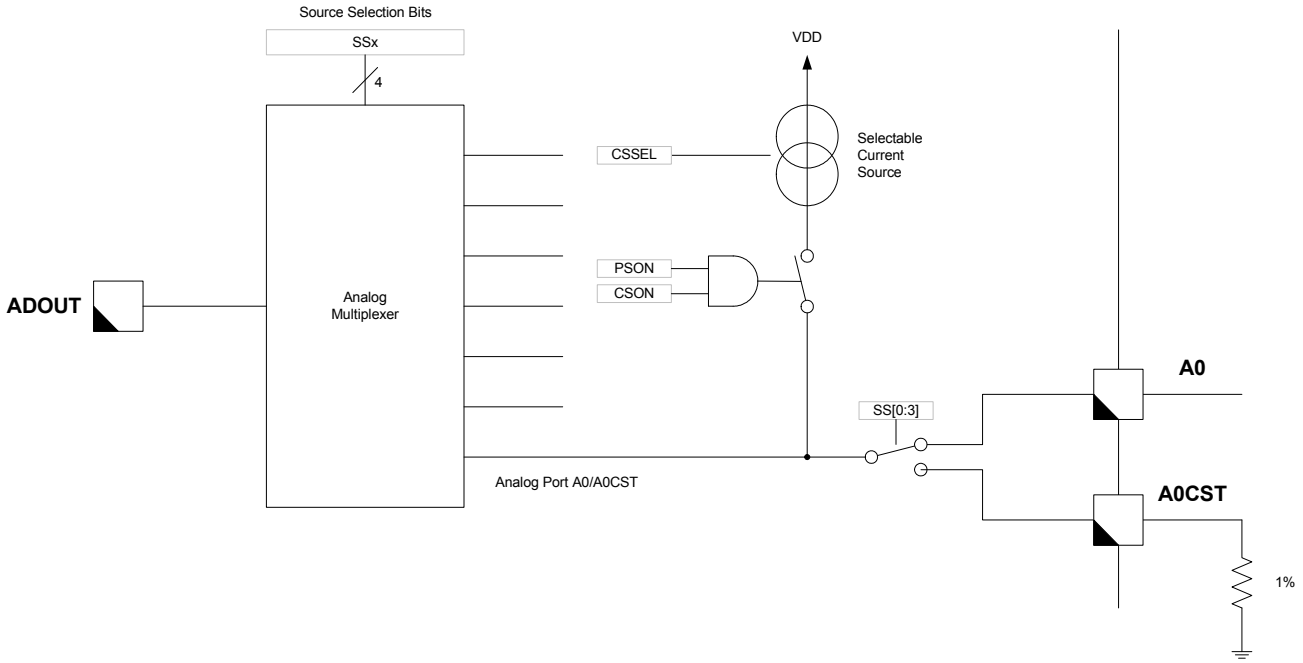


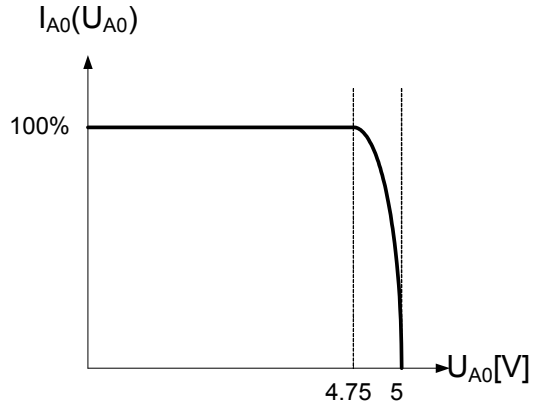
Figure 17. Analog Input and Multiplexer

A0 Current Source

The pin A0 provides a switchable current source, to be able to read in switches, NTC, etc., without the need of an additional supply line for the sensor. The overall enable of this feature is done by setting the PSON bit in the System Control register. In addition, the pin has to be selected with the SS[3:0] bits. The current source can be enabled with the CSON Bit and adjusted with the bits CSSEL[1:0].

With the CSSEL[1:0] bit's, four different current values can be selected (40, 120, 320, and 800 µA). This function is halted during STOP and SLEEP mode operations.

The current source is derived from the V_{DD} voltage, and is constant up to an output voltage of ~4.75 V.



To calibrate the current sources, an extra pin (A0CST) is envisioned. On this pin, an accurate resistor can to be connected. Switching the current sources to this resistor, allows the user to measure the current and use the measured value for calculating the current on A0.

Analog Multiplexer / ADOUT pin

The ADOUT pin is the analog output interface to the Analog-to-digital converter of the MCU. To be able to have different sources for the MCU with one single signal, an analog multiplexer is integrated in the analog die. This multiplexer has eleven different sources, which can be selected with the SS[3:0] bits in the A0MUCTL register.

Half-bridge (HB1:HB4) Current Recopy

The multiplexer is connected to the four current sense circuits on the low side FET of the half bridges. This sense circuits offers a voltage proportional to the current through the MOSFET. The resolution is depending on the CSA bit in the A0 and Multiplexer control register (A0MUCTL).

High Side (HS1:HS3) Current Recopy

The multiplexer is connected to the three high side switches. This sense circuit offers a voltage proportional to the current through the transistor.

Analog Input A0 and A0CST

A0 and A0CST are directly connected to the analog multiplexer. It offers the possibility to read analog values from the periphery.

Temperature Sensor

The analog die includes an on chip temperature sensor. This sensor offers a voltage which is proportional to the actual mean chip junction temperature.

VSUP Prescaler

The VSUP prescaler offers a possibility to measure the external supply voltage. The output of this voltage is VSUP / RATIOVSUP.

A0 and Multiplexer Control Register (A0MUCTL)

Register Name and Address: A0MUCTL - $08

	Bit7	6	5	4	3	2	1	Bit0
Read Write	CSON	CSSEL 1	CSSEL 0	CSA	SS3	SS2	SS1	SS0
Reset	0	0	0	0	0	0	0	0

CSON — Current Source on/off

This read/write bit enables the current source for the A0 or A0CST inputs. Reset clears CSON bit.

1 = Current Source enabled
0 = Current Source disabled

CSSEL[1:0] — Current Source Select Bits

These read/write bits select the current source values for A0 or A0CST input. Reset clears CSSEL[1:0] bits.

Table 7. A0 Current Source Level Selection Bits

CSSEL1	CSSEL0	Current Source Enable (typ.)
0	0	40 µA
0	1	120 µA
1	0	320 µA
1	1	800 µA

CSA — H-bridges Current Sense Amplification Select Bit

This read/write bit selects the current sense amplification of the H-Bridges HB1:HB4 current recopy. Reset clears the CSA bit.

1 = low current sense amplification
0 = high current sense amplification

SS[3:0] — Analog Source Input Select Bits

These read/write bits selects the analog input source for the ADOUT pin. Reset clears the SS[3:0] bits Analog Multiplexer Configuration Bits.

SS3	SS2	SS1	SS0	Channel
0	0	0	0	current recopy HB1
0	0	0	1	current recopy HB2
0	0	1	0	current recopy HB3
0	0	1	1	current recopy HB4
0	1	0	0	current recopy HS1
0	1	0	1	current recopy HS2
0	1	1	0	current recopy HS3
0	1	1	1	not used

HALF-BRIDGE OUTPUT REGISTER (HBOUT)

Register Name and Address: HBOUT - $01

	Bit7	6	5	4	3	2	1	Bit0
Read Write	HB4_H	HB4_L	HB3_H	HB3_L	HB2_H	HB2_L	HB1_H	HB1_L
Reset	0	0	0	0	0	0	0	0

HBx_H, HBx_L — Half-bridge Output Switches

These read/write bits select the output of each half-bridge output according to Table . Reset clears all HBx_H, HBx_L bits.

Table 8. Half-bridge Configuration

HBx_H	HBx_L	Mode
0	0	Low side and high side MOSFET off
0	1	High side MOSFET off, low side MOSFET on
1	0	High side MOSFET on, low side MOSFET off
1	1	High side MOSFET in PWM mode

Half-bridge PWM mode

The PWM mode is selected by setting both HBxL and HBxH of one half-bridge to “1”. In this mode, the high side MOSFET is controlled by the incoming PWM signal on the PWM pin (see Figure 2, page 2).

If the incoming signal is high, the high side MOSFET is switched on.

If the incoming signal is low, the high side MOSFET is switched off.

With the current recirculation mode control bit CRM in the Half-bridge Status and Control Register (HBSCTL), the recirculation behavior in PWM mode can be controlled. If CRM is set, the corresponding low side MOSFET is switched on, if the PWM controlled high side MOSFET is off.

Half-bridge Current Recopy

Each low side MOSFET has an additional sense output to allow a current recopy feature. These sense sources are internally amplified and switched to the Analog Multiplexer.

The factor for the Current Sense amplification can be selected via the CSA bit in the A0MUCTL register (see page 31)

CSA = “1”: low resolution selected

CSA = “0”: high resolution selected

Half-bridge Over-temperature Protection

The outputs are protected against over-temperature conditions. Each power output comprises two different temperature thresholds.

The first threshold is the high temperature interrupt (HTI). If the temperature reaches this threshold, the HTIF bit in the Interrupt Flag Register (IFR) is set, and an interrupt will be initiated if the HTIE bit in the Interrupt Mask register is set. In addition, this interrupt can be used to automatically turn off the power stages. This shutdown can be enabled/disabled by the HTIS0-1 Bits in the System Control Register (SYSCTL).

The high temperature interrupts flag (HTIF) is cleared (and the outputs reenabled) by writing a “1” to the HTIF flag in the Interrupt Flag Register (IFR) or by a reset. Clearing this flag has no effect as long as a high temperature condition is present.

If the HTI shutdown is disabled, a second threshold high temperature reset (HTR) will be used to turn off all power stages (HB (all Fet’s), HS, HVDD, H0) in order to protect the device.

Half-Bridge Over-current Protection

The Half-bridges are protected against short to GND, VSUP, and load shorts. The over-current protection is implemented on each HB. If an over-current condition on the high side MOSFET occurs, the high side MOSFET is automatically switched off. An over-current condition on the low side MOSFET will automatically turn off the low side MOSFET. In both cases, the corresponding HBxOCF flag in the Half-bridge Status and Control Register (HBSCTL) is set.

The over-current status flag is cleared (and the corresponding half-bridge MOSFETs reenabled) by writing a “1” to the HBxOCF in the Half-bridge Status and Control Register (HBSCTL) or by a reset.

Half-bridge Over-voltage/Under-voltage Protection

The half-bridge outputs are protected against under-voltage and over-voltage conditions. This protection is done by the low and high voltage interrupt circuitry. If one of these flags (LVIF, HVIF) are set, the outputs are automatically disabled when the VIS bit in the System Control Register (SYSCTL) is cleared.

The over-voltage and under-voltage status flags are cleared (and the outputs reenabled) by writing a “1” to the LVIF / HVIF flags in the Interrupt Flag Register (IFR), or by a reset. Clearing this flag has no effect as long as the high voltage or low voltage condition is still present.

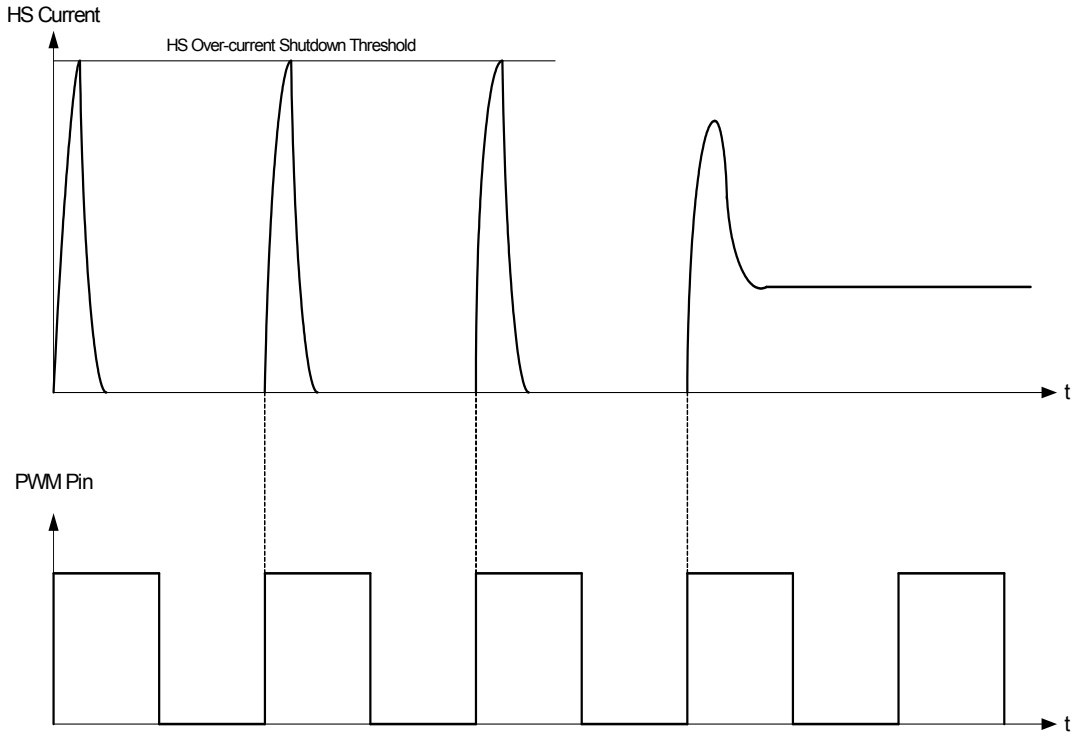


Figure 24. Inrush Current Limitation on HS Outputs

High Side Current Recopy

Each High Side has an additional sense output to allow a current recopy feature. This sense source is internally connected to a shunt resistor. The drop voltage is amplified and switched to the Analog Multiplexer.

Switchable HVDD Outputs

The HVDD pin is a switchable 5.0 V output pin. It can be used for driving external circuitry, which requires a 5.0 V voltage. The output is enabled with the PSON bit in the System Control register, and can be switched on / off with the HVDD_ON bit in the High Side Out register. Low or high voltage conditions (LVIF / HVIF) will have no influence on this circuitry.

HVDD Over-temperature Protection

The output is protected against over-temperature conditions.

HVDD Over-current Protection

The HVDD output is protected against over-current. In case the current reaches the over-current limit, the output current will be limited, and the HVDDOCF over-current flag in the System Status register is set.

HIGH SIDE OUT REGISTER (HSOUT)

Register Name and Address: HSOUT - $02

	Bit7	6	5	4	3	2	1	Bit0
Read	HVDD ON	0	HS3P WM	HS2P WM	HS1P WM	HS3O N	HS2O N	HS1O N
Write								
Reset	0	0	0	0	0	0	0	0

HVDD-ON — HVDD On Bit

This read/write bit enables the HVDD output. Reset clears HVDDON bit.

1 = HVDD enabled
0 = HVDD disabled

HSxON — High Side on/off Bits

These read/write bits turn on the High Side Fet's permanently. Reset clears the HSxON bits.

1 = High Side x is turned on
0 = High Side x is turned off

If the watchdog is enabled, it will generate a system reset, if the timer has reached its end value, or if a watchdog reset (WDRST) has occurred in the closed window.

The watchdog period can be selected with 2 bits in the WDCTL, in order to get 10ms, 20ms, 40ms and 80ms period.

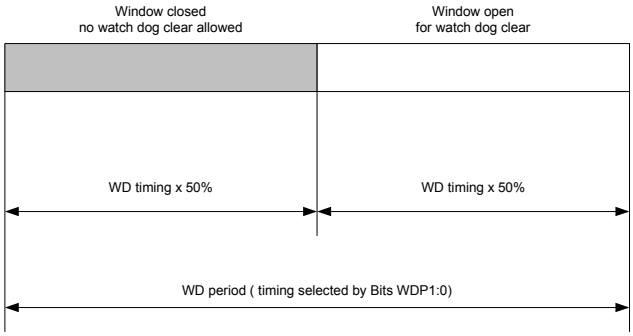


Figure 28. Window Watchdog Period

Stop mode

Operations of the watchdog function is halted in stop mode (counter/oscillator stopped). After wake-up, the watchdog timer is automatically cleared, in order to give the MCU the full time to reset the watchdog.

Sleep mode

Operations of the watchdog function is halted in sleep mode. Because the main voltage regulator asserts an LVR reset, the Watchdog functionality is disabled, and the WDRE bit is cleared as soon as sleep mode is entered. To re-enable this function bit WDRE has to be set after wake-up.

Watchdog Control Register (WDCTL)

Register Name and Address: WDCTL - $0B

	Bit7	6	5	4	3	2	1	Bit0
Read	WDRE	WDP1	WDP0	0	0	0	0	0
Write								WDRST
Reset	0	0	0	0	0	0	0	0

WDRE - Watchdog Reset Enable Bit

This read/write (write once) bit activates the watchdog. The WDRE can only be set and can not be cleared by software. Reset clears the WDRE bit.

1 = Watchdog enabled
0 = Watchdog disabled

WDP1:0 - Watchdog Period Select Bits

This read/write bit select the clock rate of the Watchdog. Reset clears the WDP1:0 bits.

Table 11. Watchdog Period Selection Bits

WDP1	WDP0	Mode
0	0	80 ms window watchdog period
0	1	40 ms window watchdog period
1	0	20 ms window watchdog period
1	1	10 ms window watchdog period

WDRST - Watchdog Reset Bit

This write only bit resets the Watchdog. Write a logic [1] to reset the watchdog timer.

1 = Reset WD and restart timer
0 = no effect

Voltage Regulator

The 908E621 contains a low power, low drop voltage regulator, to provide internal power and external power for the MCU. The on-chip regulator consist of two elements, the main regulator and the low voltage reset circuit.

The V_{DD} regulator accepts an unregulated input supply and provides a regulated V_{DD} supply to all digital sections of the device. The output of the regulator is also connected to the VDD pin to provide the 5.0 V to the microcontroller.

Run mode

During RUN mode the main voltage regulator is on. It will provide a regulated supply to all digital sections.

STOP mode

During STOP mode, the Stop mode regulator will take care of suppling a regulated output voltage. The Stop mode regulator has a limited output current capability.

SLEEP mode

In Sleep mode, the main voltage regulator external, V_{DD}, is turned off and the LVR circuitry will force the $\overline{RST\_A}$ pin low.

LOGIC COMMANDS AND REGISTERS

908E621 SERIAL PHERIPHERAL INTERFACE (SPI)

The Serial Peripheral Interface (SPI) creates the communication link between the MCU and the analog die.

The interface consists of four pins

- MOSI - Master Out Slave In (internal pulldown)
- MISO - Master In Slave Out
- $\underline{SPSCK}$ - Serial Clock (internal pulldown)
- $\overline{SS}$ - Slave Select (internal pullup)

A complete data transfer via the SPI, consists of 2 bytes. The master sends address and data, the slave returns system status and the data of the selected address.

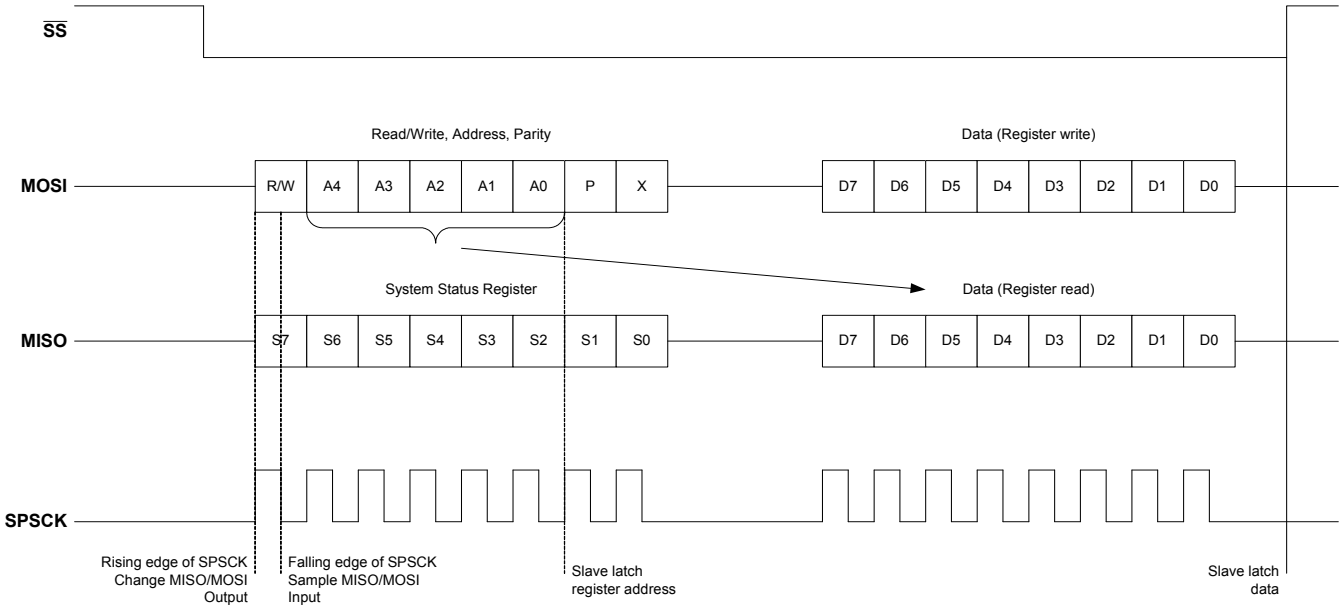


Figure 29. SPI Protocol

- During the inactive phase of $\overline{SS}$, the new data transfer will be prepared. The falling edge on the $\overline{SS}$ line, indicates the start of a new data transfer (framing), and puts MISO in the low impedance mode. The first valid data are moved to MISO with the rising edge of SPSCK.
- The MOSI, MISO will change data on a rising edge of SPSCK.
- The MOSI, MISO will be sampled on a falling edge of SPSCK.
- The data transfer is only valid, if exactly 16 sample clock edges are present in the active phase of $\overline{SS}$.
- After a write operation, the transmitted data will be latched into the register by the rising edge of $\overline{SS}$.
- Register read data is internally latched into the SPI at the time when the parity bit is transferred
- $\overline{SS}$ high will force MISO to high-impedance

Master Address Byte

A4 - A0

Includes the address of the desired register.

R/$\overline{W}$

Includes the information, if it is a read or a write operation.

- If R/$\overline{W}$ = 1 (read operation), the second byte of master contains no valid information, and the slave just transmits back register data.
- If R/$\overline{W}$ = 0 (write operation), the master sends data to be written in the second byte, the slave sends concurrently contents of selected register prior to write operation, and the write data is latched in the *SMARTMOS* registers on rising edge of $\overline{SS}$.

Parity P

Completes the total number of 1 bits of (R/W,A[4-0]) to an even number. e.g. (R/W,A[4-0]) = 100001 -> P0 = 0.

The parity bit is only evaluated during a write operations and ignored for read operations.

Bit X

Not used

Master Data Byte

This byte includes data to be written, or no valid data, during a read operation.

Slave Status Byte

This byte always includes the contents of the system status register ($0C), independent if it is a write or read operation, or which register was selected.

Slave Data Byte

This byte includes the contents of selected register, during a write operation, it includes the register content prior to the write operation.

SPI REGISTER OVERVIEW

Table 12 summarizes the SPI Register addresses and the bit names of each register.

Analog Die System Trim Values

For improved application performance, and to ensure the outlined datasheet values, the analog die needs to be trimmed. For this purpose, 3 trim values are stored in the Flash memory at addresses $FDC4 - $FDC6. These values have to be copied into the analog die SPI registers:

- copy $FDC4 into SYSTRIM1 register $0F
- copy $FDC5 into SYSTRIM2 register $10
- copy $FDC6 into SYSTRIM3 register $11

Note: These values must be copied to the respective SPI register after a reset, to ensure proper trimming of the device.

System Test Register (SYSTEST)

Register Name and Address: SYSTEST - $0E

	Bit7	6	5	4	3	2	1	Bit0
Read Write	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
Reset	0	0	0	0	0	0	0	0

Note: do not write to the reserved bits

The System Test Register is reserved for production testing and is not allowed to be written to.

System Trim Register 1 (SYSTRIM1)

Register Name and Address: IBIAS - $0F

	Bit7	6	5	4	3	2	1	Bit0
Read Write	HVDDT1	HVDDT0	0 reserved	0 reserved	ITRIM3	ITRIM2	ITRIM1	ITRIM0
Reset	0	0	0	0	0	0	0	0

Note: do not change (set) the reserved bits

HVDDT1:0 - HVDD Over-current Shutdown Delay Bits

These read/write bits allow changes to the filter time (for capacitive load) for HVDD over-current detection. Reset clears the HVDDT1:0 bits and sets the delay to the maximum value.

Table 14. HVDD Over-current Shutdown Selection Bits

HVDDT1	HVDDT0	Typical Delay
0	0	950 µs
0	1	536 µs
1	0	234 µs
1	1	78 µs

ITRIM3:0 - IRef Trim Bits

These write only bits are for trimming the internal current references IRef (also A0, A0CST). The provided trim values have to be copied into these bits after every reset. Reset clears the ITRIM3:0 bits.

Table 15. IRef Trim Bits

itrim3	itrim2	itrim2	itrim0	Adjustment
0	0	0	0	0
0	0	0	1	2%
0	0	1	0	4%
0	0	1	1	8%
0	1	0	0	12%
0	1	0	1	-2%
0	1	1	0	-4%
0	1	1	1	-8%
1	0	0	0	-12%

System Trim Register 2 (SYSTRIM2)

Register Name and Address: IFBHBTRIM - $10

	Bit7	6	5	4	3	2	1	Bit0
Read	0	0	0	0	0	0	0	0
Write	CRHBHC1	CRHBHC0	CRHB5	CRHB4	CRHB3	CRHB2	CRHB1	CRHB0
Reset	0	0	0	0	0	0	0	0

CRHBHC1:0 - Current Recopy HB1:2 Trim Bits

These write only bits are for trimming the current recopy of the half-bridge HB1 and HB2 (CSA=0). The provided trim values have to be copied into these bits after every reset. Reset clears the CRHBHC1:0 bits.

Table 16. Current Recopy Trim for HB1:2 (CSA=0)

CRHBHC1	CRHBHC0	Adjustment
0	0	0
0	1	-10%
1	0	5%
1	1	10%

CRHB5:3 - Current Recopy HB3:4 Trim Bits

These write only bits are for trimming the current recopy of the half-bridge HB3 and HB4 (CSA=1). The provided trim values have to be copied into these bits after every reset. Reset clears the CRHB5:3 bits.

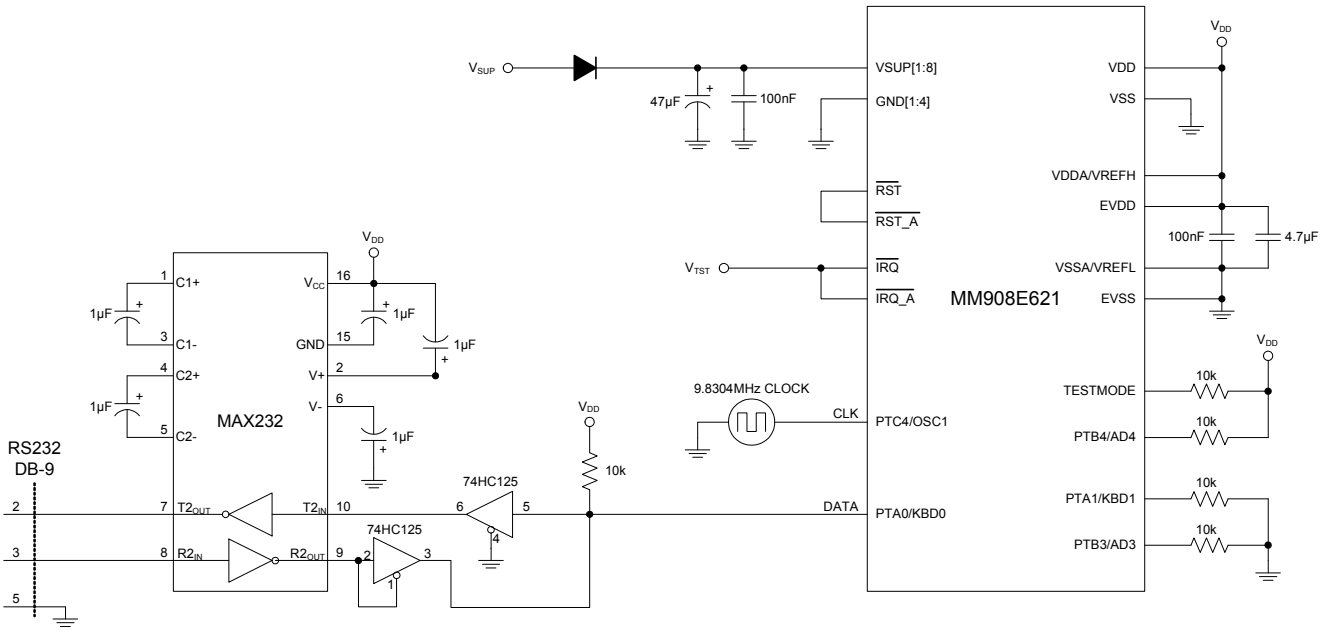


Figure 31. Normal Monitor Mode Circuit

Table 20 summarizes the possible configurations and the necessary setups.

Table 20. Monitor Mode Signal Requirements and Options

Mode	$\overline{IRQ}$	$\overline{RST}$	TESTMODE	Reset Vector	Serial Communication		Mode Selection		ICG	COP	Normal Request Time-out	Communication Speed		
					PTA0	PTA1	PTB3	PTB4				External Clock	Bus Frequency	Baud Rate
Normal Monitor	V_{TST}	V_{DD}	1	X	1	0	0	1	OFF	disabled	disabled	9.8304 MHz	2.4576 MHz	9600
Forced Monitor	V_{DD}	V_{DD}	1	$FFFF (blank)	1	0	X	X	OFF	disabled	disabled	9.8304 MHz	2.4576 MHz	9600
	GND								ON	disabled	disabled	—	Nominal 1.6 MHz	Nominal 6300
User	V_{DD}	V_{DD}	0	not $FFFF (not blank)	X	X	X	X	ON	enabled	enabled	—	Nominal 1.6 MHz	Nominal 6300

Notes

36. PTA0 must have a pullup resistor to V_{DD} in monitor mode
37. External clock is a 4.9152 MHz, 9.8304 MHz or 19.6608 MHz canned oscillator on OCS1
38. Communication speed with external clock is depending on external clock value. Baud rate is bus frequency / 256
39. X = don't care
40. V_{TST} is a high voltage V_{DD} + 3.5 V ≤ V_{TST} ≤ V_{DD} + 4.5 V

EMC/EMI RECOMMENDATIONS

This paragraph gives some device specific recommendations to improve EMC/EMI performance. Further generic design recommendations can be found on the Freescale web site www.freescale.com.

VSUP Pins (VSUP[1:8])

It is recommended to place a high quality ceramic decoupling capacitor close to the VSUP pins to improve EMC/EMI behavior.

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS B AND C TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46 mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 mm AND 0.3 mm FROM THE LEAD TIP.
9. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. THIS DIMENSION IS DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTER–LEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
10. THESE DIMENSIONS DEFINE THE PRIMARY SOLDERABLE SURFACE AREA.

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	**MECHANICAL OUTLINE**	PRINT VERSION NOT TO SCALE	
TITLE: 54LD SOIC W/B, 0.65 PITCH 4.5 X 9.8 EXPOSED PAD, CASE–OUTLINE	DOCUMENT NO: 98ASA10712D		REV: O
	CASE NUMBER: 1823–01		17 NOV 2005
	STANDARD: NON–JEDEC		

EK SUFFIX (PB-FREE)
54-PIN SOICW-EP
98ASA10712D
ISSUE 0

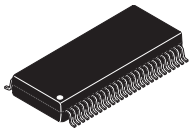
908E621

ADDITIONAL INFORMATION

THERMAL ADDENDUM (REV 1.0)

908E621

54-PIN SOICW-EP



98ASA10712D
54-PIN SOICW-EP

Note For package dimensions, refer to the 908E621 device datasheet.

INTEGRATED QUAD H-BRIDGE AND TRIPLE HIGH-SIDE DRIVER WITH EMBEDDED MCU AND LIN FOR MIRROR

Introduction

This thermal addendum is provided as a supplement to the MM908E621 technical data sheet. The addendum provides thermal performance information that may be critical in the design and development of system applications. All electrical, application and packaging information is provided in the data sheet.

Package and Thermal Considerations

This MM908E621 is a dual die package. There are two heat sources in the package independently heating with P_1 and P_2. This results in two junction temperatures, T_{J1} and T_{J2}, and a thermal resistance matrix with $R_{\theta JAmn}$.

For *m*, *n* = 1, $R_{\theta JA11}$ is the thermal resistance from Junction 1 to the reference temperature while only heat source 1 is heating with P_1.

For *m* = 1, *n* = 2, $R_{\theta JA12}$ is the thermal resistance from Junction 1 to the reference temperature while heat source 2 is heating with P_2. This applies to $R_{\theta J21}$ and $R_{\theta J22}$, respectively.

$$\begin{Bmatrix} T_{J1} \\ T_{J2} \end{Bmatrix} = \begin{bmatrix} R_{\theta JA11} & R_{\theta JA12} \\ R_{\theta JA21} & R_{\theta JA22} \end{bmatrix} \cdot \begin{Bmatrix} P_1 \\ P_2 \end{Bmatrix}$$

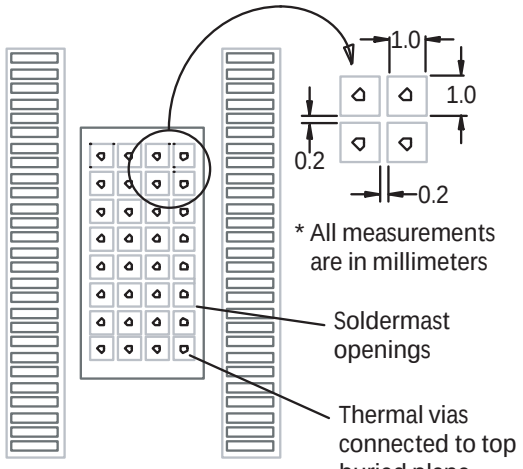
The stated values are solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment. Stated values were obtained by measurement and simulation according to the standards listed below.

Standards

Table 22. Thermal Performance Comparison

Thermal Resistance	1 = Power Chip, 2 = Logic Chip [°C/W]		
	m = 1, *n* = 1	*m* = 1, *n* = 2 *m* = 2, *n* = 1	*m* = 2, *n* = 2
$R_{\theta JAmn}$ (1)(2)	23	20	24
$R_{\theta JBmn}$ (2)(3)	9.0	6.0	10
$R_{\theta JAmn}$ (1)(4)	52	47	52
$R_{\theta JCmn}$ (5)	1.0	0	2.0

Notes:
1. Per JEDEC JESD51-2 at natural convection, still air condition.
2. 2s2p thermal test board per JEDEC JESD51-7and JESD51-5.
3. Per JEDEC JESD51-8, with the board temperature on the center trace near the power outputs.
4. Single layer thermal test board per JEDEC JESD51-3 and JESD51-5.
5. Thermal resistance between the die junction and the exposed pad, “infinite” heat sink attached to exposed pad.



54 Terminal SOIC-EP
0.65 mm Pitch
17.9 mm x 7.5 mm Body
10.3 mm x 5.1 mm Exposed Pad

Figure 34. Thermal Land Pattern for Direct Thermal Attachment Per JEDEC JESD51-5

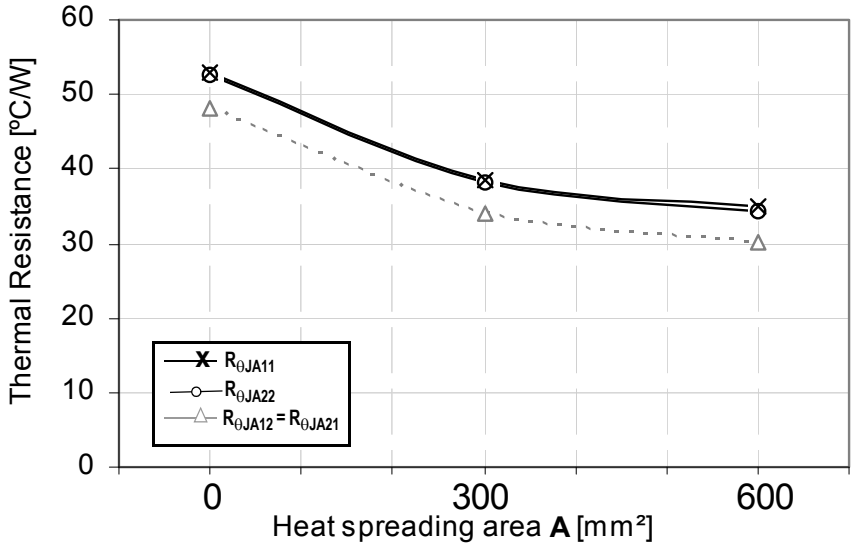


Figure 36. Device on Thermal Test Board $R_{\theta JA}$

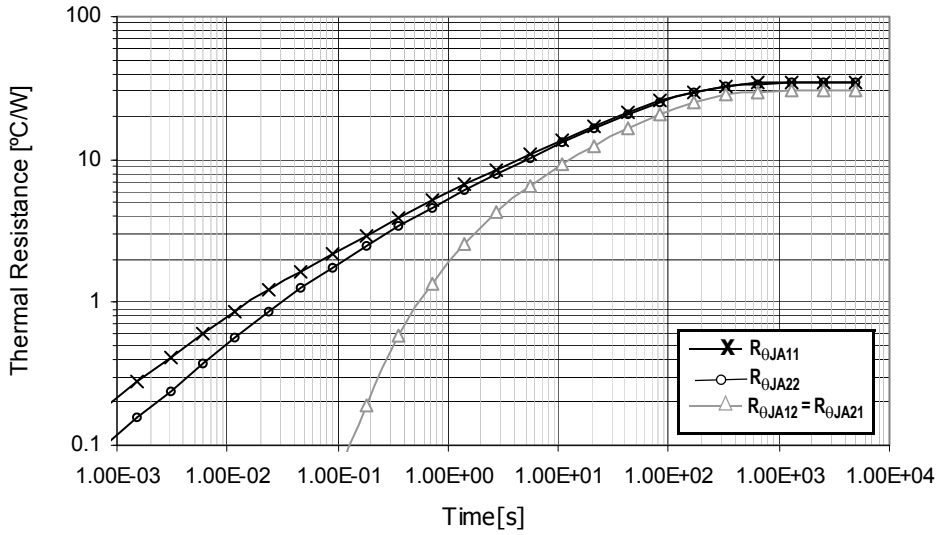


Figure 37. Transient Thermal Resistance $R_{\theta JA}$ (1.0 W Step Response)
Device on Thermal Test Board Area A = 600 (mm^2)