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Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Automotive Mirror Control
Core Processor	HC08
Program Memory Type	FLASH (16kB)
Controller Series	908E
RAM Size	512 x 8
Interface	SCI, SPI
Number of I/O	12
Voltage - Supply	9V ~ 16V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	54-SSOP (0.295", 7.50mm Width) Exposed Pad
Supplier Device Package	54-SOIC-EP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mm908e621acdwbr2

PIN CONNECTIONS

Transparent Top View of Package

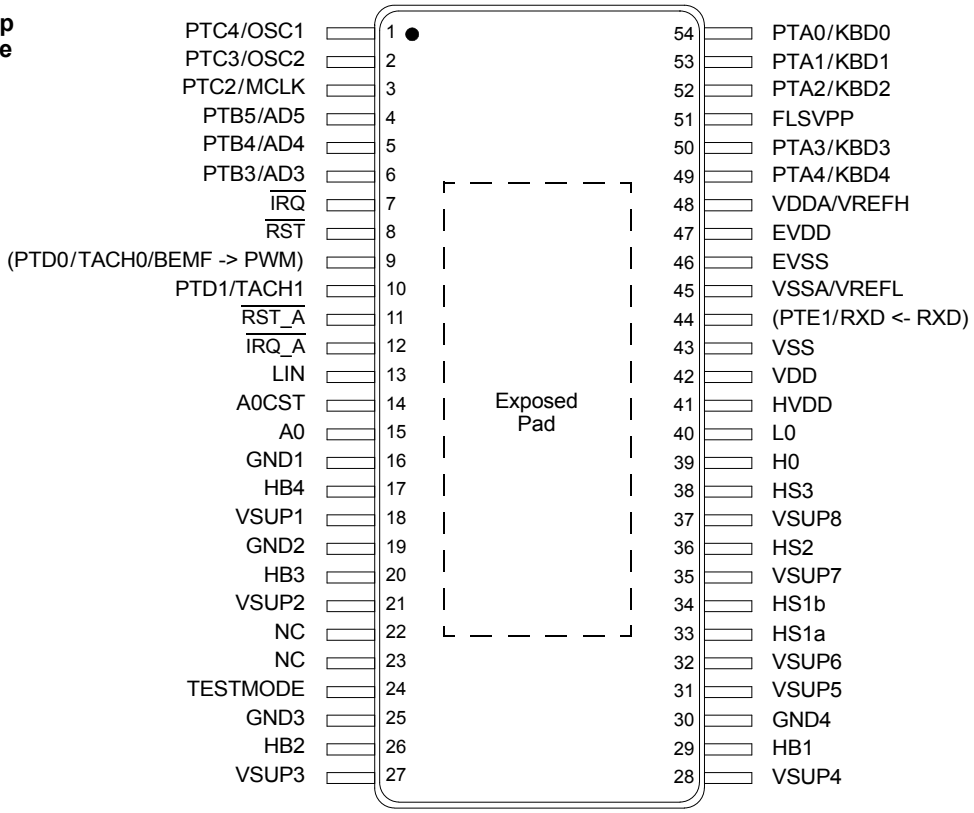


Figure 3. Pin Connections

Table 1. Pin Definitions

A functional description of each pin can be found in the Functional Pin Description section beginning on page 19.

Die	Pin	Pin Name	Formal Name	Definition
MCU	1 2 3	PTC4/OSC1 PTC3/OSC2 PTC2/MCLK	Port C I/Os	These pins are special function, bidirectional I/O port pins that are shared with other functional modules in the MCU.
MCU	4 5 6	PTB5/AD5 PTB4/AD4 PTB3/AD3	Port B I/Os	These pins are special function, bidirectional I/O port pins that are shared with other functional modules in the MCU.
MCU	7	$\overline{\text{IRQ}}$	External Interrupt Input	This pin is an asynchronous external interrupt input pin.
MCU	8	$\overline{\text{RST}}$	External Reset	This pin is bidirectional, allowing a reset of the entire system. It is driven low when any internal reset source is asserted.
MCU / Analog	9	(PTD0/TACH0/BEMF -> PWM)	PWM signal	This pin is the PWM signal test pin. It internally connects the MCU PTD0/TACH0 pin with the Analog die PWM input. Note: Do not connect in the application.
MCU	10	PTD1/TACH1	Port D I/Os	This pin is a special function, bidirectional I/O port pin that is shared with other functional modules in the MCU.
MCU / Analog	44	(PTE1/RXD <- RXD)	LIN Transceiver Output	This pin is the LIN Transceiver output test pin. It internally connects the MCU PTE1/RXD pin with the Analog die LIN transceiver output pin RXD. Note: Do not connect in the application.

Table 3. Static Electrical Characteristics (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 datasheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40 °C ≤ T_J ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SYSTEM RESETS AND INTERRUPTS					
Low Voltage Reset (LVR)					
Threshold	V_{LVRON}	3.8	4.2	4.65	V
Hysteresis	V_{LVR_HYS}	50	–	300	mV
Low Voltage Interrupt (LVI)					V
Threshold	V_{LVION}	6.0	–	7.5	
Hysteresis	V_{LVI_HYS}	0.3	–	0.8	
High Voltage Interrupt (HVI)					V
Threshold	V_{HVION}	20	–	24	
Hysteresis	V_{HVI_HYS}	0.5	–	1.5	
High Temperature Interrupt (HTI)[11]					°C
Threshold T_J	T_{ION}	125	–	150	
Hysteresis	T_{IH}	5.0	–	10.0	
High Temperature Reset (HTR)[11]					°C
Threshold T_J	T_{RON}	155	–	180	
Hysteresis	T_{IH}	5.0	–	10.0	
VOLTAGE REGULATOR[12]					
Normal Mode Output Voltage[13]					V
I_{OUT} = 60 mA, 7.5 V < V_{SUP} < 20 V	V_{DDRUN1}	4.75	5.0	5.25	
I_{OUT} = 60 mA, V_{SUP} < 7.5 V and V_{SUP} > 20 V	V_{DDRUN2}	4.75	5.0	5.25	
Normal Mode Total Output Current	I_{OUTRUN}	–	120	150	mA
Load Regulation - I_{OUT} = 60 mA, V_{SUP} = 9.0 V, T_J = 125 °C	V_{LR}	–	–	100	mV
STOP Mode Output Voltage[13]	V_{DDSTOP}	4.75	5.0	5.25	V
STOP Mode Total Output Current	$I_{OUTSTOP}$	150	500	1100	µA

Notes

11. This parameter is guaranteed by process monitoring but is not production tested.
12. Specification with external low ESR ceramic capacitor 1.0 µF< C < 4.7 µF and 200 mΩ ≤ ESR ≤ 10 Ω. Its not recommended to use capacitor values above 4.7 µF
13. When switching from Normal to Stop mode or from Stop mode to Normal mode, the output voltage can vary within the output voltage specification.

Table 3. Static Electrical Characteristics (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 datasheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40 °C ≤ T_J ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
HIGH SIDE OUTPUTS HS2 AND HS3(18)					
Switch On Resistance T_J = 25 °C, I_{LOAD} = 1.0 A	$R_{DS(ON)-HS23}$	–	440	500	mΩ
Over-current Shutdown	I_{HSOC23}	3.6	–	5.6	A
Over-current Shutdown blanking time(16)	t_{OCB}	–	4-8	–	µs
Current to Voltage Ratio(17) V_{ADOUT} [V] / I_{HS} [A], (measured and trimmed I_{HS} = 2.0 A)	$CR_{RATIOHS23}$	1.16	1.66	2.16	V/A
High Side Switching Frequency(16)	f_{PWMHS}	–	–	25	kHz
High Side Freewheeling Diode Forward Voltage T_J = 25 °C, I_{LOAD} = 1.0 A	V_{HSF}	–	0.9	–	V
Leakage Current	I_{LEAKHS}	–	<0.2	10	µA
HALF-BRIDGE OUTPUTS HB1 AND HB2					
Switch On Resistance High Side, T_J = 25°C, I_{LOAD} = 1.0A Low Side, T_J = 25°C, I_{LOAD} = 1.0A	$R_{DS(ON)-HB12}$	 – –	 750 750	 900 900	mΩ
Over-current Shutdown High Side Low Side	I_{HBOC12}	 1.0 1.0	 – –	 1.5 1.5	A
Over-current Shutdown blanking time(19)	t_{OCB}	–	4-8	–	µs
Switching Frequency(19)	f_{PWM}	–	–	25	kHz
Freewheeling Diode Forward Voltage High Side, T_J = 25 °C, I_{LOAD} = 1.0 A Low Side, T_J = 25 °C, I_{LOAD} = 1.0 A	 V_{HSF} V_{LSF}	 – –	 0.9 0.9	 – –	V
Leakage Current	I_{LEAKHB}	–	<0.2	10	µA
Low Side Current to Voltage Ratio(20) V_{ADOUT} [V] / I_{HB} [A], CSA = 1, (measured and trimmed I_{HB} = 200 mA) V_{ADOUT} [V] / I_{HB} [A], CSA = 0, (measured and trimmed I_{HB} = 500 mA)	$CR_{RATIOHB12}$	 17.5 3.5	 25.0 5.0	 32.5 6.5	V/A

Notes
16. This parameter is guaranteed by process monitoring but is not production tested.
17. This parameter is guaranteed only if correct trimming was applied.
18. The high side HS3 can be only used for resistive loads.
19. This parameter is guaranteed by process monitoring but is not production tested.
20. This parameter is guaranteed only if correct trimming was applied

Table 3. Static Electrical Characteristics (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 datasheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40 °C ≤ T_J ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
HALF-BRIDGE OUTPUTS HB3 AND HB4					
Switch On Resistance	$R_{DS(ON)-HB34}$				mΩ
High Side, T_J = 25 °C, I_{LOAD} = 1.0 A		–	275	325	
Low Side, T_J = 25 °C, I_{LOAD} = 1.0 A		–	275	325	
Over-current Shutdown	I_{HBOC34}				A
High Side		4.8	–	7.2	
Low Side		4.8	–	7.2	
Over-current Shutdown blanking time(21)	t_{OCB}	–	4-8	–	µs
Switching Frequency(21)	f_{PWM}	–	–	25	kHz
Freewheeling Diode Forward Voltage					V
High Side, T_J = 25 °C, I_{LOAD} = 1.0 A	V_{HSF}	–	0.9	–	
Low Side, T_J = 25 °C, I_{LOAD} = 1.0 A	V_{LSF}	–	0.9	–	
Leakage Current	I_{LEAKHB}	–	<0.2	10	µA
Low Side Current to Voltage Ratio(22)	$CR_{RATIOHB34}$				V/A
V_{ADOUT} [V] / I_{HB} [A], CSA = 1, (measured and trimmed I_{HB} = 500 mA)		3.5	5.0	6.5	
V_{ADOUT} [V] / I_{HB} [A], CSA = 0, (measured and trimmed I_{HB} = 2.0 A)		0.7	1.0	1.3	
SWITCHABLE V_{DD} OUTPUT HVDD					
Over-current Shutdown	I_{HVDDOC}	25	35	50	mA
Over-current Shutdown Blanking Time(23)	$t_{HVDDOCB}$				µs
HVDDT1:0 = 00		–	950	–	
HVDDT1:0 = 01		–	536	–	
HVDDT1:0 = 10		–	234	–	
HVDDT1:0 = 11		–	78	–	
Over-current Flag Delay(23)	$t_{HVDDOCFD}$	–	0.5	–	ms
Dropout Voltage @ I_{LOAD} = 20 mA	$V_{HVDDDROP}$	–	110	300	mV
V_{SUP} DOWN SCALER(24)					
Voltage Ratio (RATIO $_{VSUP}$ = V_{SUP} / V_{ADOUT})	$RATIO_{VSUP}$	4.75	5.0	5.25	–
INTERNAL DIE TEMPERATURE SENSOR(24)					
Voltage / Temperature Slope(23)	S_{TTOV}	–	26	–	mV/°C
Output Voltage @25°C	V_{T25}	1.7	1.9	2.1	V

Notes
21. This parameter is guaranteed by process monitoring but is not production tested.
22. This parameter is guaranteed only if correct trimming was applied
23. This parameter is guaranteed by process monitoring but is not production tested.
24. This parameter is guaranteed only if correct trimming was applied

Table 4. Dynamic Electrical Characteristics (continued)

All characteristics are for the analog chip only. Please refer to the 68HC908EY16 datasheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0V ≤ V_{SUP} ≤ 16V, -40°C ≤ T_J ≤ 125°C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SPI INTERFACE TIMING					
SPI Operating Recommended Frequency(33)	f_{SPIOP}	0.25	—	4.0	MHz
State Machine					
Reset Low Level Duration after V_{DD} High	t_{RST}	0.8	1.25	1.94	ms
Normal Request Timeout	$t_{NORMREQ}$	51	80	150	ms
Window Watchdog Timer(34)					
Watchdog Period (WDP1:0 = 00)	t_{WD80}	52	80	124	ms
Watchdog Period (WDP1:0 = 01)	t_{WD40}	26	40	62	ms
Watchdog Period (WDP1:0 = 10)	t_{WD20}	13	20	31	ms
Watchdog Period (WDP1:0 = 11)	t_{WD10}	6.5	10	15.5	ms

Notes

33. This parameter is guaranteed by process monitoring but is not production tested.
34. This parameter is guaranteed only if correct trimming was applied. Additionally See Watchdog Period Range Value (AWD Trim) on page 46

MICROCONTROLLER PARAMETRICS

Table 5. Microcontroller

For a detailed microcontroller description, refer to the MC68HC908EY16 datasheet.

Module	Description
Core	High Performance HC08 Core with a Maximum Internal Bus Frequency of 8.0 MHz
Timer	Two 16-Bit Timers with 2 Channels (TIM A and TIM B)
Flash	16 k Bytes
RAM	512 Bytes
ADC	10-Bit Analog-to-Digital Converter
SPI	SPI Module
ESCI	Standard Serial Communication Interface (SCI) Module Bit-Time Measurement Arbitration Prescaler with Fine Baud Rate Adjustment
ICG	Internal Clock Generation Module

EXTERNAL RESET PIN ($\overline{\text{RST}}$)

A logic [0] on the $\overline{\text{RST}}$ pin forces the MCU to a known startup state. $\overline{\text{RST}}$ is bidirectional, allowing a reset of the entire system. It is driven LOW when any internal reset source is asserted.

This pin contains an internal pull-up resistor that is always activated, even when the reset pin is pulled LOW.

For details refer to the 68HC908EY16 datasheet.

POWER SUPPLY PINS (VSUP1:VSUP8)

VSUP1:VSUP8 are device power supply pins. The nominal input voltage is designed for operation from 12 V systems. Owing to the low ON-resistance and current requirements of the half-bridge driver outputs and high side output drivers, multiple VSUP pins are provided.

All VSUP pins must be connected to get full chip functionality.

POWER GROUND PINS (GND1:GND4)

GND1:GND4 are device power ground connections. Owing to the low ON-resistance and current requirements of the half-bridge driver outputs and high side output drivers, multiple pins are provided.

GND1 and GND2 pins must be connected to get full chip functionality.

HALF-BRIDGE OUTPUT PINS (HB1:HB4)

The 908E621 device includes power MOSFETs configured as four half-bridge driver outputs. The HB3:HB4 have a lower $R_{DS(ON)}$, to run higher currents (e.g. fold motor), than the HB1:B2 outputs.

The HB1:HB4 outputs are short-circuit and over-temperature protected, and they feature current recopy. Over-current protection is done on both high side and low side FET's. The current recopy are done on the low side MOSFETs.

HIGH SIDE OUTPUT PINS (HS1:HS3)

The HS output pins are a low $R_{DS(ON)}$ high side switches. Each HS switch is protected against over-temperature and over-current. The output is capable of limiting the inrush current with an automatic PWM or feature a real PWM capability using the PWM input.

The HS1 has a lower $R_{DS(ON)}$, to run higher currents (e.g. heater), than the HS2 and HS3 outputs.

For the HS1 two pins (HS1a:HS1b) are necessary for the current capability and have to be connected externally.

Important: The HS3 can be only used to drive resistive loads.

HALL-EFFECT SENSOR INPUT PIN (H0)

The Hall-effect sensor input pin H0 provides an input for Hall-effect sensors (2-pin or 3-pin) or a switch.

ANALOG INPUT PINS (A0, A0CST)

These pins are analog inputs with selectable current source values. The A0CST intent is to trim the A0 input.

WAKE-UP INPUT PIN (L0)

This pin is 40 V rated input. It can be used as wake-up source for a system wake-up. The input is falling or rising edge sensitive.

Important: If unused this pin should be connected to VSUP or GND to avoid parasitic transitions. In Low Power mode this could lead to random wake-up events.

SWITCHABLE V_{DD} OUTPUT PIN (HVDD)

The HVDD pin is a switchable V_{DD} output for driving resistive loads requiring a regulated 5.0 V supply (e.g., 3 pin Hall-effect sensors or potentiometers). The output is short-circuit protected.

LIN BUS PIN (LIN)

The LIN pin represents the single wire bus transmitter and receiver. It is suited for automotive bus systems and is based on the LIN bus specification.

+5.0 V VOLTAGE REGULATOR OUTPUT PIN (VDD)

The VDD pin is needed to place an external capacitor to stabilize the regulated output voltage. The VDD pin is intended to supply the embedded microcontroller.

Important: The VDD pin should not be used to supply other loads; use the HVDD pin for this purpose. The VDD, EVDD and VDDA/VREFH pins must be connected together.

VOLTAGE REGULATOR GROUND PIN (VSS)

The VSS pin is the ground pin for the connection of all non-power ground connections (microcontroller and sensors). **Important**: VSS, EVSS and VSSA/VREFL pins must be connected together.

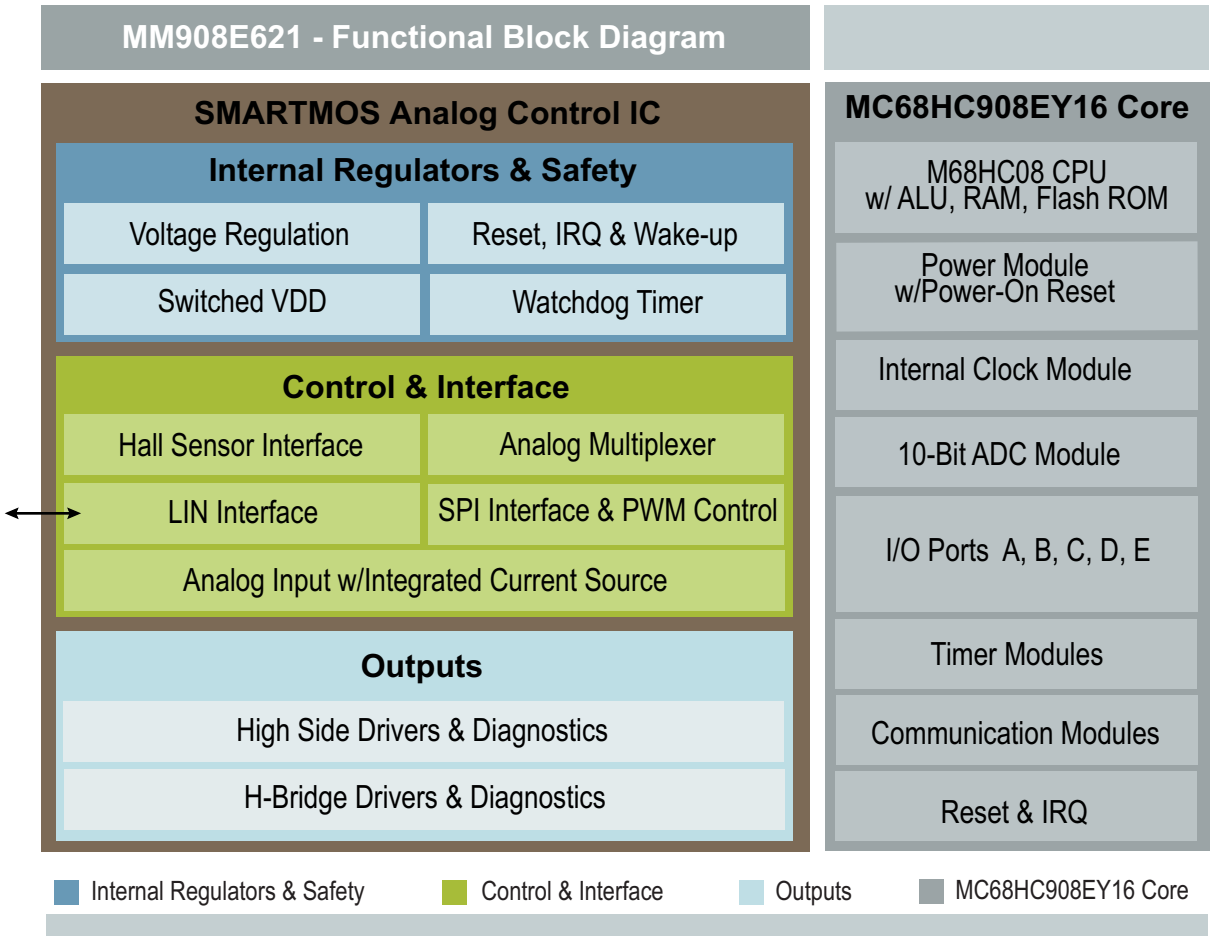
RESET PIN ($\overline{\text{RST\_A}}$)

$\overline{\text{RST\_A}}$ is the bidirectional reset pin of the analog die. It is an open drain with pullup resistor and must be connected to the $\overline{\text{RST}}$ pin of the MCU.

INTERRUPT PIN ($\overline{\text{IRQ\_A}}$)

$\overline{\text{IRQ\_A}}$ is the interrupt output pin of the analog die indicating errors or wake-up events. It is an open drain with pullup resistor and must be connected to the $\overline{\text{IRQ}}$ pin of the MCU.

FUNCTIONAL INTERNAL BLOCK DESCRIPTION



SMARTMOS ANALOG CONTROL IC

INTERNAL REGULATORS & SAFETY:

VOLTAGE REGULATION

The voltage regulator circuitry provides the regulated voltage for the Analog IC as well as the VDD/VSS rails for the core IC. The on-chip regulator consists of two elements, the main regulator, and the low voltage reset circuit. The V_{DD} regulator accepts an unregulated input supply, and provides a regulated V_{DD} supply to all digital sections of the device. The output of the regulator is also connected to the VDD pin, to provide the 5.0 V to the microcontroller.

SWITCHED VDD

This function provides a switchable +5.0 V V_{DD} rail for an external load.

WATCHDOG TIMER

The watchdog timer module generates a reset, in case of a watchdog timeout or wrong watchdog timer reset. A watchdog reset event will reset all registers in the SPI, excluding the RSR.

RESET, IRQ & WAKE-UP

There are several functions on the Analog IC that can generate a reset or wake-up signal to the core IC. There is a pin that is used to detect an external wake-up event. The Reset signal has many possible sources in the Analog IC circuitry. The IRQ function on the Analog IC, will notify the core IC of pending system critical conditions.

CONTROL & INTERFACE:

HALL SENSOR INTERFACE

This interface can be configured to support an input pin as a general purpose input, or as a hall-effect sensor input, to be able to read 3-pin / 2-pin hall sensors or switches.

Table 6. Operating Modes Overview

Device Mode	Voltage Regulator	Wake-up Capabilities	$\overline{\text{RST\_A}}$ Output	MCU monitoring/ Watchdog Function	Power Stages	LIN Interface
Reset	V_{DD} ON	N/A	LOW	Disabled	Disabled	Disabled
Normal Request	V_{DD} ON	N/A	HIGH	$t_{NORMREQ}$ (80 ms typical) timeout to set PSON bit in System Control Register	Disabled	Disabled
Normal (Run)	V_{DD} ON	N/A	HIGH	Window Watchdog active if enabled	Enabled	Enabled
Stop	V_{DD} ON with limited current capability	LIN wake-up, L0 state change (SPI PSON=1)(35)	HIGH	Disabled	Disabled	Recessive state with wake-up capability
Sleep	V_{DD} OFF	LIN wake-up L0 state change	LOW	Disabled	Disabled	Recessive state with wake-up capability

Notes
35. The SPI is still active in Stop mode. However, due to the limited current capability of the voltage regulator in Stop mode, the PSON bit has to be set before the increased current caused from a running MCU causes an LVR.

OPERATING MODES OF THE MCU

For a detailed description of the operating modes of the MCU, refer to the MC68HC908EY16 datasheet.

INTERRUPTS

The 908E621 has seven different interrupt sources. An interrupt pulse on the $\overline{\text{IRQ\_A}}$ pin is generated to report an event or fault to the MCU. All interrupts are maskable and can be enabled/disabled via the SPI (Interrupt Mask Register). After reset, all interrupts are automatically disabled.

Low Voltage Interrupt

Low voltage interrupt (LVI) is related to external supply voltage VSUP. If this voltage falls below the LVI threshold, it will set the LVIF bit in the Interrupt Flag Register. If the low voltage interrupt is enabled (LVIE = 1), an interrupt will be initiated.

During Sleep and Stop mode, the low voltage interrupt circuitry is disabled.

High Voltage Interrupt

The High voltage Interrupt (HVI) is related to the external supply voltage VSUP. If this voltage rises above the HVI threshold, it will set the HVIF bit in the Interrupt Flag Register. If the High voltage Interrupt is enabled (HVIE = 1), an interrupt will be initiated.

During Stop and Sleep mode, the HVI circuitry is disabled.

High Temperature Interrupt

The high temperature interrupt (HTI) is generated by the on chip temperature sensors. If the chip temperature is above the HTI threshold, the HTIF bit in the Interrupt Flag Register will be set. If the high temperature interrupt is enabled (HTIE = 1), an interrupt will be initiated.

During Stop and Sleep mode, the HTI circuitry is disabled.

LIN Interrupt

The LIN Interrupt is related to the Stop mode. If the LIN interrupt is enabled (LINIE = 1) in Stop mode, an interrupt is asserted if a rising edge is detected, and the bus was dominant longer than T_{PROPWL}. After the wake-up / interrupt, the LINIF indicates the reason for the wake-up / interrupt.

Power Stage Fail Interrupt

The power stage fail flag indicates an error condition on any of the power stages (see Figure 14, page 27). If the power stage fail interrupt is enabled (PSFIE = 1), an interrupt will be initiated if:

During Stop and Sleep mode, the PSFI circuitry is disabled.

HO Input Interrupt

The H0 interrupt flag H0IF is set in run mode by a state change of the H0F flag (rising or falling edge on the enabled input). The interrupt function is available if the input is selected as General Purpose, or as a 2-pin Hall sensor input. The interrupt is maskable with the H0IE bit in the Interrupt Mask Register.

During Stop and Sleep mode, the H0I circuitry is disabled.

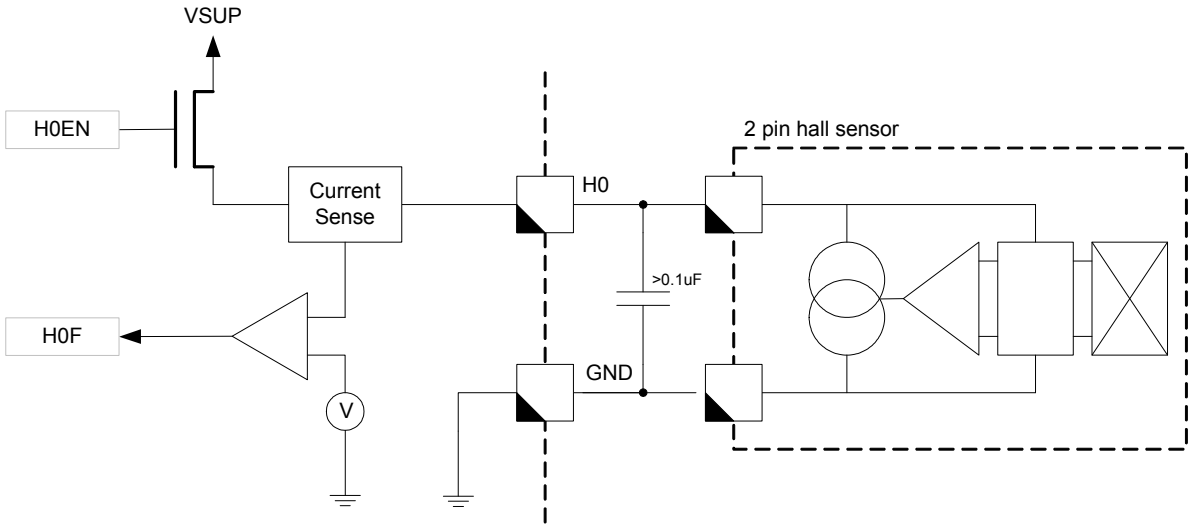


Figure 19. H0 Used as 2-pin Hall-sensor Input

General Purpose Input

H0 is selected as a general purpose input, if the H0MS bit in the H0/L0 Status and Control Register (HLSCTL) is cleared. In this mode, the input is usable as a standard 5.0 V input. The H0 input has a selectable internal pull-up resistor. The pull-up can be switched off with the H0PD bit in the H0/L0 Status and Control Register (HLSCTL). After reset, the internal pull-up is enabled.

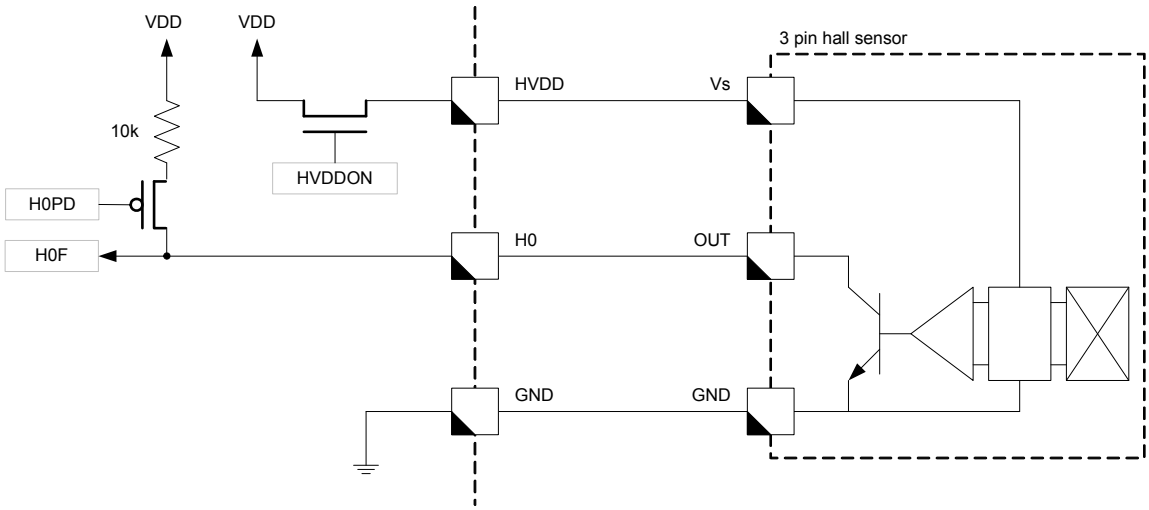


Figure 20. H0 Used as 3 Pin Hall-effect Sensor Input

Table 9. High Side Configuration Bits

HSxPWM	HSxON	Mode
0	0	High side MOSFET off
0	1	High side MOSFET on if over-current, the over-current flag (HSxOCF) is set, and the high side MOSFET is turned off
1	0	In this mode, the PWM duty cycle is either controlled by the PWM input signal, or if the over-current shutdown value is reached by the part itself. Without reaching the over-current shutdown, the high side driver is directly driven from the PWM input signal. If the Input signal is high, the output is on. If low, the output is off (PWM control). If the current reaches the over-current shutdown value, the high side will be automatically turned off. With the next rising edge of the PWM input signal, the output will turn on again (current limitation). The HSxOCF bit will be set. The software has to distinguish between an inrush current and a real short on the output.
1	1	High side MOSFET is switched on and the inrush current limitation is enabled. This means the high side will start automatically with a current limitation around the over-current shutdown threshold. (PWM signal must be applied, see Figure 24) If the high side enters current limitation, the HSxOCF bit is set, but the output is not disabled. The software needs to distinguish between an inrush current and a real short on the output.

High Side Over-voltage / Under-voltage Protection

The outputs are protected against under /over-voltage conditions. This protection is done by the low and high voltage interrupt circuitry. If an over /under-voltage condition is detected (LVIF / HVIF), and Bit VIS in the High Side Status Register is cleared, the output is disabled.

The over /under-voltage status flags are cleared (and the output reenabled), by writing a logic [1] to the LVIF / HVIF flags in the Interrupt Flag Register, or by reset. Clearing this flag has no effect as long as a high or low voltage condition is present.

HIGH SIDE OVER-TEMPERATURE PROTECTION

The outputs are protected against over-temperature conditions.

Each power output comprises two different temperature thresholds.

The first threshold is the high temperature interrupt (HTI). If the temperature reach this threshold, the HTI bit in the interrupt flag register is set and an interrupt will be generated, if the HTIE bit in the interrupt mask register is set. In addition, this interrupt can be used to automatically turn off the power stages (all high sides, on Half-bridges just the high side FET's). This shutdown can be enabled/disabled by the HTIS0 bit.

The high temperature interrupts flag (HTIE) is cleared (and the outputs reenabled) by writing a logic [1] to the HTIF flag in the Interrupt Status Register, or by reset. Clearing this flag has no effect as long as a high temperature condition is present.

If the HTIS shutdown is disabled, a second threshold (HTR) will be used to turn off all power stages (HB (all Fet's), HS, HVDD, H0) in order to protect the device.

High Side Over-current Protection

The HS outputs are protected against over-current. When the over-current limit is reached, the output will be automatically switched off and the over-current flag is set.

Due to the high inrush current of bulbs, a special feature was implemented to avoid a over-current shutdown during this inrush current. If a PWM frequency will be supplied to the PWM input during the switch on of a bulb, the inrush current will be limited to the over-current shutdown limit. This means, if the current reaches the over-current shutdown, the high side will be switched off, but each rising edge on the PWM input will enable the driver again. The duty cycle supplied by the MCU has no influence on the switch-on time of the high side driver.

In order to distinguish between a shutdown due to an inrush current or a real shutdown, the software checks if the over-current status flag (HSxOCF) in the High Side Status register is set beyond a certain period of time.

If the watchdog is enabled, it will generate a system reset, if the timer has reached its end value, or if a watchdog reset (WDRST) has occurred in the closed window.

The watchdog period can be selected with 2 bits in the WDCTL, in order to get 10ms, 20ms, 40ms and 80ms period.

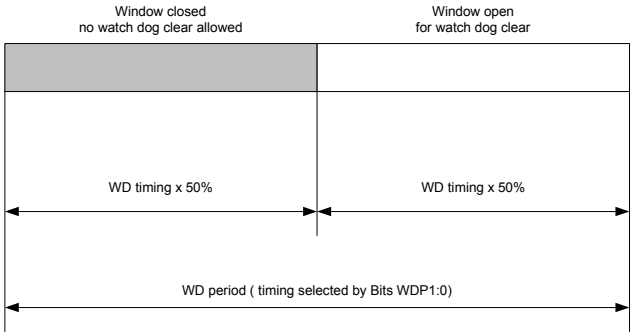


Figure 28. Window Watchdog Period

Stop mode

Operations of the watchdog function is halted in stop mode (counter/oscillator stopped). After wake-up, the watchdog timer is automatically cleared, in order to give the MCU the full time to reset the watchdog.

Sleep mode

Operations of the watchdog function is halted in sleep mode. Because the main voltage regulator asserts an LVR reset, the Watchdog functionality is disabled, and the WDRE bit is cleared as soon as sleep mode is entered. To re-enable this function bit WDRE has to be set after wake-up.

Watchdog Control Register (WDCTL)

Register Name and Address: WDCTL - $0B

	Bit7	6	5	4	3	2	1	Bit0
Read	WDRE	WDP1	WDP0	0	0	0	0	0
Write								WDRST
Reset	0	0	0	0	0	0	0	0

WDRE - Watchdog Reset Enable Bit

This read/write (write once) bit activates the watchdog. The WDRE can only be set and can not be cleared by software. Reset clears the WDRE bit.

1 = Watchdog enabled
0 = Watchdog disabled

WDP1:0 - Watchdog Period Select Bits

This read/write bit select the clock rate of the Watchdog. Reset clears the WDP1:0 bits.

Table 11. Watchdog Period Selection Bits

WDP1	WDP0	Mode
0	0	80 ms window watchdog period
0	1	40 ms window watchdog period
1	0	20 ms window watchdog period
1	1	10 ms window watchdog period

WDRST - Watchdog Reset Bit

This write only bit resets the Watchdog. Write a logic [1] to reset the watchdog timer.

1 = Reset WD and restart timer
0 = no effect

Voltage Regulator

The 908E621 contains a low power, low drop voltage regulator, to provide internal power and external power for the MCU. The on-chip regulator consist of two elements, the main regulator and the low voltage reset circuit.

The V_{DD} regulator accepts an unregulated input supply and provides a regulated V_{DD} supply to all digital sections of the device. The output of the regulator is also connected to the VDD pin to provide the 5.0 V to the microcontroller.

Run mode

During RUN mode the main voltage regulator is on. It will provide a regulated supply to all digital sections.

STOP mode

During STOP mode, the Stop mode regulator will take care of suppling a regulated output voltage. The Stop mode regulator has a limited output current capability.

SLEEP mode

In Sleep mode, the main voltage regulator external, V_{DD}, is turned off and the LVR circuitry will force the $\overline{RST\_A}$ pin low.

LOGIC COMMANDS AND REGISTERS

908E621 SERIAL PHERIPHERAL INTERFACE (SPI)

The Serial Peripheral Interface (SPI) creates the communication link between the MCU and the analog die.

The interface consists of four pins

- MOSI - Master Out Slave In (internal pulldown)
- MISO - Master In Slave Out
- $\underline{SPSCK}$ - Serial Clock (internal pulldown)
- $\overline{SS}$ - Slave Select (internal pullup)

A complete data transfer via the SPI, consists of 2 bytes. The master sends address and data, the slave returns system status and the data of the selected address.

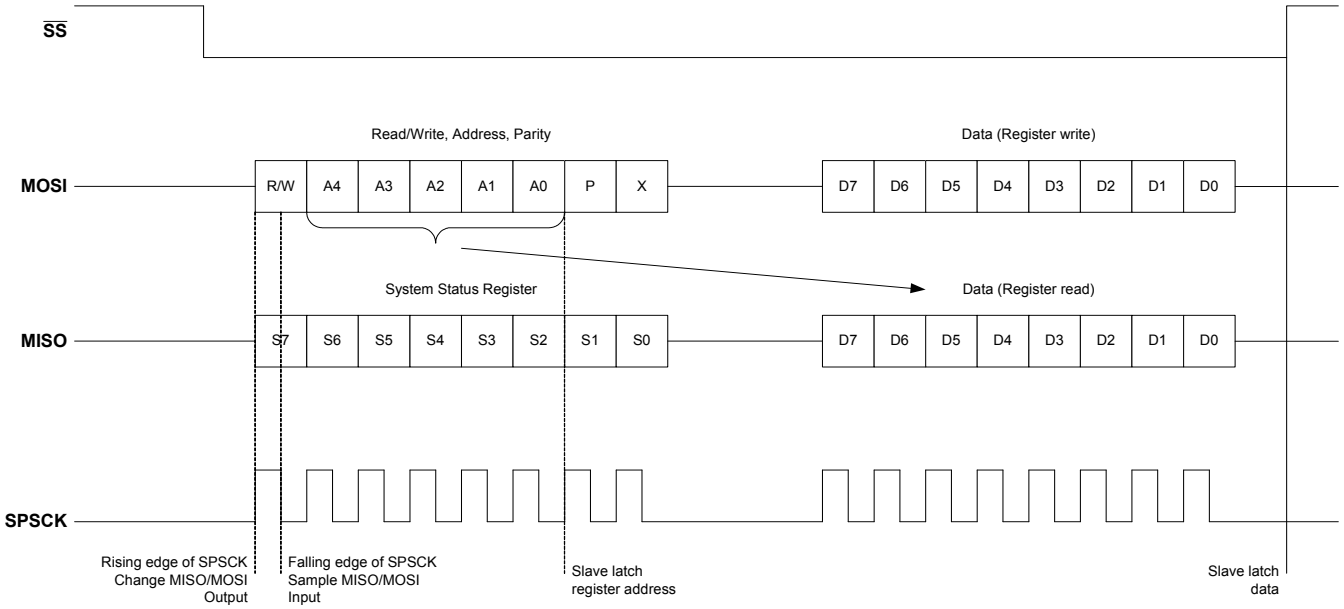


Figure 29. SPI Protocol

- During the inactive phase of $\overline{SS}$, the new data transfer will be prepared. The falling edge on the $\overline{SS}$ line, indicates the start of a new data transfer (framing), and puts MISO in the low impedance mode. The first valid data are moved to MISO with the rising edge of SPSCK.
- The MOSI, MISO will change data on a rising edge of SPSCK.
- The MOSI, MISO will be sampled on a falling edge of SPSCK.
- The data transfer is only valid, if exactly 16 sample clock edges are present in the active phase of $\overline{SS}$.
- After a write operation, the transmitted data will be latched into the register by the rising edge of $\overline{SS}$.
- Register read data is internally latched into the SPI at the time when the parity bit is transferred
- $\overline{SS}$ high will force MISO to high-impedance

Master Address Byte

A4 - A0

Includes the address of the desired register.

R/$\overline{W}$

Includes the information, if it is a read or a write operation.

- If R/$\overline{W}$ = 1 (read operation), the second byte of master contains no valid information, and the slave just transmits back register data.
- If R/$\overline{W}$ = 0 (write operation), the master sends data to be written in the second byte, the slave sends concurrently contents of selected register prior to write operation, and the write data is latched in the *SMARTMOS* registers on rising edge of $\overline{SS}$.

Parity P

Completes the total number of 1 bits of (R/W,A[4-0]) to an even number. e.g. (R/W,A[4-0]) = 100001 -> P0 = 0.

The parity bit is only evaluated during a write operations and ignored for read operations.

Bit X

Not used

Master Data Byte

This byte includes data to be written, or no valid data, during a read operation.

Slave Status Byte

This byte always includes the contents of the system status register ($0C), independent if it is a write or read operation, or which register was selected.

Slave Data Byte

This byte includes the contents of selected register, during a write operation, it includes the register content prior to the write operation.

SPI REGISTER OVERVIEW

Table 12 summarizes the SPI Register addresses and the bit names of each register.

Table 12. SPI Register Overview

Addr	Register Name	R/W	Bit							
			7	6	5	4	3	2	1	0
$00	System Control (SYSCTL)	R	PSON	0	0	HTIS1	HTIS0	VIS	SRS1	SRS0
		W		STOP	SLEEP					
$01	Half-bridge Output (HBOUT)	R	HB4_H	HB4_L	HB3_H	HB3_L	HB2_H	HB2_L	HB1_H	HB1_L
		W								
$02	High Side Output (HSOUT)	R	HVDDON	0	HS3PWM	HS2PWM	HS1PWM	HS3ON	HS2ON	HS1ON
		W								
$03	Half-bridge Status and Control (HBSCTL)	R	CRM	0	0	0	HB4OCF	HB3OCF	HB2OCF	HB1OCF
		W								
$04	High Side Status and Control (HSSCTL)	R	HVDDOCF	0	0	0	0	HS3OCF	HS2OCF	HS1OCF
		W								
$05	Reserved	R	reserved							
		W								
$06	Reserved	R	reserved							
		W								
$07	H0/L0 Status and Control (HLSCTL)	R	L0F	0	0	H0OCF	H0F	H0EN	H0PD	H0MS
		W								
$08	A0 and Multiplexer Control (A0MUCTL)	R	CSON	CSSEL1	CSSEL0	CSA	SS3	SS2	SS1	SS0
		W								
$09	Interrupt Mask (IMR)	R	L0IE	H0IE	LINIE	HTRD	HTIE	LVIE	HVIE	PSFIE
		W								
$0A	Interrupt Flag (IFR)	R	L0IF	H0IF	LINIF	0	HTIF	LVIF	HVIF	PSFIF
		W								
$0B	Watchdog Control (WDCTL)	R	WDRE	WDP1	WDP0	0	0	0	0	0
		W								WDRST
$0C	System Status (SYSSTAT)	R	LINCL	HTIF	VF	H0F	HVDDF	HSF	HBF	0
		W								
$0D	Reset Status (RSR)	R	POR	PINR	WDR	HTR	LVR	0	LINWF	L0WF
		W								
$0E	System Test (SYSTEST)	R	reserved							
		W								
$0F	System Trim 1 (SYSTRIM1)	R	HVDDT1	HVDDT0	reserved	reserved	itrim3	itrim2	itrim1	itrim0
		W								
$10	System Trim 2 (SYSTRIM2)	R	0	0	0	0	0	0	0	0
		W	CRHBHC1	CRHBHC0	CRHB5	CRHB4	CRHB3	CRHB2	CRHB1	CRHB0
$11	System Trim 3 (SYSTRIM3)	R	0	0	0	0	0	0	0	0
		W	CRHBHC3	CRHBHC2	CRHS5	CRHS4	CRHS3	CRHS2	CRHS1	CRHS0

Analog Die System Trim Values

For improved application performance, and to ensure the outlined datasheet values, the analog die needs to be trimmed. For this purpose, 3 trim values are stored in the Flash memory at addresses $FDC4 - $FDC6. These values have to be copied into the analog die SPI registers:

- copy $FDC4 into SYSTRIM1 register $0F
- copy $FDC5 into SYSTRIM2 register $10
- copy $FDC6 into SYSTRIM3 register $11

Note: These values must be copied to the respective SPI register after a reset, to ensure proper trimming of the device.

System Test Register (SYSTEST)

Register Name and Address: SYSTEST - $0E

	Bit7	6	5	4	3	2	1	Bit0
Read Write	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
Reset	0	0	0	0	0	0	0	0

Note: do not write to the reserved bits

The System Test Register is reserved for production testing and is not allowed to be written to.

System Trim Register 1 (SYSTRIM1)

Register Name and Address: IBIAS - $0F

	Bit7	6	5	4	3	2	1	Bit0
Read Write	HVDDT1	HVDDT0	0 reserved	0 reserved	ITRIM3	ITRIM2	ITRIM1	ITRIM0
Reset	0	0	0	0	0	0	0	0

Note: do not change (set) the reserved bits

HVDDT1:0 - HVDD Over-current Shutdown Delay Bits

These read/write bits allow changes to the filter time (for capacitive load) for HVDD over-current detection. Reset clears the HVDDT1:0 bits and sets the delay to the maximum value.

Table 14. HVDD Over-current Shutdown Selection Bits

HVDDT1	HVDDT0	Typical Delay
0	0	950 µs
0	1	536 µs
1	0	234 µs
1	1	78 µs

ITRIM3:0 - IRef Trim Bits

These write only bits are for trimming the internal current references IRef (also A0, A0CST). The provided trim values have to be copied into these bits after every reset. Reset clears the ITRIM3:0 bits.

Table 15. IRef Trim Bits

itrim3	itrim2	itrim2	itrim0	Adjustment
0	0	0	0	0
0	0	0	1	2%
0	0	1	0	4%
0	0	1	1	8%
0	1	0	0	12%
0	1	0	1	-2%
0	1	1	0	-4%
0	1	1	1	-8%
1	0	0	0	-12%

System Trim Register 2 (SYSTRIM2)

Register Name and Address: IFBHBTRIM - $10

	Bit7	6	5	4	3	2	1	Bit0
Read	0	0	0	0	0	0	0	0
Write	CRHBHC1	CRHBHC0	CRHB5	CRHB4	CRHB3	CRHB2	CRHB1	CRHB0
Reset	0	0	0	0	0	0	0	0

CRHBHC1:0 - Current Recopy HB1:2 Trim Bits

These write only bits are for trimming the current recopy of the half-bridge HB1 and HB2 (CSA=0). The provided trim values have to be copied into these bits after every reset. Reset clears the CRHBHC1:0 bits.

Table 16. Current Recopy Trim for HB1:2 (CSA=0)

CRHBHC1	CRHBHC0	Adjustment
0	0	0
0	1	-10%
1	0	5%
1	1	10%

CRHB5:3 - Current Recopy HB3:4 Trim Bits

These write only bits are for trimming the current recopy of the half-bridge HB3 and HB4 (CSA=1). The provided trim values have to be copied into these bits after every reset. Reset clears the CRHB5:3 bits.

TYPICAL APPLICATIONS

DEVELOPMENT SUPPORT

As the 908E621 has the MC68HC908EY16 MCU embedded, typically all the development tools available for the MCU also apply for this device. However, due to the additional analog die circuitry and the nominal +12 V supply voltage, some additional items have to be considered:

- nominal 12 V rather than the 5.0 or 3.0 V supply
- high voltage V_{TST} might be applied not only to $\overline{IRQ}$ pin, but $\overline{IRQ\_A}$ pin
- MCU monitoring (Normal request timeout) has to be disabled

For a detailed information on the MCU related development support, see the MC68HC908EY16 datasheet - section development support.

The programming is principally possible at two stages in the manufacturing process, first on chip level, before the IC is soldered onto a pcb board, and second after the IC is soldered onto the pcb board.

Chip level programming

At the Chip level, the easiest way is to only power the MCU with +5.0 V (see Figure 30), and not to provide the analog chip with VSUP. In this setup, all the analog pins should be left open (e.g. VSUP[1:8]), and interconnections between the MCU and analog die have to be separated (e.g. $\overline{IRQ}$ - $\overline{IRQ\_A}$).

This mode is well described in the MC68HC908EY16 datasheet, section development support.

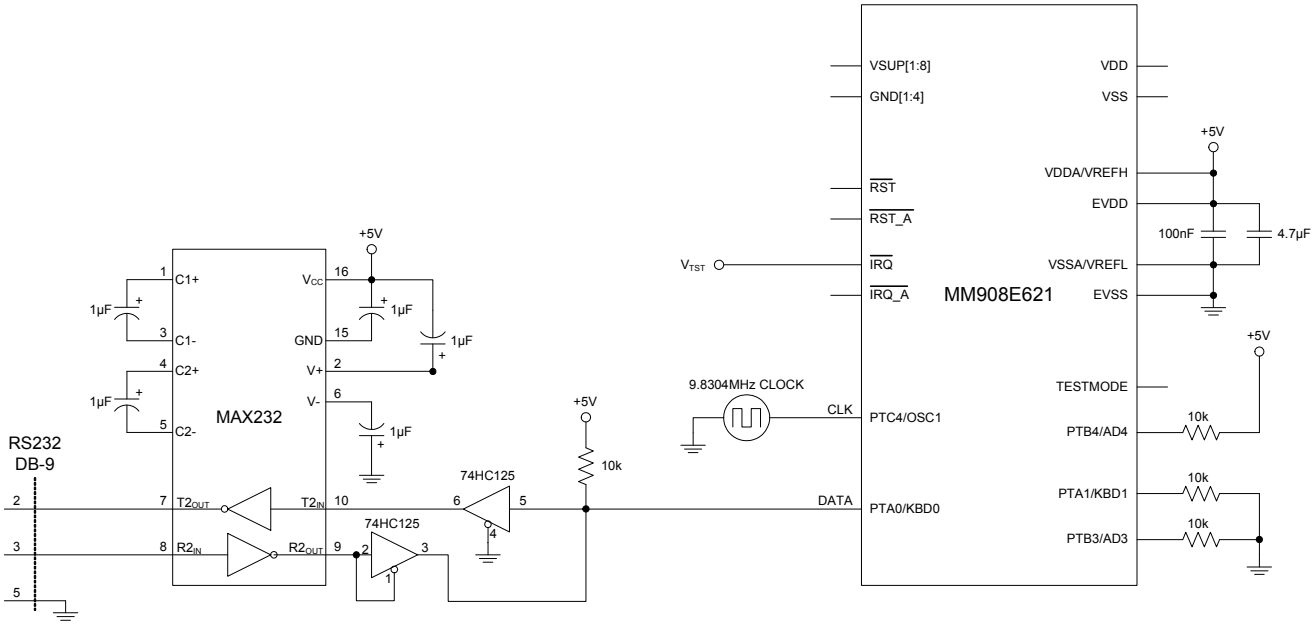


Figure 30. Normal Monitor Mode Circuit (MCU only)

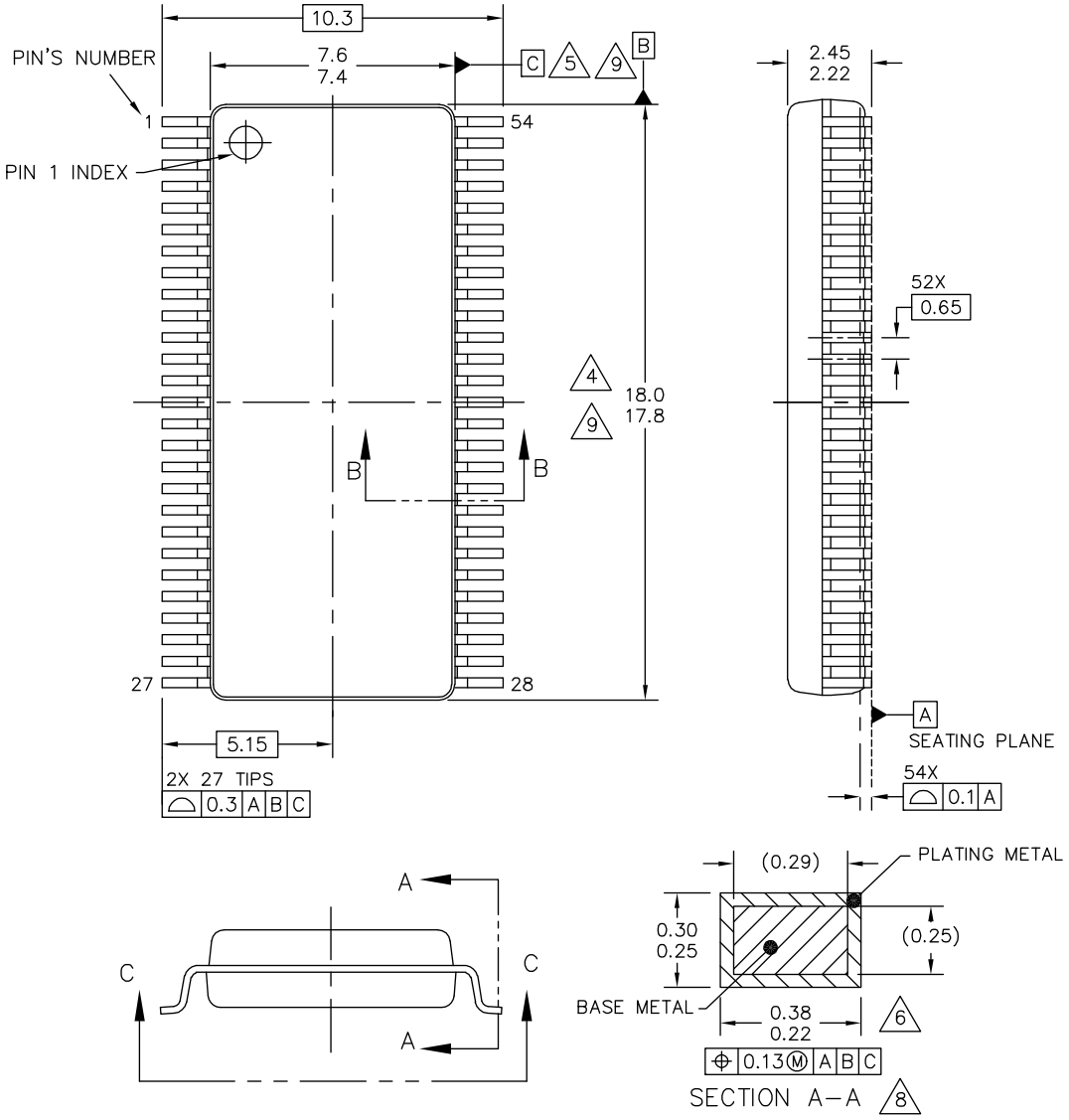
Of course it is also possible to supply the whole system with V_{SUP} instead (12 V) as described in Figure 31, page 50.

PCB level programming

If the IC is soldered onto the pcb board, it is typically not possible to separately power the MCU with +5.0 V. The whole system has to be powered up providing V_{SUP} (see Figure 31).

PACKAGE DIMENSIONS

Important For the most current revision of the package, visit www.freescale.com and do a keyword search on the 98A drawing number: 98ASA10712D.



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TITLE: 54LD SOIC W/B, 0.65 PITCH 4.5 X 9.8 EXPOSED PAD, CASE–OUTLINE	DOCUMENT NO: 98ASA10712D	REV: O
	CASE NUMBER: 1823–01	17 NOV 2005
	STANDARD: NON–JEDEC	

EK SUFFIX (PB-FREE)
54-PIN SOICW-EP
98ASA10712D
ISSUE 0

908E621

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS B AND C TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46 mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 mm AND 0.3 mm FROM THE LEAD TIP.
9. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. THIS DIMENSION IS DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTER–LEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
10. THESE DIMENSIONS DEFINE THE PRIMARY SOLDERABLE SURFACE AREA.

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TITLE: 54LD SOIC W/B, 0.65 PITCH 4.5 X 9.8 EXPOSED PAD, CASE–OUTLINE	DOCUMENT NO: 98ASA10712D		REV: O
	CASE NUMBER: 1823–01		17 NOV 2005
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908E621

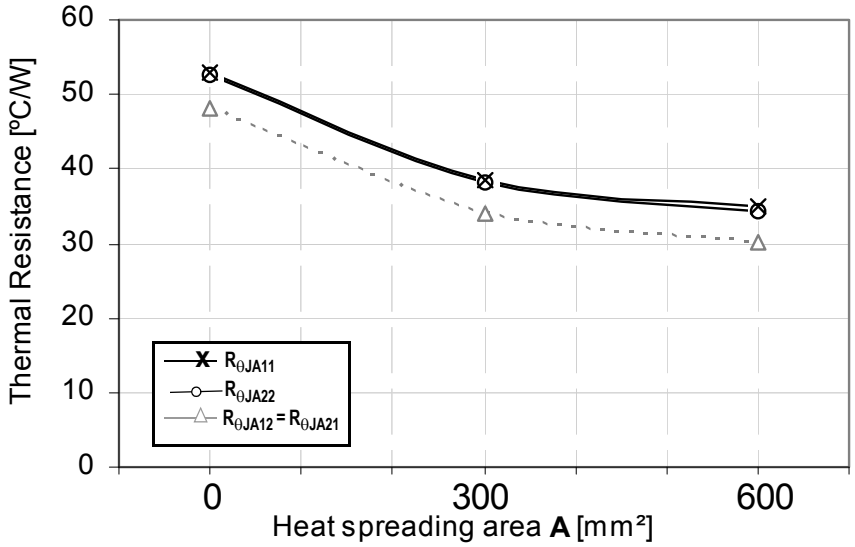

Figure 36. Device on Thermal Test Board $R_{\theta JA}$

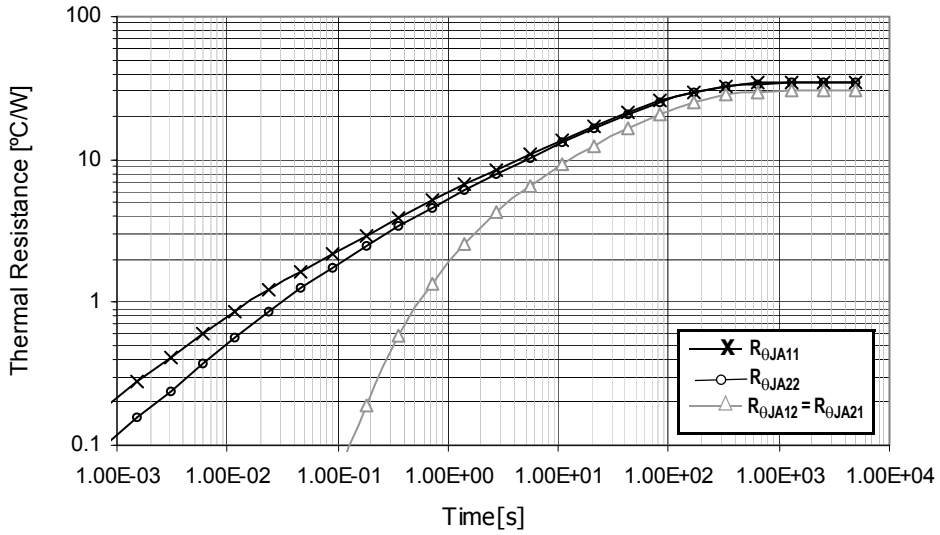

Figure 37. Transient Thermal Resistance $R_{\theta JA}$ (1.0 W Step Response)
Device on Thermal Test Board Area A = 600 (mm^2)

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
3.0	2/2007	• Implemented Revision History page • Changed Table 3, Statistic Electrical Characteristics, Hall-Effect Sensor Input H0 - 2pin Hall Sensor Input Mode (H0MS = 1), Sense Current Hysteresis on page 13 from a Minimum of 800 to 600 and Typical from 1100 to none. • Removed “Advance” watermark and updated to final Data Sheet. • Removed Peak Package Reflow Temperature During Reflow (solder reflow) parameter from Electrical Characteristics on page 6. Added note with instructions from www.freescale.com.
4.0	6/2007	• Updated to Final by removing “Advance Information” from page 1.
5.0	6/2008	• Changed STOP Mode Total Output Current on page 9 from 850 to 1100μA • Changed Sense Current Hysteresis on page 13 from 800 to 650μA • Changed Normal Request Timeout on page 15 from 124 to 150ms • Updated Freescale form and style to the current format • Updated package drawing • Added Functional Internal Block Description section
6.0	4/2012	• Added MM908E621ACPEK/R2 to the ordering information. • Removed MM908E621ACDWB/R2 from the data sheet • Updated Freescale form and style to the current format

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