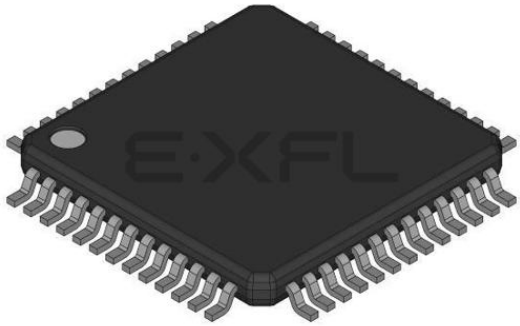

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Number of I/O	20
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Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	52-LQFP
Supplier Device Package	52-QFP (10x10)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc68hc908lj12cfb

List of Tables

1.6.9 Port A Input/Output (I/O) Pins (PTA7–PTA0)

PTA7–PTA0 are special function, bidirectional port pins (**Section 17.**). PTA7/ADC3–PTA4/ADC0 are shared with the ADC (**Section 15.**), and PTA3/KBI3–PTA0/KBI0 are shared with the KBI module (**Section 19.**).

1.6.10 Port B I/O Pins (PTB7–PTB0)

PTB7–PTB0 are special function, bidirectional port pins (**Section 17.**). PTB0/TxD–PTB1/RxD are shared with the SCI module (**Section 13.**), PTB5/T2CH1–PTB4/T2CH0 are shared with the TIM2 (**Section 11.**), PTB3/T1CH1–PTB2/T1CH0 are shared with the TIM1(**Section 11.**), PTB6/ADC4–PTB7/ADC5 are shared with the ADC (**Section 15.**).

1.6.11 Port C I/O Pins (PTC7–PTC0)

PTC7–PTC0 are special function, bidirectional port pins (**Section 17.**). PTC7/FP26–PTC0/FP19 are shared with the LCD frontplane drivers (**Section 16.**).

1.6.12 Port D I/O Pins (PTD7–PTD0)

PTD7–PTD0 are special function, bidirectional port pins (**Section 17.**). PTD7/KBI7–PTD4/KBI4 are shared with KBI module (**Section 19.**). PTD3/SPSCK–PTD0/$\overline{SS}$ are shared with SPI module (**Section 14.**).

1.6.13 LCD Backplane and Frontplane (BP0–BP2, FP0/BP3, FP1–FP18)

BP0–BP2 are the LCD backplane driver pins and FP1– FP18 are the frontplane driver pins. FP0/BP3 is the shared driver pin between FP0 and BP3 (**Section 16.**).

BPR0 is used only for BPR[7:0] = $FF, for no block protection.

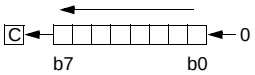
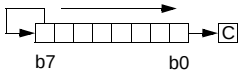
The resultant 16-bit address is used for specifying the start address of the FLASH memory for block protection. The FLASH is protected from this start address to the end of FLASH memory, at $FFFF. With this mechanism, the protect start address can be XX00 or XX80 (at page boundaries — 128 bytes) within the FLASH memory.

Examples of protect start address:

BPR[7:0]	Start of Address of Protect Range
$00 or $01	$C000 (11**00 0000 0**000 0000) The entire FLASH memory is protected.
$02 or $03	$C080 (11**00 0000 1**000 0000)
$04 or $05	$C100 (11**00 0001 0**000 0000)
$06 or $07	$C180 (11**00 0001 1**000 0000)
$08 or $09	$C200 (11**00 0010 0**000 0000)
and so on...	
$F8 or $F9	$FE00 (11**11 1110 0**000 0000)
$FA or $FB	$FE80 (11**11 1110 1**000 0000)
$FC or $FD	$FF00 (11**11 1111 0**000 0000)
$FE	$FF80 (11**11 1111 1**000 0000)
$FF	The entire FLASH memory is not protected.

Note:
The end address of the protected range is always $FFFF.

Table 6-1. Instruction Set Summary (Sheet 1 of 8)

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Cycles
			V	H	I	N	Z	C				
ADC #*opr* ADC *opr* ADC *opr* ADC *opr*,X ADC *opr*,X ADC ,X ADC *opr*,SP ADC *opr*,SP	Add with Carry	A ← (A) + (M) + (C)	↕	↕	–	↕	↕	↕	IMM DIR EXT IX2 IX1 IX SP1 SP2	A9 B9 C9 D9 E9 F9 9EE9 9ED9	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5
ADD #*opr* ADD *opr* ADD *opr* ADD *opr*,X ADD *opr*,X ADD ,X ADD *opr*,SP ADD *opr*,SP	Add without Carry	A ← (A) + (M)	↕	↕	–	↕	↕	↕	IMM DIR EXT IX2 IX1 IX SP1 SP2	AB BB CB DB EB FB 9EEB 9EDB	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5
AIS #*opr*	Add Immediate Value (Signed) to SP	SP ← (SP) + (16 « M)	–	–	–	–	–	–	IMM	A7	ii	2
AIX #*opr*	Add Immediate Value (Signed) to H:X	H:X ← (H:X) + (16 « M)	–	–	–	–	–	–	IMM	AF	ii	2
AND #*opr* AND *opr* AND *opr* AND *opr*,X AND *opr*,X AND ,X AND *opr*,SP AND *opr*,SP	Logical AND	A ← (A) & (M)	0	–	–	↕	↕	–	IMM DIR EXT IX2 IX1 IX SP1 SP2	A4 B4 C4 D4 E4 F4 9EE4 9ED4	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5
ASL *opr* ASLA ASLX ASL *opr*,X ASL ,X ASL *opr*,SP	Arithmetic Shift Left (Same as LSL)		↕	–	–	↕	↕	↕	DIR INH INH IX1 IX SP1	38 48 58 68 78 9E68	dd ff ff	4 1 1 4 3 5
ASR *opr* ASRA ASRX ASR *opr*,X ASR *opr*,X ASR *opr*,SP	Arithmetic Shift Right		↕	–	–	↕	↕	↕	DIR INH INH IX1 IX SP1	37 47 57 67 77 9E67	dd ff ff	4 1 1 4 3 5
BCC *rel*	Branch if Carry Bit Clear	PC ← (PC) + 2 + rel ? (C) = 0	–	–	–	–	–	–	REL	24	rr	3
BCLR *n*, *opr*	Clear Bit n in M	Mn ← 0	–	–	–	–	–	–	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	11 13 15 17 19 1B 1D 1F	dd dd dd dd dd dd dd dd	4 4 4 4 4 4 4 4

8.3 Features

Features of the CGM include:

- Phase-locked loop with output frequency in integer multiples of an integer dividend of the crystal reference
- Low-frequency crystal operation with low-power operation and high-output frequency resolution
- Programmable prescaler for power-of-two increases in frequency
- Programmable hardware voltage-controlled oscillator (VCO) for low-jitter operation
- Automatic bandwidth control mode for low-jitter operation
- Automatic frequency lock detector
- CPU interrupt on entry or exit from locked condition
- Configuration register bit to allow oscillator operation during stop mode

8.4 Functional Description

The CGM consists of three major sub-modules:

- Oscillator module — The oscillator module generates the constant reference frequency clock, CGMRCLK (buffered CGMXCLK).
- Phase-locked loop (PLL) — The PLL generates the programmable VCO frequency clock, CGMVCLK, and the divided, CGMPCLK. The CGMPCLK is one of the reference clocks to the base clock selector circuit.
- Base clock selector circuit — This software-controlled circuit selects the one of three clocks as the base clock, CGMOUT: CGMXCLK, CGMXCLK divided by two, or CGMPCLK divided by two.

Figure 8-1 shows the structure of the CGM.

Figure 8-2 is a summary of the CGM registers.

8.4.7 Special Programming Exceptions

The programming method described in **8.4.6 Programming the PLL** does not account for three possible exceptions. A value of 0 for R, N, or L is meaningless when used in the equations given. To account for these exceptions:

- A 0 value for R or N is interpreted exactly the same as a value of 1.
- A 0 value for L disables the PLL and prevents its selection as the source for the base clock.

(See **8.4.8 Base Clock Selector Circuit**.)

8.4.8 Base Clock Selector Circuit

This circuit is used to select either the oscillator clock, CGMXCLK, or the divided VCO clock, CGMPCLK, as the source of the base clock, CGMOUT. The two input clocks go through a transition control circuit that waits up to three CGMXCLK cycles and three CGMPCLK cycles to change from one clock source to the other. During this time, CGMOUT is held in stasis. The output of the transition control circuit is then divided by two to correct the duty cycle. Therefore, the bus clock frequency, which is one-half of CGMOUT, is one-fourth the frequency of the selected clock (CGMXCLK or CGMPCLK).

For the CGMXCLK, the divide-by-2 can be by-passed by setting the DIV2CLK bit in the CONFIG2 register. Therefore, the bus clock frequency can be one-half of CGMXCLK.

The BCS bit in the PLL control register (PCTL) selects which clock drives CGMOUT. The divided VCO clock cannot be selected as the base clock source if the PLL is not turned on. The PLL cannot be turned off if the divided VCO clock is selected. The PLL cannot be turned on or off simultaneously with the selection or deselection of the divided VCO clock. The divided VCO clock also cannot be selected as the base clock source if the factor L is programmed to a 0. This value would set up a condition inconsistent with the operation of the PLL, so that the PLL would be disabled and the oscillator clock would be forced as the source of the base clock.

9.8.1 SIM Break Status Register

The SIM break status register (SBSR) contains a flag to indicate that a break caused an exit from stop mode or wait mode.

Address: $FE00

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	R	R	R	R	R	R	SBSW	R
Write:							Note	
Reset:							0	

Note: Writing a logic 0 clears SBSW. R = Reserved

Figure 9-20. SIM Break Status Register (SBSR)

SBSW — Break Wait Bit

This status bit is set when a break interrupt causes an exit from wait mode or stop mode. Clear SBSW by writing a logic 0 to it. Reset clears SBSW.

1 = Stop mode or wait mode was exited by break interrupt
0 = Stop mode or wait mode was not exited by break interrupt

SBSW can be read within the break interrupt routine. The user can modify the return address on the stack by subtracting 1 from it. The following code is an example.

```
This code works if the H register has been pushed onto the stack in the break
service routine software. This code should be executed at the end of the break
service routine software.
HIBYTE   EQU
LOBYTE   EQU
         If not SBSW, do RTI
         BRCLR   SBSW,SBSR, RETURN    ;See if wait mode or stop mode was exited by
                                      ;break.
         TST     LOBYTE,SP            ;If RETURNLO is not zero,
         BNE     DOLO                 ;then just decrement low byte.
         DEC     HIBYTE,SP            ;Else deal with high byte, too.
DOLO     DEC     LOBYTE,SP            ;Point to WAIT/STOP opcode.
RETURN   PULH                         ;Restore H register.
         RTI
```

11.10.3 TIM Counter Modulo Registers

The read/write TIM modulo registers contain the modulo value for the TIM counter. When the TIM counter reaches the modulo value, the overflow flag (TOF) becomes set, and the TIM counter resumes counting from $0000 at the next timer clock. Writing to the high byte (TMODH) inhibits the TOF bit and overflow interrupts until the low byte (TMODL) is written. Reset sets the TIM counter modulo registers.

Address: T1MODH, $0023 and T2MODH, $002E

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
Reset:	1	1	1	1	1	1	1	1

Figure 11-7. TIM Counter Modulo Register High (TMODH)

Address: T1MODL, $0024 and T2MODL, $002F

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
Reset:	1	1	1	1	1	1	1	1

Figure 11-8. TIM Counter Modulo Register Low (TMODL)

NOTE: *Reset the TIM counter before writing to the TIM counter modulo registers.*

Section 13. Infrared Serial Communications Interface Module (IRSCI)

13.1 Contents

The infrared sub-module receives two clock sources from the SCI module: SCI_R16XCLK and SCI_R32XCLK. Both reference clocks are used to generate the narrow pulses during data transmission.
The SCI_R16XCLK and SCI_R32XCLK are internal clocks with frequencies that are 16 and 32 times the baud rate respectively. Both SCI_R16XCLK and SCI_R32XCLK clocks are used for transmitting data. The SCI_R16XCLK clock is used only for receiving data.

NOTE: *For proper SCI function (transmit or receive), the bus clock MUST be programmed to at least 32 times that of the selected baud rate.*
When the infrared sub-module is disabled, signals on the TxD and RxD pins pass through unchanged to the SCI module.

13.6 Infrared Functional Description

Figure 13-3 shows the structure of the infrared sub-module.

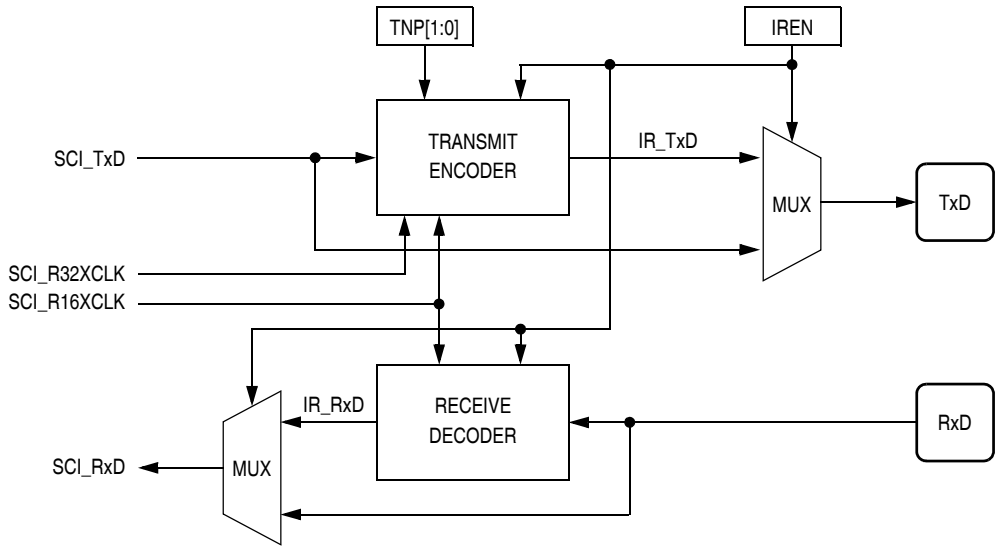


Figure 13-3. Infrared Sub-Module Diagram

The infrared sub-module provides the capability of transmitting narrow pulses to an infrared LED and receiving narrow pulses and transforming them to serial bits, which are sent to the SCI module. The infrared sub-module receives two clocks from the SCI. One of these two clocks is selected as the base clock to generate the 3/16, 1/16, or 1/32 bit width narrow pulses during transmission.

13.7.3.2 Character Reception

During an SCI reception, the receive shift register shifts characters in from the RxD pin. The SCI data register (SCDR) is the read-only buffer between the internal data bus and the receive shift register.

After a complete character shifts into the receive shift register, the data portion of the character transfers to the SCDR. The SCI receiver full bit, SCRF, in SCI status register 1 (SCS1) becomes set, indicating that the received byte can be read. If the SCI receive interrupt enable bit, SCRIE, in SCC2 is also set, the SCRF bit generates a receiver CPU interrupt request.

13.7.3.3 Data Sampling

The receiver samples the RxD pin at the RT clock rate. The RT clock is an internal signal with a frequency 16 times the baud rate. To adjust for baud rate mismatch, the RT clock is resynchronized at the following times (see **Figure 13-9**):

- After every start bit
- After the receiver detects a data bit change from logic 1 to logic 0 (after the majority of data bit samples at RT8, RT9, and RT10 returns a valid logic 1 and the majority of the next RT8, RT9, and RT10 samples returns a valid logic 0)

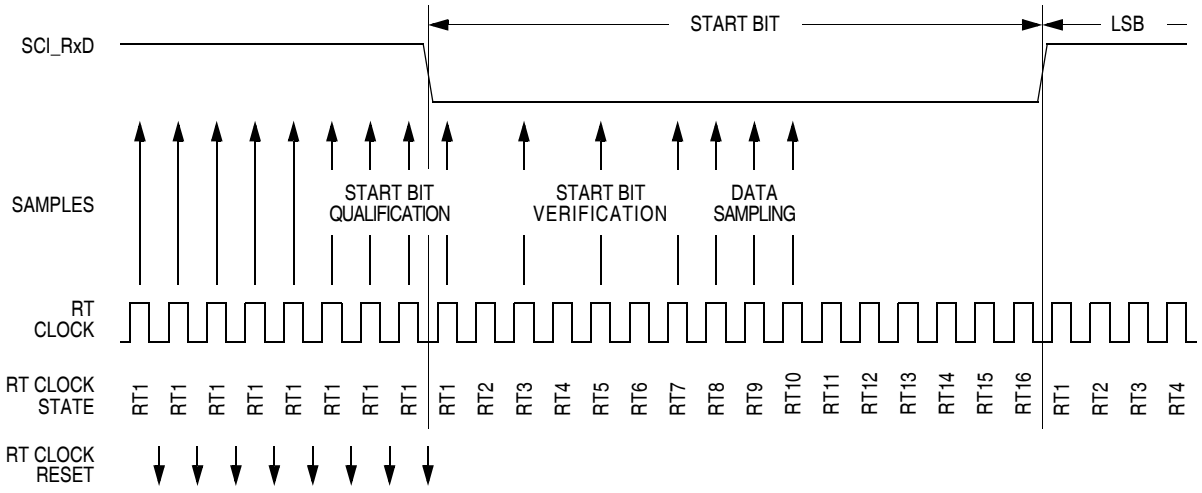


Figure 13-9. Receiver Data Sampling

13.8 Low-Power Modes

The WAIT and STOP instructions put the MCU in low power-consumption standby modes.

13.8.1 Wait Mode

The SCI module remains active after the execution of a WAIT instruction. In wait mode, the SCI module registers are not accessible by the CPU. Any enabled CPU interrupt request from the SCI module can bring the MCU out of wait mode.

If SCI module functions are not required during wait mode, reduce power consumption by disabling the module before executing the WAIT instruction.

Refer to **9.7 Low-Power Modes** for information on exiting wait mode.

13.8.2 Stop Mode

The SCI module is inactive after the execution of a STOP instruction. The STOP instruction does not affect SCI register states. SCI module operation resumes after an external interrupt.

Because the internal clock is inactive during stop mode, entering stop mode during an SCI transmission or reception results in invalid data.

Refer to **9.7 Low-Power Modes** for information on exiting stop mode.

DMARE — DMA Receive Enable Bit

CAUTION: *The DMA module is not included on this MCU. Writing a logic 1 to DMARE or DMATE may adversely affect MCU performance.*

1 = DMA not enabled to service SCI receiver DMA service requests generated by the SCRF bit (SCI receiver CPU interrupt requests enabled)
0 = DMA not enabled to service SCI receiver DMA service requests generated by the SCRF bit (SCI receiver CPU interrupt requests enabled)

DMATE — DMA Transfer Enable Bit

CAUTION: *The DMA module is not included on this MCU. Writing a logic 1 to DMARE or DMATE may adversely affect MCU performance.*

1 = SCTE DMA service requests enabled; SCTE CPU interrupt requests disabled
0 = SCTE DMA service requests disabled; SCTE CPU interrupt requests enabled

ORIE — Receiver Overrun Interrupt Enable Bit

This read/write bit enables SCI error CPU interrupt requests generated by the receiver overrun bit, OR. Reset clears ORIE.
1 = SCI error CPU interrupt requests from OR bit enabled
0 = SCI error CPU interrupt requests from OR bit disabled

NEIE — Receiver Noise Error Interrupt Enable Bit

This read/write bit enables SCI error CPU interrupt requests generated by the noise error bit, NE. Reset clears NEIE.
1 = SCI error CPU interrupt requests from NE bit enabled
0 = SCI error CPU interrupt requests from NE bit disabled

FEIE — Receiver Framing Error Interrupt Enable Bit

This read/write bit enables SCI error CPU interrupt requests generated by the framing error bit, FE. Reset clears FEIE.
1 = SCI error CPU interrupt requests from FE bit enabled
0 = SCI error CPU interrupt requests from FE bit disabled

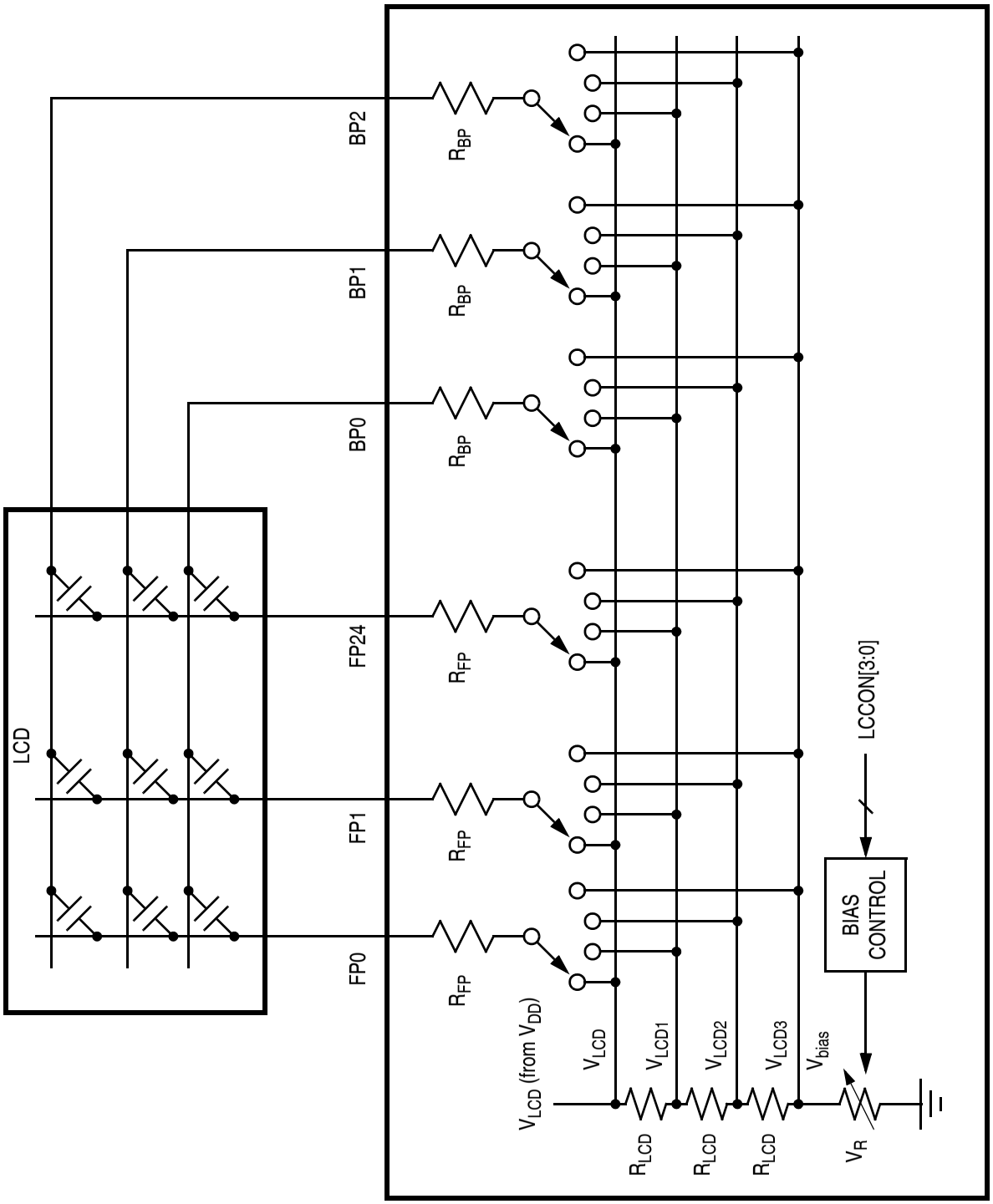


Figure 16-3. Simplified LCD Schematic (1/3 Duty, 1/3 Bias)

19.6.1 Keyboard Status and Control Register

- Flags keyboard interrupt requests
- Acknowledges keyboard interrupt requests
- Masks keyboard interrupt requests
- Controls keyboard interrupt triggering sensitivity

Address: $001B

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	KEYF	0	IMASKK	MODEK
Write:						ACKK		
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 19-3. Keyboard Status and Control Register (KBSCR)

KEYF — Keyboard Flag Bit

This read-only bit is set when a keyboard interrupt is pending. Reset clears the KEYF bit.

1 = Keyboard interrupt pending
0 = No keyboard interrupt pending

ACKK — Keyboard Acknowledge Bit

Writing a logic 1 to this write-only bit clears the keyboard interrupt request. ACKK always reads as logic 0. Reset clears ACKK.

IMASKK — Keyboard Interrupt Mask Bit

Writing a logic 1 to this read/write bit prevents the output of the keyboard interrupt mask from generating interrupt requests. Reset clears the IMASKK bit.

1 = Keyboard interrupt requests masked
0 = Keyboard interrupt requests not masked

MODEK — Keyboard Triggering Sensitivity Bit

This read/write bit controls the triggering sensitivity of the keyboard interrupt pins. Reset clears MODEK.

1 = Keyboard interrupt requests on falling edges and low levels
0 = Keyboard interrupt requests on falling edges only

Section 20. Computer Operating Properly (COP)

20.1 Contents

20.2 Introduction

The computer operating properly (COP) module contains a free-running counter that generates a reset if allowed to overflow. The COP module helps software recover from runaway code. Prevent a COP reset by clearing the COP counter periodically. The COP module can be disabled through the COPD bit in the configuration register 1 (CONFIG1).

The LVI trip point selection bits, LVISEL[1:0], select the trip point voltage, V_{TRIPF}, to be configured for 5V or 3.3V operation. The actual trip points are shown in **Section 23. Electrical Specifications**.

Setting LVI interrupt enable bit, LVIIE, enables LVI interrupts whenever the LVIOUT bit toggles (from logic 0 to logic 1, or from logic 1 to logic 0).

NOTE: *After a power-on reset (POR) the user must configure the LVISEL[1:0} bits for 3.3V or 5V operation before enabling the LVI module (by clearing the LVIPWRD bit in CONFIG1 register).*

NOTE: *If the user requires 3.3V mode and enables the LVI module after configuring the LVISEL[1;0] bits to 3.3V operation mode while the V_{DD} supply is not above the V_{TRIPF} for 3.3V mode, the MCU will immediately go into reset. The LVI in this case will hold the MCU in reset until either V_{DD} goes above the rising 3.3V trip point, V_{TRIPR}, which will release reset or V_{DD} decreases to approximately 0V which will re-trigger the power-on reset.*

LVISTOP, LVIPWRD, LVIRSTD, and LVISEL[1:0] are in the configuration registers. See **Section 5. Configuration Registers (CONFIG)** for details of the LVI's configuration bits. Once an LVI reset occurs, the MCU remains in reset until V_{DD} rises above a voltage, V_{TRIPR}, which causes the MCU to exit reset. See **9.4.2.5 Low-Voltage Inhibit (LVI) Reset** for details of the interaction between the SIM and the LVI. The output of the comparator controls the state of the LVIOUT flag in the LVI status register (LVISR). The LVIIE, LVIIF, and LVIIAK bits in the LVISR control LVI interrupt functions.

An LVI reset also drives the $\overline{RST}$ pin low to provide low-voltage protection to external peripheral devices.

22.4.1 Flag Protection During Break Interrupts

The BCFE bit in the SIM break flag control register (SBFCR) enables software to clear status bits during the break state.

22.4.2 CPU During Break Interrupts

The CPU starts a break interrupt by:

- Loading the instruction register with the SWI instruction
- Loading the program counter with $FFFC and $FFFD ($FEFC and $FEFD in monitor mode)

The break interrupt begins after completion of the CPU instruction in progress. If the break address register match occurs on the last cycle of a CPU instruction, the break interrupt begins immediately.

22.4.3 TIM1 and TIM2 During Break Interrupts

A break interrupt stops the timer counters.

22.4.4 COP During Break Interrupts

The COP is disabled during a break interrupt when V_{TST} is present on the $\overline{RST}$ pin.

22.5 Low-Power Modes

The WAIT and STOP instructions put the MCU in low power-consumption standby modes.

22.5.1 Wait Mode

If enabled, the break module is active in wait mode. In the break routine, the user can subtract one from the return address on the stack if SBSW is set (see **Section 9. System Integration Module (SIM)**). Clear the SBSW bit by writing logic 0 to it.

BRKA — Break Active Bit

This read/write status and control bit is set when a break address match occurs. Writing a logic 1 to BRKA generates a break interrupt. Clear BRKA by writing a logic 0 to it before exiting the break routine. Reset clears the BRKA bit.

1 = (When read) Break address match

0 = (When read) No break address match

22.6.2 Break Address Registers

The break address registers (BRKH and BRKL) contain the high and low bytes of the desired breakpoint address. Reset clears the break address registers.

Address: $FE0C

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
Reset:	0	0	0	0	0	0	0	0

Figure 22-4. Break Address Register High (BRKH)

Address: $FE0D

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
Reset:	0	0	0	0	0	0	0	0

Figure 22-5. Break Address Register Low (BRKL)

22.6.3 SIM Break Status Register

The SIM break status register (SBSR) contains a flag to indicate that a break caused an exit from wait mode. The flag is useful in applications requiring a return to wait mode after exiting from a break interrupt.

23.10 5.0V Oscillator Characteristics

Table 23-8. 5.0V Oscillator Specifications

Characteristic	Symbol	Min	Typ	Max	Unit
Internal oscillator clock frequency	f_{ICLK}	46k	47k(1)	48k	Hz
External reference clock to OSC1(2)	f_{OSC}	dc	—	20M	Hz
Crystal reference frequency(3)	f_{XCLK}		32.768k	4.9152M	Hz
Crystal load capacitance(4)	C_L	—	—	—	
Crystal fixed capacitance	C_1	—	$2 \times C_L$ (25p)	—	F
Crystal tuning capacitance	C_2	—	$2 \times C_L$ (25p)	—	F
Feedback bias resistor	R_B	—	10M	—	Ω
Series resistor(5)	R_S	—	100k	—	Ω

Notes:
1. Typical value reflect average measurements at midpoint of voltage range, 25 °C only.
2. No more than 10% duty cycle deviation from 50%.
3. Fundamental mode crystals only.
4. Consult crystal manufacturer's data.
5. Not Required for high frequency crystals.

23.11 3.3V Oscillator Characteristics

Table 23-9. 3.3V Oscillator Specifications

Characteristic	Symbol	Min	Typ	Max	Unit
Internal oscillator clock frequency	f_{ICLK}	42.8k	43.4k(1)	44k	Hz
External reference clock to OSC1(2)	f_{OSC}	dc	—	16M	Hz
Crystal reference frequency(3)	f_{XCLK}		32.768k	4.9152M	Hz
Crystal load capacitance(4)	C_L	—	—	—	
Crystal fixed capacitance	C_1	—	$2 \times C_L$ (25p)	—	F
Crystal tuning capacitance	C_2	—	$2 \times C_L$ (25p)	—	F
Feedback bias resistor	R_B	—	10M	—	Ω
Series resistor(5)	R_S	—	100k	—	Ω

Notes:
1. Typical value reflect average measurements at midpoint of voltage range, 25 °C only.
2. No more than 10% duty cycle deviation from 50%.
3. Fundamental mode crystals only.
4. Consult crystal manufacturer's data.
5. Not Required for high frequency crystals.