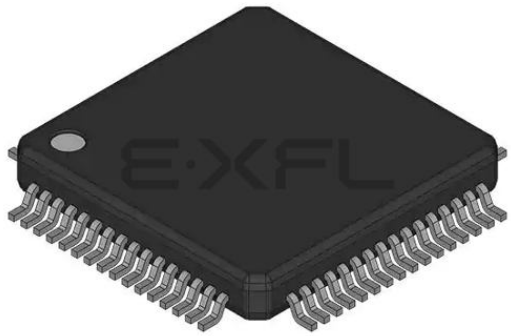

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Product Status	Active
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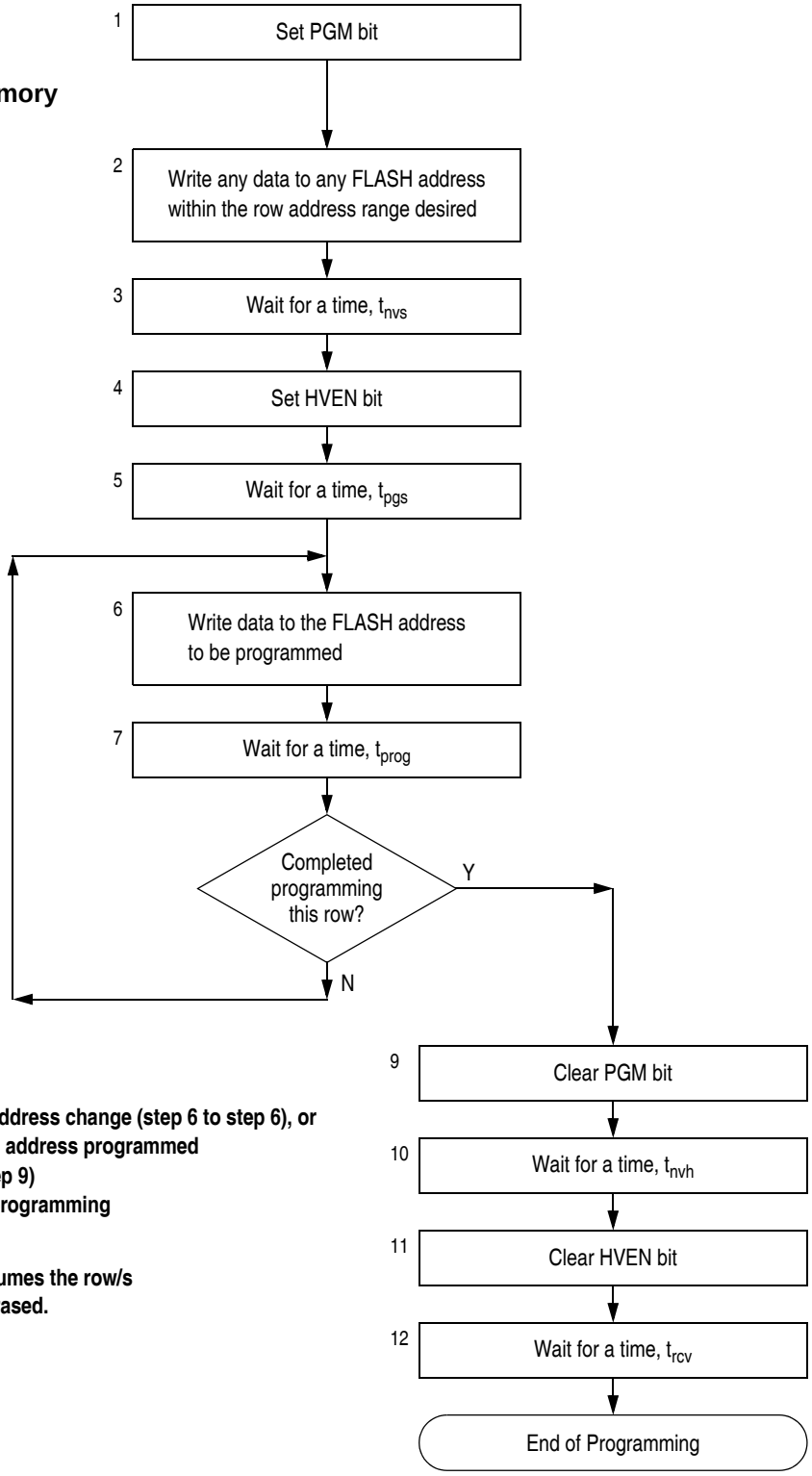
Number of I/O	32
Program Memory Size	12KB (12K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcl908lj12cpbe

Algorithm for programming a row (64 bytes) of FLASH memory



NOTE:

The time between each FLASH address change (step 6 to step 6), or the time between the last FLASH address programmed to clearing PGM bit (step 6 to step 9) must not exceed the maximum programming time, t_{PROG} max.

This row program algorithm assumes the row/s to be programmed are initially erased.

Figure 4-3. FLASH Programming Flowchart

5.4 Configuration Register 1 (CONFIG1)

Address: $001F

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	COPRS	LVISTOP	LVIRSTD	LVIPWRD	0	SSREC	STOP	COPD
Write:								
Reset:	0	0	0	1	0	0	0	0

= Unimplemented

Figure 5-2. Configuration Register 1 (CONFIG1)

COPRS — COP Rate Select

COPRS selects the COP time-out period. Reset clears COPRS. (See **Section 20. Computer Operating Properly (COP)**.)

1 = COP time out period = $2^{13} – 2^4$ ICLK cycles
0 = COP time out period = $2^{18} – 2^4$ ICLK cycles

LVISTOP — LVI Enable in Stop Mode

When the LVIPWRD bit is clear, setting the LVISTOP bit enables the LVI to operate during stop mode. Reset clears LVISTOP. (See **Section 21. Low-Voltage Inhibit (LVI)**.)

1 = LVI enabled during stop mode
0 = LVI disabled during stop mode

LVIRSTD — LVI Reset Disable

LVIRSTD disables the reset signal from the LVI module. (See **Section 21. Low-Voltage Inhibit (LVI)**.)

1 = LVI module resets disabled
0 = LVI module resets enabled

LVIPWRD — LVI Power Disable Bit

LVIPWRD disables the LVI module. (See **Section 21. Low-Voltage Inhibit (LVI)**.) Reset sets LVIPWRD.

1 = LVI module power disabled
0 = LVI module power enabled

Table 6-1. Instruction Set Summary (Sheet 3 of 8)

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Cycles
			V	H	I	N	Z	C				
BRCLR *n*,*opr*,*rel*	Branch if Bit *n* in M Clear	PC ← (PC) + 3 + *rel* ? (Mn) = 0	–	–	–	–	–	↕	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	01 03 05 07 09 0B 0D 0F	dd rr dd rr dd rr dd rr dd rr dd rr dd rr dd rr	5 5 5 5 5 5 5 5
BRN *rel*	Branch Never	PC ← (PC) + 2	–	–	–	–	–	–	REL	21	rr	3
BRSET *n*,*opr*,*rel*	Branch if Bit *n* in M Set	PC ← (PC) + 3 + *rel* ? (Mn) = 1	–	–	–	–	–	↕	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	00 02 04 06 08 0A 0C 0E	dd rr dd rr dd rr dd rr dd rr dd rr dd rr dd rr	5 5 5 5 5 5 5 5
BSET *n*,*opr*	Set Bit *n* in M	Mn ← 1	–	–	–	–	–	–	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	10 12 14 16 18 1A 1C 1E	dd dd dd dd dd dd dd dd	4 4 4 4 4 4 4 4
BSR *rel*	Branch to Subroutine	PC ← (PC) + 2; push (PCL) SP ← (SP) – 1; push (PCH) SP ← (SP) – 1 PC ← (PC) + *rel*	–	–	–	–	–	–	REL	AD	rr	4
CBEQ *opr*,*rel* CBEQA #*opr*,*rel* CBEQX #*opr*,*rel* CBEQ *opr*,X+,*rel* CBEQ X+,*rel* CBEQ *opr*,SP,*rel*	Compare and Branch if Equal	PC ← (PC) + 3 + rel ? (A) – (M) = $00 PC ← (PC) + 3 + rel ? (A) – (M) = $00 PC ← (PC) + 3 + rel ? (X) – (M) = $00 PC ← (PC) + 3 + rel ? (A) – (M) = $00 PC ← (PC) + 2 + rel ? (A) – (M) = $00 PC ← (PC) + 4 + rel ? (A) – (M) = $00	–	–	–	–	–	–	DIR IMM IMM IX1+ IX+ SP1	31 41 51 61 71 9E61	dd rr ii rr ii rr ff rr rr ff rr	5 4 4 5 4 6
CLC	Clear Carry Bit	C ← 0	–	–	–	–	–	0	INH	98		1
CLI	Clear Interrupt Mask	I ← 0	–	–	0	–	–	–	INH	9A		2
CLR *opr* CLRA CLRX CLRH CLR *opr*,X CLR ,X CLR *opr*,SP	Clear	M ← $00 A ← $00 X ← $00 H ← $00 M ← $00 M ← $00 M ← $00	0	–	–	0	1	–	DIR INH INH INH IX1 IX SP1	3F 4F 5F 8C 6F 7F 9E6F	dd ff ff	3 1 1 1 3 2 4

Table 6-1. Instruction Set Summary (Sheet 5 of 8)

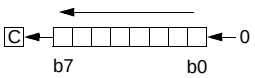
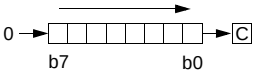
Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Cycles
			V	H	I	N	Z	C				
INC *opr* INCA INCX INC *opr*,X INC ,X INC *opr*,SP	Increment	M ← (M) + 1 A ← (A) + 1 X ← (X) + 1 M ← (M) + 1 M ← (M) + 1 M ← (M) + 1	↕	–	–	↕	↕	–	DIR INH INH IX1 IX SP1	3C 4C 5C 6C 7C 9E6C	dd ff ff	4 1 1 4 3 5
JMP *opr* JMP *opr* JMP *opr*,X JMP *opr*,X JMP ,X	Jump	PC ← Jump Address	–	–	–	–	–	–	DIR EXT IX2 IX1 IX	BC CC DC EC FC	dd hh ll ee ff ff 	2 3 4 3 2
JSR *opr* JSR *opr* JSR *opr*,X JSR *opr*,X JSR ,X	Jump to Subroutine	PC ← (PC) + *n* (*n* = 1, 2, or 3) Push (PCL); SP ← (SP) – 1 Push (PCH); SP ← (SP) – 1 PC ← Unconditional Address	–	–	–	–	–	–	DIR EXT IX2 IX1 IX	BD CD DD ED FD	dd hh ll ee ff ff 	4 5 6 5 4
LDA #*opr* LDA *opr* LDA *opr* LDA *opr*,X LDA *opr*,X LDA ,X LDA *opr*,SP LDA *opr*,SP	Load A from M	A ← (M)	0	–	–	↕	↕	–	IMM DIR EXT IX2 IX1 IX SP1 SP2	A6 B6 C6 D6 E6 F6 9EE6 9ED6	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5
LDHX #*opr* LDHX *opr*	Load H:X from M	H:X ← (M:M + 1)	0	–	–	↕	↕	–	IMM DIR	45 55	ii jj dd	3 4
LDX #*opr* LDX *opr* LDX *opr* LDX *opr*,X LDX *opr*,X LDX ,X LDX *opr*,SP LDX *opr*,SP	Load X from M	X ← (M)	0	–	–	↕	↕	–	IMM DIR EXT IX2 IX1 IX SP1 SP2	AE BE CE DE EE FE 9EEE 9EDE	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5
LSL *opr* LSLA LSLX LSL *opr*,X (Same as ASL) LSL ,X LSL *opr*,SP	Logical Shift Left		↕	–	–	↕	↕	↕	DIR INH INH IX1 IX SP1	38 48 58 68 78 9E68	dd ff ff	4 1 1 4 3 5
LSR *opr* LSRA LSR*X* LSR *opr*,X LSR ,X LSR *opr*,SP	Logical Shift Right		↕	–	–	0	↕	↕	DIR INH INH IX1 IX SP1	34 44 54 64 74 9E64	dd ff ff	4 1 1 4 3 5

Table 9-3. Vector Addresses

Priority	INT Flag	Address	Vector
Lowest	IF17	$FFDA	Real Time Clock Vector (High)
		$FFDB	Real Time Clock Vector (Low)
	IF16	$FFDC	ADC Conversion Complete Vector (High)
		$FFDD	ADC Conversion Complete Vector (Low)
	IF15	$FFDE	Keyboard Vector (High)
		$FFDF	Keyboard Vector (Low)
	IF14	$FFE0	SCI Transmit Vector (High)
		$FFE1	SCI Transmit Vector (Low)
	IF13	$FFE2	SCI Receive Vector (High)
		$FFE3	SCI Receive Vector (Low)
	IF12	$FFE4	SCI Error Vector (High)
		$FFE5	SCI Error Vector (Low)
	IF11	$FFE6	SPI Receive Vector (High)
		$FFE7	SPI Receive Vector (Low)
	IF10	$FFE8	SPI Transmit Vector (High)
		$FFE9	SPI Transmit Vector (Low)
	IF9	$FFEA	TIM2 Overflow Vector (High)
		$FFEB	TIM2 Overflow Vector (Low)
	IF8	$FFEC	TIM2 Channel 1 Vector (High)
		$FFED	TIM2 Channel 1 Vector (Low)
	IF7	$FFEE	TIM2 Channel 0 Vector (High)
		$FFEF	TIM2 Channel 0 Vector (Low)
	IF6	$FFF0	TIM1 Overflow Vector (High)
		$FFF1	TIM1 Overflow Vector (Low)
	IF5	$FFF2	TIM1 Channel 1 Vector (High)
		$FFF3	TIM1 Channel 1 Vector (Low)
	IF4	$FFF4	TIM1 Channel 0 Vector (High)
		$FFF5	TIM1 Channel 0 Vector (Low)
	IF3	$FFF6	PLL Vector (High)
		$FFF7	PLL Vector (Low)
	IF2	$FFF8	LVI Vector (High)
		$FFF9	LVI Vector (Low)
	IF1	$FFFA	$\overline{\text{IRQ}}$ Vector (High)
		$FFFB	$\overline{\text{IRQ}}$ Vector (Low)
	—	$FFFC	SWI Vector (High)
		$FFFD	SWI Vector (Low)
Highest	—	$FFFE	Reset Vector (High)
		$FFFF	Reset Vector (Low)

9.8.3 SIM Break Flag Control Register

The SIM break control register contains a bit that enables software to clear status bits while the MCU is in a break state.

Address: $FE03

	Bit 7	6	5	4	3	2	1	Bit 0
Read: / Write:	BCFE	R	R	R	R	R	R	R
Reset:	0							

R = Reserved

Figure 9-22. SIM Break Flag Control Register (SBFCR)

BCFE — Break Clear Flag Enable Bit

This read/write bit enables software to clear status bits by accessing status registers while the MCU is in a break state. To clear status bits during the break state, the BCFE bit must be set.

1 = Status bits clearable during break

0 = Status bits not clearable during break

10.4.1 Entering Monitor Mode

Table 10-1 shows the pin conditions for entering monitor mode. As specified in the table, monitor mode may be entered after a POR and will allow communication at 9600 baud provided one of the following sets of conditions is met:

1. If $FFFE and $FFFF do not contain $FF (programmed state):
   - The external clock is 4.9152 MHz with PTC1 low or 9.8304 MHz with PTC1 high
   - $\overline{IRQ} = V_{TST}$ (PLL off)
2. If $FFFE and $FFFF both contain $FF (erased state):
   - The external clock is 9.8304 MHz
   - $\overline{IRQ} = V_{DD}$ (this can be implemented through the internal $\overline{IRQ}$ pullup; PLL off)
3. If $FFFE and $FFFF both contain $FF (erased state):
   - The external clock is 32.768 kHz (crystal)
   - $\overline{IRQ} = V_{SS}$ (this setting initiates the PLL to boost the external 32.768 kHz to an internal bus frequency of 2.4576 MHz)

If V_{TST} is applied to $\overline{IRQ}$ and PTC1 is low upon monitor mode entry (above condition set 1), the bus frequency is a divide-by-two of the input clock. If PTC1 is high with V_{TST} applied to $\overline{IRQ}$ upon monitor mode entry, the bus frequency will be a divide-by-four of the input clock. Holding the PTC1 pin low when entering monitor mode causes a bypass of a divide-by-two stage at the oscillator only if V_{TST} is applied to $\overline{IRQ}$. In this event, the CGMOUT frequency is equal to the CGMXCLK frequency, and the OSC1 input directly generates internal bus clocks. In this case, the OSC1 signal must have a 50% duty cycle at maximum bus frequency.

If entering monitor mode without high voltage on $\overline{IRQ}$ (above condition set 2 or 3, where applied voltage is either V_{DD} or V_{SS}), then all port A pin requirements and conditions, including the PTC1 frequency divisor selection, are not in effect. This is to reduce circuit requirements when performing in-circuit programming.

10.6.7 EE_WRITE

EE_WRITE is used to write a set of data from the data array to FLASH.

Table 10-17. EE_WRITE Routine

Routine Name	EE_WRITE
Routine Description	Emulated EEPROM write. Data size ranges from 2 to 15 bytes at a time.
Calling Address	$FC00
Stack Used	17 bytes
Data Block Format	Bus speed (BUS_SPD) Data size (DATASIZE)(1) Starting address (ADDRH)(2) Starting address (ADDRL)(1) Data 1 : Data N

Notes:
1. The minimum data size is 2 bytes. The maximum data size is 15 bytes.
2. The start address must be a page boundary start address, e.g. $xx00 or $xx80.

The start location of the FLASH to be programmed is specified by the address ADDRH:ADDRL and the number of bytes in the data array is specified by DATASIZE. The minimum number of bytes that can be programmed in one routine call is 2 bytes, the maximum is 15 bytes. ADDRH:ADDRL must always be the start of boundary address (the page start address: $XX00 or $0080) and DATASIZE must be the same size when accessing the same page.

In some applications, the user may want to repeatedly store and read a set of data from an area of non-volatile memory. This is easily possible when using an EEPROM array. As the write and erase operations can be executed on a byte basis. For FLASH memory, the minimum erase size is the page — 128 bytes per page for MC68HC908LJ12. If the data array size is less than the page size, writing and erasing to the same page cannot fully utilize the page. Unused locations in the page will be wasted. The EE_WRITE routine is designed to emulate the properties similar to the EEPROM. Allowing a more efficient use of the FLASH page for data storage.

12.6.7 Hour Register (HRR)

This read/write register contains the current value of the hour counter. This register can be read at any time without affecting the counter count. Writing to this register loads the value to the hour counter and the counter continues to count from this new value.

The hour counter rolls over to 0 ($00) after reaching 23 ($17). Writing a value other than 0 to 23 to this register has no effect.

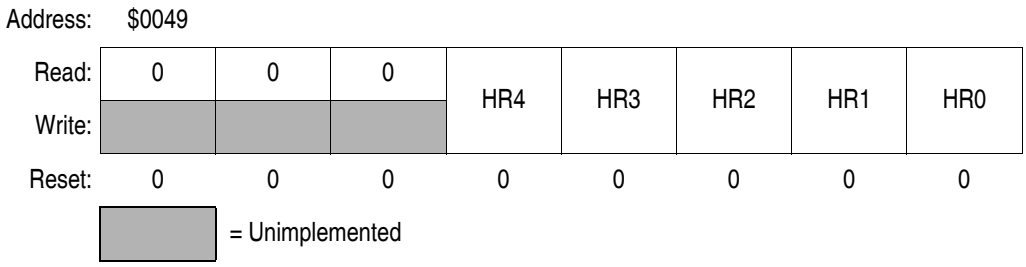


Figure 12-10. Hour Register (HRR)

12.6.8 Day Register (DAYR)

This read/write register contains the current value of the day-of-month counter. This register can be read at any time without affecting the counter count. Writing to this register loads the value to the day counter and the counter continues to count from this new value.

The day counter rolls over to 1 ($01) after reaching 28 ($1B), 29 ($1C), 30 ($1D), or 31 ($1E), depending on the value in the month and year registers. Writing a value that is not valid for the month and year to this register has no effect.

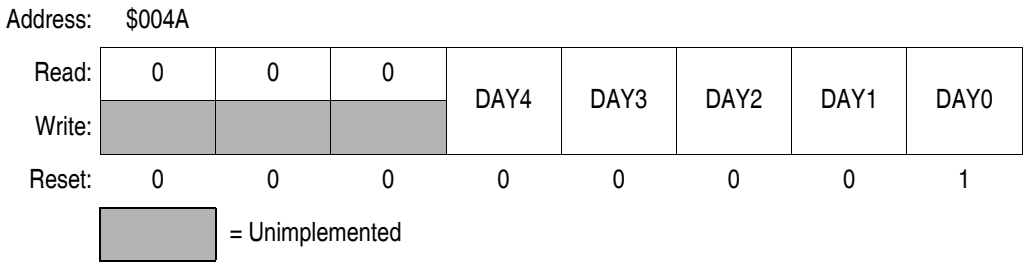


Figure 12-11. Day Register (DAYR)

To locate the start bit, data recovery logic does an asynchronous search for a logic 0 preceded by three logic 1s. When the falling edge of a possible start bit occurs, the RT clock begins to count to 16.

To verify the start bit and to detect noise, data recovery logic takes samples at RT3, RT5, and RT7. **Table 13-2** summarizes the results of the start bit verification samples.

Table 13-2. Start Bit Verification

RT3, RT5, and RT7 Samples	Start Bit Verification	Noise Flag
000	Yes	0
001	Yes	1
010	Yes	1
011	No	0
100	Yes	1
101	No	0
110	No	0
111	No	0

If start bit verification is not successful, the RT clock is reset and a new search for a start bit begins.

To determine the value of a data bit and to detect noise, recovery logic takes samples at RT8, RT9, and RT10. **Table 13-3** summarizes the results of the data bit samples.

Table 13-3. Data Bit Recovery

RT8, RT9, and RT10 Samples	Data Bit Determination	Noise Flag
000	0	0
001	0	1
010	0	1
011	1	1
100	0	1
101	1	1
110	1	1
111	1	0

13.11.5 SCI Status Register 2 (SCS2)

SCI status register 2 contains flags to signal the following conditions:

- Break character detected
- Incoming data

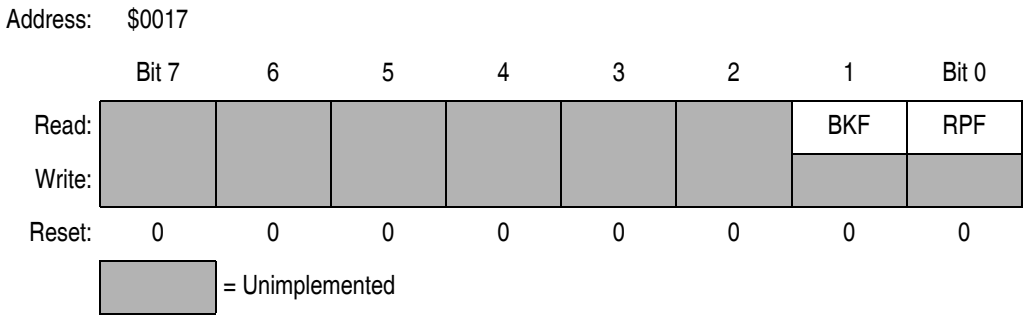


Figure 13-17. SCI Status Register 2 (SCS2)

BKF — Break Flag Bit

This clearable, read-only bit is set when the SCI detects a break character on the RxD pin. In SCS1, the FE and SCRF bits are also set. In 9-bit character transmissions, the R8 bit in SCC3 is cleared. BKF does not generate a CPU interrupt request. Clear BKF by reading SCS2 with BKF set and then reading the SCDR. Once cleared, BKF can become set again only after logic 1s again appear on the RxD pin followed by another break character. Reset clears the BKF bit.

1 = Break character detected
0 = No break character detected

RPF — Reception in Progress Flag Bit

This read-only bit is set when the receiver detects a logic 0 during the RT1 time period of the start bit search. RPF does not generate an interrupt request. RPF is reset after the receiver detects false start bits (usually from noise or a baud rate mismatch) or when the receiver detects an idle character. Polling RPF before disabling the SCI module or entering stop mode can show whether a reception is in progress.

1 = Reception in progress
0 = No reception in progress

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$003C	ADC Status and Control Register (ADSCR)	Read:	COCO	AIEN	ADCO	ADCH4	ADCH3	ADCH2	ADCH1	ADCH0
		Write:								
		Reset:	0	0	0	1	1	1	1	1
$003D	ADC Data Register High (ADRH)	Read:	ADx	ADx	ADx	ADx	ADx	ADx	ADx	ADx
		Write:	R	R	R	R	R	R	R	R
		Reset:	0	0	0	0	0	0	0	0
$003E	ADC Data Register Low (ADRL)	Read:	ADx	ADx	ADx	ADx	ADx	ADx	ADx	ADx
		Write:	R	R	R	R	R	R	R	R
		Reset:	0	0	0	0	0	0	0	0
$003F	ADC Clock Register (ADCLK)	Read:	ADIV2	ADIV1	ADIV0	ADICLK	MODE1	MODE0	0	0
		Write:								R
		Reset:	0	0	0	0	0	1	0	0

= Unimplemented R = Reserved

Figure 15-1. ADC I/O Register Summary

15.4 Functional Description

The ADC provides six pins for sampling external sources at pins PTA4/ADC0–PTA7/ADC3 and PTB6/ADC4–PTB7/ADC5. An analog multiplexer allows the single ADC converter to select one of nine ADC channels as ADC voltage in (V_{ADIN}). V_{ADIN} is converted by the successive approximation register-based analog-to-digital converter. When the conversion is completed, ADC places the result in the ADC data register, high and low byte (ADRH and ADRL), and sets a flag or generates an interrupt.

Figure 15-2 shows the structure of the ADC module.

15.4.1 ADC Port I/O Pins

PTA4–PTA7 and PTB6–PTB7 are general-purpose I/O pins that are shared with the ADC channels. The channel select bits, ADCH[4:0], define which ADC channel/port pin will be used as the input signal. The ADC overrides the port I/O logic by forcing that pin as input to the ADC. The remaining ADC channels/port pins are controlled by the port I/O

15.8.2 ADC Data Register

The ADC data register consist of a pair of 8-bit registers: high byte (ADRH), and low byte (ADRL). This pair form a 16-bit register to store the 10-bit ADC result for the selected ADC result justification mode.

In 8-bit truncated mode, the ADRL holds the eight most significant bits (MSBs) of the 10-bit result. The ADRL is updated each time an ADC conversion completes. In 8-bit truncated mode, ADRL contains no interlocking with ADRH. (See **Figure 15-5 . ADRH and ADRL in 8-Bit Truncated Mode**.)

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$003D	ADC Data Register High (ADRH)	Read:	0	0	0	0	0	0	0	0
		Write:	R	R	R	R	R	R	R	R
		Reset:	0	0	0	0	0	0	0	0
$003E	ADC Data Register Low (ADRL)	Read:	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2
		Write:	R	R	R	R	R	R	R	R
		Reset:	0	0	0	0	0	0	0	0

Figure 15-5. ADRH and ADRL in 8-Bit Truncated Mode

In right justified mode the ADRH holds the two MSBs, and the ADRL holds the eight least significant bits (LSBs), of the 10-bit result. ADRH and ADRL are updated each time a single channel ADC conversion completes. Reading ADRH latches the contents of ADRL. Until ADRL is read all subsequent ADC results will be lost.
(See **Figure 15-6 . ADRH and ADRL in Right Justified Mode**.)

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$003D	ADC Data Register High (ADRH)	Read:	0	0	0	0	0	0	AD9	AD8
		Write:	R	R	R	R	R	R	R	R
		Reset:	0	0	0	0	0	0	0	0
$003E	ADC Data Register Low (ADRL)	Read:	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
		Write:	R	R	R	R	R	R	R	R
		Reset:	0	0	0	0	0	0	0	0

Figure 15-6. ADRH and ADRL in Right Justified Mode

If the external clock (CGMXCLK) is equal to or greater than 1MHz, CGMXCLK can be used as the clock source for the ADC. If CGMXCLK is less than 1MHz, use the PLL-generated bus clock as the clock source. As long as the internal ADC clock is at f_{ADIC}, correct operation can be guaranteed.

1 = Internal bus clock

0 = External clock, CGMXCLK

$$f_{ADIC} = \frac{\text{CGMXCLK or bus frequency}}{\text{ADIV[2:0]}}$$

MODE1 and MODE0 — Modes of Result Justification

MODE1 and MODE0 selects between four modes of operation. The manner in which the ADC conversion results will be placed in the ADC data registers is controlled by these modes of operation. Reset returns right-justified mode.

Table 15-3. ADC Mode Select

MODE1	MODE0	ADC Clock Rate
0	0	8-bit truncated mode
0	1	Right justified mode
1	0	Left justified mode
1	1	Left justified sign data mode

16.9.2 LCD Clock Register (LCDCLK)

The LCD clock register (LCDCLK):

- Selects the fast charge duty cycle
- Selects LCD driver duty cycle
- Selects LCD waveform base clock

Address: $004F

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	FCCTL1	FCCTL0	DUTY1	DUTY0	LCLK2	LCLK1	LCLK0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 16-17. LCD Clock Register (LCDCLK)

FCCTL[1:0] — Fast Charge Duty Cycle Select

These read/write bits select the duty cycle of the fast charge duration. Reset clears these bits. (See **16.5.4 Fast Charge and Low Current**)

Table 16-4. Fast Charge Duty Cycle Selection

FCCTL1:FCCTL0	Fast Charge Duty Cycle
00	In each LCDCLK/2 period, each bias resistor is reduced to 37 kΩ for a duration of LCDCLK/32.
01	In each LCDCLK/2 period, each bias resistor is reduced to 37 kΩ for a duration of LCDCLK/64.
10	In each LCDCLK/2 period, each bias resistor is reduced to 37 kΩ for a duration of LCDCLK/128.
11	Not used

ADC[3:0] — ADC channels 3 to 0

ADC[3:0] are pins used for the input channels to the analog-to-digital converter module. The channel select bits, ADCH[4:0], in the ADC status and control register define which port pin will be used as an ADC input and overrides any control from the port I/O logic. See **Section 15. Analog-to-Digital Converter (ADC)**.

NOTE: *Care must be taken when reading port A while applying analog voltages to ADC[3:0] pins. If the appropriate ADC channel is not enabled, excessive current drain may occur if analog voltages are applied to the PTAx/ADCx pin, while PTA is read as a digital input. Those ports not selected as analog input channels are considered digital I/O ports.*

17.3.2 Data Direction Register A (DDRA)

Data direction register A determines whether each port A pin is an input or an output. Writing a logic 1 to a DDRA bit enables the output buffer for the corresponding port A pin; a logic 0 disables the output buffer.

Address: $0004

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDRA7	DDRA6	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0
Reset:	0	0	0	0	0	0	0	0

Figure 17-3. Data Direction Register A (DDRA)

DDRA[7:0] — Data Direction Register A Bits

These read/write bits control port A data direction. Reset clears DDRA[7:0], configuring all port A pins as inputs.

1 = Corresponding port A pin configured as output
0 = Corresponding port A pin configured as input

NOTE: *Avoid glitches on port A pins by writing to the port A data register before changing data direction register A bits from 0 to 1. **Figure 17-4** shows the port A I/O logic.*

KBI[7:4] — Keyboard Interrupt Pins

KBI[7:4] are input pins to the keyboard interrupt module. The corresponding control bits, KBIE[7:4], in the keyboard interrupt enable register, KBIER, select which port pins will be used as a keyboard interrupt input and overrides any control from the port I/O logic. See **Section 19. Keyboard Interrupt Module (KBI)**

17.6.2 Data Direction Register D (DDRD)

Data direction register D determines whether each port D pin is an input or an output. Writing a logic 1 to a DDRD bit enables the output buffer for the corresponding port D pin; a logic 0 disables the output buffer.

NOTE: *For those devices packaged in a 52-pin LQFP, PTD0–PTD7 are not connected. DDRD0–DDRD7 should be set to a 1 to configure PTD0–PTD7 as outputs.*

Address: $0007

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDRD7	DDRD6	DDRD5	DDRD4	DDRD3	DDRD2	DDRD1	DDRD0
Reset:	0	0	0	0	0	0	0	0

Figure 17-13. Data Direction Register D (DDRD)

DDRD[7:0] — Data Direction Register D Bits

These read/write bits control port D data direction. Reset clears DDRD[7:0], configuring all port D pins as inputs.

1 = Corresponding port D pin configured as output
0 = Corresponding port D pin configured as input

NOTE: *Avoid glitches on port D pins by writing to the port D data register before changing data direction register D bits from 0 to 1. **Figure 17-14** shows the port D I/O logic.*

22.6.4 SIM Break Flag Control Register

The SIM break flag control register (SBFCR) contains a bit that enables software to clear status bits while the MCU is in a break state.

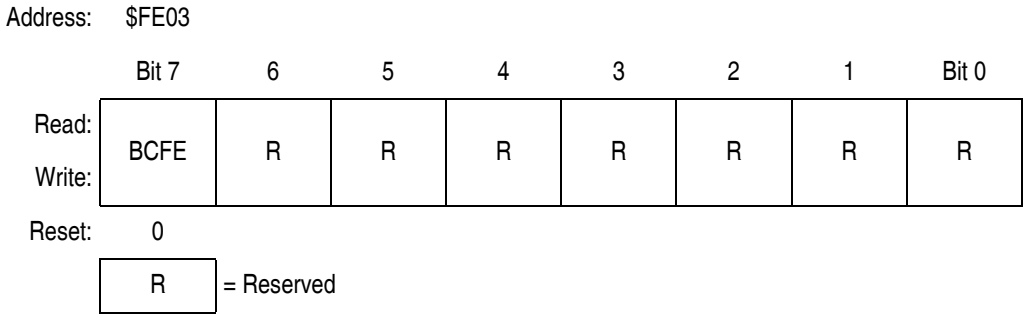


Figure 22-7. SIM Break Flag Control Register (SBFCR)

BCFE — Break Clear Flag Enable Bit

This read/write bit enables software to clear status bits by accessing status registers while the MCU is in a break state. To clear status bits during the break state, the BCFE bit must be set.

1 = Status bits clearable during break

0 = Status bits not clearable during break

23.6 5.0V DC Electrical Characteristics

Table 23-4. 5.0V DC Electrical Characteristics

Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
Output high voltage (I_{LOAD} = –2.0 mA) All ports	V_{OH}	V_{DD}–0.8	—	—	V
Output low voltage (I_{LOAD} = 1.6mA) All ports (I_{LOAD} = 8.0 mA) PTB2–PTB5 (I_{LOAD} = 15.0 mA) PTB0/TxD–PTB1	V_{OL}	—	—	0.4	V
Input high voltage All ports, $\overline{RST}$, $\overline{IRQ}$, OSC1	V_{IH}	0.7 × V_{DD}	—	V_{DD}	V
Input low voltage All ports, $\overline{RST}$, $\overline{IRQ}$, OSC1	V_{IL}	V_{SS}	—	0.3 × V_{DD}	V
V_{DD} supply current Run[3], f_{OP} = 8 MHz with all modules on with ADC on with ADC off Wait[4], f_{OP} = 8 MHz (all modules off) Stop, f_{OP} = 8 kHz[5] 25°C (with OSC, RTC, LCD[6], LVI on) 25°C (with OSC, RTC, LCD[6] on) 25°C (with OSC, RTC on) 25°C (all modules off)	I_{DD}	 — — — — — — — —	 — — — — — — — —	 18 15 12 10 350 50 30 1	 mA mA mA mA µA µA µA µA
Digital I/O ports Hi-Z leakage current All ports, $\overline{RST}$	I_{IL}	—	—	± 10	µA
Input current $\overline{IRQ}$	I_{IN}	—	—	± 1	µA
Capacitance Ports (as input or output)	C_{OUT} C_{IN}	— —	— —	12 8	pF
POR re-arm voltage[7]	V_{POR}	0	—	100	mV
POR rise-time ramp rate[8]	R_{POR}	0.035	—	—	V/ms
Monitor mode entry voltage (at $\overline{IRQ}$ pin)	V_{TST}	1.5 × V_{DD}	—	8	V
Pullup resistors[9] PTA0–PTA3, PTD4–PTD7 configured as KBI0–KBI7 $\overline{RST}$, $\overline{IRQ}$	R_{PU1} R_{PU2}	— —	28 28	— —	kΩ kΩ
Low-voltage inhibit, trip falling voltage	V_{TRIPF}	4.00	4.32	4.70	V
Low-voltage inhibit, trip rising voltage	V_{TRIPR}	4.00	4.32	4.70	V

23.7 3.3V DC Electrical Characteristics

Table 23-5. 3.3V DC Electrical Characteristics

Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
Output high voltage (I_{LOAD} = –1.0 mA) All ports	V_{OH}	V_{DD}–0.4	—	—	V
Output low voltage (I_{LOAD} = 0.8mA) All ports (I_{LOAD} = 4.0 mA) PTB2–PTB5 (I_{LOAD} = 10.0 mA) PTB0/TxD–PTB1	V_{OL}	—	—	0.4	V
Input high voltage All ports, $\overline{RST}$, $\overline{IRQ}$, OSC1	V_{IH}	0.7 × V_{DD}	—	V_{DD}	V
Input low voltage All ports, $\overline{RST}$, $\overline{IRQ}$, OSC1	V_{IL}	V_{SS}	—	0.3 × V_{DD}	V
V_{DD} supply current					
Run[3], f_{OP} = 4 MHz					
with all modules on	I_{DD}	—	—	8	mA
with ADC on		—	—	6	mA
with ADC off		—	—	5	mA
Wait[4], f_{OP} = 4 MHz (all modules off)		—	—	3.5	mA
Stop, f_{OP} = 8 kHz[5]					
25°C (with OSC, RTC, LCD[6], LVI on)		—	—	280	µA
25°C (with OSC, RTC, LCD[6] on)		—	—	38	µA
25°C (with OSC, RTC on)		—	—	25	µA
25°C (all modules off)		—	—	1	µA
Digital I/O ports Hi-Z leakage current All ports, $\overline{RST}$	I_{IL}	—	—	± 10	µA
Input current $\overline{IRQ}$	I_{IN}	—	—	± 1	µA
Capacitance Ports (as input or output)	C_{OUT} C_{IN}	— —	— —	12 8	pF
POR re-arm voltage[7]	V_{POR}	0	—	100	mV
POR rise-time ramp rate[8]	R_{POR}	0.02	—	—	V/ms
Monitor mode entry voltage (at $\overline{IRQ}$ pin)	V_{HI}	1.5 × V_{DD}	—	2 × V_{DD}	V
Pullup resistors[9]					
PTA0–PTA3, PTD4–PTD7 configured as KBI0–KBI7	R_{PU1}	—	26	—	kΩ
$\overline{RST}$, $\overline{IRQ}$	R_{PU2}	—	28	—	kΩ
Low-voltage inhibit, trip falling voltage	V_{TRIPF}	2.40	2.57	2.88	V
Low-voltage inhibit, trip rising voltage	V_{TRIPR}	2.46	2.63	2.97	V