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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	24MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, WDT
Number of I/O	51
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 15x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f351spfm-ge1

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- **Dual operation flash memory (only flash memory devices with A-suffix)**
  - Erase/write and read can be executed in the different bank (Upper Bank/Lower Bank) at the same time.
- **Models that support + 125 °C**
  - Devices without A-suffix (excluding evaluation device) : The maximum operating frequency is 16 MHz (at T_A = +125 °C) .
  - Devices with A-suffix (excluding evaluation device) : The maximum operating frequency is 24 MHz (at T_A = +125 °C) .
- **Flash security function**
  - Protects the content of Flash memory (MB90F352x and MB90F357x only)
- **External bus interface**
  - 4 Mbytes external memory space

* : I^2C license :
Purchase of Fujitsu I^2C components conveys a license under the Philips I^2C Patent Rights to use, these components in an I^2C system provided that the system conforms to the I^2C Standard Specification as defined by Philips.

■ PRODUCT LINEUP 1

Part Number / Parameter	MB90F351, MB90F352	MB90F351S, MB90F352S	MB90F351A, MB90F352A	MB90F351TA, MB90F352TA	MB90F351AS, MB90F352AS	MB90F351TAS, MB90F352TAS
CPU	F^2MC-16LX CPU					
System clock	On-chip PLL clock multiplier (×1, ×2, ×3, ×4, ×6, 1/2 when PLL stops) Minimum instruction execution time : 42 ns (oscillation clock 4 MHz, PLL × 6)					
ROM	Flash memory 64Kbytes : MB90F351(S) 128Kbytes : MB90F352(S)		Dual operation flash memory 64Kbytes : MB90F351A(S), MB90F351TA(S) 128Kbytes : MB90F352A(S), MB90F352TA(S)			
RAM	4 Kbytes					
Emulator-specific power supply*1	—					
Sub clock pin (X0A, X1A) (Max 100 kHz)	Yes	No	Yes		No	
Clock monitor function	No					
Low voltage/CPU operation detection reset	No		No	Yes	No	Yes
Operating voltage range	3.5 V to 5.5 V : at normal operating (not using A/D converter) 4.0 V to 5.5 V : at using A/D converter/Flash programming 4.5 V to 5.5 V : at using external bus					
Operating temperature range	–40 °C to +105 °C (+125 °C up to 16 MHz machine clock)		–40 °C to +125 °C			
Package	LQFP-64					
UART	2 channels					
	Wide range of baud rate settings using a dedicated reload timer Special synchronous options for adapting to different synchronous serial protocols LIN functionality working either as master or slave LIN device					
I^2C (400 Kbps)	1 channel					
A/D Converter	15 channels					
	10-bit or 8-bit resolution Conversion time : Min 3 µs includes sample time (per one channel)					
16-bit Reload Timer (4 channels)	Operation clock frequency : fsys/2^1, fsys/2^3, fsys/2^5 (fsys = Machine clock frequency) Supports External Event Count function.					
16-bit I/O Timer (2 channels)	I/O Timer 0 (clock input FRCK0) corresponds to ICU 0/1. I/O Timer 1 (clock input FRCK1) corresponds to ICU 4/5/6/7, OCU 4/5/6/7.					
	Signals an interrupt when overflowing. Supports Timer Clear when a match with Output Compare (Channel 0, 4) . Operation clock frequency : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4, fsys/2^5, fsys/2^6, fsys/2^7 (fsys = Machine clock frequency)					
16-bit Output Compare	4 channels					
	Signals an interrupt when 16-bit I/O Timer matches with output compare registers. A pair of compare registers can be used to generate an output signal.					

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■ PRODUCT LINEUP 3

Part Number / Parameter	MB90F356A, MB90F357A	MB90F356TA, MB90F357TA	MB90F356AS, MB90F357AS	MB90F356TAS, MB90F357TAS
CPU	F^2MC-16LX CPU			
System clock	On-chip PLL clock multiplier (×1, ×2, ×3, ×4, ×6, 1/2 when PLL stops) Minimum instruction execution time : 42 ns (oscillation clock 4 MHz, PLL × 6)			
ROM	Dual operation flash memory 64Kbytes : MB90F356A(S), MB90F356TA(S) 128Kbytes : MB90F357A(S), MB90F357TA(S)			
RAM	4 Kbytes			
Emulator-specific power supply*1	—			
Sub clock pin (X0A, X1A)	Yes		No (internal CR oscillation can be used as sub clock)	
Clock monitor function	Yes			
Low voltage/CPU operation detection reset	No	Yes	No	Yes
Operating voltage range	3.5 V to 5.5 V : at normal operating (not using A/D converter) 3.5 V to 5.5 V : at using A/D converter/Flash programming 3.5 V to 5.5 V : at using external bus			
Operating temperature range	–40 °C to +125 °C			
Package	LQFP-64			
UART	2 channels			
	Wide range of baud rate settings using a dedicated reload timer Special synchronous options for adapting to different synchronous serial protocols LIN functionality working either as master or slave LIN device			
I^2C (400 Kbps)	1 channel			
A/D Converter	15 channels			
	10-bit or 8-bit resolution Conversion time : Min 3 µs includes sample time (per one channel)			
16-bit Reload Timer (4 channels)	Operation clock frequency : fsys/2^1, fsys/2^3, fsys/2^5 (fsys = Machine clock frequency) Supports External Event Count function.			
16-bit I/O Timer (2 channels)	I/O Timer 0 (clock input FRCK0) corresponds to ICU 0/1. I/O Timer 1 (clock input FRCK1) corresponds to ICU 4/5/6/7, OCU 4/5/6/7.			
	Signals an interrupt when overflowing. Supports Timer Clear when a match with Output Compare (Channel 0, 4) . Operation clock frequency : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4, fsys/2^5, fsys/2^6, fsys/2^7 (fsys = Machine clock frequency)			
16-bit Output Compare	4 channels			
	Signals an interrupt when 16-bit I/O Timer matches with output compare registers. A pair of compare registers can be used to generate an output signal.			

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Parameter \ Part Number	MB90356A, MB90357A	MB90356TA, MB90357TA	MB90356AS, MB90357AS	MB90356TAS, MB90357TAS	MB90V340A-103	MB90V340A-104
16-bit Output Compare	4 channels				8 channels	
	Signals an interrupt when 16-bit I/O Timer matches with output compare registers. A pair of compare registers can be used to generate an output signal.					
16-bit Input Capture	6 channels				8 channels	
	Retains freerun timer value by (rising edge, falling edge or rising & falling edge), signals an interrupt.					
8/16-bit Programmable Pulse Generator	6 channels (16-bit)/10 channels (8-bit) 8-bit reload counters × 12 8-bit reload registers for L pulse width × 12 8-bit reload registers for H pulse width × 12				8 channels (16-bit)/16 channels (8-bit) 8-bit reload counters × 16 8-bit reload registers for L pulse width × 16 8-bit reload registers for H pulse width × 16	
	Supports 8-bit and 16-bit operation modes. A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler + 8-bit reload counter. Operation clock frequency : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4 or 128 µs@fosc = 4 MHz (fsys = Machine clock frequency, fosc = Oscillation clock frequency)					
CAN Interface	1 channel				3 channels	
	Conforms to CAN Specification Version 2.0 Part A and B. Automatic re-transmission in case of error Automatic transmission responding to Remote Frame Prioritized 16 message buffers for data and ID Supports multiple messages. Flexible configuration of acceptance filtering : Full bit compare/Full bit mask/Two partial bit masks Supports up to 1 Mbps.					
External Interrupt	8 channels				16 channels	
	Can be used rising edge, falling edge, starting up by H/L level input, external interrupt, extended intelligent I/O services (EI^{2}OS) and DMA.					
D/A converter	—				2 channels	
I/O Ports	Virtually all external pins can be used as general purpose I/O port. All push-pull outputs Bit-wise settable as input/output or peripheral module signal Settable as CMOS schmitt trigger/ automotive inputs TTL input level settable for external bus (only for external bus pin)					
Flash Memory	—					
Corresponding EVA name	MB90V340A-104		MB90V340A-103		—	

* : It is setting of Jumper switch (TOOL VCC) when Emulator (MB2147-01) is used.
Please refer to the Emulator hardware manual about details.

■ PACKAGES AND PRODUCT CORRESPONDENCE

Package	MB90V340A -101 -102 -103 -104	MB90F351 MB90F351S MB90F352 MB90F352S	MB90F351A (S) , MB90F351TA (S) MB90F352A (S) , MB90F352TA (S) MB90F356A (S) , MB90F356TA (S) MB90F357A (S) , MB90F357TA (S) MB90351A (S) , MB90351TA (S) MB90352A (S) , MB90352TA (S) MB90356A (S) , MB90356TA (S) MB90357A (S) , MB90357TA (S)
PGA-299C-A01	◯	×	×
FPT-64P-M09 (12 mm □, 0.65 mm pitch)	×	◯	×
FPT-64P-M23 (12 mm □, 0.65 mm pitch)	×	×	◯
FPT-64P-M24 (10 mm □, 0.50 mm pitch)	×	×	◯*

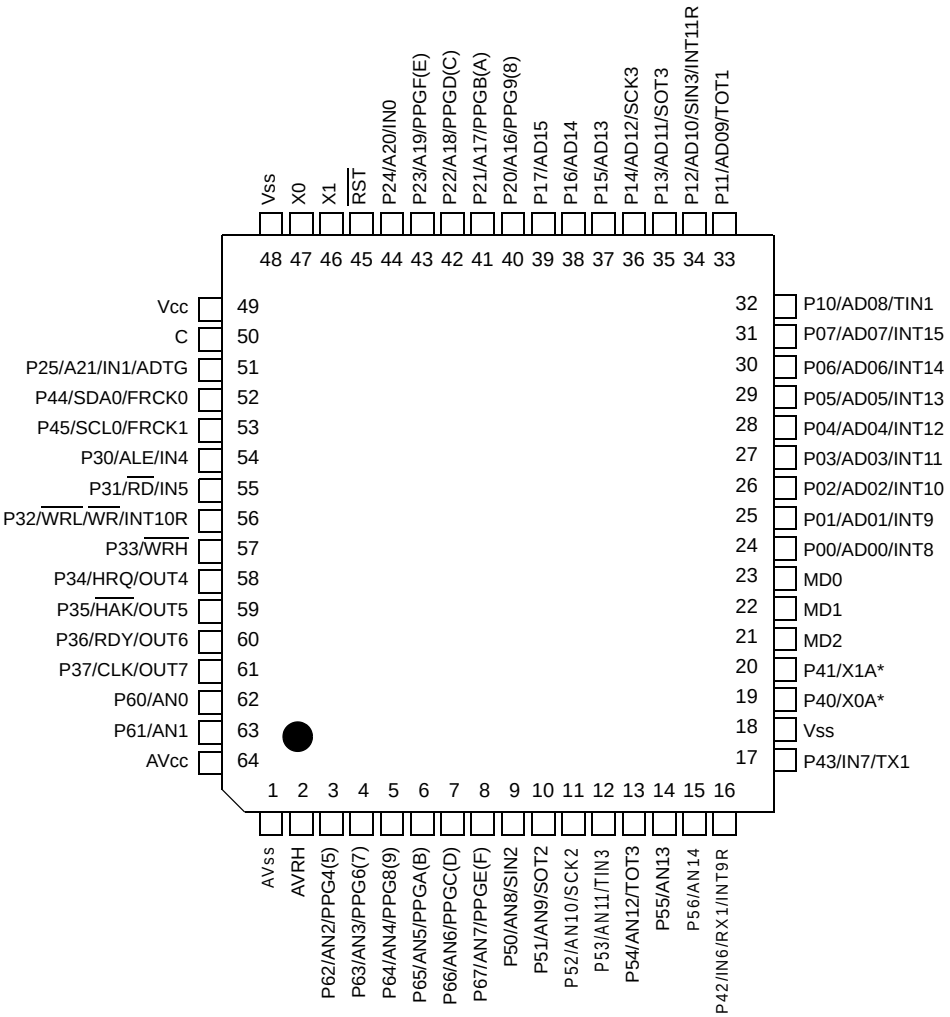
* : This device is under development.
◯ : Yes, × : No

Note : Refer to “■ PACKAGE DIMENSIONS” for detail of each package.

■ PIN ASSIGNMENTS

- MB90F351(S), MB90F352(S),MB90F351A(S), MB90F351TA(S), MB90F352A(S), MB90F352TA(S), MB90F356A(S), MB90F356TA(S), MB90F357A(S), MB90F357TA(S),MB90351A(S), MB90351TA(S), MB90352A(S), MB90352TA(S),MB90356A(S), MB90356TA(S), MB90357A(S), MB90357TA(S),

(TOP VIEW)
(LQFP-64P)



(FPT-64P-M09, FPT-64P-M23, FPT-64P-M24)

* : Devices without S-suffix : X0A, X1A
Devices with S-suffix : P40, P41

Pin No. LQFP64*	Pin name	Circuit type	Function
24 to 31	P00 to P07	G	General purpose I/O ports. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD00 to AD07		Input/output pins of external address data bus lower 8 bits. This function is enabled when the external bus is enabled.
	INT8 to INT15		External interrupt request input pins for INT8 to INT15
32	P10	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD08		Input/output pin for external bus address data bus bit 8. This function is enabled when external bus is enabled.
	TIN1		Event input pin for reload timer1
33	P11	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD09		Input/output pin for external bus address data bus bit 9. This function is enabled when external bus is enabled.
	TOT1		Output pin for reload timer1
34	P12	N	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD10		Input/output pin for external bus address data bus bit 10. This function is enabled when external bus is enabled.
	SIN3		Serial data input pin for UART3
	INT11R		External interrupt request input pin for INT11
35	P13	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD11		Input/output pin for external bus address data bus bit 11. This function is enabled when external bus is enabled.
	SOT3		Serial data output pin for UART3
36	P14	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD12		Input/output pin for external bus address data bus bit 12. This function is enabled when external bus is enabled.
	SCK3		Clock input/output pin for UART3
37	P15	N	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD13		Input/output pin for external bus address data bus bit 13. This function is enabled when external bus is enabled.
38	P16	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD14		Input/output pin for external bus address data bus bit 14. This function is enabled when external bus is enabled.

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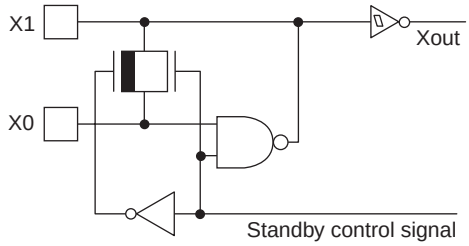
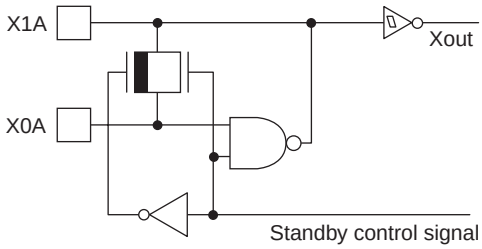
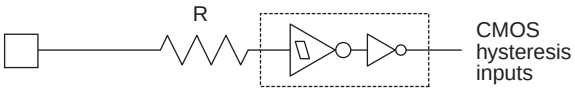
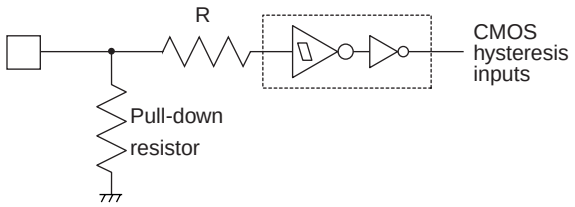
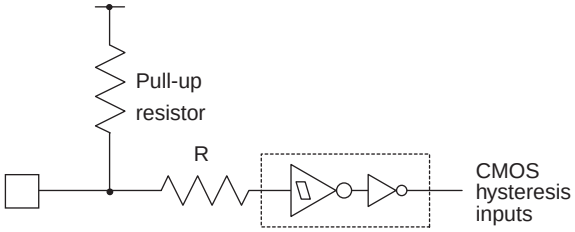
■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		Oscillation circuit • High-speed oscillation feedback resistor = approx. 1 MΩ
B		Oscillation circuit • Low-speed oscillation feedback resistor = approx. 10 MΩ
C		Mask ROM device: • CMOS hysteresis input pin Flash memory device: • CMOS input pin
D		Mask ROM device: • CMOS hysteresis input pin • Pull-down resistor value: approx. 50 kΩ Flash memory device: • CMOS input pin • No Pull-down
E		CMOS hysteresis input pin • Pull-up resistor value: approx. 50 kΩ

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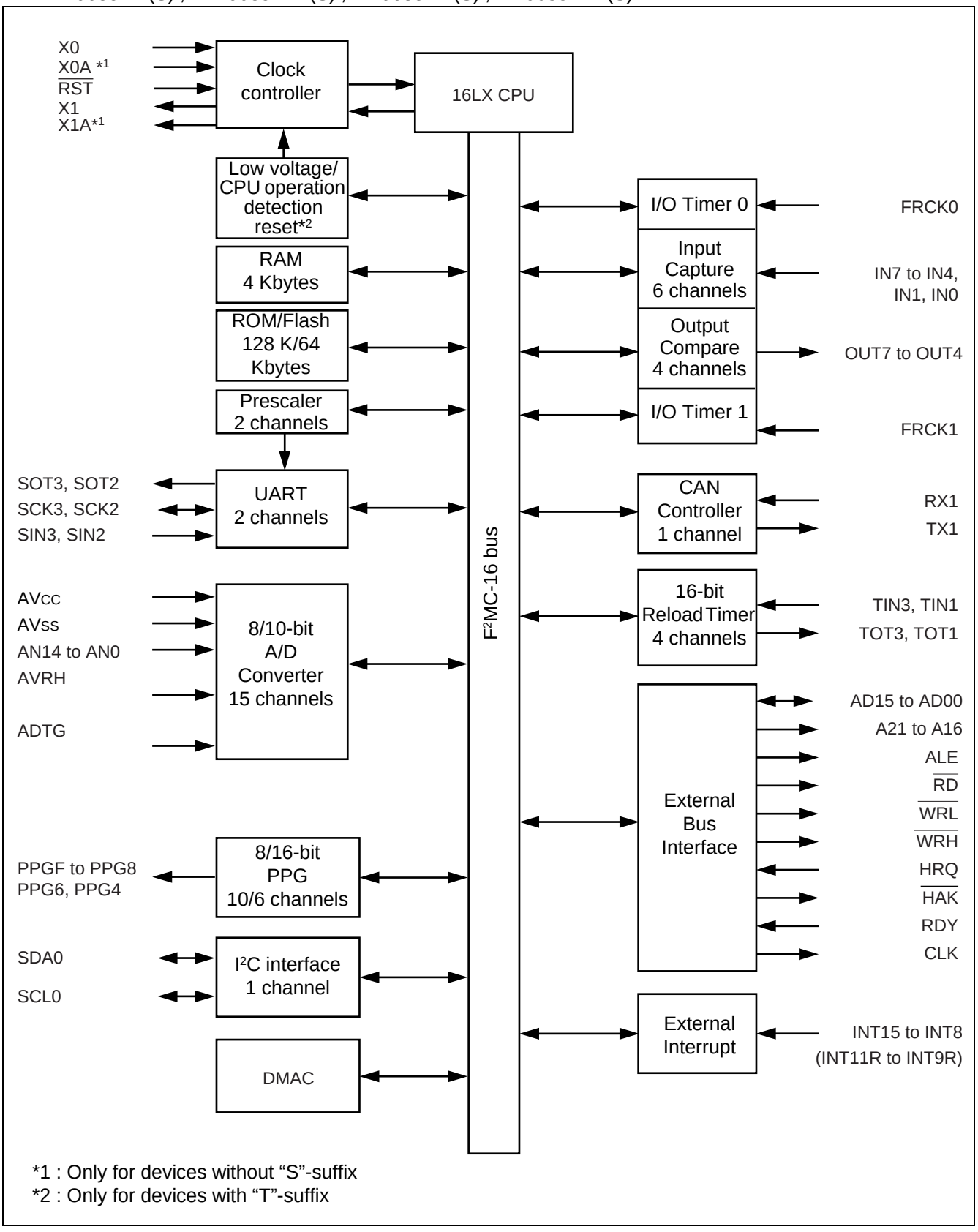
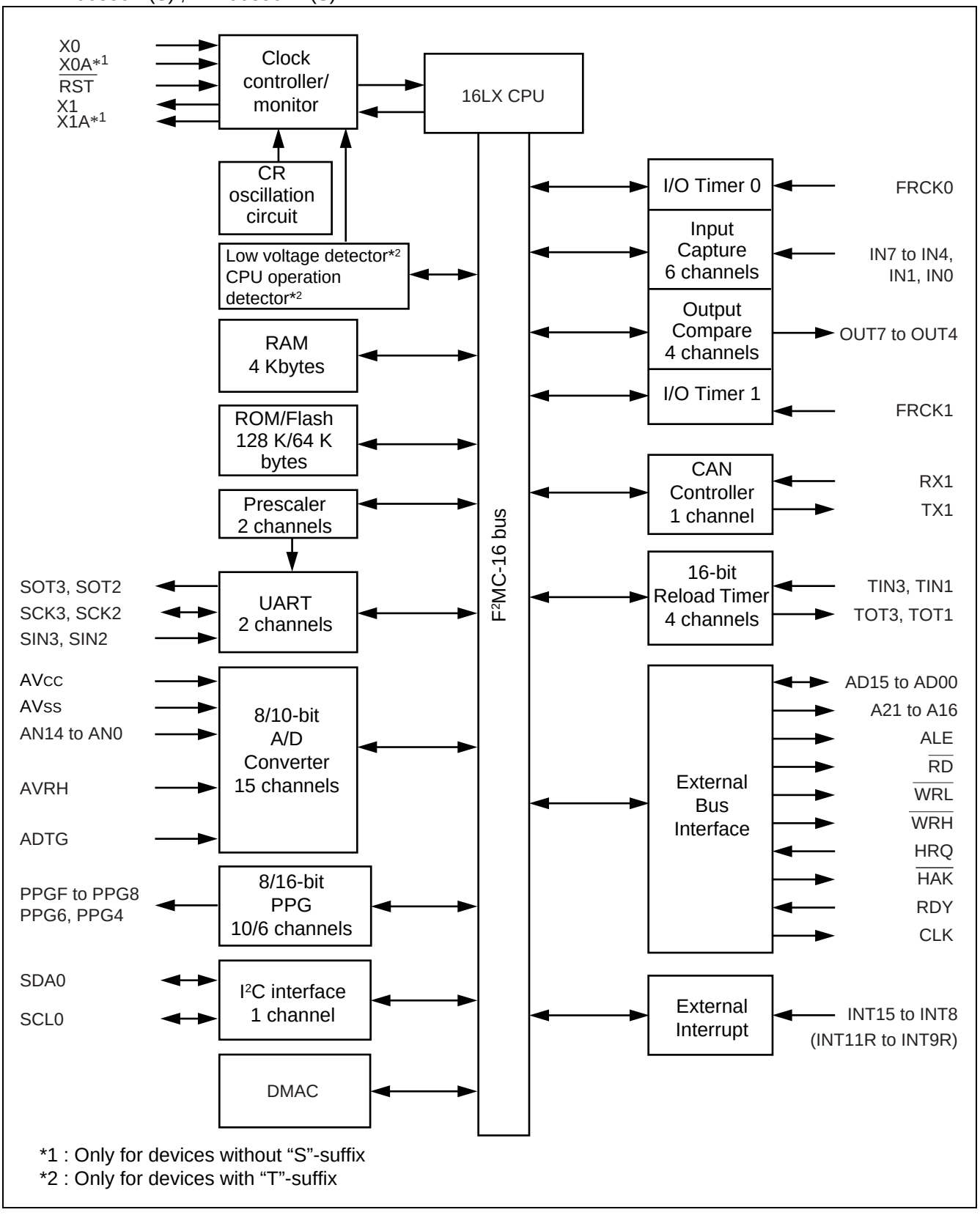
- MB90F352 (S) , MB90F351 (S) , MB90F352A (S) , MB90F352TA (S) , MB90F351A (S) , MB90F351TA (S) , MB90352A (S) , MB90352TA (S) , MB90351A (S) , MB90351TA (S)



*1 : Only for devices without “S”-suffix
*2 : Only for devices with “T”-suffix

- MB90F357A (S) , MB90F357TA (S) , MB90F356A (S) , MB90F356TA (S) , MB90357A (S) , MB90357TA (S) , MB90356A (S) , MB90356TA (S)



*1 : Only for devices without “S”-suffix
*2 : Only for devices with “T”-suffix

Address	Register	Abbreviation	Access	Resource name	Initial value
7950H	Serial Mode Register 3	SMR3	W, R/W	UART3	00000000B
7951H	Serial Control Register 3	SCR3	W, R/W		00000000B
7952H	Reception/Transmission Data Register 3	RDR3/ TDR3	R/W		00000000B
7953H	Serial Status Register 3	SSR3	R,R/W		00001000B
7954H	Extended Communication Control Register 3	ECCR3	R,W, R/W		000000XXB
7955H	Extended Status/Control Register 3	ESCR3	R/W		00000100B
7956H	Baud Rate Generator Register 30	BGR30	R/W		00000000B
7957H	Baud Rate Generator Register 31	BGR31	R/W		00000000B
7958H, 7959H	Reserved				
7960H	Clock Monitor Function Control Register	CSVCR	R, R/W	Clock Monitor	00011100B
7961H to 796DH	Reserved				
796EH	CAN Direct Mode Register	CDMR	R/W	CAN Clock Sync	XXXXXXX0B
796FH	Reserved				
7970H	I²C Bus Status Register 0	IBSR0	R	I²C Interface 0	00000000B
7971H	I²C Bus Control Register 0	IBCR0	W,R/W		00000000B
7972H	I²C 10-bit Slave Address Register 0	ITBAL0	R/W		00000000B
7973H		ITBAH0	R/W		00000000B
7974H	I²C 10-bit Slave Address Mask Register 0	ITMKL0	R/W		11111111B
7975H		ITMKH0	R/W		00111111B
7976H	I²C 7-bit Slave Address Register 0	ISBA0	R/W		00000000B
7977H	I²C 7-bit Slave Address Mask Register 0	ISMK0	R/W		01111111B
7978H	I²C data register 0	IDAR0	R/W		00000000B
7979H, 797AH	Reserved				
797BH	I²C Clock Control Register 0	ICCR0	R/W	I²C Interface 0	00011111B
797CH to 79A1H	Reserved				
79A2H	Flash Write Control Register 0	FWR0	R/W	Dual Operation Flash	00000000B
79A3H	Flash Write Control Register 1	FWR1	R/W		00000000B
79A4H	Sector Change Setting Register	SSR0	R/W		00XXXXX0B
79A5H to 79C1H	Reserved				

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Address	Register	Abbreviation	Access	Resource name	Initial value
79C2H	Setting Prohibited				
79C3H to 79DFH	Reserved				
79E0H	Detect Address Setting Register 0	PADR0	R/W	Address Match Detection 0	XXXXXXXXB
79E1H	Detect Address Setting Register 0	PADR0	R/W		XXXXXXXXB
79E2H	Detect Address Setting Register 0	PADR0	R/W		XXXXXXXXB
79E3H	Detect Address Setting Register 1	PADR1	R/W		XXXXXXXXB
79E4H	Detect Address Setting Register 1	PADR1	R/W		XXXXXXXXB
79E5H	Detect Address Setting Register 1	PADR1	R/W		XXXXXXXXB
79E6H	Detect Address Setting Register 2	PADR2	R/W		XXXXXXXXB
79E7H	Detect Address Setting Register 2	PADR2	R/W		XXXXXXXXB
79E8H	Detect Address Setting Register 2	PADR2	R/W		XXXXXXXXB
79E9H to 79EFH	Reserved				
79F0H	Detect Address Setting Register 3	PADR3	R/W	Address Match Detection 1	XXXXXXXXB
79F1H	Detect Address Setting Register 3	PADR3	R/W		XXXXXXXXB
79F2H	Detect Address Setting Register 3	PADR3	R/W		XXXXXXXXB
79F3H	Detect Address Setting Register 4	PADR4	R/W		XXXXXXXXB
79F4H	Detect Address Setting Register 4	PADR4	R/W		XXXXXXXXB
79F5H	Detect Address Setting Register 4	PADR4	R/W		XXXXXXXXB
79F6H	Detect Address Setting Register 5	PADR5	R/W		XXXXXXXXB
79F7H	Detect Address Setting Register 5	PADR5	R/W		XXXXXXXXB
79F8H	Detect Address Setting Register 5	PADR5	R/W		XXXXXXXXB
79F9H to 7BFFH	Reserved				
7C00H to 7CFFH	Reserved for CAN Interface 1. Refer to “■ CAN CONTROLLERS”				
7D00H to 7DFFH	Reserved for CAN Interface 1. Refer to “■ CAN CONTROLLERS”				
7E00H to 7FFFH	Reserved				

Notes :
- Initial value of “X” represents unknown value.
- Any write access to reserved addresses in I/O map should not be performed. A read access to reserved addresses results reading “X”.

List of Message Buffers (ID Registers)

Address CAN1	Register	Abbreviation	Access	Initial Value
$007C00_H$ to $007C1F_H$	General-purpose RAM	—	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007C20_H$	ID register 0	IDR0	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007C21_H$				
$007C22_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007C23_H$				
$007C24_H$	ID register 1	IDR1	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007C25_H$				
$007C26_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007C27_H$				
$007C28_H$	ID register 2	IDR2	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007C29_H$				
$007C2A_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007C2B_H$				
$007C2C_H$	ID register 3	IDR3	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007C2D_H$				
$007C2E_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007C2F_H$				
$007C30_H$	ID register 4	IDR4	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007C31_H$				
$007C32_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007C33_H$				
$007C34_H$	ID register 5	IDR5	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007C35_H$				
$007C36_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007C37_H$				
$007C38_H$	ID register 6	IDR6	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007C39_H$				
$007C3A_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007C3B_H$				
$007C3C_H$	ID register 7	IDR7	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007C3D_H$				
$007C3E_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007C3F_H$				

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Interrupt cause	EI²OS corre-sponding	DMA ch number	Interrupt vector		Interrupt control register	
			Number	Address	Number	Address
UART 2 RX	Y2	14	#39	FFFF60H	ICR14	0000BEH
UART 2 TX	Y1	15	#40	FFFF5CH		
Flash Memory	N	—	#41	FFFF58H	ICR15	0000BFH
Delayed interrupt	N	—	#42	FFFF54H		

Y1 : Usable

Y2 : Usable, with EI²OS stop function

N : Unusable

Notes :
- The peripheral resources sharing the ICR register have the same interrupt level.
- When two peripheral resources share the ICR register, only one can use EI²OSat a time.
- When either of the two peripheral resources sharing the ICR register specifies EI²OS, the other one cannot use interrupts.

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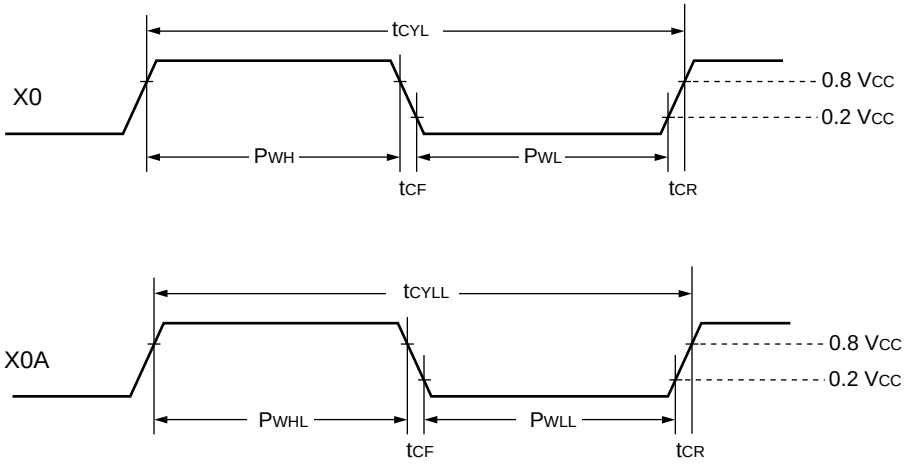
(MB90F352(S)/MB90F351(S): T_A = –40 °C to +105 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)
(MB90F352(S)/MB90F351(S): T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 16 MHz, V_{SS} = AV_{SS} = 0 V)
(Device other than above: T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

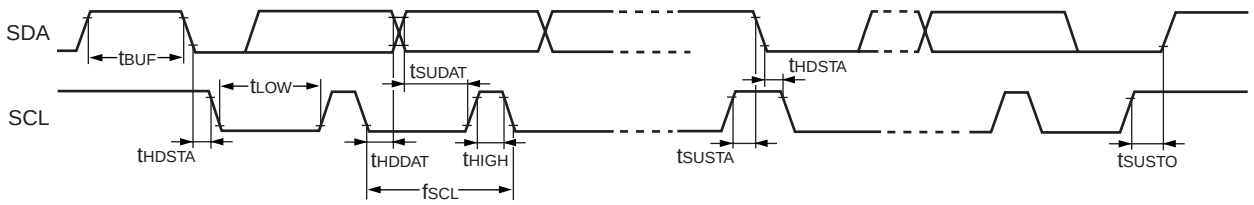
Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Internal operating clock frequency (machine clock)	f_{CP}	—	1.5	—	24	MHz	MB90F352/(S), MB90F351/(S) When using main clock (T_A ≤ +105 °C)
					16		MB90F352/(S), MB90F351/(S) When using main clock (T_A ≤ +125 °C)
			1.5	—	24	MHz	Device other than above, When using main clock
	f_{CPL}	—	—	8.192	50	kHz	When using sub clock
Internal operating clock cycle time (machine clock)	t_{CP}	—	41.67	—	666	ns	MB90F352/(S), MB90F351/(S) When using main clock (T_A ≤ +105 °C)
			62.5				MB90F352/(S), MB90F351/(S) When using main clock (T_A ≤ +125 °C)
			41.67	—	666	ns	Device other than above, When using main clock
	t_{CPL}	—	20	122.1	—	µs	When using sub clock

• Clock Timing



Note : The rating of the input data set-up time in the device connected to the bus cannot be satisfied depending on the load capacitance or pull-up resistor.
Be sure to adjust the pull-up resistor of SDA and SCL if the rating of the input data set-up time cannot be satisfied.

- Timing definition



5. A/D Converter

(MB90F352(S)/MB90F351(S): T_A = –40 °C to +105 °C, 3.0 V ≤ AVRH, V_{CC} = AV_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)
(MB90F352(S)/MB90F351(S): T_A = –40 °C to +125 °C, 3.0 V ≤ AVRH, V_{CC} = AV_{CC} = 5.0 V ± 10%, f_{CP} ≤ 16 MHz, V_{SS} = AV_{SS} = 0 V)
(Device other than above: T_A = –40 °C to +125 °C, 3.0 V ≤ AVRH, V_{CC} = AV_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

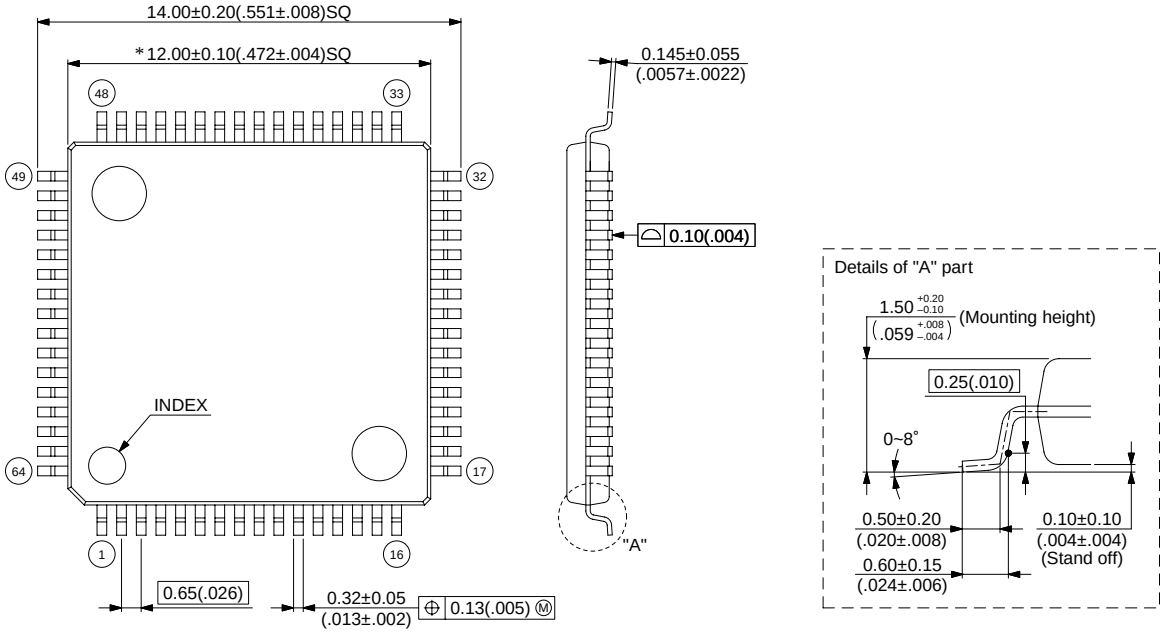
Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	—	—	±3.0	LSB	
Nonlinearity error	—	—	—	—	±2.5	LSB	
Differential nonlinearity error	—	—	—	—	±1.9	LSB	
Zero reading voltage	V_{OT}	AN0 to AN14	AV_{SS} – 1.5	AV_{SS} + 0.5	AV_{SS} + 2.5	LSB	
Full scale reading voltage	V_{FST}	AN0 to AN14	AVRH – 3.5	AVRH – 1.5	AVRH + 0.5	LSB	
Compare time	—	—	1.0	—	16,500	µs	4.5 V ≤ AV_{CC} ≤ 5.5 V
			2.0				4.0 V ≤ AV_{CC} < 4.5 V
Sampling time	—	—	0.5	—	∞	µs	4.5 V ≤ AV_{CC} ≤ 5.5 V
			1.2				4.0 V ≤ AV_{CC} < 4.5 V
Analog port input current	I_{AIN}	AN0 to AN14	–0.3	—	+0.3	µA	
Analog input voltage range	V_{AIN}	AN0 to AN14	AV_{SS}	—	AVRH	V	
Reference voltage range	—	AVRH	AV_{SS} + 2.7	—	AV_{CC}	V	
Power supply current	I_A	AV_{CC}	—	3.5	7.5	mA	
	I_{AH}	AV_{CC}	—	—	5	µA	*
Reference voltage supply current	I_R	AVRH	—	600	900	µA	
	I_{RH}	AVRH	—	—	5	µA	*
Offset between input channels	—	AN0 to AN14	—	—	4	LSB	

* : If A/D converter is not operating, a current when CPU is stopped is applicable (V_{CC} = AV_{CC} = AVRH = 5.0 V) .

■ PACKAGE DIMENSIONS

64-pin plastic LQFP
(FPT-64P-M09)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.

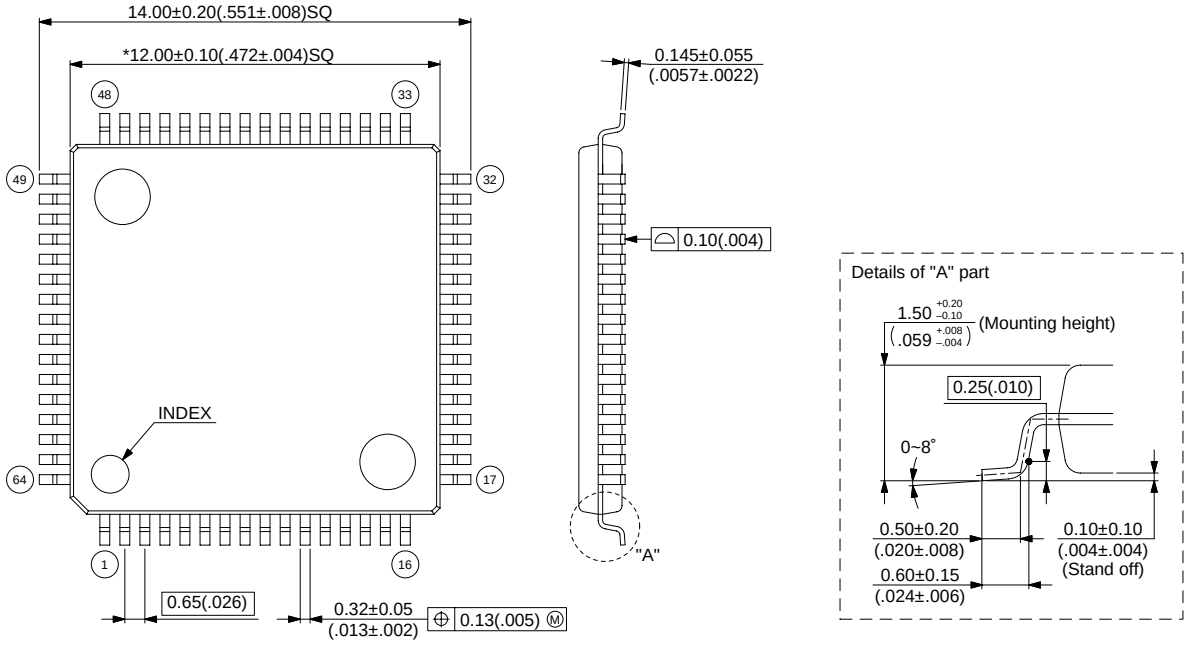


Dimensions in mm (inches) .
Note : The values in parentheses are reference values.

(Continued)

64-pin plastic LQFP
(FPT-64P-M23)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



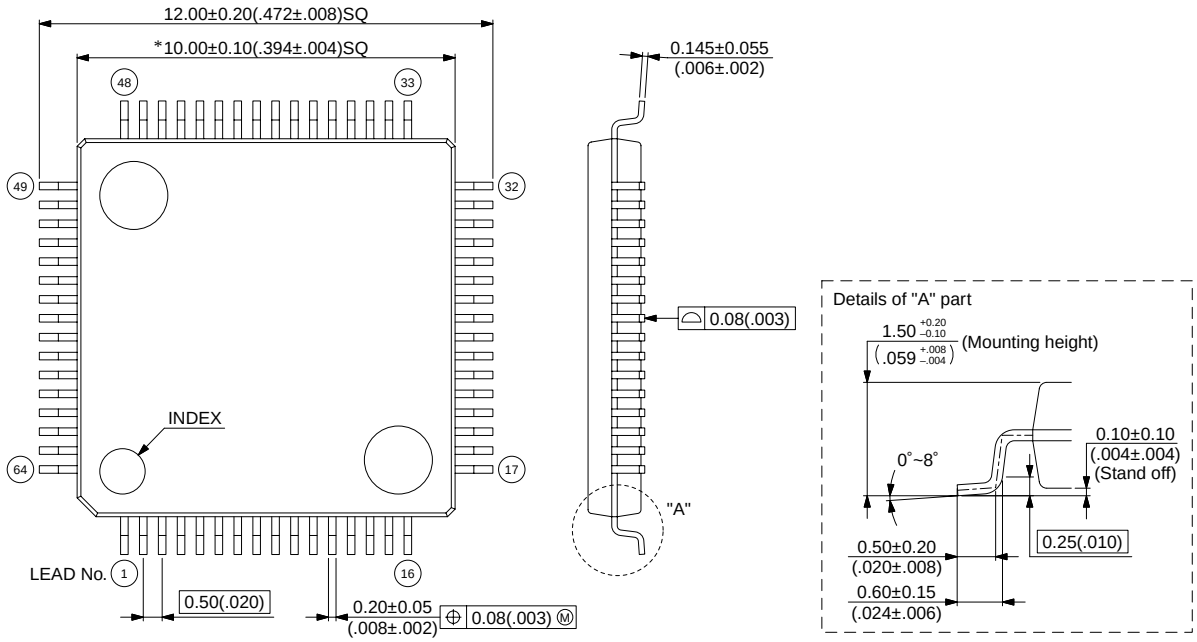
Dimensions in mm (inches) .
Note : The values in parentheses are reference values.

(Continued)

(Continued)

64-pin plastic LQFP
(FPT-64P-M24)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches) .
Note : The values in parentheses are reference values.