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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	24MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, WDT
Number of I/O	51
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 15x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-QFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f352spfm-gs-104e1

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Parameter \ Part Number	MB90351A, MB90352A	MB90351TA, MB90352TA	MB90351AS, MB90352AS	MB90351TAS, MB90352TAS	MB90V340A-101	MB90V340A-102
16-bit Output Compare	4 channels				8 channels	
	Signals an interrupt when 16-bit I/O Timer matches output compare registers. A pair of compare registers can be used to generate an output signal.					
16-bit Input Capture	6 channels				8 channels	
	Retains freerun timer value by (rising edge, falling edge or rising & falling edge), signals an interrupt.					
8/16-bit Programmable Pulse Generator	6 channels (16-bit)/10 channels (8-bit) 8-bit reload counters × 12 8-bit reload registers for L pulse width × 12 8-bit reload registers for H pulse width × 12				8 channels (16-bit)/ 16 channels (8-bit) 8-bit reload counters × 16 8-bit reload registers for L pulse width × 16 8-bit reload registers for H pulse width × 16	
	Supports 8-bit and 16-bit operation modes. A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler + 8-bit reload counter. Operation clock frequency : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4 or 128 µs@fosc = 4 MHz (fsys = Machine clock frequency, fosc = Oscillation clock frequency)					
CAN Interface	1 channel				3 channels	
	Conforms to CAN Specification Version 2.0 Part A and B. Automatic re-transmission in case of error Automatic transmission responding to Remote Frame Prioritized 16 message buffers for data and ID Supports multiple messages. Flexible configuration of acceptance filtering : Full bit compare/Full bit mask/Two partial bit masks Supports up to 1 Mbps.					
External Interrupt	8 channels				16 channels	
	Can be used rising edge, falling edge, starting up by H/L level input, external interrupt, extended intelligent I/O services (EI^{2}OS) and DMA.					
D/A converter	—				2 channels	
I/O Ports	Virtually all external pins can be used as general purpose I/O port. All push-pull outputs Bit-wise settable as input/output or peripheral signal Settable as CMOS schmitt trigger/ automotive inputs TTL input level settable for external bus (only for external bus pin)					
Flash Memory	—					
Corresponding EVA name	MB90V340A-102		MB90V340A-101		—	

* : It is setting of Jumper switch (TOOL VCC) when Emulator (MB2147-01) is used.
Please refer to the Emulator hardware manual about details.

■ PRODUCT LINEUP 3

Part Number / Parameter	MB90F356A, MB90F357A	MB90F356TA, MB90F357TA	MB90F356AS, MB90F357AS	MB90F356TAS, MB90F357TAS
CPU	F^2MC-16LX CPU			
System clock	On-chip PLL clock multiplier (×1, ×2, ×3, ×4, ×6, 1/2 when PLL stops) Minimum instruction execution time : 42 ns (oscillation clock 4 MHz, PLL × 6)			
ROM	Dual operation flash memory 64Kbytes : MB90F356A(S), MB90F356TA(S) 128Kbytes : MB90F357A(S), MB90F357TA(S)			
RAM	4 Kbytes			
Emulator-specific power supply*1	—			
Sub clock pin (X0A, X1A)	Yes		No (internal CR oscillation can be used as sub clock)	
Clock monitor function	Yes			
Low voltage/CPU operation detection reset	No	Yes	No	Yes
Operating voltage range	3.5 V to 5.5 V : at normal operating (not using A/D converter) 3.5 V to 5.5 V : at using A/D converter/Flash programming 3.5 V to 5.5 V : at using external bus			
Operating temperature range	–40 °C to +125 °C			
Package	LQFP-64			
UART	2 channels			
	Wide range of baud rate settings using a dedicated reload timer Special synchronous options for adapting to different synchronous serial protocols LIN functionality working either as master or slave LIN device			
I^2C (400 Kbps)	1 channel			
A/D Converter	15 channels			
	10-bit or 8-bit resolution Conversion time : Min 3 µs includes sample time (per one channel)			
16-bit Reload Timer (4 channels)	Operation clock frequency : fsys/2^1, fsys/2^3, fsys/2^5 (fsys = Machine clock frequency) Supports External Event Count function.			
16-bit I/O Timer (2 channels)	I/O Timer 0 (clock input FRCK0) corresponds to ICU 0/1. I/O Timer 1 (clock input FRCK1) corresponds to ICU 4/5/6/7, OCU 4/5/6/7.			
	Signals an interrupt when overflowing. Supports Timer Clear when a match with Output Compare (Channel 0, 4) . Operation clock frequency : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4, fsys/2^5, fsys/2^6, fsys/2^7 (fsys = Machine clock frequency)			
16-bit Output Compare	4 channels			
	Signals an interrupt when 16-bit I/O Timer matches with output compare registers. A pair of compare registers can be used to generate an output signal.			

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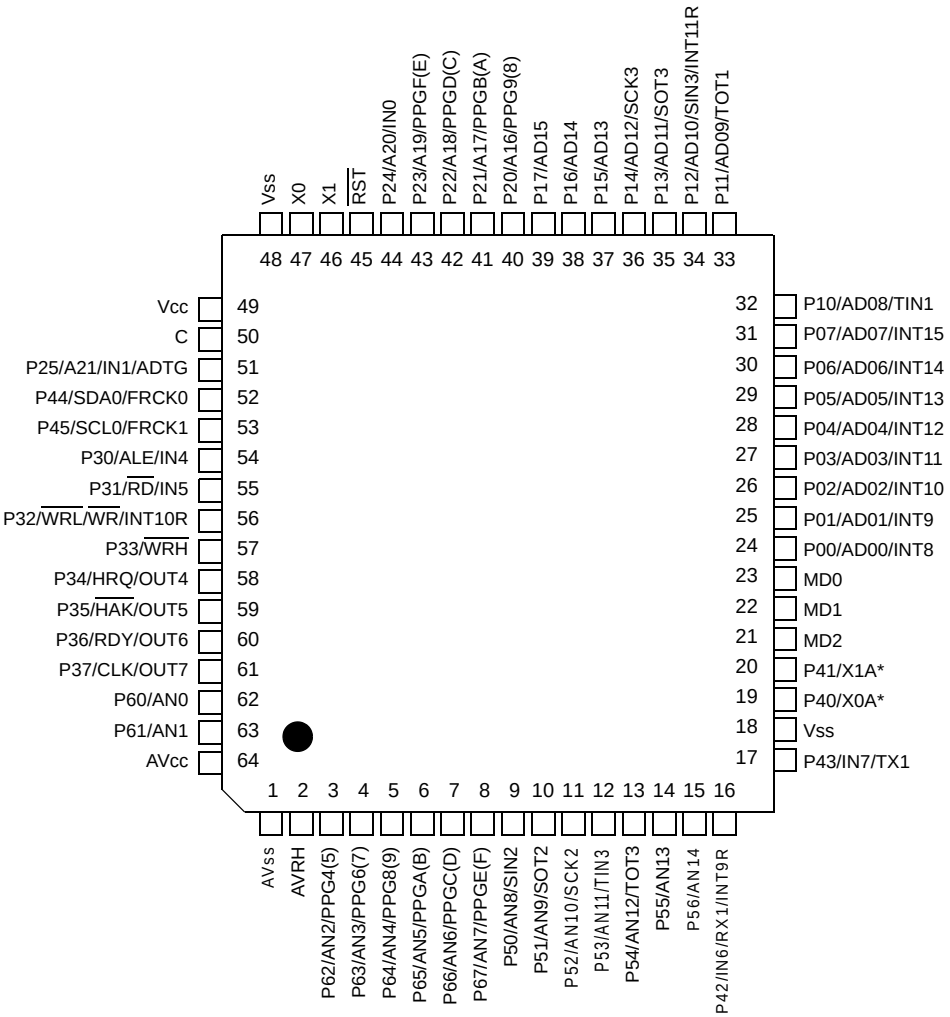
■ PIN ASSIGNMENTS

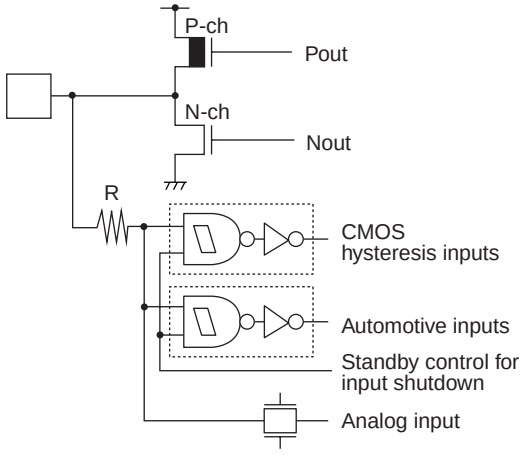
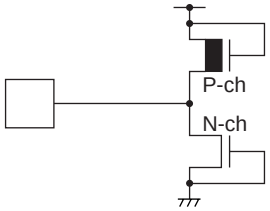
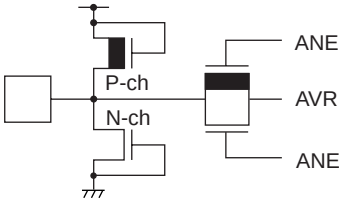
- MB90F351(S), MB90F352(S),MB90F351A(S), MB90F351TA(S), MB90F352A(S), MB90F352TA(S), MB90F356A(S), MB90F356TA(S), MB90F357A(S), MB90F357TA(S),MB90351A(S), MB90351TA(S), MB90352A(S), MB90352TA(S),MB90356A(S), MB90356TA(S), MB90357A(S), MB90357TA(S),

(TOP VIEW)
(LQFP-64P)



(FPT-64P-M09, FPT-64P-M23, FPT-64P-M24)

* : Devices without S-suffix : X0A, X1A
Devices with S-suffix : P40, P41

Type	Circuit	Remarks
I		• CMOS level output (I_{OL} = 4 mA, I_{OH} = –4 mA) • CMOS hysteresis inputs (With the stand-by-time input shutdown function) • Automotive input (With the standby-time input shutdown function) • A/D analog input
K		• Power supply input protection circuit
L		• A/D converter reference voltage power supply input pin, with the protection circuit • Flash memory devices do not have a protection circuit against V_{CC} for pin AVRH.

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16. Flash security Function

The security byte is located in the area of the flash memory.
If protection code 01_H is written in the security byte, the flash memory is in the protected state by security.
Therefore please do not write 01_H in this address if you do not use the security function.
Please refer to following table for the address of the security byte.

	Flash memory size	Address for security bit
MB90F352(S) MB90F352A(S) MB90F352TA(S) MB90F357A(S) MB90F357TA(S)	Embedded 1 Mbit Flash Memory	FE0001$_H$

17. Correspondence with T_A = +105 °C or more

If used exceeding T_A = +105 °C, please contact Fujitsu sales representatives for reliability limitations.

18. Low voltage/CPU operation reset circuit

The low voltage detection reset circuit is a function that monitors power supply voltage in order to detect when a voltage drops below a given voltage level. When a low voltage condition is detected, an internal reset signal is generated.
The CPU operation detection reset circuit is a 20-bit counter that uses oscillation as a count clock and generates an internal reset signal if not cleared within a given time after startup.

(1) Low voltage detection reset circuit

Detection voltage
4.0 V ± 0.3 V

When a low voltage condition is detected, the low voltage detection flag (LVRC : LVRF) is set to “1” and an internal reset signal is output.
Because the low voltage detection reset circuit continues to operate even in stop mode, detection of a low voltage condition generates an internal reset and releases stop mode.
During an internal RAM write cycle, low voltage reset is generated after the completion of writing. During the output of this internal reset, the reset output from the low voltage detection reset circuit is suppressed.

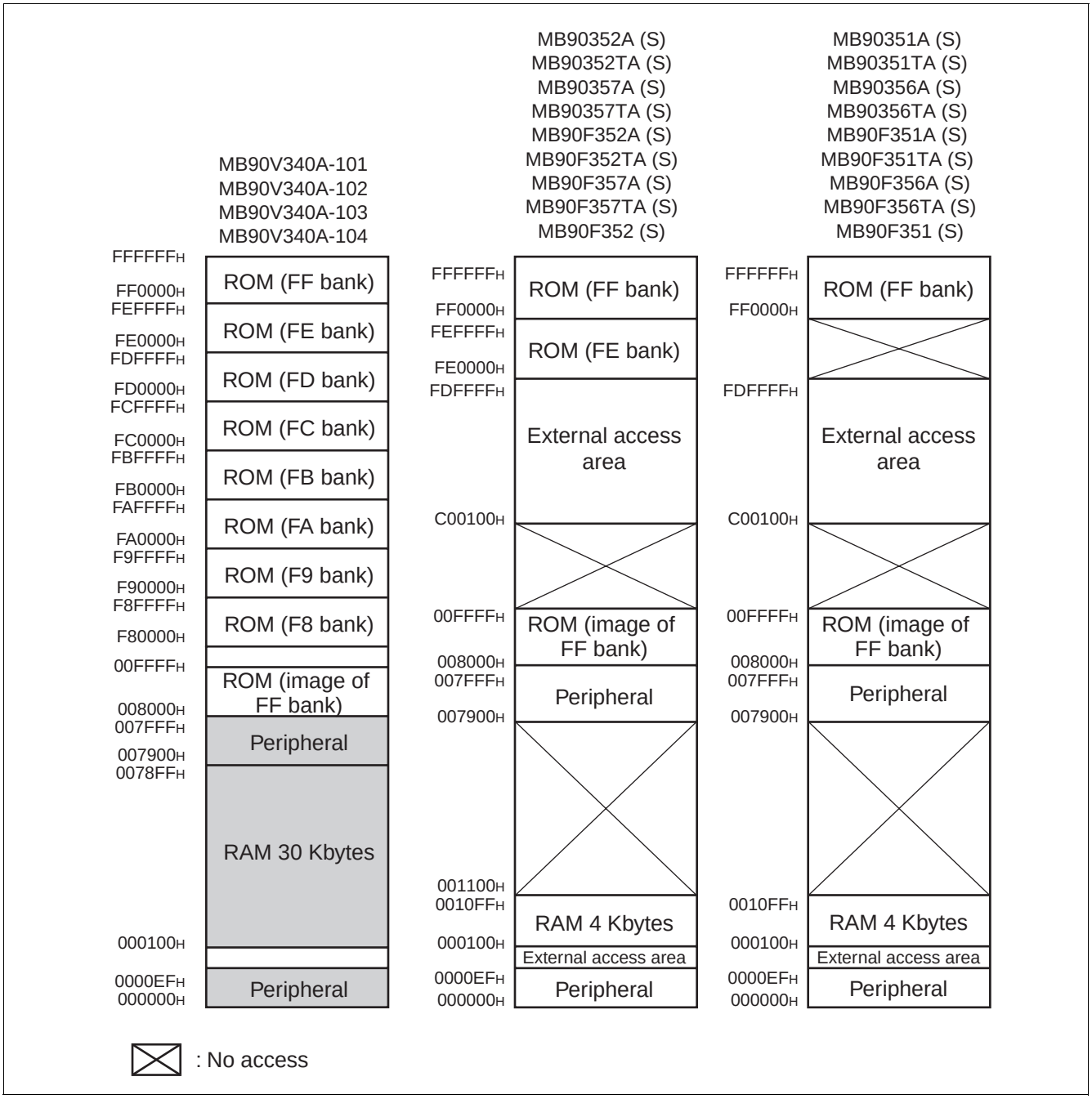
(2) CPU operation detection reset circuit

The CPU operation detection reset circuit is a counter that prevents program runaway. The counter starts automatically after a power-on reset, and must be continually cleared within a given time. If the given time interval elapses and the counter has not been cleared, a cause such as infinite program looping is assumed and an internal reset signal is generated. The internal reset generated from the CPU operation detection circuit has a width of 5 machine cycles.

Interval time
$2^{20}/F_C$ (approx. 262 ms*)

* : This value assumes the interval time at an oscillation clock frequency of 4 MHz.
During recovery from standby mode, the detection period is the maximum interval plus 20 µs.

■ MEMORY MAP



Note : The high-order portion of bank 00 gives the image of the FF bank ROM to make the small model of the C compiler effective. Since the low-order 16 bits are the same, the table in ROM can be referenced without using the far specification in the pointer declaration.
For example, an attempt to access 00C000H accesses the value at FFC000H in ROM.
The ROM area in bank FF exceeds 32 Kbytes, and its entire image cannot be shown in bank 00.
The image between FF8000H and FFFFFFH is visible in bank 00, while the image between FF0000H and FF7FFFH is visible only in bank FF.

■ I/O MAP

Address	Register	Abbreviation	Access	Resource name	Initial value
00_H	Port 0 Data Register	PDR0	R/W	Port 0	$XXXXXXXX_B$
01_H	Port 1 Data Register	PDR1	R/W	Port 1	$XXXXXXXX_B$
02_H	Port 2 Data Register	PDR2	R/W	Port 2	$XXXXXXXX_B$
03_H	Port 3 Data Register	PDR3	R/W	Port 3	$XXXXXXXX_B$
04_H	Port 4 Data Register	PDR4	R/W	Port 4	$XXXXXXXX_B$
05_H	Port 5 Data Register	PDR5	R/W	Port 5	$XXXXXXXX_B$
06_H	Port 6 Data Register	PDR6	R/W	Port 6	$XXXXXXXX_B$
07_H to $0A_H$	Reserved				
$0B_H$	Port 5 Analog Input Enable Register	ADER5	R/W	Port 5, A/D	11111111_B
$0C_H$	Port 6 Analog Input Enable Register	ADER6	R/W	Port 6, A/D	11111111_B
$0D_H$	Reserved				
$0E_H$	Input Level Select Register 0	ILSR0	R/W	Ports	00000000_B
$0F_H$	Input Level Select Register 1	ILSR1	R/W	Ports	00000000_B
10_H	Port 0 Direction Register	DDR0	R/W	Port 0	00000000_B
11_H	Port 1 Direction Register	DDR1	R/W	Port 1	00000000_B
12_H	Port 2 Direction Register	DDR2	R/W	Port 2	$XX000000_B$
13_H	Port 3 Direction Register	DDR3	R/W	Port 3	00000000_B
14_H	Port 4 Direction Register	DDR4	R/W	Port 4	$XX000000_B$
15_H	Port 5 Direction Register	DDR5	R/W	Port 5	$X0000000_B$
16_H	Port 6 Direction Register	DDR6	R/W	Port 6	00000000_B
17_H to 19_H	Reserved				
$1A_H$	SIN input Level Setting Register	DDRA	W	UART2, UART3	$X00XXXXX_B$
$1B_H$	Reserved				
$1C_H$	Port 0 Pull-up Control Register	PUCR0	R/W	Port 0	00000000_B
$1D_H$	Port 1 Pull-up Control Register	PUCR1	R/W	Port 1	00000000_B
$1E_H$	Port 2 Pull-up Control Register	PUCR2	R/W	Port 2	00000000_B
$1F_H$	Port 3 Pull-up Control Register	PUCR3	R/W	Port 3	00000000_B
20_H to 37_H	Reserved				
38_H	PPG 4 Operation Mode Control Register	PPGC4	W, R/W	16-bit Programmable Pulse Generator 4/5	$0X000XX1_B$
39_H	PPG 5 Operation Mode Control Register	PPGC5	W, R/W		$0X000001_B$
$3A_H$	PPG 4/5 Count Clock Select Register	PPG45	R/W		$000000X0_B$
$3B_H$	Address Detect Control Register 1	PACSR1	R/W	Address Match Detection 1	00000000_B

(Continued)

Address	Register	Abbrevia-tion	Access	Resource name	Initial value
$A4_H$	DMA Stop Status Register	DSSR	R/W	DMA	00000000_B
$A5_H$	Automatic Ready Function Selection Register	ARSR	W	External Memory Access	$0011XX00_B$
$A6_H$	External Address Output Control Register	HACR	W		00000000_B
$A7_H$	Bus Control Signal Selection Register	ECSR	W		$0000000X_B$
$A8_H$	Watchdog Control Register	WDTC	R,W	Watchdog Timer	$XXXXX111_B$
$A9_H$	Timebase Timer Control Register	TBTC	W,R/W	Timebase timer	$1XX00100_B$
AA_H	Watch Timer Control Register	WTC	R,R/W	Watch Timer	$1X001000_B$
AB_H	Reserved				
AC_H	DMA Enable Register L	DERL	R/W	DMA	00000000_B
AD_H	DMA Enable Register H	DERH	R/W		00000000_B
AE_H	Flash Control Status Register (Flash Devices only. Otherwise reserved)	FMCS	R,R/W	Flash Memory	$000X0000_B$
AF_H	Reserved				
$B0_H$	Interrupt Control Register 00	ICR00	W,R/W	Interrupt Control	00000111_B
$B1_H$	Interrupt Control Register 01	ICR01	W,R/W		00000111_B
$B2_H$	Interrupt Control Register 02	ICR02	W,R/W		00000111_B
$B3_H$	Interrupt Control Register 03	ICR03	W,R/W		00000111_B
$B4_H$	Interrupt Control Register 04	ICR04	W,R/W		00000111_B
$B5_H$	Interrupt Control Register 05	ICR05	W,R/W		00000111_B
$B6_H$	Interrupt Control Register 06	ICR06	W,R/W		00000111_B
$B7_H$	Interrupt Control Register 07	ICR07	W,R/W		00000111_B
$B8_H$	Interrupt Control Register 08	ICR08	W,R/W		00000111_B
$B9_H$	Interrupt Control Register 09	ICR09	W,R/W		00000111_B
BA_H	Interrupt Control Register 10	ICR10	W,R/W		00000111_B
BB_H	Interrupt Control Register 11	ICR11	W,R/W		00000111_B
BC_H	Interrupt Control Register 12	ICR12	W,R/W		00000111_B
BD_H	Interrupt Control Register 13	ICR13	W,R/W		00000111_B
BE_H	Interrupt Control Register 14	ICR14	W,R/W		00000111_B
BF_H	Interrupt Control Register 15	ICR15	W,R/W		00000111_B
$C0_H$ to $C9_H$	Reserved				

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
7908H	Reload Register L4	PRLL4	R/W	16-bit Programmable Pulse Generator 4/5	XXXXXXXXB
7909H	Reload Register H4	PRLH4	R/W		XXXXXXXXB
790AH	Reload Register L5	PRLL5	R/W		XXXXXXXXB
790BH	Reload Register H5	PRLH5	R/W		XXXXXXXXB
790CH	Reload Register L6	PRLL6	R/W	16-bit Programmable Pulse Generator 6/7	XXXXXXXXB
790DH	Reload Register H6	PRLH6	R/W		XXXXXXXXB
790EH	Reload Register L7	PRLL7	R/W		XXXXXXXXB
790FH	Reload Register H7	PRLH7	R/W		XXXXXXXXB
7910H	Reload Register L8	PRLL8	R/W	16-bit Programmable Pulse Generator 8/9	XXXXXXXXB
7911H	Reload Register H8	PRLH8	R/W		XXXXXXXXB
7912H	Reload Register L9	PRLL9	R/W		XXXXXXXXB
7913H	Reload Register H9	PRLH9	R/W		XXXXXXXXB
7914H	Reload Register LA	PRLLA	R/W	16-bit Programmable Pulse Generator A/B	XXXXXXXXB
7915H	Reload Register HA	PRLHA	R/W		XXXXXXXXB
7916H	Reload Register LB	PRLLB	R/W		XXXXXXXXB
7917H	Reload Register HB	PRLHB	R/W		XXXXXXXXB
7918H	Reload Register LC	PRLLC	R/W	16-bit Programmable Pulse Generator C/D	XXXXXXXXB
7919H	Reload Register HC	PRLHC	R/W		XXXXXXXXB
791AH	Reload Register LD	PRLLD	R/W		XXXXXXXXB
791BH	Reload Register HD	PRLHD	R/W		XXXXXXXXB
791CH	Reload Register LE	PRLLE	R/W	16-bit Programmable Pulse Generator E/F	XXXXXXXXB
791DH	Reload Register HE	PRLHE	R/W		XXXXXXXXB
791EH	Reload Register LF	PRLLF	R/W		XXXXXXXXB
791FH	Reload Register HF	PRLHF	R/W		XXXXXXXXB
7920H	Input Capture Register 0	IPCP0	R	Input Capture 0/1	XXXXXXXXB
7921H	Input Capture Register 0	IPCP0	R		XXXXXXXXB
7922H	Input Capture Register 1	IPCP1	R		XXXXXXXXB
7923H	Input Capture Register 1	IPCP1	R		XXXXXXXXB
7924H to 7927H	Reserved				
7928H	Input Capture Register 4	IPCP4	R	Input Capture 4/5	XXXXXXXXB
7929H	Input Capture Register 4	IPCP4	R		XXXXXXXXB
792AH	Input Capture Register 5	IPCP5	R		XXXXXXXXB
792BH	Input Capture Register 5	IPCP5	R		XXXXXXXXB

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
7950H	Serial Mode Register 3	SMR3	W, R/W	UART3	00000000B
7951H	Serial Control Register 3	SCR3	W, R/W		00000000B
7952H	Reception/Transmission Data Register 3	RDR3/ TDR3	R/W		00000000B
7953H	Serial Status Register 3	SSR3	R,R/W		00001000B
7954H	Extended Communication Control Register 3	ECCR3	R,W, R/W		000000XXB
7955H	Extended Status/Control Register 3	ESCR3	R/W		00000100B
7956H	Baud Rate Generator Register 30	BGR30	R/W		00000000B
7957H	Baud Rate Generator Register 31	BGR31	R/W		00000000B
7958H, 7959H	Reserved				
7960H	Clock Monitor Function Control Register	CSVCR	R, R/W	Clock Monitor	00011100B
7961H to 796DH	Reserved				
796EH	CAN Direct Mode Register	CDMR	R/W	CAN Clock Sync	XXXXXXX0B
796FH	Reserved				
7970H	I²C Bus Status Register 0	IBSR0	R	I²C Interface 0	00000000B
7971H	I²C Bus Control Register 0	IBCR0	W,R/W		00000000B
7972H	I²C 10-bit Slave Address Register 0	ITBAL0	R/W		00000000B
7973H		ITBAH0	R/W		00000000B
7974H	I²C 10-bit Slave Address Mask Register 0	ITMKL0	R/W		11111111B
7975H		ITMKH0	R/W		00111111B
7976H	I²C 7-bit Slave Address Register 0	ISBA0	R/W		00000000B
7977H	I²C 7-bit Slave Address Mask Register 0	ISMK0	R/W		01111111B
7978H	I²C data register 0	IDAR0	R/W		00000000B
7979H, 797AH	Reserved				
797BH	I²C Clock Control Register 0	ICCR0	R/W	I²C Interface 0	00011111B
797CH to 79A1H	Reserved				
79A2H	Flash Write Control Register 0	FWR0	R/W	Dual Operation Flash	00000000B
79A3H	Flash Write Control Register 1	FWR1	R/W		00000000B
79A4H	Sector Change Setting Register	SSR0	R/W		00XXXXX0B
79A5H to 79C1H	Reserved				

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Address CAN1	Register	Abbreviation	Access	Initial Value
007C40H	ID register 8	IDR8	R/W	XXXXXXXXB XXXXXXXXB
007C41H				
007C42H				XXXXXXXXB XXXXXXXXB
007C43H				
007C44H	ID register 9	IDR9	R/W	XXXXXXXXB XXXXXXXXB
007C45H				
007C46H				XXXXXXXXB XXXXXXXXB
007C47H				
007C48H	ID register 10	IDR10	R/W	XXXXXXXXB XXXXXXXXB
007C49H				
007C4AH				XXXXXXXXB XXXXXXXXB
007C4BH				
007C4CH	ID register 11	IDR11	R/W	XXXXXXXXB XXXXXXXXB
007C4DH				
007C4EH				XXXXXXXXB XXXXXXXXB
007C4FH				
007C50H	ID register 12	IDR12	R/W	XXXXXXXXB XXXXXXXXB
007C51H				
007C52H				XXXXXXXXB XXXXXXXXB
007C53H				
007C54H	ID register 13	IDR13	R/W	XXXXXXXXB XXXXXXXXB
007C55H				
007C56H				XXXXXXXXB XXXXXXXXB
007C57H				
007C58H	ID register 14	IDR14	R/W	XXXXXXXXB XXXXXXXXB
007C59H				
007C5AH				XXXXXXXXB XXXXXXXXB
007C5BH				
007C5CH	ID register 15	IDR15	R/W	XXXXXXXXB XXXXXXXXB
007C5DH				
007C5EH				XXXXXXXXB XXXXXXXXB
007C5FH				

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(MB90F352(S)/MB90F351(S): T_A = –40 °C to +105 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)
(MB90F352(S)/MB90F351(S): T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 16 MHz, V_{SS} = AV_{SS} = 0 V)
(Device other than above: T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I_{CCT}	V_{CC}	V_{CC} = 5.0 V, Internal frequency: 8 kHz, During operating clock monitor function, At watch mode T_A = +25°C	—	25	150	µA	MB90F356A MB90F357A MB90356A MB90357A
			V_{CC} = 5.0 V, Internal CR oscillation/ 4 division, At watch mode T_A = +25°C	—	25	150	µA	MB90F356AS MB90F357AS MB90356AS MB90357AS
			V_{CC} = 5.0 V, Internal frequency: 8 kHz, During stopping clock monitor function, At watch mode T_A = +25°C	—	60	140	µA	MB90F351TA MB90F352TA MB90F356TA MB90F357TA MB90351TA MB90352TA MB90356TA MB90357TA
			V_{CC} = 5.0 V, Internal frequency: 8 kHz, During operating clock monitor function, At watch mode T_A = +25°C	—	80	250	µA	MB90F356TA MB90F357TA MB90356TA MB90357TA
			V_{CC} = 5.0 V, Internal CR oscillation/ 4 division, At watch mode T_A = +25°C	—	80	250	µA	MB90F356TAS MB90F357TAS MB90356TAS MB90357TAS
	I_{CCH}		V_{CC} = 5.0 V, At Stop mode, T_A = +25°C	—	7	25	µA	Devices without “T”-suffix
				—	60	130	µA	Devices with “T”-suffix
Input capacity	C_{IN}	Other than C, AV_{CC}, AV_{SS}, AVRH, V_{CC}, V_{SS},	—	—	5	15	pF	

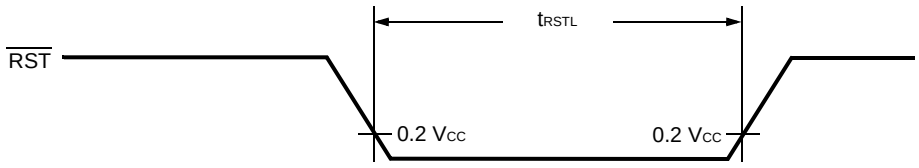
(2) Reset Standby Input

(MB90F352(S)/MB90F351(S): T_A = –40 °C to +105 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)
(MB90F352(S)/MB90F351(S): T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 16 MHz, V_{SS} = AV_{SS} = 0 V)
(Device other than above: T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

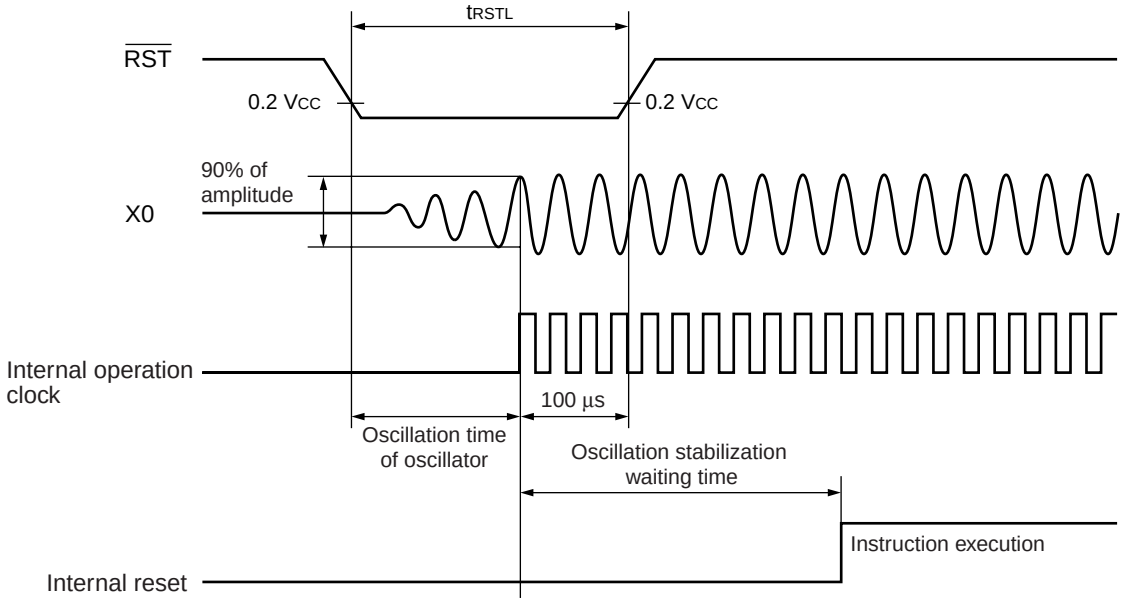
Parameter	Symbol	Pin	Value		Unit	Remarks
			Min	Max		
Reset input time	t_{RSTL}	$\overline{RST}$	500	—	ns	Under normal operation
			Oscillation time of oscillator* + 100 µs	—	µs	In Stop mode, Sub Clock mode, Sub Sleep mode and Watch mode
			100	—	µs	In Main timer mode and PLL timer mode

* : Oscillation time of oscillator is the time that the amplitude reaches 90%.
In the crystal oscillator, the oscillation time is between several ms to tens of ms. In FAR / ceramic oscillators, the oscillation time is between hundreds of µs to several ms. With an external clock, the oscillation time is 0 ms.

Under normal operation:



In Stop mode, Sub Clock mode, Sub Sleep mode, Watch mode:



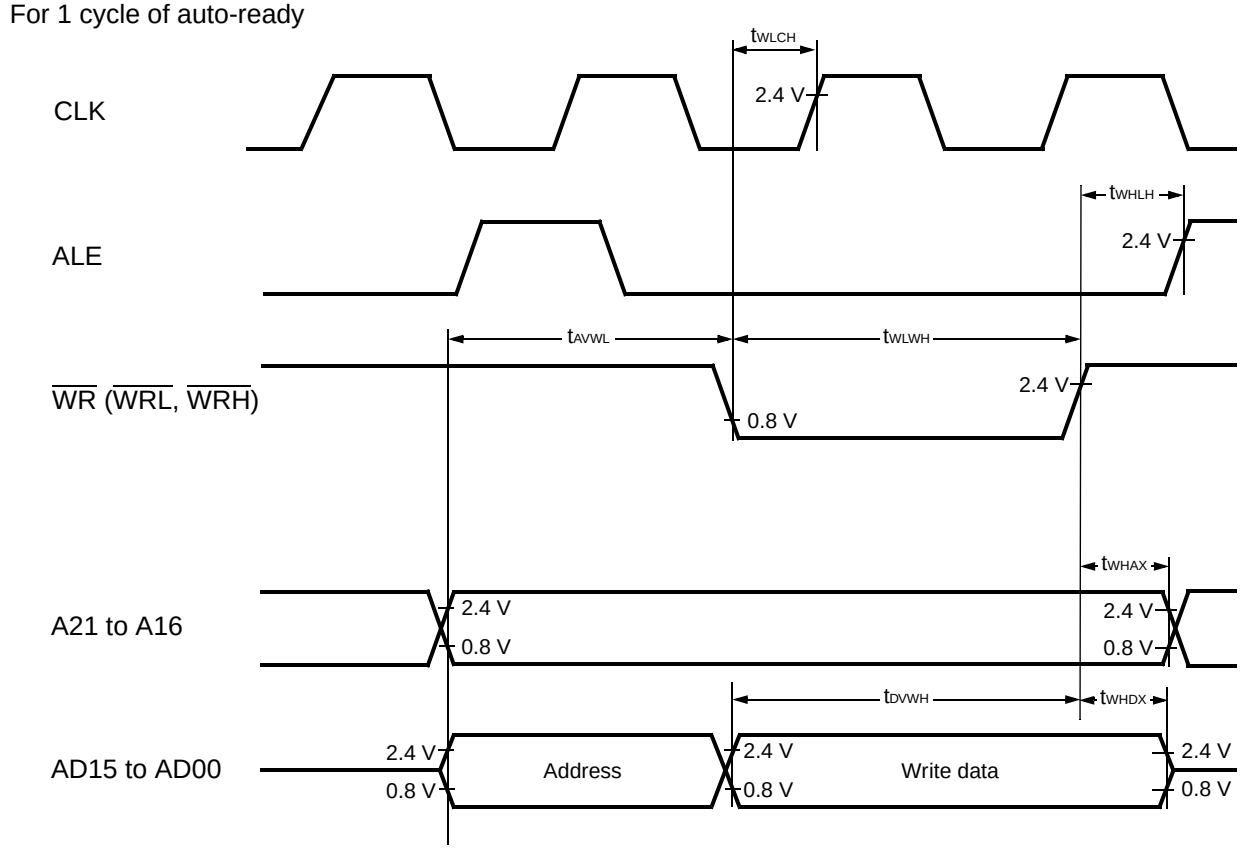
(6) Bus Timing (Write)

(T_A = –40°C to +105°C, V_{CC} = 5.0 V ± 10 %, V_{SS} = 0.0 V, f_{CP} ≤ 24 MHz)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Valid address ⇒ $\overline{WR}$ ↓ time	t_{AVWL}	A21 to A16, AD15 to AD00, $\overline{WR}$	—	t_{CP}–15	—	ns	
$\overline{WR}$ pulse width	t_{WLWH}	$\overline{WR}$		(n*+3/2)t_{CP} – 20	—	ns	
Valid data output ⇒ $\overline{WR}$ ↑ time	t_{DVWH}	AD15 to AD00, $\overline{WR}$		(n*+3/2)t_{CP} – 20	—	ns	
$\overline{WR}$ ↑ ⇒ Data hold time	t_{WHDX}	AD15 to AD00, $\overline{WR}$		15	—	ns	
$\overline{WR}$ ↑ ⇒ Address valid time	t_{WHAX}	A21 to A16, $\overline{WR}$		t_{CP}/2 – 10	—	ns	
$\overline{WR}$ ↑ ⇒ ALE ↑ time	t_{WHLH}	$\overline{WR}$, ALE		t_{CP}/2 – 15	—	ns	
$\overline{WR}$ ↓ ⇒ CLK ↑ time	t_{WLCH}	$\overline{WR}$, CLK		t_{CP}/2 – 15	—	ns	

* : n: Number of ready cycles

For 1 cycle of auto-ready



5. A/D Converter

(MB90F352(S)/MB90F351(S): T_A = –40 °C to +105 °C, 3.0 V ≤ AVRH, V_{CC} = AV_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)
(MB90F352(S)/MB90F351(S): T_A = –40 °C to +125 °C, 3.0 V ≤ AVRH, V_{CC} = AV_{CC} = 5.0 V ± 10%, f_{CP} ≤ 16 MHz, V_{SS} = AV_{SS} = 0 V)
(Device other than above: T_A = –40 °C to +125 °C, 3.0 V ≤ AVRH, V_{CC} = AV_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	—	—	±3.0	LSB	
Nonlinearity error	—	—	—	—	±2.5	LSB	
Differential nonlinearity error	—	—	—	—	±1.9	LSB	
Zero reading voltage	V_{OT}	AN0 to AN14	AV_{SS} – 1.5	AV_{SS} + 0.5	AV_{SS} + 2.5	LSB	
Full scale reading voltage	V_{FST}	AN0 to AN14	AVRH – 3.5	AVRH – 1.5	AVRH + 0.5	LSB	
Compare time	—	—	1.0	—	16,500	µs	4.5 V ≤ AV_{CC} ≤ 5.5 V
			2.0				4.0 V ≤ AV_{CC} < 4.5 V
Sampling time	—	—	0.5	—	∞	µs	4.5 V ≤ AV_{CC} ≤ 5.5 V
			1.2				4.0 V ≤ AV_{CC} < 4.5 V
Analog port input current	I_{AIN}	AN0 to AN14	–0.3	—	+0.3	µA	
Analog input voltage range	V_{AIN}	AN0 to AN14	AV_{SS}	—	AVRH	V	
Reference voltage range	—	AVRH	AV_{SS} + 2.7	—	AV_{CC}	V	
Power supply current	I_A	AV_{CC}	—	3.5	7.5	mA	
	I_{AH}	AV_{CC}	—	—	5	µA	*
Reference voltage supply current	I_R	AVRH	—	600	900	µA	
	I_{RH}	AVRH	—	—	5	µA	*
Offset between input channels	—	AN0 to AN14	—	—	4	LSB	

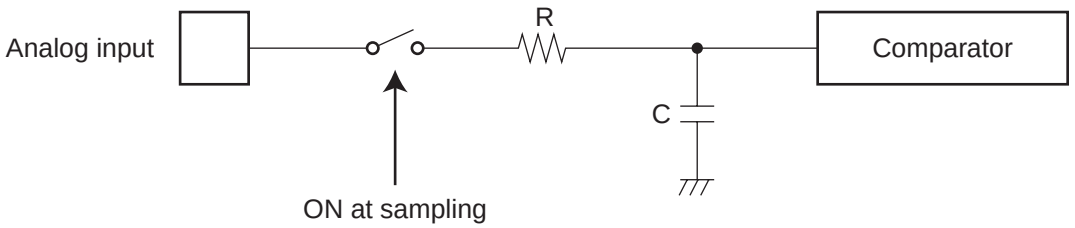
* : If A/D converter is not operating, a current when CPU is stopped is applicable (V_{CC} = AV_{CC} = AVRH = 5.0 V) .

Notes on A/D Converter Section

- **About the external impedance of the analog input and its sampling time**

  A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision. Therefore to satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. Also if the sampling time cannot be sufficient, connect a capacitor of about 0.1 µF to the analog input pin.

· Analog input equivalence circuit



MB90F352(S), MB90F351A(S), MB90F352A(S), MB90F351TA(S), MB90F352TA(S), MB90F356A(S), MB90F357A(S), MB90F356TA(S), MB90F357TA(S),

	R	C
$4.5\ V \leqq AV_{CC} \leqq 5.5\ V$	2.0 kΩ (Max)	16.0 pF (Max)
$4.0\ V \leqq AV_{CC} \leqq 4.5\ V$	8.2 kΩ (Max)	16.0 pF (Max)

MB90V340A-101/102/103/104, MB90351A(S), MB90352A(S), MB90351TA(S), MB90352TA(S), MB90356A(S), MB90357A(S), MB90356TA(S), MB90357TA(S),

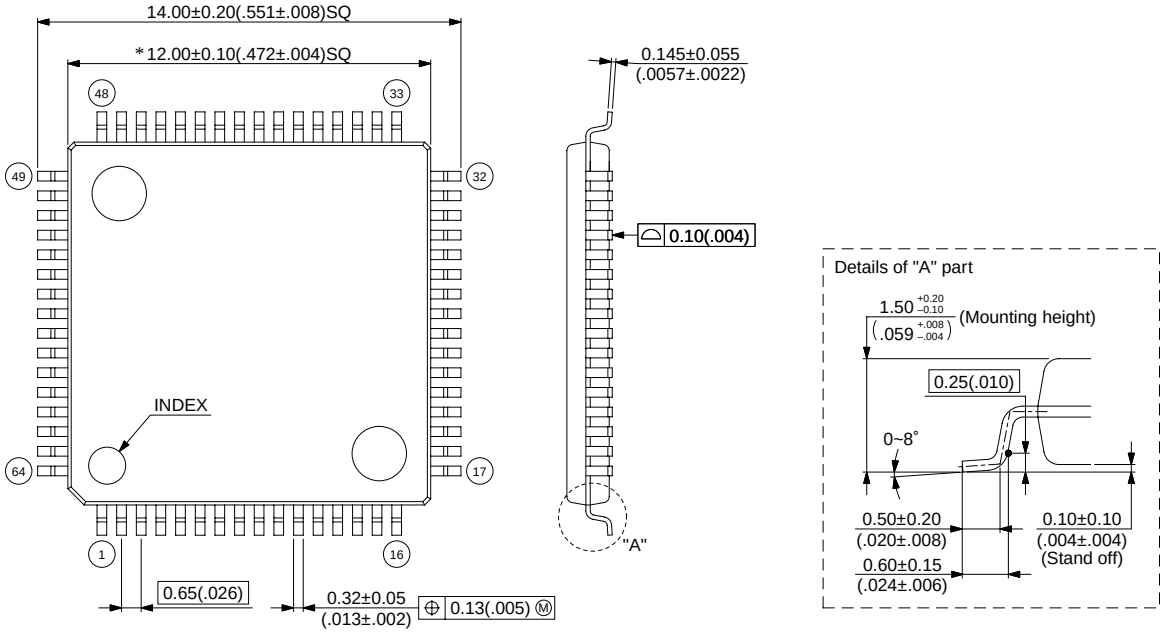
	R	C
$4.5\ V \leqq AV_{CC} \leqq 5.5\ V$	2.0 kΩ (Max)	14.4 pF (Max)
$4.0\ V \leqq AV_{CC} \leqq 4.5\ V$	8.2 kΩ (Max)	14.4 pF (Max)

Note : The value is reference value.

■ PACKAGE DIMENSIONS

64-pin plastic LQFP
(FPT-64P-M09)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.

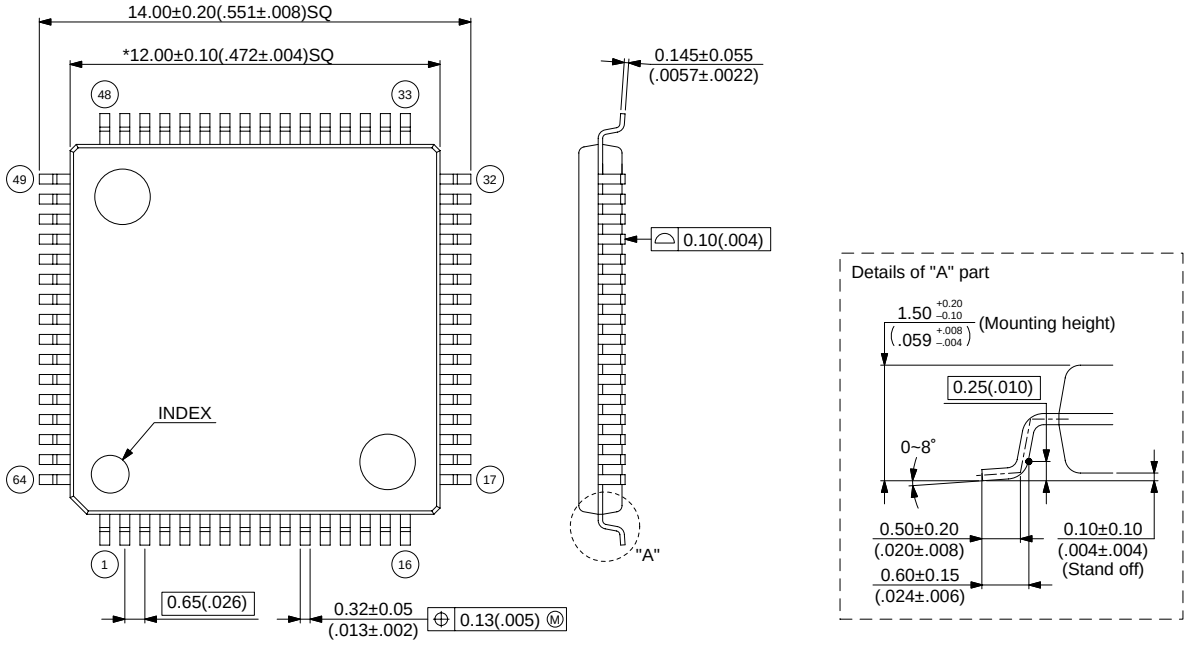


Dimensions in mm (inches) .
Note : The values in parentheses are reference values.

(Continued)

64-pin plastic LQFP
(FPT-64P-M23)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



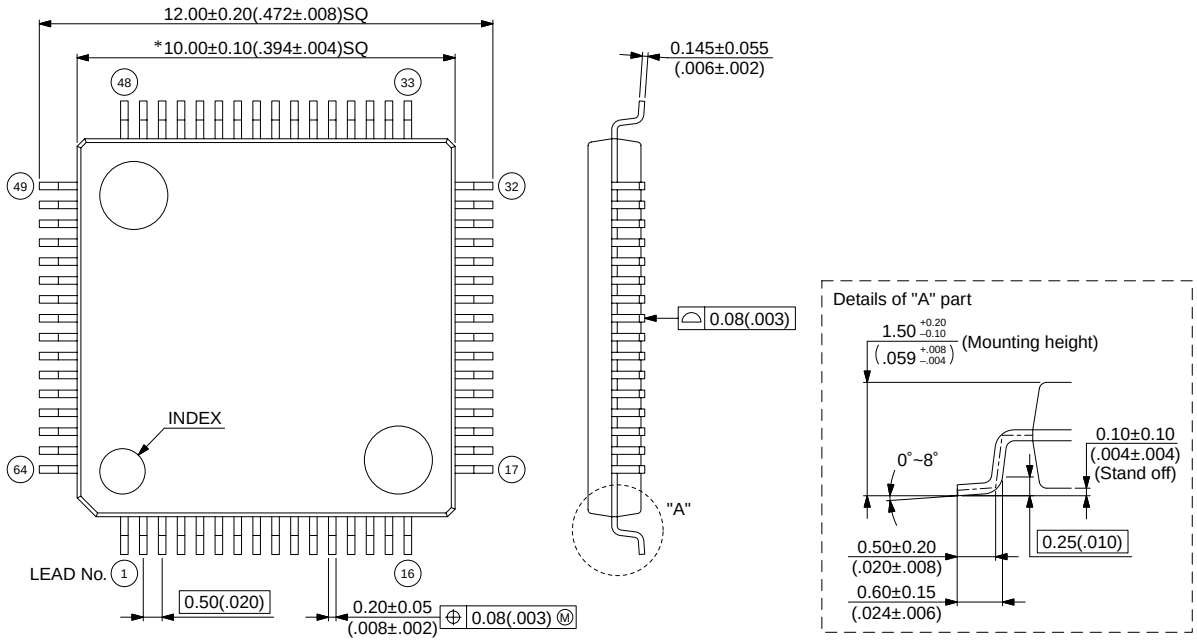
Dimensions in mm (inches) .
Note : The values in parentheses are reference values.

(Continued)

(Continued)

64-pin plastic LQFP
(FPT-64P-M24)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches) .
Note : The values in parentheses are reference values.

The information for microcontroller supports is shown in the following homepage.
http://www.fujitsu.com/global/services/microelectronics/product/micom/support/index.html

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