Infineon Technologies - MB90F352SPFM-GS-113E1 Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	24MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, WDT
Number of I/O	51
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 15x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-QFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f352spfm-gs-113e1

■ PRODUCT LINEUP 1

Part Number / Parameter	MB90F351, MB90F352	MB90F351S, MB90F352S	MB90F351A, MB90F352A	MB90F351TA, MB90F352TA	MB90F351AS, MB90F352AS	MB90F351TAS, MB90F352TAS
CPU	F^2MC-16LX CPU					
System clock	On-chip PLL clock multiplier (×1, ×2, ×3, ×4, ×6, 1/2 when PLL stops) Minimum instruction execution time : 42 ns (oscillation clock 4 MHz, PLL × 6)					
ROM	Flash memory 64Kbytes : MB90F351(S) 128Kbytes : MB90F352(S)		Dual operation flash memory 64Kbytes : MB90F351A(S), MB90F351TA(S) 128Kbytes : MB90F352A(S), MB90F352TA(S)			
RAM	4 Kbytes					
Emulator-specific power supply*1	—					
Sub clock pin (X0A, X1A) (Max 100 kHz)	Yes	No	Yes		No	
Clock monitor function	No					
Low voltage/CPU operation detection reset	No		No	Yes	No	Yes
Operating voltage range	3.5 V to 5.5 V : at normal operating (not using A/D converter) 4.0 V to 5.5 V : at using A/D converter/Flash programming 4.5 V to 5.5 V : at using external bus					
Operating temperature range	–40 °C to +105 °C (+125 °C up to 16 MHz machine clock)		–40 °C to +125 °C			
Package	LQFP-64					
UART	2 channels					
	Wide range of baud rate settings using a dedicated reload timer Special synchronous options for adapting to different synchronous serial protocols LIN functionality working either as master or slave LIN device					
I^2C (400 Kbps)	1 channel					
A/D Converter	15 channels					
	10-bit or 8-bit resolution Conversion time : Min 3 µs includes sample time (per one channel)					
16-bit Reload Timer (4 channels)	Operation clock frequency : fsys/2^1, fsys/2^3, fsys/2^5 (fsys = Machine clock frequency) Supports External Event Count function.					
16-bit I/O Timer (2 channels)	I/O Timer 0 (clock input FRCK0) corresponds to ICU 0/1. I/O Timer 1 (clock input FRCK1) corresponds to ICU 4/5/6/7, OCU 4/5/6/7.					
	Signals an interrupt when overflowing. Supports Timer Clear when a match with Output Compare (Channel 0, 4) . Operation clock frequency : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4, fsys/2^5, fsys/2^6, fsys/2^7 (fsys = Machine clock frequency)					
16-bit Output Compare	4 channels					
	Signals an interrupt when 16-bit I/O Timer matches with output compare registers. A pair of compare registers can be used to generate an output signal.					

(Continued)

(Continued)

Parameter \ Part Number	MB90F356A, MB90F357A	MB90F356TA, MB90F357TA	MB90F356AS, MB90F357AS	MB90F356TAS, MB90F357TAS
16-bit Input Capture	6 channels			
	Retains freerun timer value by (rising edge, falling edge or rising & falling edge), signals an interrupt.			
8/16-bit Programmable Pulse Generator	6 channels (16-bit)/10 channels (8-bit) 8-bit reload counters × 12 8-bit reload registers for L pulse width × 12 8-bit reload registers for H pulse width × 12			
	Supports 8-bit and 16-bit operation modes. A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler + 8-bit reload counter. Operation clock frequency : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4 or 128 µs@fosc = 4 MHz (fsys = Machine clock frequency, fosc = Oscillation clock frequency)			
CAN Interface	1 channel			
	Conforms to CAN Specification Version 2.0 Part A and B. Automatic re-transmission in case of error Automatic transmission responding to Remote Frame Prioritized 16 message buffers for data and ID Supports multiple messages. Flexible configuration of acceptance filtering : Full bit compare/Full bit mask/Two partial bit masks Supports up to 1 Mbps.			
External Interrupt	8 channels			
	Can be used rising edge, falling edge, starting up by H/L level input, external interrupt, extended intelligent I/O services (EI^{2}OS) and DMA.			
D/A converter	—			
I/O Ports	Virtually all external pins can be used as general purpose I/O port. All push-pull outputs Bit-wise settable as input/output or peripheral module signal Settable as CMOS schmitt trigger/ automotive inputs TTL input level settable for external bus (only for external bus pin)			
Flash Memory	Supports automatic programming, Embedded Algorithm™*2 Write/Erase/Erase-Suspend/Resume commands A flag indicating completion of the algorithm Number of erase cycles : 10,000 times Data retention time : 10 years Boot block configuration Erase can be performed on each block. Block protection with external programming voltage Flash Security Feature for protecting the content of the Flash (MB90F357x only)			
Corresponding EVA name	MB90V340A-104		MB90V340A-103	

*1 : It is setting of Jumper switch (TOOL VCC) when Emulator (MB2147-01) is used.
Please refer to the Emulator hardware manual about details.

*2 : Embedded Algorithm is a trademark of Advanced Micro Devices Inc.

■ PRODUCT LINEUP 4

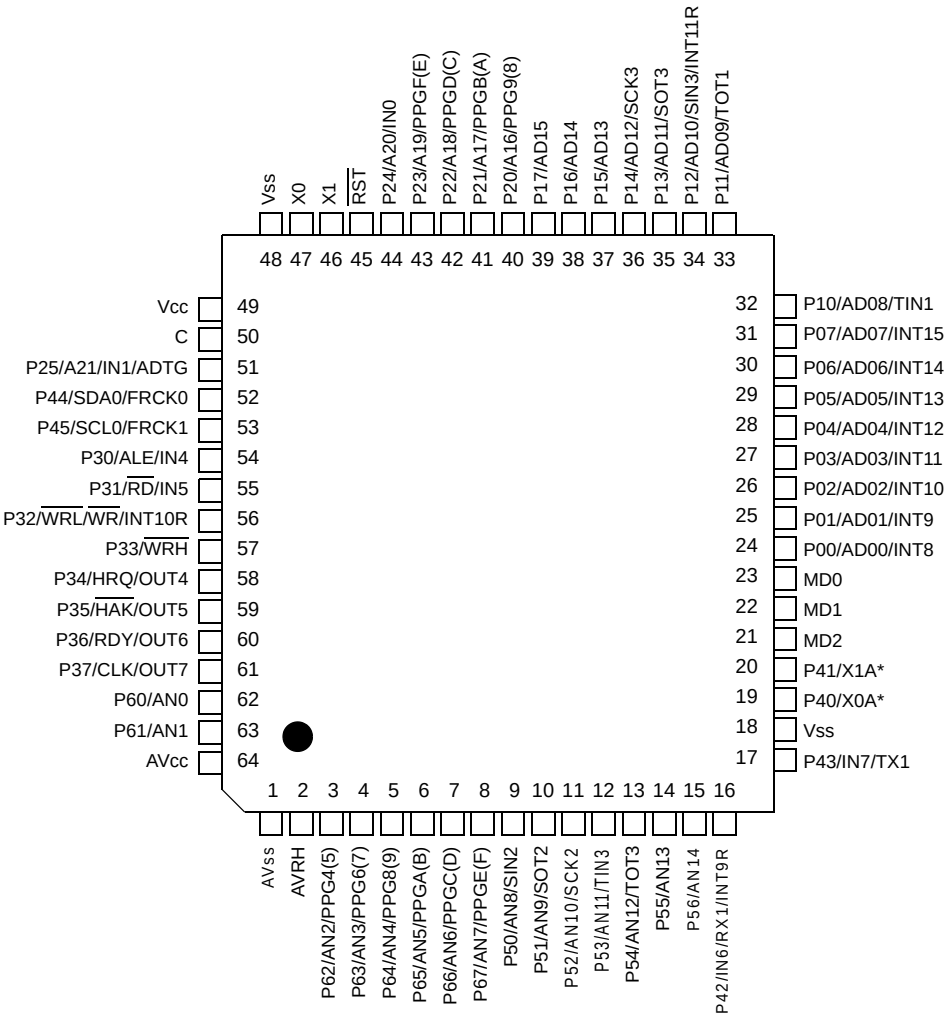
Part Number / Parameter	MB90356A, MB90357A	MB90356TA, MB90357TA	MB90356AS, MB90357AS	MB90356TAS, MB90357TAS	MB90V340A-103	MB90V340A-104
CPU	F²MC-16LX CPU					
System clock	On-chip PLL clock multiplier (×1, ×2, ×3, ×4, ×6, 1/2 when PLL stops) Minimum instruction execution time : 42 ns (oscillation clock 4 MHz, PLL × 6)					
ROM	MASK ROM 64Kbytes : MB90356A(S), MB90356TA(S) 128Kbytes : MB90357A(S), MB90357TA(S)				External	
RAM	4 Kbytes				30 Kbytes	
Emulator-specific power supply*	—				Yes	
Sub clock pin (X0A, X1A)	Yes		No (internal CR oscillation can be used as sub clock)		No (internal CR oscillation can be used as sub clock)	Yes
Clock monitor function	Yes					
Low voltage/CPU operation detection reset	No	Yes	No	Yes	No	
Operating voltage range	3.5 V to 5.5 V : at normal operating (not using A/D converter) 4.0 V to 5.5 V : at using A/D converter 4.5 V to 5.5 V : at using external bus				5 V ± 10%	
Operating temperature range	−40 °C to +125 °C				—	
Package	LQFP-64				PGA-299	
UART	2 channels				5 channels	
	Wide range of baud rate settings using a dedicated reload timer Special synchronous options for adapting to different synchronous serial protocols LIN functionality working either as master or slave LIN device					
I²C (400 Kbps)	1 channel				2 channels	
A/D Converter	15 channels				24 channels	
	10-bit or 8-bit resolution Conversion time : Min 3 µs includes sample time (per one channel)					
16-bit Reload Timer (4 channels)	Operation clock frequency : fsys/2^1, fsys/2^3, fsys/2^5 (fsys = Machine clock frequency) Supports External Event Count function.					
16-bit I/O Timer (2 channels)	I/O Timer 0 (clock input FRCK0) corresponds to ICU 0/1. I/O Timer 1 (clock input FRCK1) corresponds to ICU 4/5/6/7, OCU 4/5/6/7.				I/O Timer 0 corresponds to ICU 0/1/2/3, OCU 0/1/2/3. I/O Timer 1 corresponds to ICU 4/5/6/7, OCU 4/5/6/7.	
	Signals an interrupt when overflowing. Supports Timer Clear when a match with Output Compare (Channel 0, 4) . Operation clock frequency : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4, fsys/2^5, fsys/2^6, fsys/2^7 (fsys = Machine clock frequency)					

(Continued)

■ PIN ASSIGNMENTS

- MB90F351(S), MB90F352(S),MB90F351A(S), MB90F351TA(S), MB90F352A(S), MB90F352TA(S), MB90F356A(S), MB90F356TA(S), MB90F357A(S), MB90F357TA(S),MB90351A(S), MB90351TA(S), MB90352A(S), MB90352TA(S),MB90356A(S), MB90356TA(S), MB90357A(S), MB90357TA(S),

(TOP VIEW)
(LQFP-64P)



(FPT-64P-M09, FPT-64P-M23, FPT-64P-M24)

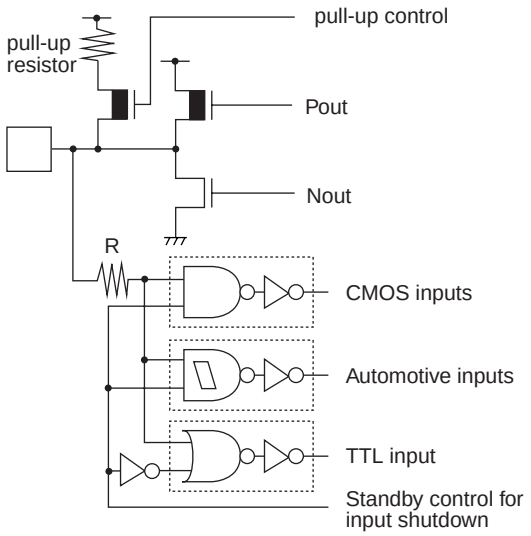
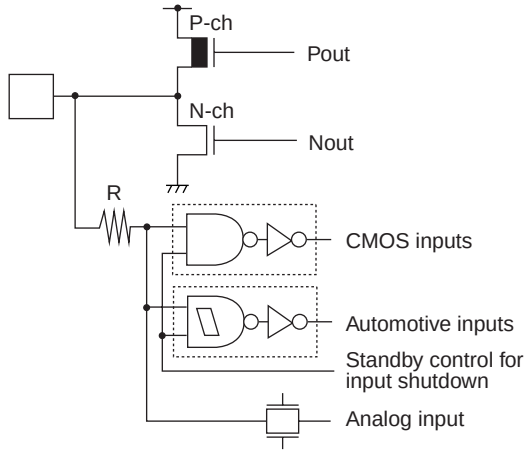
* : Devices without S-suffix : X0A, X1A
Devices with S-suffix : P40, P41

■ PIN DESCRIPTION

Pin No. LQFP64*	Pin name	Circuit type	Function
46	X1	A	Oscillation output pin
47	X0		Oscillation input pin
45	$\overline{RST}$	E	Reset input pin
3 to 8	P62 to P67	I	General purpose I/O ports
	AN2 to AN7		Analog input pins for A/D converter
	PPG4 (5) , 6 (7) , 8 (9) , A (B) , C (D) , E (F)		Output pins for PPGs
9	P50	O	General purpose I/O port
	AN8		Analog input pin for A/D converter
	SIN2		Serial data input pin for UART2
10	P51	I	General purpose I/O port
	AN9		Analog input pin for A/D converter
	SOT2		Serial data output pin for UART2
11	P52	I	General purpose I/O port
	AN10		Analog input pin for A/D converter
	SCK2		Serial clock I/O pin for UART2
12	P53	I	General purpose I/O port
	AN11		Analog input pin for A/D converter
	TIN3		Event input pin for reload timer3
13	P54	I	General purpose I/O port
	AN12		Analog input pin for A/D converter
	TOT3		Output pin for reload timer3
14, 15	P55, P56	I	General purpose I/O ports
	AN13, AN14		Analog input pins for A/D converter
16	P42	F	General purpose I/O port
	IN6		Data sample input pin for input capture ICU6
	RX1		RX input pin for CAN1
	INT9R		External interrupt request input pin for INT9
17	P43	F	General purpose I/O port
	IN7		Data sample input pin for input capture ICU7
	TX1		TX output pin for CAN1
19, 20	P40, P41	F	General purpose I/O ports (devices with S-suffix and MB90V340A-101/103)
	X0A, X1A	B	X0A : Oscillation input pins for sub clock X1A : Oscillation output pins for sub clock (devices without S-suffix and MB90V340A-102/104)

(Continued)

(Continued)

Type	Circuit	Remarks
N		• CMOS level output (I_{OL} = 4 mA, I_{OH} = –4 mA) • CMOS inputs (With the standby-time input shutdown function) • Automotive input (With the standby-time input shutdown function) • TTL input (With the standby-time input shutdown function) • Programmable pull-up resistor: approx. 50 kΩ
O		• CMOS level output (I_{OL} = 4 mA, I_{OH} = –4 mA) • CMOS inputs (With the standby-time input shutdown function) • Automotive input (With the standby-time input shutdown function) • A/D analog input

9. Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs

Make sure to turn on the A/D converter power supply (AV_{CC}, AVRH) and analog inputs (AN0 to AN14) after turning-on the digital power supply (V_{CC}) .

Turn-off the digital power after turning off the A/D converter power supply and analog inputs. In this case, make sure that the voltage does not exceed AVRH or AV_{CC} (turning on/off the analog and digital power supplies simultaneously is acceptable).

10. Connection of Unused Pins of A/D Converter if A/D Converter is used

Connect unused pins of A/D converter to $AV_{CC} = V_{CC}$, $AV_{SS} = AVRH = V_{SS}$.

11. Notes on Energization

To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during energization at 50 µs or more (0.2 V to 2.7 V) .

12. Stabilization of power supply voltage

A sudden change in the power supply voltage may cause the device to malfunction even within the specified V_{CC} power supply voltage operating range. Therefore, the V_{CC} power supply voltage should be stabilized.

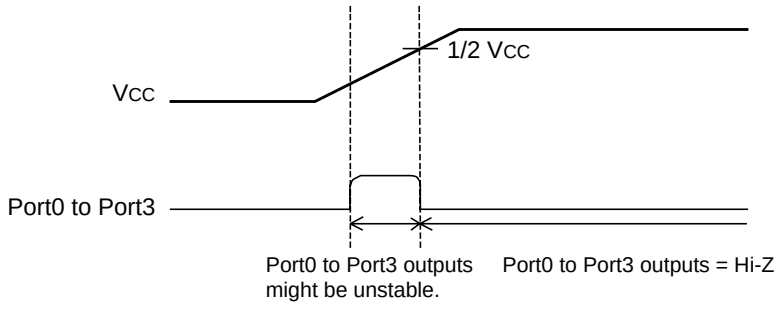
For reference, the power supply voltage should be controlled so that V_{CC} ripple variations (peak-to-peak value) at commercial frequencies (50 Hz to 60 Hz) fall below 10% of the standard V_{CC} power supply voltage and the coefficient of fluctuation does not exceed 0.1 V/ms at instantaneous power switching.

13. Initialization

In the device, there are internal registers which are initialized only by a power-on reset. To initialize these registers, turn on the power again.

14. Port 0 to port 3 output during Power-on (External-bus mode)

As shown below, when power is turned on in external-bus mode, there is a possibility that output signal of Port 0 to Port 3 might be unstable.



15. Notes on using CAN Function

To use CAN function, please set “1” to DIRECT bit of CAN direct mode register (CDMR).
If DIRECT bit is set to “0” (initial value), wait states will be performed when accessing CAN registers.

Note : Please refer to section “22.15 CAN Direct Mode Register” in Hardware Manual of MB90350 series for detail of CAN direct mode register.

16. Flash security Function

The security byte is located in the area of the flash memory.
If protection code 01_H is written in the security byte, the flash memory is in the protected state by security.
Therefore please do not write 01_H in this address if you do not use the security function.
Please refer to following table for the address of the security byte.

	Flash memory size	Address for security bit
MB90F352(S) MB90F352A(S) MB90F352TA(S) MB90F357A(S) MB90F357TA(S)	Embedded 1 Mbit Flash Memory	FE0001$_H$

17. Correspondence with T_A = +105 °C or more

If used exceeding T_A = +105 °C, please contact Fujitsu sales representatives for reliability limitations.

18. Low voltage/CPU operation reset circuit

The low voltage detection reset circuit is a function that monitors power supply voltage in order to detect when a voltage drops below a given voltage level. When a low voltage condition is detected, an internal reset signal is generated.
The CPU operation detection reset circuit is a 20-bit counter that uses oscillation as a count clock and generates an internal reset signal if not cleared within a given time after startup.

(1) Low voltage detection reset circuit

Detection voltage
4.0 V ± 0.3 V

When a low voltage condition is detected, the low voltage detection flag (LVRC : LVRF) is set to “1” and an internal reset signal is output.
Because the low voltage detection reset circuit continues to operate even in stop mode, detection of a low voltage condition generates an internal reset and releases stop mode.
During an internal RAM write cycle, low voltage reset is generated after the completion of writing. During the output of this internal reset, the reset output from the low voltage detection reset circuit is suppressed.

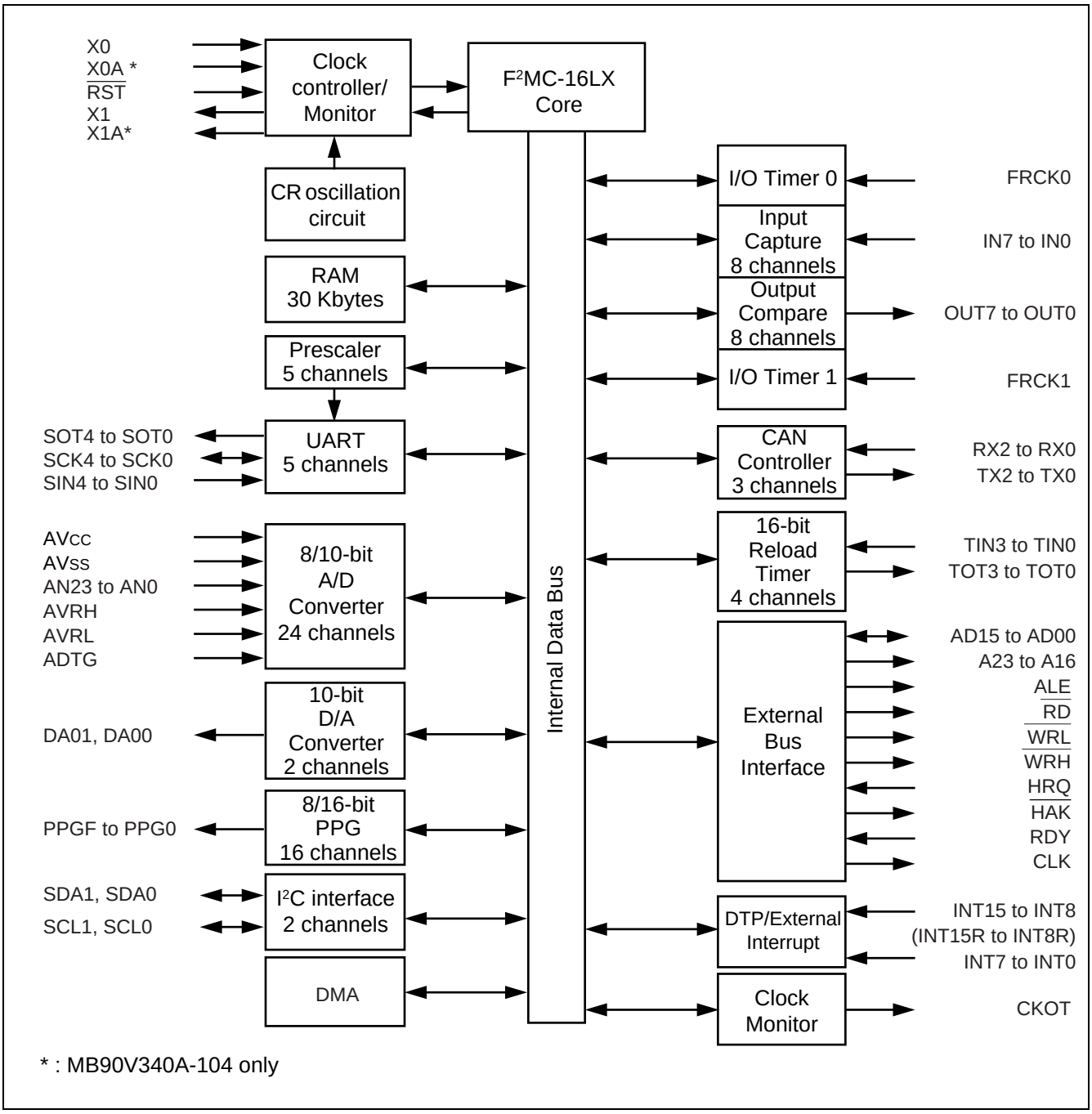
(2) CPU operation detection reset circuit

The CPU operation detection reset circuit is a counter that prevents program runaway. The counter starts automatically after a power-on reset, and must be continually cleared within a given time. If the given time interval elapses and the counter has not been cleared, a cause such as infinite program looping is assumed and an internal reset signal is generated. The internal reset generated from the CPU operation detection circuit has a width of 5 machine cycles.

Interval time
$2^{20}/F_C$ (approx. 262 ms*)

* : This value assumes the interval time at an oscillation clock frequency of 4 MHz.
During recovery from standby mode, the detection period is the maximum interval plus 20 µs.

- MB90V340A-103/104



* : MB90V340A-104 only

Address	Register	Abbreviation	Access	Resource name	Initial value
5E$_H$	Output Compare Control Status Register 6	OCS6	R/W	Output Compare 6/7	0000XX00$_B$
5F$_H$	Output Compare Control Status Register 7	OCS7	R/W		0XX00000$_B$
60$_H$	Timer Control Status Register 0	TMCSR0	R/W	16-bit Reload Timer 0	00000000$_B$
61$_H$	Timer Control Status Register 0	TMCSR0	R/W		XXXX0000$_B$
62$_H$	Timer Control Status Register 1	TMCSR1	R/W	16-bit Reload Timer 1	00000000$_B$
63$_H$	Timer Control Status Register 1	TMCSR1	R/W		XXXX0000$_B$
64$_H$	Timer Control Status Register 2	TMCSR2	R/W	16-bit Reload Timer 2	00000000$_B$
65$_H$	Timer Control Status Register 2	TMCSR2	R/W		XXXX0000$_B$
66$_H$	Timer Control Status Register 3	TMCSR3	R/W	16-bit Reload Timer 3	00000000$_B$
67$_H$	Timer Control Status Register 3	TMCSR3	R/W		XXXX0000$_B$
68$_H$	A/D Control Status Register 0	ADCS0	R/W	A/D Converter	000XXXX0$_B$
69$_H$	A/D Control Status Register 1	ADCS1	R/W		0000000X$_B$
6A$_H$	A/D Data Register 0	ADCR0	R		00000000$_B$
6B$_H$	A/D Data Register 1	ADCR1	R		XXXXXX00$_B$
6C$_H$	ADC Setting Register 0	ADSR0	R/W		00000000$_B$
6D$_H$	ADC Setting Register 1	ADSR1	R/W		00000000$_B$
6E$_H$	Low Voltage/CPU Operation Detection Reset Control Register	LVRC	R/W, W	Low Voltage/CPU Operation Detection Reset	00111000$_B$
6F$_H$	ROM Mirror Function Select Register	ROMM	W	ROM Mirror	XXXXXXX1$_B$
70$_H$ to 7F$_H$	Reserved				
80$_H$ to 8F$_H$	Reserved for CAN Interface 1. Refer to “■ CAN CONTROLLERS”				
90$_H$ to 9A$_H$	Reserved				
9B$_H$	DMA Descriptor Channel Specification Register	DCSR	R/W	DMA	00000000$_B$
9C$_H$	DMA Status Register L	DSRL	R/W		00000000$_B$
9D$_H$	DMA Status Register H	DSRH	R/W		00000000$_B$
9E$_H$	Address Detect Control Register 0	PACSR0	R/W	Address Match Detection 0	00000000$_B$
9F$_H$	Delayed Interrupt/Release Register	DIRR	R/W	Delayed Interrupt	XXXXXXX0$_B$
A0$_H$	Low-power Consumption Mode Control Register	LPMCR	W,R/W	Low Power Consumption Control Circuit	00011000$_B$
A1$_H$	Clock Selection Register	CKSCR	R,R/W	Low Power Consumption Control Circuit	11111100$_B$
A2$_H$, A3$_H$	Reserved				

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
7950H	Serial Mode Register 3	SMR3	W, R/W	UART3	00000000B
7951H	Serial Control Register 3	SCR3	W, R/W		00000000B
7952H	Reception/Transmission Data Register 3	RDR3/ TDR3	R/W		00000000B
7953H	Serial Status Register 3	SSR3	R,R/W		00001000B
7954H	Extended Communication Control Register 3	ECCR3	R,W, R/W		000000XXB
7955H	Extended Status/Control Register 3	ESCR3	R/W		00000100B
7956H	Baud Rate Generator Register 30	BGR30	R/W		00000000B
7957H	Baud Rate Generator Register 31	BGR31	R/W		00000000B
7958H, 7959H	Reserved				
7960H	Clock Monitor Function Control Register	CSVCR	R, R/W	Clock Monitor	00011100B
7961H to 796DH	Reserved				
796EH	CAN Direct Mode Register	CDMR	R/W	CAN Clock Sync	XXXXXXX0B
796FH	Reserved				
7970H	I²C Bus Status Register 0	IBSR0	R	I²C Interface 0	00000000B
7971H	I²C Bus Control Register 0	IBCR0	W,R/W		00000000B
7972H	I²C 10-bit Slave Address Register 0	ITBAL0	R/W		00000000B
7973H		ITBAH0	R/W		00000000B
7974H	I²C 10-bit Slave Address Mask Register 0	ITMKL0	R/W		11111111B
7975H		ITMKH0	R/W		00111111B
7976H	I²C 7-bit Slave Address Register 0	ISBA0	R/W		00000000B
7977H	I²C 7-bit Slave Address Mask Register 0	ISMK0	R/W		01111111B
7978H	I²C data register 0	IDAR0	R/W		00000000B
7979H, 797AH	Reserved				
797BH	I²C Clock Control Register 0	ICCR0	R/W	I²C Interface 0	00011111B
797CH to 79A1H	Reserved				
79A2H	Flash Write Control Register 0	FWR0	R/W	Dual Operation Flash	00000000B
79A3H	Flash Write Control Register 1	FWR1	R/W		00000000B
79A4H	Sector Change Setting Register	SSR0	R/W		00XXXXX0B
79A5H to 79C1H	Reserved				

(Continued)

(MB90F352(S)/MB90F351(S): T_A = –40 °C to +105 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)
(MB90F352(S)/MB90F351(S): T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 16 MHz, V_{SS} = AV_{SS} = 0 V)
(Device other than above: T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I_{CCL}	V_{CC}	V_{CC} = 5.0 V, Internal frequency: 8 kHz, During operating clock monitor function, At sub clock operation T_A = +25°C	—	100	200	µA	MB90F356A MB90F357A MB90356A MB90357A
			V_{CC} = 5.0 V, Internal CR oscillation/ 4 division, At sub clock operation T_A = +25°C	—	100	200	µA	MB90F356AS MB90F357AS MB90356AS MB90357AS
			V_{CC} = 5.0 V, Internal frequency: 8 kHz, During stopping clock monitor function, At sub clock operation T_A = +25°C	—	120	240	µA	MB90F351TA MB90F352TA MB90F356TA MB90F357TA MB90351TA MB90352TA MB90356TA MB90357TA
			V_{CC} = 5.0 V, Internal frequency: 8 kHz, During operating clock monitor function, At sub clock operation T_A = +25°C	—	150	300	µA	MB90F356TA MB90F357TA MB90356TA MB90357TA
			V_{CC} = 5.0 V, Internal CR oscillation/ 4 division, At sub clock operation T_A = +25°C	—	150	300	µA	MB90F356TAS MB90F357TAS MB90356TAS MB90357TAS
	I_{CCLS}		V_{CC} = 5.0 V, Internal frequency: 8 kHz, During stopping clock monitor function, At sub sleep T_A = +25°C	—	20	50	µA	MB90F351 MB90F352 MB90F351A MB90F352A MB90F356A MB90F357A MB90351A MB90352A MB90356A MB90357A

(Continued)

4. AC Characteristics

(1) Clock Timing

(MB90F352(S)/MB90F351(S): T_A = –40 °C to +105 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)
(MB90F352(S)/MB90F351(S): T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 16 MHz, V_{SS} = AV_{SS} = 0 V)
(Device other than above: T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_C	X0, X1	3	—	16	MHz	1/2 (at PLL stop) When using an oscillation circuit
			4	—	16	MHz	1 multiplied PLL When using an oscillation circuit
			4	—	12	MHz	2 multiplied PLL When using an oscillation circuit
			4	—	8	MHz	3 multiplied PLL When using an oscillation circuit
			4	—	6	MHz	4 multiplied PLL When using an oscillation circuit
			—	—	4	MHz	6 multiplied PLL When using an oscillation circuit
		X0	3	—	24	MHz	1/2 (at PLL stop), When using an external clock
			4	—	24	MHz	1 multiplied PLL When using an external clock
			4	—	12	MHz	2 multiplied PLL When using an external clock
			4	—	8	MHz	3 multiplied PLL When using an external clock
			4	—	6	MHz	4 multiplied PLL When using an external clock
			—	—	4	MHz	6 multiplied PLL When using an external clock
	f_{CL}	X0A, X1A	—	32.768	100	kHz	
Clock cycle time	t_{CYL}	X0, X1	62.5	—	333	ns	When using an oscillation circuit
		X0	41.67	—	333	ns	When using an external clock
	t_{CYLL}	X0A, X1A	10	30.5	—	µs	
Input clock pulse width	P_{WH}, P_{WL}	X0	10	—	—	ns	Duty ratio is about 30% to 70%.
	P_{WHL}, P_{WLL}	X0A	5	15.2	—	µs	
Input clock rise and fall time	t_{CR}, t_{CF}	X0	—	—	5	ns	When using an external clock

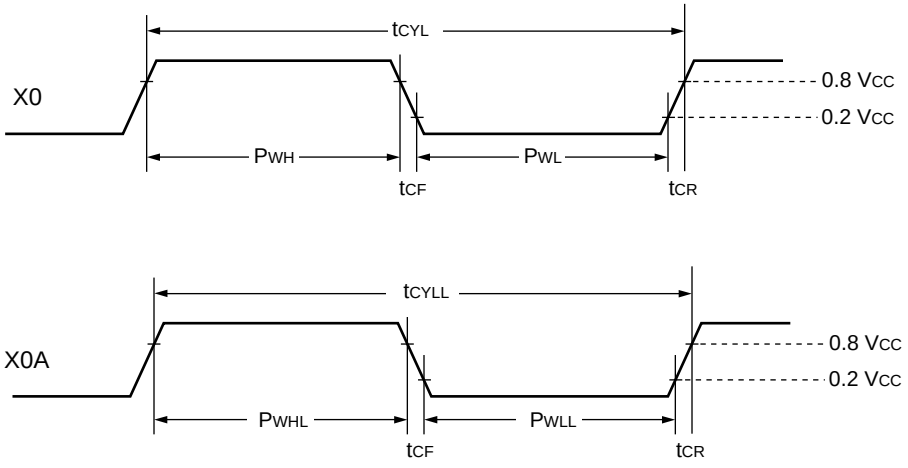
(Continued)

(Continued)

(MB90F352(S)/MB90F351(S): T_A = –40 °C to +105 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)
(MB90F352(S)/MB90F351(S): T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 16 MHz, V_{SS} = AV_{SS} = 0 V)
(Device other than above: T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Internal operating clock frequency (machine clock)	f_{CP}	—	1.5	—	24	MHz	MB90F352/(S), MB90F351/(S) When using main clock (T_A ≤ +105 °C)
					16		MB90F352/(S), MB90F351/(S) When using main clock (T_A ≤ +125 °C)
			1.5	—	24	MHz	Device other than above, When using main clock
	f_{CPL}	—	—	8.192	50	kHz	When using sub clock
Internal operating clock cycle time (machine clock)	t_{CP}	—	41.67	—	666	ns	MB90F352/(S), MB90F351/(S) When using main clock (T_A ≤ +105 °C)
			62.5				MB90F352/(S), MB90F351/(S) When using main clock (T_A ≤ +125 °C)
			41.67	—	666	ns	Device other than above, When using main clock
	t_{CPL}	—	20	122.1	—	µs	When using sub clock

• Clock Timing

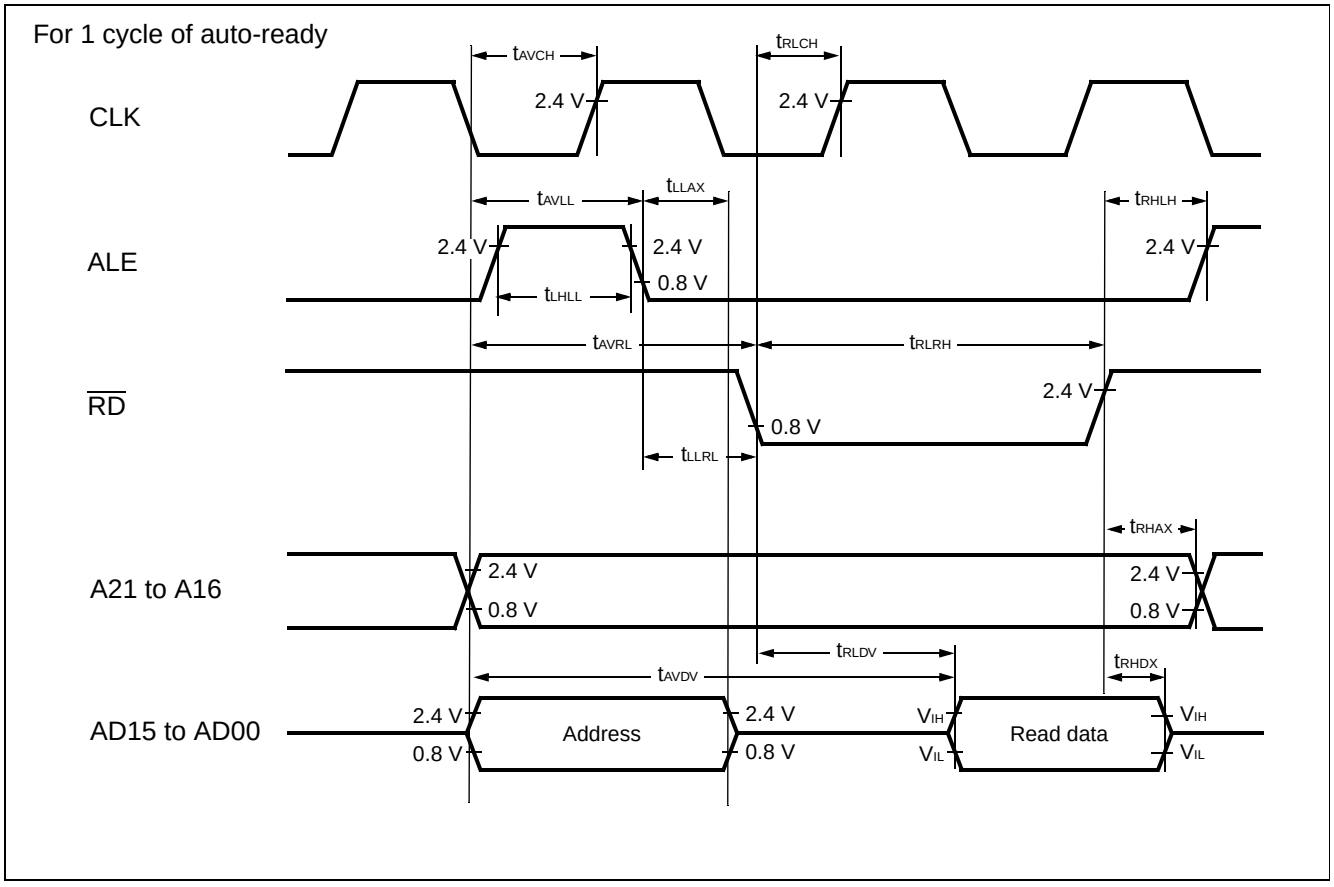


(5) Bus Timing (Read)

(T_A = –40°C to +105°C, V_{CC} = 5.0 V ± 10 %, V_{SS} = 0.0 V, f_{CP} ≤ 24 MHz)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
ALE pulse width	t_{LHLL}	ALE	—	$t_{CP}/2 - 10$	—	ns	
Valid address ⇒ ALE ↓ time	t_{AVLL}	ALE, A21 to A16, AD15 to AD00		$t_{CP}/2 - 20$	—	ns	
ALE ↓ ⇒ Address valid time	t_{LLAX}	ALE, AD15 to AD00		$t_{CP}/2 - 15$	—	ns	
Valid address ⇒ $\overline{RD}$ ↓ time	t_{AVRL}	A21 toA16, AD15 to AD00, $\overline{RD}$		$t_{CP} - 15$	—	ns	
Valid address ⇒ Valid data input	t_{AVDV}	A21 to A16, AD15 to AD00		—	$5\ t_{CP}/2 - 60$	ns	
$\overline{RD}$ pulse width	t_{RLRH}	$\overline{RD}$		$(n^*+3/2)\ t_{CP} - 20$	—	ns	
$\overline{RD}$ ↓ ⇒ Valid data input	t_{RLDV}	$\overline{RD}$, AD15 to AD00		—	$(n^*+3/2)\ t_{CP} - 50$	ns	
$\overline{RD}$ ↑ ⇒ Data hold time	t_{RHDX}	$\overline{RD}$, AD15 to AD00		0	—	ns	
$\overline{RD}$ ↑ ⇒ ALE ↑ time	t_{RHLH}	$\overline{RD}$, ALE		$t_{CP}/2 - 15$	—	ns	
$\overline{RD}$ ↑ ⇒ Address valid time	t_{RHAX}	$\overline{RD}$, A21 to A16		$t_{CP}/2 - 10$	—	ns	
Valid address ⇒ CLK ↑ time	t_{AVCH}	A21 to A16, AD15 to AD00, CLK		$t_{CP}/2 - 16$	—	ns	
$\overline{RD}$ ↓ ⇒ CLK ↑ time	t_{RLCH}	$\overline{RD}$, CLK		$t_{CP}/2 - 15$	—	ns	
ALE ↓ ⇒ $\overline{RD}$ ↓ time	t_{LLRL}	ALE, $\overline{RD}$		$t_{CP}/2 - 15$	—	ns	

* : n: number of ready cycles


For 1 cycle of auto-ready
CLK
ALE
RD
A21 to A16
AD15 to AD00
tAVCH
tRLCH
2.4 V
tAVLL
tLLAX
tRHLH
0.8 V
tLHLL
tAVRL
tRLRH
tLLRL
tRHAX
tRLDV
tRHDX
tAVDV
Address
Read data
VIH
VIL

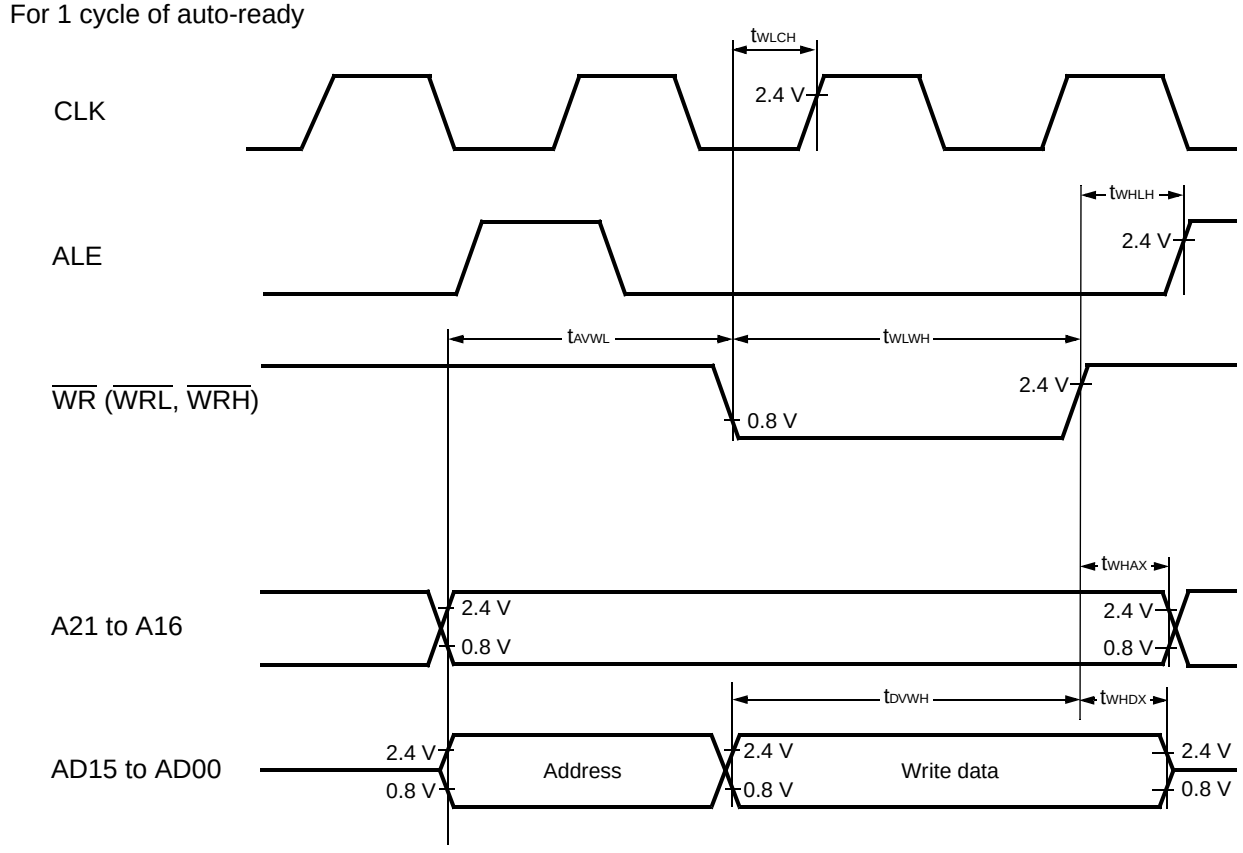
(6) Bus Timing (Write)

(T_A = –40°C to +105°C, V_{CC} = 5.0 V ± 10 %, V_{SS} = 0.0 V, f_{CP} ≤ 24 MHz)

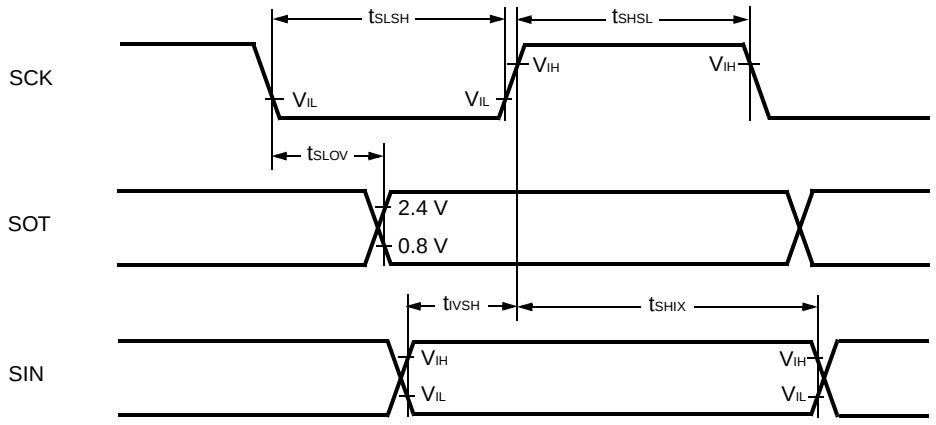
Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Valid address ⇒ $\overline{WR}$ ↓ time	t_{AVWL}	A21 to A16, AD15 to AD00, $\overline{WR}$	—	t_{CP}–15	—	ns	
$\overline{WR}$ pulse width	t_{WLWH}	$\overline{WR}$		(n*+3/2)t_{CP} – 20	—	ns	
Valid data output ⇒ $\overline{WR}$ ↑ time	t_{DVWH}	AD15 to AD00, $\overline{WR}$		(n*+3/2)t_{CP} – 20	—	ns	
$\overline{WR}$ ↑ ⇒ Data hold time	t_{WHDX}	AD15 to AD00, $\overline{WR}$		15	—	ns	
$\overline{WR}$ ↑ ⇒ Address valid time	t_{WHAX}	A21 to A16, $\overline{WR}$		t_{CP}/2 – 10	—	ns	
$\overline{WR}$ ↑ ⇒ ALE ↑ time	t_{WHLH}	$\overline{WR}$, ALE		t_{CP}/2 – 15	—	ns	
$\overline{WR}$ ↓ ⇒ CLK ↑ time	t_{WLCH}	$\overline{WR}$, CLK		t_{CP}/2 – 15	—	ns	

* : n: Number of ready cycles

For 1 cycle of auto-ready



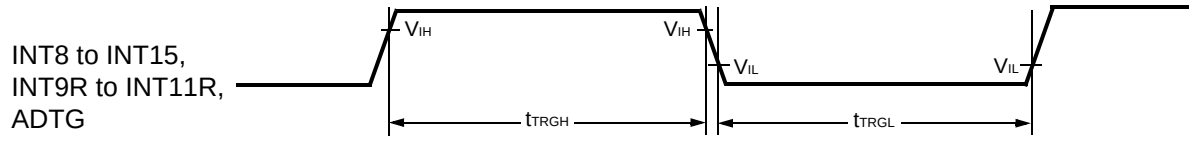
- External Shift Clock Mode



(10) Trigger Input Timing

(MB90F352(S)/MB90F351(S): T_A = –40 °C to +105 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)
(MB90F352(S)/MB90F351(S): T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 16 MHz, V_{SS} = AV_{SS} = 0 V)
(Device other than above: T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH} t_{TRGL}	INT8 to INT15, INT9R to INT11R, ADTG	—	5 t_{CP}	—	ns	

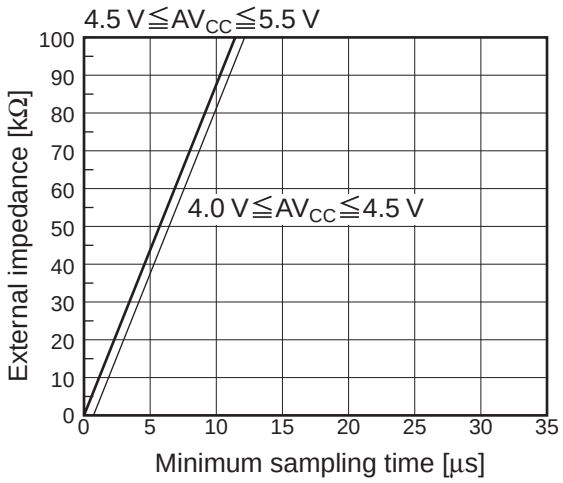


• Flash memory device

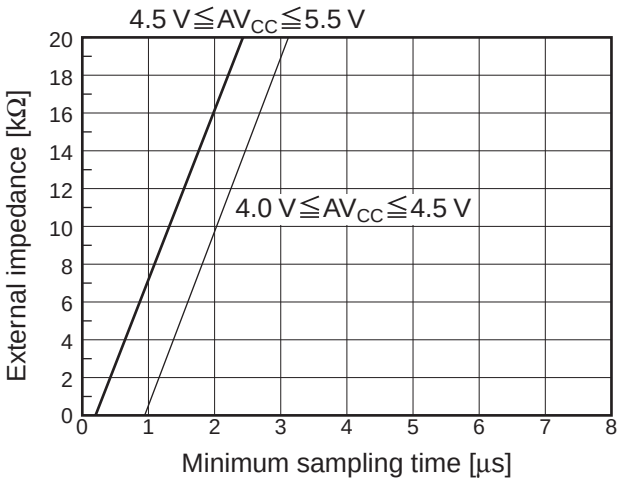
· Relation between External impedance and minimum sampling time

(MB90F352(S), MB90F351A(S), MB90F352A(S), MB90F351TA(S), MB90F352TA(S), MB90F356A(S), MB90F357A(S), MB90F356TA(S), MB90F357TA(S))

[External impedance = 0 kΩ to 100 kΩ]



[External impedance = 0 kΩ to 20 kΩ]

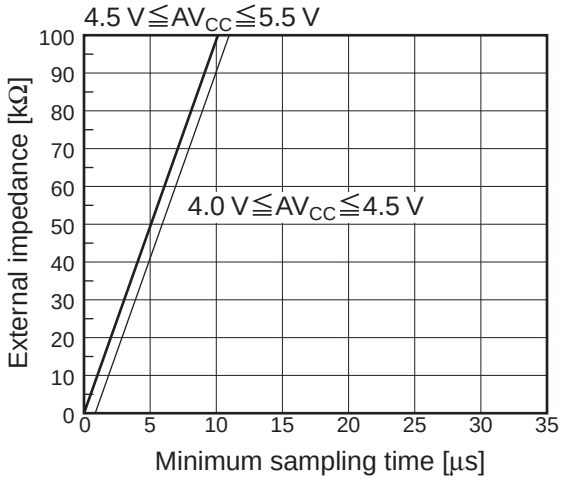


• MASK ROM device

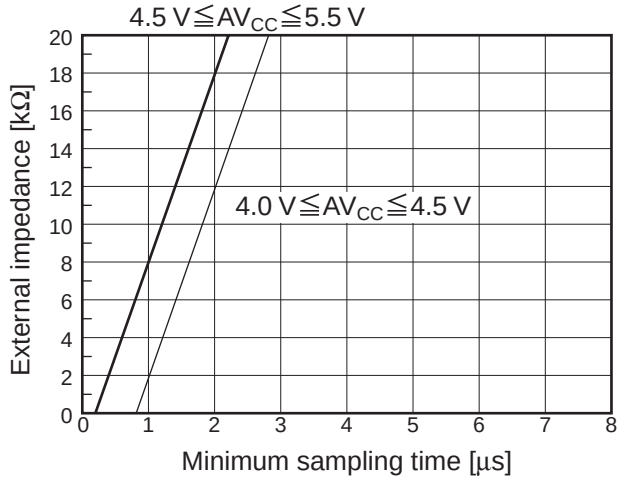
· Relation between External impedance and minimum sampling time

(MB90V340A-101/102/103/104, MB90351A(S), MB90352A(S), MB90351TA(S), MB90352TA(S), MB90356A(S), MB90357A(S), MB90356TA(S), MB90357TA(S))

[External impedance = 0 kΩ to 100 kΩ]



[External impedance = 0 kΩ to 20kΩ]



• **About the error**

Values of relative errors grow larger, as |AVRH – AVSS| becomes smaller.

7. Flash Memory Program/Erase Characteristics

Flash Memory

Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	T_A = +25 °C V_{CC} = 5.0 V	—	1	15	s	Excludes programming prior to erasure
Chip erase time		—	9	—	s	Excludes programming prior to erasure
Word (16-bit width) programming time		—	16	3,600	µs	Except for the overhead time of the system level
Program/Erase cycle	—	10,000	—	—	cycle	
Flash Memory Data Retention Time	Average T_A = +85 °C	20	—	—	year	*

* : This value comes from the technology qualification.
(Using Arrhenius equation to translate high temperature measurements into normalized value at +85 °C)

Dual Operation Flash Memory

Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time (4 Kbytes sector)	T_A = +25 °C V_{CC} = 5.0 V	—	0.2	0.5	s	Excludes programming prior to erasure
Sector erase time (16 Kbytes sector)		—	0.5	7.5	s	Excludes programming prior to erasure
Chip erase time		—	4.6	—	s	Excludes programming prior to erasure
Word (16-bit width) programming time		—	64	3,600	µs	Except for the overhead time of the system level
Program/Erase cycle	—	10,000	—	—	cycle	
Flash Memory Data Retention Time	Average T_A = +85 °C	20	—	—	year	*

* : This value comes from the technology qualification.
(Using Arrhenius equation to translate high temperature measurements into normalized value at +85 °C)