Infineon Technologies - MB90F352SPFM-GS-114E1 Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	24MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, WDT
Number of I/O	51
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 15x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-QFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f352spfm-gs-114e1

■ PRODUCT LINEUP 1

Part Number / Parameter	MB90F351, MB90F352	MB90F351S, MB90F352S	MB90F351A, MB90F352A	MB90F351TA, MB90F352TA	MB90F351AS, MB90F352AS	MB90F351TAS, MB90F352TAS
CPU	F^2MC-16LX CPU					
System clock	On-chip PLL clock multiplier (×1, ×2, ×3, ×4, ×6, 1/2 when PLL stops) Minimum instruction execution time : 42 ns (oscillation clock 4 MHz, PLL × 6)					
ROM	Flash memory 64Kbytes : MB90F351(S) 128Kbytes : MB90F352(S)		Dual operation flash memory 64Kbytes : MB90F351A(S), MB90F351TA(S) 128Kbytes : MB90F352A(S), MB90F352TA(S)			
RAM	4 Kbytes					
Emulator-specific power supply*1	—					
Sub clock pin (X0A, X1A) (Max 100 kHz)	Yes	No	Yes		No	
Clock monitor function	No					
Low voltage/CPU operation detection reset	No		No	Yes	No	Yes
Operating voltage range	3.5 V to 5.5 V : at normal operating (not using A/D converter) 4.0 V to 5.5 V : at using A/D converter/Flash programming 4.5 V to 5.5 V : at using external bus					
Operating temperature range	–40 °C to +105 °C (+125 °C up to 16 MHz machine clock)		–40 °C to +125 °C			
Package	LQFP-64					
UART	2 channels					
	Wide range of baud rate settings using a dedicated reload timer Special synchronous options for adapting to different synchronous serial protocols LIN functionality working either as master or slave LIN device					
I^2C (400 Kbps)	1 channel					
A/D Converter	15 channels					
	10-bit or 8-bit resolution Conversion time : Min 3 µs includes sample time (per one channel)					
16-bit Reload Timer (4 channels)	Operation clock frequency : fsys/2^1, fsys/2^3, fsys/2^5 (fsys = Machine clock frequency) Supports External Event Count function.					
16-bit I/O Timer (2 channels)	I/O Timer 0 (clock input FRCK0) corresponds to ICU 0/1. I/O Timer 1 (clock input FRCK1) corresponds to ICU 4/5/6/7, OCU 4/5/6/7.					
	Signals an interrupt when overflowing. Supports Timer Clear when a match with Output Compare (Channel 0, 4) . Operation clock frequency : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4, fsys/2^5, fsys/2^6, fsys/2^7 (fsys = Machine clock frequency)					
16-bit Output Compare	4 channels					
	Signals an interrupt when 16-bit I/O Timer matches with output compare registers. A pair of compare registers can be used to generate an output signal.					

(Continued)

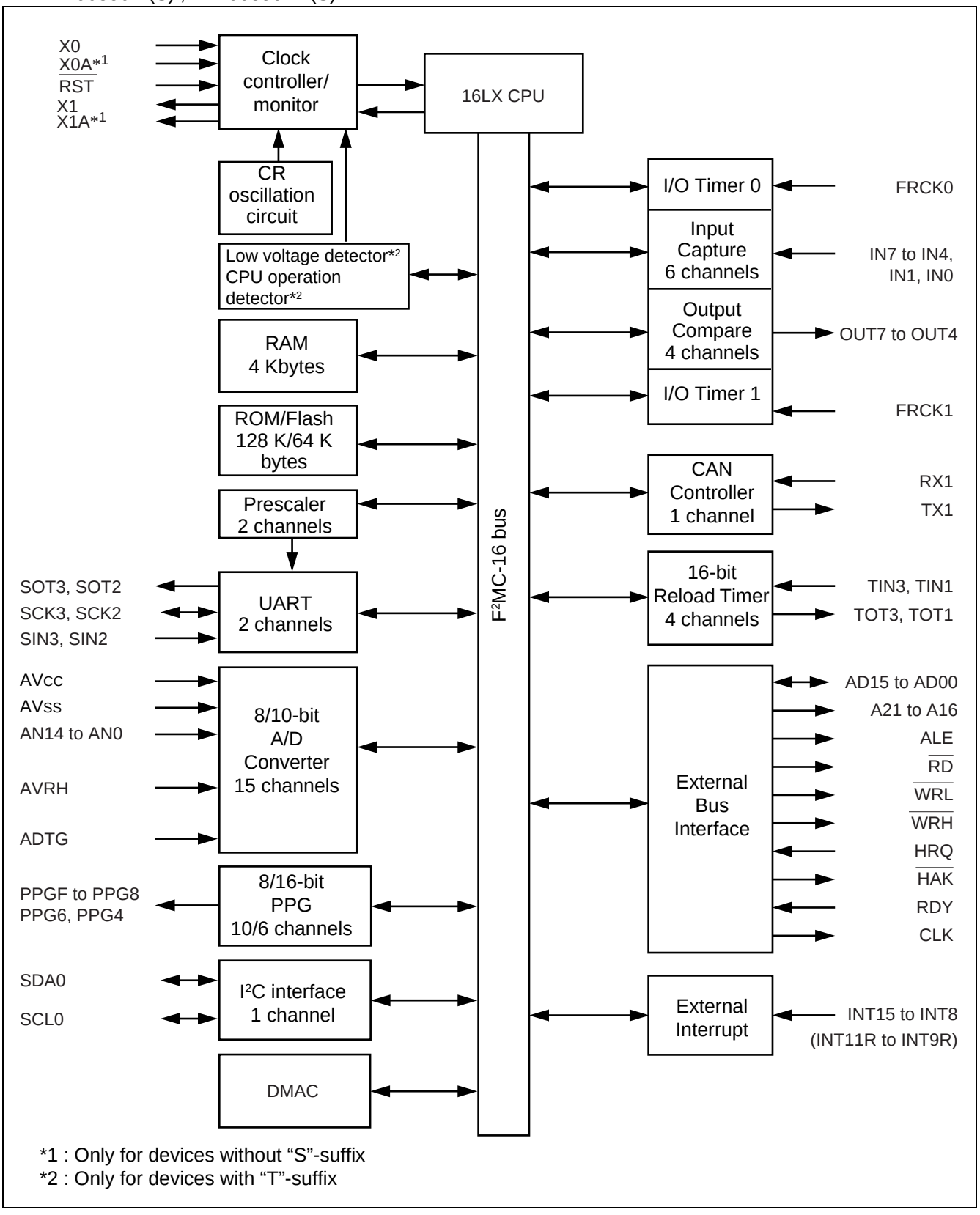
(Continued)

Parameter \ Part Number	MB90F356A, MB90F357A	MB90F356TA, MB90F357TA	MB90F356AS, MB90F357AS	MB90F356TAS, MB90F357TAS
16-bit Input Capture	6 channels			
	Retains freerun timer value by (rising edge, falling edge or rising & falling edge), signals an interrupt.			
8/16-bit Programmable Pulse Generator	6 channels (16-bit)/10 channels (8-bit) 8-bit reload counters × 12 8-bit reload registers for L pulse width × 12 8-bit reload registers for H pulse width × 12			
	Supports 8-bit and 16-bit operation modes. A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler + 8-bit reload counter. Operation clock frequency : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4 or 128 µs@fosc = 4 MHz (fsys = Machine clock frequency, fosc = Oscillation clock frequency)			
CAN Interface	1 channel			
	Conforms to CAN Specification Version 2.0 Part A and B. Automatic re-transmission in case of error Automatic transmission responding to Remote Frame Prioritized 16 message buffers for data and ID Supports multiple messages. Flexible configuration of acceptance filtering : Full bit compare/Full bit mask/Two partial bit masks Supports up to 1 Mbps.			
External Interrupt	8 channels			
	Can be used rising edge, falling edge, starting up by H/L level input, external interrupt, extended intelligent I/O services (EI^{2}OS) and DMA.			
D/A converter	—			
I/O Ports	Virtually all external pins can be used as general purpose I/O port. All push-pull outputs Bit-wise settable as input/output or peripheral module signal Settable as CMOS schmitt trigger/ automotive inputs TTL input level settable for external bus (only for external bus pin)			
Flash Memory	Supports automatic programming, Embedded Algorithm™*2 Write/Erase/Erase-Suspend/Resume commands A flag indicating completion of the algorithm Number of erase cycles : 10,000 times Data retention time : 10 years Boot block configuration Erase can be performed on each block. Block protection with external programming voltage Flash Security Feature for protecting the content of the Flash (MB90F357x only)			
Corresponding EVA name	MB90V340A-104		MB90V340A-103	

*1 : It is setting of Jumper switch (TOOL VCC) when Emulator (MB2147-01) is used.
Please refer to the Emulator hardware manual about details.

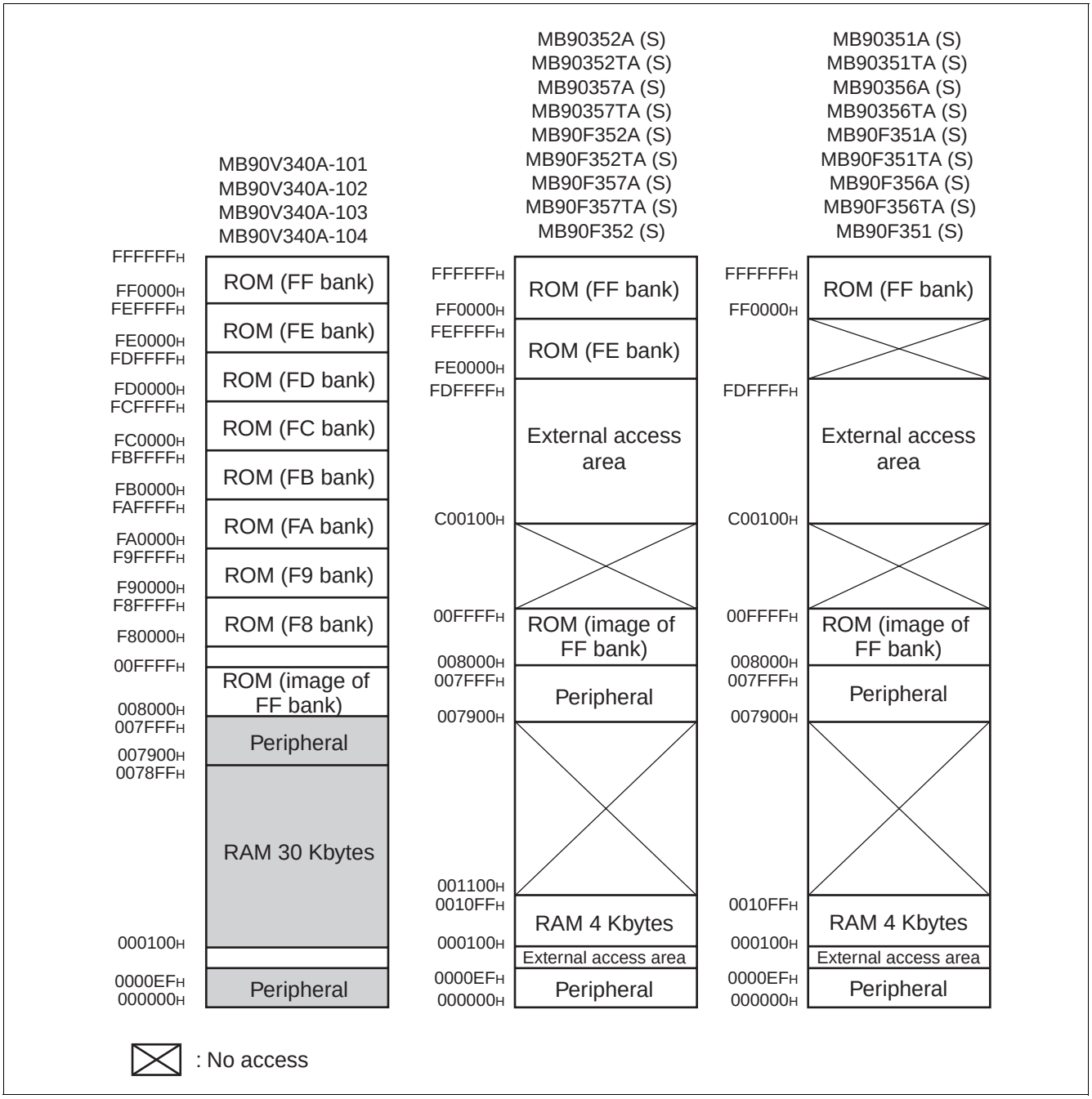
*2 : Embedded Algorithm is a trademark of Advanced Micro Devices Inc.

- MB90F357A (S) , MB90F357TA (S) , MB90F356A (S) , MB90F356TA (S) , MB90357A (S) , MB90357TA (S) , MB90356A (S) , MB90356TA (S)



*1 : Only for devices without “S”-suffix
*2 : Only for devices with “T”-suffix

■ MEMORY MAP



Note : The high-order portion of bank 00 gives the image of the FF bank ROM to make the small model of the C compiler effective. Since the low-order 16 bits are the same, the table in ROM can be referenced without using the far specification in the pointer declaration.
For example, an attempt to access 00C000H accesses the value at FFC000H in ROM.
The ROM area in bank FF exceeds 32 Kbytes, and its entire image cannot be shown in bank 00.
The image between FF8000H and FFFFFFH is visible in bank 00, while the image between FF0000H and FF7FFFH is visible only in bank FF.

Address	Register	Abbreviation	Access	Resource name	Initial value
3C$_H$	PPG 6 Operation Mode Control Register	PPGC6	W, R/W	16-bit Programmable Pulse Generator 6/7	0X000XX1$_B$
3D$_H$	PPG 7 Operation Mode Control Register	PPGC7	W, R/W		0X000001$_B$
3E$_H$	PPG 6/7 Count Clock Select Register	PPG67	R/W		000000X0$_B$
3F$_H$	Reserved				
40$_H$	PPG 8 Operation Mode Control Register	PPGC8	W, R/W	16-bit Programmable Pulse Generator 8/9	0X000XX1$_B$
41$_H$	PPG 9 Operation Mode Control Register	PPGC9	W, R/W		0X000001$_B$
42$_H$	PPG 8/9 Count Clock Select Register	PPG89	R/W		000000X0$_B$
43$_H$	Reserved				
44$_H$	PPG A Operation Mode Control Register	PPGCA	W, R/W	16-bit Programmable Pulse Generator A/B	0X000XX1$_B$
45$_H$	PPG B Operation Mode Control Register	PPGCB	W, R/W		0X000001$_B$
46$_H$	PPG A/B Count Clock Select Register	PPGAB	R/W		000000X0$_B$
47$_H$	Reserved				
48$_H$	PPG C Operation Mode Control Register	PPGCC	W,R/W	16-bit Programmable Pulse Generator C/D	0X000XX1$_B$
49$_H$	PPG D Operation Mode Control Register	PPGCD	W,R/W		0X000001$_B$
4A$_H$	PPG C/D Count Clock Select Register	PPGCD	R/W		000000X0$_B$
4B$_H$	Reserved				
4C$_H$	PPG E Operation Mode Control Register	PPGCE	W,R/W	16-bit Programmable Pulse Generator E/F	0X000XX1$_B$
4D$_H$	PPG F Operation Mode Control Register	PPGCF	W,R/W		0X000001$_B$
4E$_H$	PPG E/F Count Clock Select Register	PPGEF	R/W		000000X0$_B$
4F$_H$	Reserved				
50$_H$	Input Capture Control Status Register 0/1	ICS01	R/W	Input Capture 0/1	00000000$_B$
51$_H$	Input Capture Edge Register 0/1	ICE01	R/W, R		XXX0X0XX$_B$
52$_H$, 53$_H$	Reserved				
54$_H$	Input Capture Control Status Register 4/5	ICS45	R/W	Input Capture 4/5	00000000$_B$
55$_H$	Input Capture Edge Register 4/5	ICE45	R		XXXXXXXX$_B$
56$_H$	Input Capture Control Status Register 6/7	ICS67	R/W	Input Capture 6/7	00000000$_B$
57$_H$	Input Capture Edge Register 6/7	ICE67	R/W, R		XXX000XX$_B$
58$_H$ to 5B$_H$	Reserved				
5C$_H$	Output Compare Control Status Register 4	OCS4	R/W	Output Compare 4/5	0000XX00$_B$
5D$_H$	Output Compare Control Status Register 5	OCS5	R/W		0XX00000$_B$

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
792C$_H$	Input Capture Register 6	IPCP6	R	Input Capture 6/7	XXXXXXXX$_B$
792D$_H$	Input Capture Register 6	IPCP6	R		XXXXXXXX$_B$
792E$_H$	Input Capture Register 7	IPCP7	R		XXXXXXXX$_B$
792F$_H$	Input Capture Register 7	IPCP7	R		XXXXXXXX$_B$
7930$_H$ to 7937$_H$	Reserved				
7938$_H$	Output Compare Register 4	OCCP4	R/W	Output Compare 4/5	XXXXXXXX$_B$
7939$_H$	Output Compare Register 4	OCCP4	R/W		XXXXXXXX$_B$
793A$_H$	Output Compare Register 5	OCCP5	R/W		XXXXXXXX$_B$
793B$_H$	Output Compare Register 5	OCCP5	R/W		XXXXXXXX$_B$
793C$_H$	Output Compare Register 6	OCCP6	R/W	Output Compare 6/7	XXXXXXXX$_B$
793D$_H$	Output Compare Register 6	OCCP6	R/W		XXXXXXXX$_B$
793E$_H$	Output Compare Register 7	OCCP7	R/W		XXXXXXXX$_B$
793F$_H$	Output Compare Register 7	OCCP7	R/W		XXXXXXXX$_B$
7940$_H$	Timer Data Register 0	TCDT0	R/W	I/O Timer 0	00000000$_B$
7941$_H$	Timer Data Register 0	TCDT0	R/W		00000000$_B$
7942$_H$	Timer Control Status Register 0	TCCSL0	R/W		00000000$_B$
7943$_H$	Timer Control Status Register 0	TCCSH0	R/W		0XXXXXXX$_B$
7944$_H$	Timer Data Register 1	TCDT1	R/W	I/O Timer 1	00000000$_B$
7945$_H$	Timer Data Register 1	TCDT1	R/W		00000000$_B$
7946$_H$	Timer Control Status Register 1	TCCSL1	R/W		00000000$_B$
7947$_H$	Timer Control Status Register 1	TCCSH1	R/W		0XXXXXXX$_B$
7948$_H$	Timer Register 0/Reload Register 0	TMR0/ TMRLR0	R/W	16-bit Reload Timer 0	XXXXXXXX$_B$
7949$_H$			R/W		XXXXXXXX$_B$
794A$_H$	Timer Register 1/Reload Register 1	TMR1/ TMRLR1	R/W	16-bit Reload Timer 1	XXXXXXXX$_B$
794B$_H$			R/W		XXXXXXXX$_B$
794C$_H$	Timer Register 2/Reload Register 2	TMR2/ TMRLR2	R/W	16-bit Reload Timer 2	XXXXXXXX$_B$
794D$_H$			R/W		XXXXXXXX$_B$
794E$_H$	Timer Register 3/Reload Register 3	TMR3/ TMRLR3	R/W	16-bit Reload Timer 3	XXXXXXXX$_B$
794F$_H$			R/W		XXXXXXXX$_B$

(Continued)

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
79C2H	Setting Prohibited				
79C3H to 79DFH	Reserved				
79E0H	Detect Address Setting Register 0	PADR0	R/W	Address Match Detection 0	XXXXXXXXB
79E1H	Detect Address Setting Register 0	PADR0	R/W		XXXXXXXXB
79E2H	Detect Address Setting Register 0	PADR0	R/W		XXXXXXXXB
79E3H	Detect Address Setting Register 1	PADR1	R/W		XXXXXXXXB
79E4H	Detect Address Setting Register 1	PADR1	R/W		XXXXXXXXB
79E5H	Detect Address Setting Register 1	PADR1	R/W		XXXXXXXXB
79E6H	Detect Address Setting Register 2	PADR2	R/W		XXXXXXXXB
79E7H	Detect Address Setting Register 2	PADR2	R/W		XXXXXXXXB
79E8H	Detect Address Setting Register 2	PADR2	R/W		XXXXXXXXB
79E9H to 79EFH	Reserved				
79F0H	Detect Address Setting Register 3	PADR3	R/W	Address Match Detection 1	XXXXXXXXB
79F1H	Detect Address Setting Register 3	PADR3	R/W		XXXXXXXXB
79F2H	Detect Address Setting Register 3	PADR3	R/W		XXXXXXXXB
79F3H	Detect Address Setting Register 4	PADR4	R/W		XXXXXXXXB
79F4H	Detect Address Setting Register 4	PADR4	R/W		XXXXXXXXB
79F5H	Detect Address Setting Register 4	PADR4	R/W		XXXXXXXXB
79F6H	Detect Address Setting Register 5	PADR5	R/W		XXXXXXXXB
79F7H	Detect Address Setting Register 5	PADR5	R/W		XXXXXXXXB
79F8H	Detect Address Setting Register 5	PADR5	R/W		XXXXXXXXB
79F9H to 7BFFH	Reserved				
7C00H to 7CFFH	Reserved for CAN Interface 1. Refer to “■ CAN CONTROLLERS”				
7D00H to 7DFFH	Reserved for CAN Interface 1. Refer to “■ CAN CONTROLLERS”				
7E00H to 7FFFH	Reserved				

Notes :
- Initial value of “X” represents unknown value.
- Any write access to reserved addresses in I/O map should not be performed. A read access to reserved addresses results reading “X”.

List of Message Buffers (ID Registers)

Address CAN1	Register	Abbreviation	Access	Initial Value
$007C00_H$ to $007C1F_H$	General-purpose RAM	—	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007C20_H$	ID register 0	IDR0	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007C21_H$				
$007C22_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007C23_H$				
$007C24_H$	ID register 1	IDR1	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007C25_H$				
$007C26_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007C27_H$				
$007C28_H$	ID register 2	IDR2	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007C29_H$				
$007C2A_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007C2B_H$				
$007C2C_H$	ID register 3	IDR3	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007C2D_H$				
$007C2E_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007C2F_H$				
$007C30_H$	ID register 4	IDR4	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007C31_H$				
$007C32_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007C33_H$				
$007C34_H$	ID register 5	IDR5	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007C35_H$				
$007C36_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007C37_H$				
$007C38_H$	ID register 6	IDR6	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007C39_H$				
$007C3A_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007C3B_H$				
$007C3C_H$	ID register 7	IDR7	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007C3D_H$				
$007C3E_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007C3F_H$				

(Continued)

List of Message Buffers (DLC Registers and Data Registers)

Address CAN1	Register	Abbreviation	Access	Initial Value
007C60H	DLC register 0	DLCR0	R/W	XXXXXXXXB
007C61H				
007C62H	DLC register 1	DLCR1	R/W	XXXXXXXXB
007C63H				
007C64H	DLC register 2	DLCR2	R/W	XXXXXXXXB
007C65H				
007C66H	DLC register 3	DLCR3	R/W	XXXXXXXXB
007C67H				
007C68H	DLC register 4	DLCR4	R/W	XXXXXXXXB
007C69H				
007C6AH	DLC register 5	DLCR5	R/W	XXXXXXXXB
007C6BH				
007C6CH	DLC register 6	DLCR6	R/W	XXXXXXXXB
007C6DH				
007C6EH	DLC register 7	DLCR7	R/W	XXXXXXXXB
007C6FH				
007C70H	DLC register 8	DLCR8	R/W	XXXXXXXXB
007C71H				
007C72H	DLC register 9	DLCR9	R/W	XXXXXXXXB
007C73H				
007C74H	DLC register 10	DLCR10	R/W	XXXXXXXXB
007C75H				
007C76H	DLC register 11	DLCR11	R/W	XXXXXXXXB
007C77H				
007C78H	DLC register 12	DLCR12	R/W	XXXXXXXXB
007C79H				
007C7AH	DLC register 13	DLCR13	R/W	XXXXXXXXB
007C7BH				
007C7CH	DLC register 14	DLCR14	R/W	XXXXXXXXB
007C7DH				
007C7EH	DLC register 15	DLCR15	R/W	XXXXXXXXB
007C7FH				

(Continued)

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	
	AV_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	$V_{CC} = AV_{CC}$*2
	AVRH	V_{SS} – 0.3	V_{SS} + 6.0	V	$AV_{CC} \geq$ AVRH*2
Input voltage*1	V_I	V_{SS} – 0.3	V_{SS} + 6.0	V	*3
Output voltage*1	V_O	V_{SS} – 0.3	V_{SS} + 6.0	V	*3
Maximum Clamp Current	I_{CLAMP}	–4.0	+4.0	mA	*5
Total Maximum Clamp Current	$\Sigma\|I_{CLAMP}\|$	—	40	mA	*5
“L” level maximum output current	I_{OL}	—	15	mA	*4
“L” level average output current	I_{OLAV}	—	4	mA	*4
“L” level maximum overall output current	ΣI_{OL}	—	100	mA	*4
“L” level average overall output current	ΣI_{OLAV}	—	50	mA	*4
“H” level maximum output current	I_{OH}	—	–15	mA	*4
“H” level average output current	I_{OHAV}	—	–4	mA	*4
“H” level maximum overall output current	ΣI_{OH}	—	–100	mA	*4
“H” level average overall output current	ΣI_{OHAV}	—	–50	mA	*4
Power consumption	P_D	—	240	mW	MB90F351(S), MB90F352(S) +105 °C < $T_A \leq$ +125 °C, Normal operation : maximum frequency 16 MHz
		—	320	mW	MB90F351(S), MB90F352(S) –40 °C < $T_A \leq$ +105 °C, Normal operation : maximum frequency 24 MHz
		—	320	mW	Device other than above
Operating temperature	T_A	–40	+105	°C	
		–40	+125	°C	*6
Storage temperature	T_{STG}	–55	+150	°C	

(Continued)

(Continued)

*1: This parameter is based on V_{SS} = AV_{SS} = 0 V

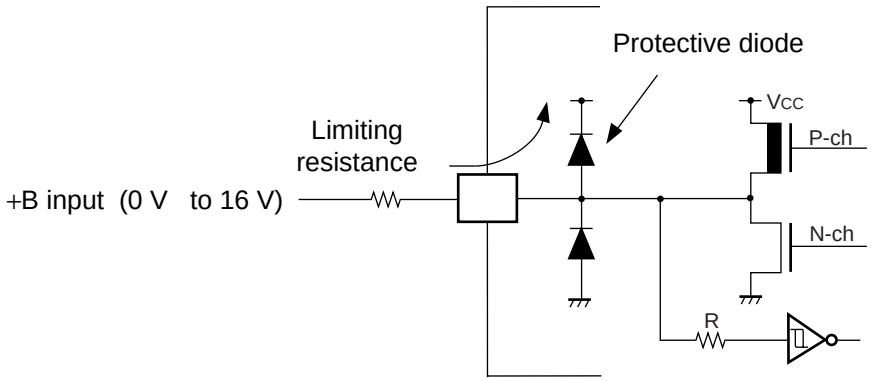
*2: Set AV_{CC} and V_{CC} to the same voltage. Make sure that AV_{CC} does not exceed V_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} when the power is switched on.

*3: V_I and V_O should not exceed V_{CC} + 0.3 V. V_I should not exceed the specified ratings. However if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating.

*4: Applicable to pins: P00 to P07, P10 to P17, P20 to P25, P30 to P37, P40 to P45, P50 to P56, P60 to P67

*5: • Applicable to pins: P00 to P07, P10 to P17, P20 to P25, P30 to P37, P40 to P45, P50 to P56 (for evaluation device : P50 to P55) , P60 to P67
- Use within recommended operating conditions.
- Use at DC voltage (current)
- The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting power supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the +B input pin open.
- Sample recommended circuits:

• Input/output equivalent circuits



*6 : If used exceeding T_A = +105 °C, be sure to contact Fujitsu for reliability limitations.

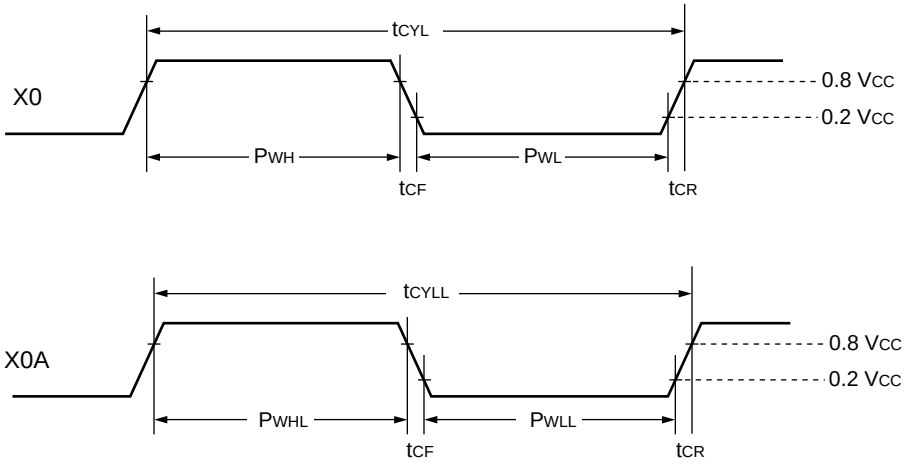
WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

(Continued)

(MB90F352(S)/MB90F351(S): T_A = –40 °C to +105 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)
(MB90F352(S)/MB90F351(S): T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 16 MHz, V_{SS} = AV_{SS} = 0 V)
(Device other than above: T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Internal operating clock frequency (machine clock)	f_{CP}	—	1.5	—	24	MHz	MB90F352/(S), MB90F351/(S) When using main clock (T_A ≤ +105 °C)
					16		MB90F352/(S), MB90F351/(S) When using main clock (T_A ≤ +125 °C)
			1.5	—	24	MHz	Device other than above, When using main clock
	f_{CPL}	—	—	8.192	50	kHz	When using sub clock
Internal operating clock cycle time (machine clock)	t_{CP}	—	41.67	—	666	ns	MB90F352/(S), MB90F351/(S) When using main clock (T_A ≤ +105 °C)
			62.5				MB90F352/(S), MB90F351/(S) When using main clock (T_A ≤ +125 °C)
			41.67	—	666	ns	Device other than above, When using main clock
	t_{CPL}	—	20	122.1	—	µs	When using sub clock

• Clock Timing



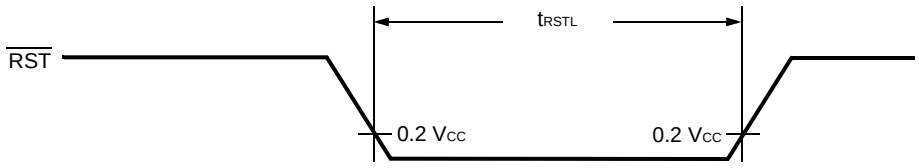
(2) Reset Standby Input

(MB90F352(S)/MB90F351(S): T_A = –40 °C to +105 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)
(MB90F352(S)/MB90F351(S): T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 16 MHz, V_{SS} = AV_{SS} = 0 V)
(Device other than above: T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

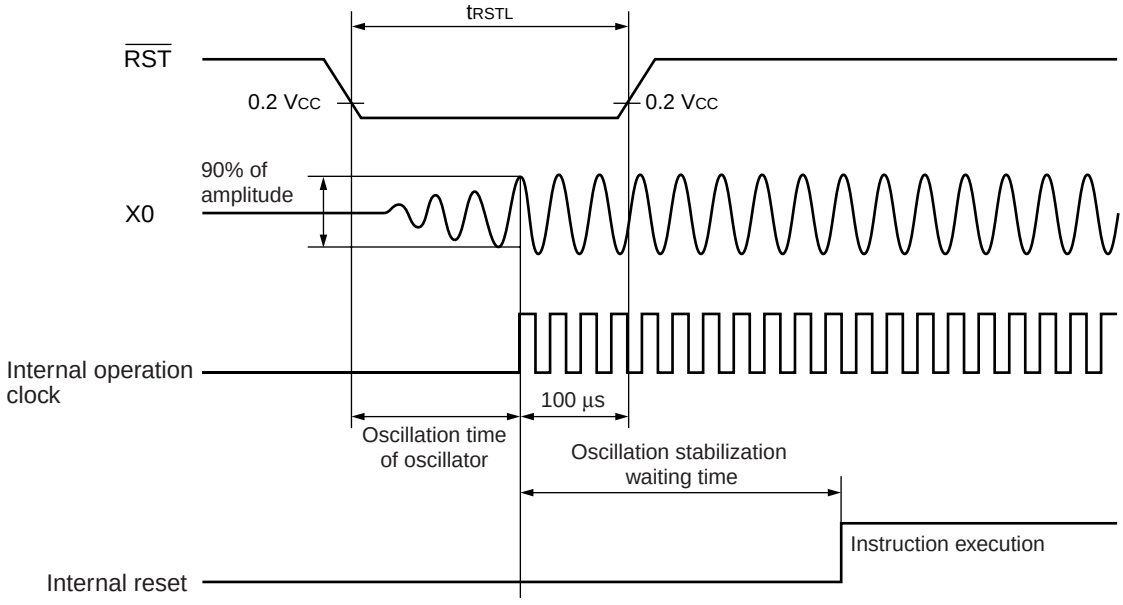
Parameter	Symbol	Pin	Value		Unit	Remarks
			Min	Max		
Reset input time	t_{RSTL}	$\overline{RST}$	500	—	ns	Under normal operation
			Oscillation time of oscillator* + 100 µs	—	µs	In Stop mode, Sub Clock mode, Sub Sleep mode and Watch mode
			100	—	µs	In Main timer mode and PLL timer mode

* : Oscillation time of oscillator is the time that the amplitude reaches 90%.
In the crystal oscillator, the oscillation time is between several ms to tens of ms. In FAR / ceramic oscillators, the oscillation time is between hundreds of µs to several ms. With an external clock, the oscillation time is 0 ms.

Under normal operation:



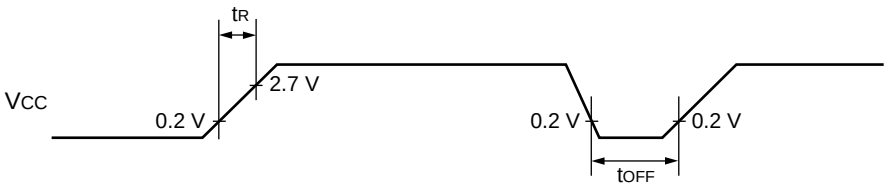
In Stop mode, Sub Clock mode, Sub Sleep mode, Watch mode:



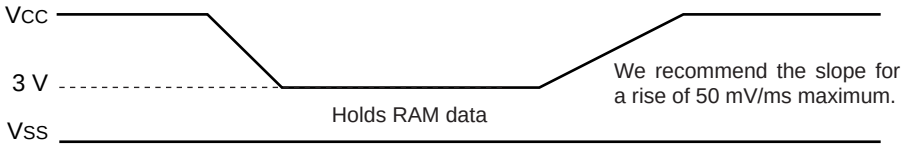
(3) Power On Reset

(MB90F352(S)/MB90F351(S): T_A = –40 °C to +105 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)
(MB90F352(S)/MB90F351(S): T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 16 MHz, V_{SS} = AV_{SS} = 0 V)
(Device other than above: T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Power on rise time	t_R	V_{CC}	—	0.05	30	ms	
Power off time	t_{OFF}	V_{CC}		1	—	ms	Due to repetitive operation



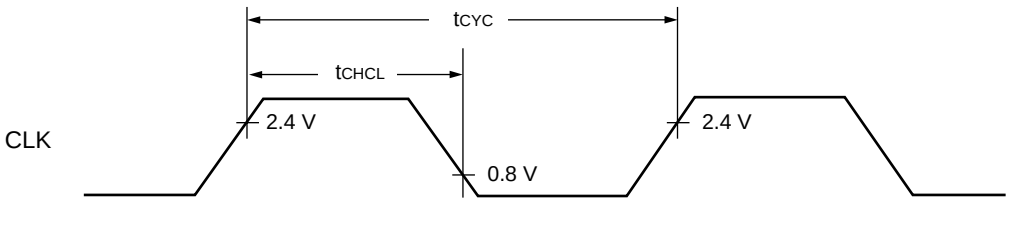
If you change the power supply voltage too rapidly, a power on reset may occur. We recommend that you start up smoothly by restraining voltages when changing the power supply voltage during operation, as shown in the figure below. Perform while not using the PLL clock. However, if voltage drops are within 1 V/s, you can operate while using the PLL clock.

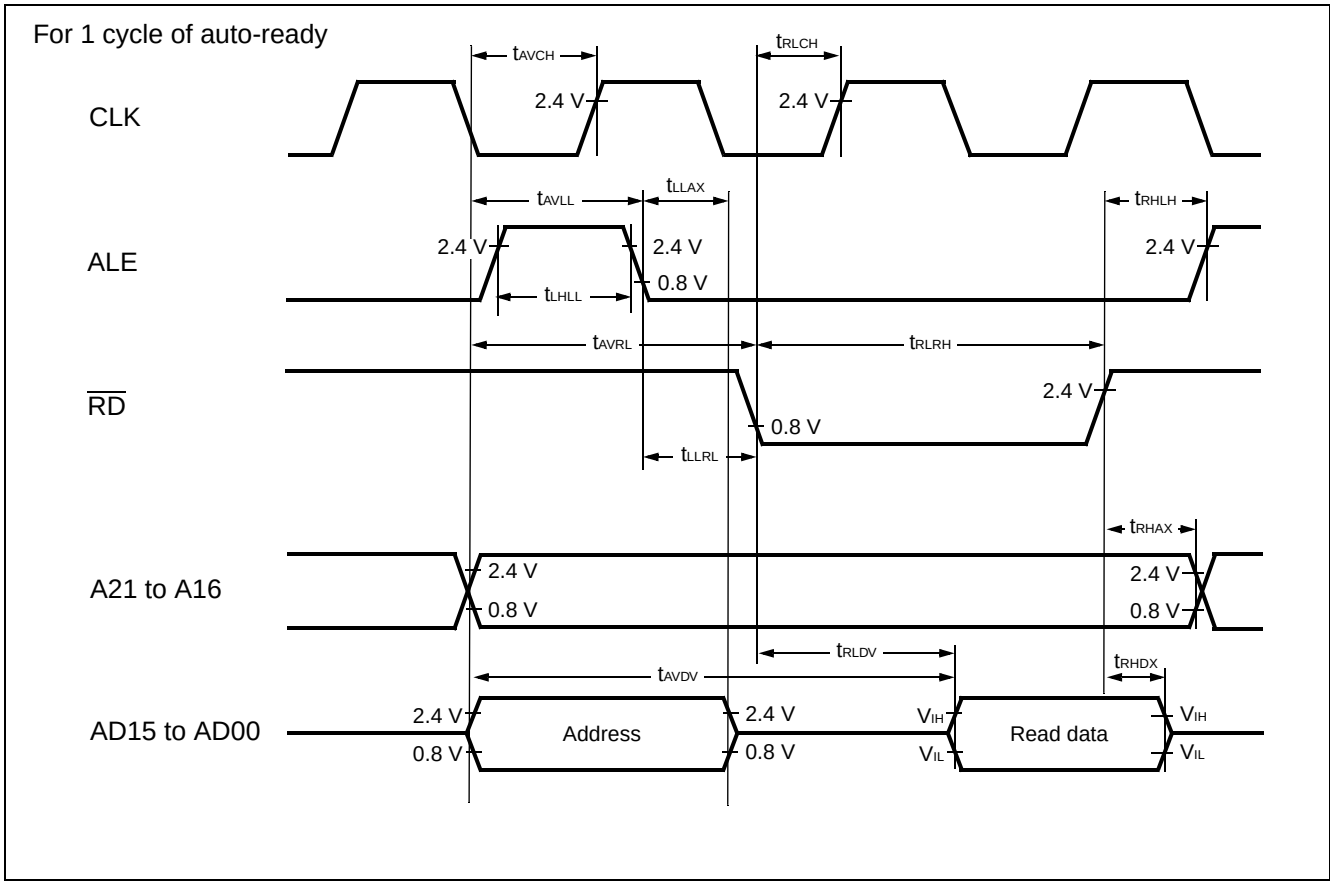


(4) Clock Output Timing

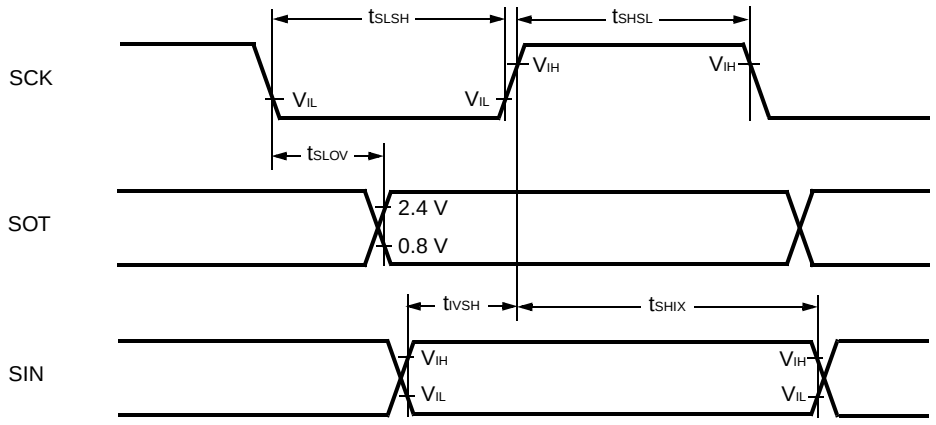
(T_A = –40 °C to +105 °C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, f_{CP} ≤ 24 MHz)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Cycle time	t_{CYC}	CLK	—	62.5	—	ns	f_{CP} = 16 MHz
				41.76	—	ns	f_{CP} = 24 MHz
CLK ↑ → CLK ↓	t_{CHCL}	CLK	—	20	—	ns	f_{CP} = 16 MHz
				13	—	ns	f_{CP} = 24 MHz




For 1 cycle of auto-ready
CLK
ALE
RD
A21 to A16
AD15 to AD00
tAVCH
tRLCH
2.4 V
tAVLL
tLLAX
tRHLH
0.8 V
tLHLL
tAVRL
tRLRH
tLLRL
tRHAX
tRLDV
tRHDX
tAVDV
Address
Read data
VIH
VIL

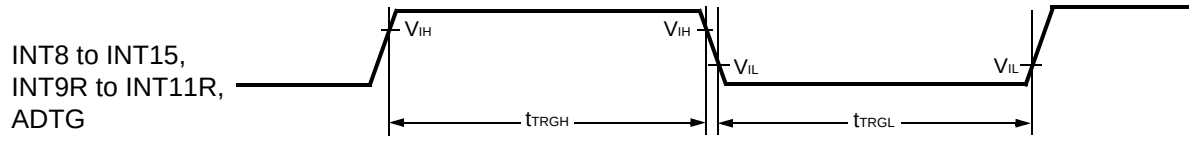
- External Shift Clock Mode



(10) Trigger Input Timing

(MB90F352(S)/MB90F351(S): T_A = –40 °C to +105 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)
(MB90F352(S)/MB90F351(S): T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 16 MHz, V_{SS} = AV_{SS} = 0 V)
(Device other than above: T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH} t_{TRGL}	INT8 to INT15, INT9R to INT11R, ADTG	—	5 t_{CP}	—	ns	



(13) I²C Timing

(MB90F352(S)/MB90F351(S): T_A = –40 °C to +105 °C, V_{CC} = AV_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)
(MB90F352(S)/MB90F351(S): T_A = –40 °C to +125 °C, V_{CC} = AV_{CC} = 5.0 V ± 10%, f_{CP} ≤ 16 MHz, V_{SS} = AV_{SS} = 0 V)
(Device other than above: T_A = –40 °C to +125 °C, V_{CC} = AV_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Condition	Standard-mode		Fast-mode*4		Unit
			Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	R = 1.7 kΩ, C = 50 pF*1	0	100	0	400	kHz
Hold time for (repeated) START condition SDA↓→SCL↓	t_{HDSTA}		4.0	—	0.6	—	µs
"L" width of the SCL clock	t_{LOW}		4.7	—	1.3	—	µs
"H" width of the SCL clock	t_{HIGH}		4.0	—	0.6	—	µs
Set-up time for a repeated START condition SCL↑→SDA↓	t_{SUSTA}		4.7	—	0.6	—	µs
Data hold time SCL↓→SDA↓↑	t_{HDDAT}		0	3.45*2	0	0.9*3	µs
Data set-up time SDA↓↑→SCL↑	t_{SUDAT}		250*5	—	100*5	—	ns
Set-up time for STOP condition SCL↑→SDA↑	t_{SUSTO}		4.0	—	0.6	—	µs
Bus free time between STOP condition and START condition	t_{BUS}		4.7	—	1.3	—	µs

*1 : R,C : Pull-up resistor and load capacitor of the SCL and SDA lines.

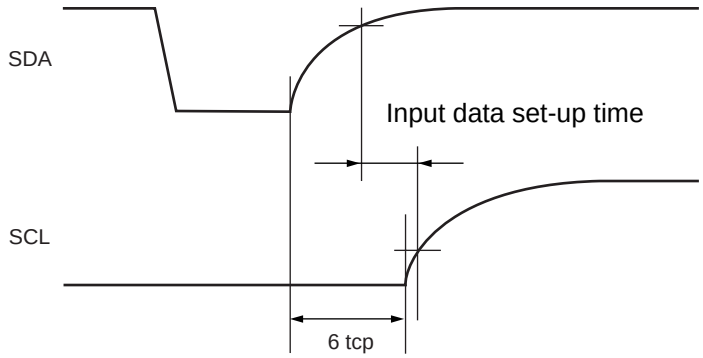
*2 : The maximum t_{HDDAT} has only to be met if the device does not stretch the "L" width (t_{LOW}) of the SCL signal.

*3 : A Fast-mode I²C -bus device can be used in a Standard-mode I²C-bus system, but the requirement t_{SUDAT} ≥ 250 ns must then be met.

*4 : For use at over 100 kHz, set the machine clock to at least 6 MHz.

*5 : Refer to "• Note of SDA, SCL set-up time".

• Note of SDA, SCL set-up time

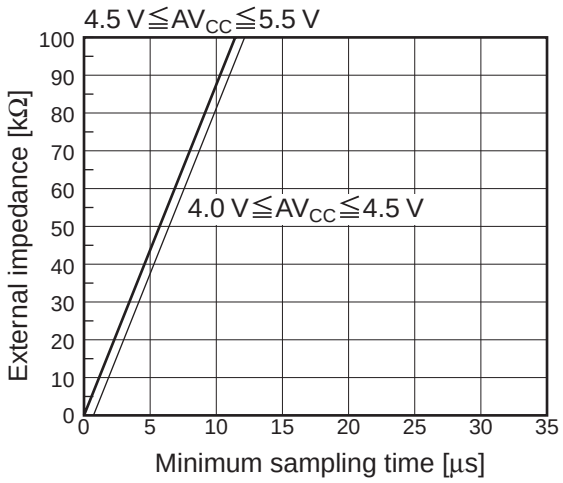


• Flash memory device

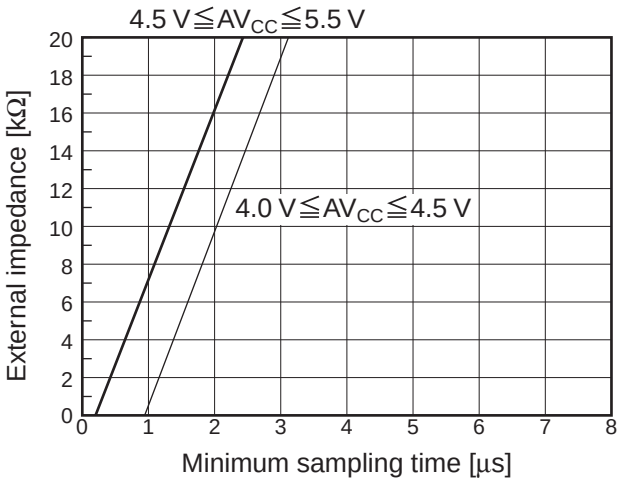
· Relation between External impedance and minimum sampling time

(MB90F352(S), MB90F351A(S), MB90F352A(S), MB90F351TA(S), MB90F352TA(S), MB90F356A(S), MB90F357A(S), MB90F356TA(S), MB90F357TA(S))

[External impedance = 0 kΩ to 100 kΩ]



[External impedance = 0 kΩ to 20 kΩ]

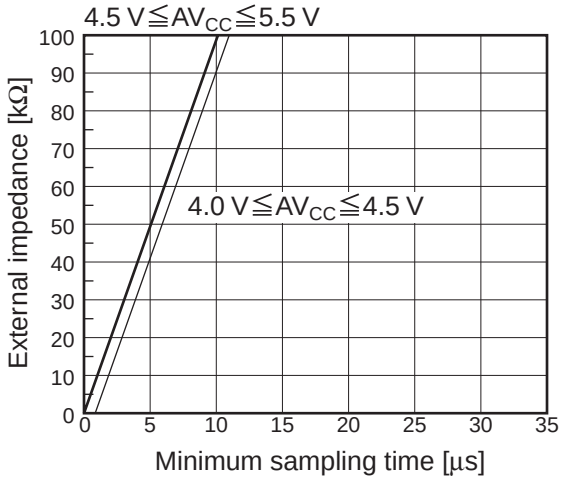


• MASK ROM device

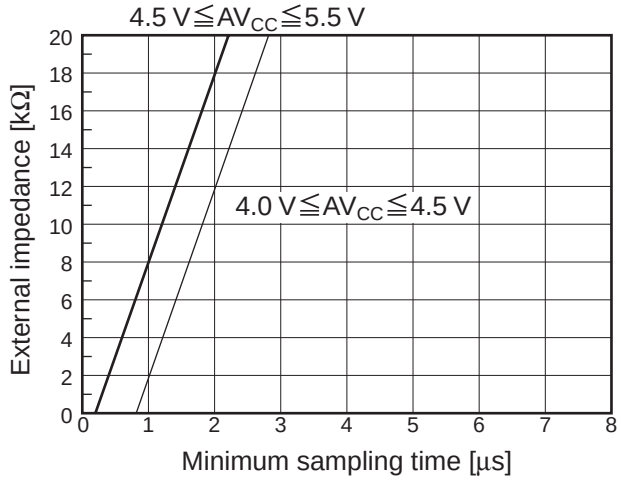
· Relation between External impedance and minimum sampling time

(MB90V340A-101/102/103/104, MB90351A(S), MB90352A(S), MB90351TA(S), MB90352TA(S), MB90356A(S), MB90357A(S), MB90356TA(S), MB90357TA(S))

[External impedance = 0 kΩ to 100 kΩ]



[External impedance = 0 kΩ to 20kΩ]



• **About the error**

Values of relative errors grow larger, as |AVRH – AVSS| becomes smaller.

7. Flash Memory Program/Erase Characteristics

Flash Memory

Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	T_A = +25 °C V_{CC} = 5.0 V	—	1	15	s	Excludes programming prior to erasure
Chip erase time		—	9	—	s	Excludes programming prior to erasure
Word (16-bit width) programming time		—	16	3,600	µs	Except for the overhead time of the system level
Program/Erase cycle	—	10,000	—	—	cycle	
Flash Memory Data Retention Time	Average T_A = +85 °C	20	—	—	year	*

* : This value comes from the technology qualification.
(Using Arrhenius equation to translate high temperature measurements into normalized value at +85 °C)

Dual Operation Flash Memory

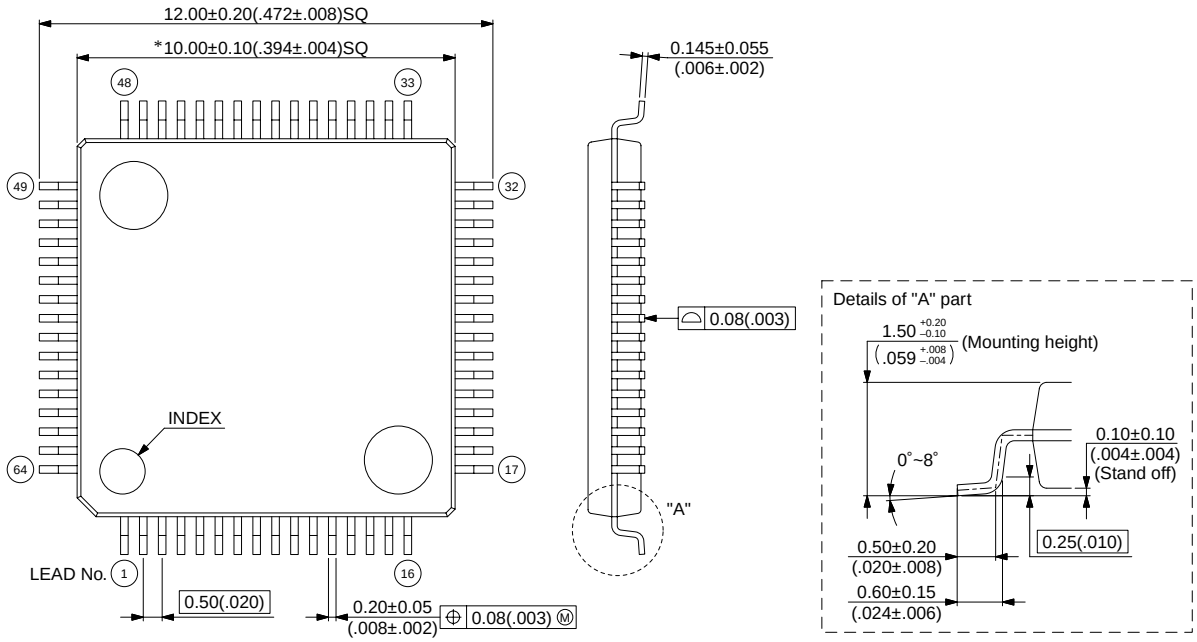
Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time (4 Kbytes sector)	T_A = +25 °C V_{CC} = 5.0 V	—	0.2	0.5	s	Excludes programming prior to erasure
Sector erase time (16 Kbytes sector)		—	0.5	7.5	s	Excludes programming prior to erasure
Chip erase time		—	4.6	—	s	Excludes programming prior to erasure
Word (16-bit width) programming time		—	64	3,600	µs	Except for the overhead time of the system level
Program/Erase cycle	—	10,000	—	—	cycle	
Flash Memory Data Retention Time	Average T_A = +85 °C	20	—	—	year	*

* : This value comes from the technology qualification.
(Using Arrhenius equation to translate high temperature measurements into normalized value at +85 °C)

(Continued)

64-pin plastic LQFP
(FPT-64P-M24)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches) .
Note : The values in parentheses are reference values.