Infineon Technologies - MB90F352SPFM-GS-115E1 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	24MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, WDT
Number of I/O	51
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 15x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-QFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f352spfm-gs-115e1

- **I/O port**
  - General-purpose input/output port (CMOS output)
    - 49 ports (devices without S-suffix : devices that correspond to sub clock)
    - 51 ports (devices with S-suffix : devices that do not correspond to sub clock)
- **Sub clock pin (X0A, X1A)**
  - Yes (using the external oscillation) : devices without S-suffix
  - No (using the sub clock mode at internal CR oscillation) : devices with S-suffix
- **Timer**
  - Timebase timer, watch timer, watchdog timer : 1 channel
  - 8/16-bit PPG timer : 8-bit × 10 channels or 16-bit × 6 channels
  - 16-bit reload timer : 4 channels
  - 16- bit input/output timer
    - 16-bit freerun timer : 2 channels (FRT0 : ICU0/1, FRT1 : ICU 4/5/6/7, OCU 4/5/6/7)
    - 16- bit input capture: (ICU) : 6 channels
    - 16-bit output compare : (OCU) : 4 channels
- **FULL-CAN interface : 1 channel**
  - Compliant with Ver2.0 part A and Ver2.0 part B CAN specifications
  - Flexible message buffering (mailbox and FIFO buffering can be mixed)
  - CAN wake-up function
- **UART (LIN/SCI) : 2 channels**
  - Equipped with full-duplex double buffer
  - Clock-asynchronous or clock-synchronous serial transmission is available.
- **I²C interface* : 1 channel**
  - Up to 400 Kbit/s transfer rate
- **DTP/External interrupt : 8 channels, CAN wakeup : 1 channel**
  - Module for activation of extended intelligent I/O service (EI²OS), DMA, and generation of external interrupt by external input.
- **Delay interrupt generator module**
  - Generates interrupt request for task switching.
- **8/10-bit A/D converter : 15 channels**
  - Resolution is selectable between 8-bit and 10-bit.
  - Activation by external trigger input is allowed.
  - Conversion time : 3 μs (at 24-MHz machine clock, including sampling time)
- **Program patch function**
  - Address matching detection for 6 address pointers.
- **Capable of changing input voltage level for port**
  - Automotive/CMOS-Schmitt (initial level is Automotive in single chip mode)
  - TTL level (corresponds to external bus pins only, initial level of these pins is TTL in external bus mode)
- **Low voltage/CPU operation detection reset (devices with T-suffix)**
  - Detects low voltage (4.0 V ± 0.3 V) and resets automatically
  - Resets automatically when program is runaway and counter is not cleared within interval time (approx. 262 ms : external 4 MHz)

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■ PRODUCT LINEUP 2

Parameter \ Part Number	MB90351A, MB90352A	MB90351TA, MB90352TA	MB90351AS, MB90352AS	MB90351TAS, MB90352TAS	MB90V340A-101	MB90V340A-102
CPU	F^2MC-16LX CPU					
System clock	On-chip PLL clock multiplier (×1, ×2, ×3, ×4, ×6, 1/2 when PLL stops) Minimum instruction execution time : 42 ns (oscillation clock 4 MHz, PLL × 6)					
ROM	MASK ROM 64Kbytes : MB90351A(S), MB90351TA(S) 128Kbytes : MB90352A(S), MB90352TA(S)				External	
RAM	4 Kbytes				30 Kbytes	
Emulator-specific power supply*	—				Yes	
Sub clock pin (X0A, X1A) (Max 100 kHz)	Yes		No		No	Yes
Clock monitor function	No					
Low voltage/CPU operation detection reset	No	Yes	No	Yes	No	
Operating voltage range	3.5 V to 5.5 V : at normal operating (not using A/D converter) 4.0 V to 5.5 V : at using A/D converter 4.5 V to 5.5 V : at using external bus				5 V ± 10%	
Operating temperature range	−40 °C to +125 °C				—	
Package	LQFP-64				PGA-299	
UART	2 channels				5 channels	
	Wide range of baud rate settings using a dedicated reload timer Special synchronous options for adapting to different synchronous serial protocols LIN functionality working either as master or slave LIN device					
I^2C (400 Kbps)	1 channel				2 channels	
A/D Converter	15 channels				24 channels	
	10-bit or 8-bit resolution Conversion time : Min 3 µs includes sample time (per one channel)					
16-bit Reload Timer (4 channels)	Operation clock frequency : fsys/2^1, fsys/2^3, fsys/2^5 (fsys = Machine clock frequency) Supports External Event Count function.					
16-bit I/O Timer (2 channels)	I/O Timer 0 (clock input FRCK0) corresponds to ICU 0/1. I/O Timer 1 (clock input FRCK1) corresponds to ICU 4/5/6/7, OCU 4/5/6/7.				I/O Timer 0 corresponds to ICU 0/1/2/3, OCU 0/1/2/3. I/O Timer 1 corresponds to ICU 4/5/6/7, OCU 4/5/6/7.	
	Signals an interrupt when overflowing. Supports Timer Clear when a match with Output Compare (Channel 0, 4) . Operation clock frequency : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4, fsys/2^5, fsys/2^6, fsys/2^7 (fsys = Machine clock frequency)					

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■ PRODUCT LINEUP 3

Part Number / Parameter	MB90F356A, MB90F357A	MB90F356TA, MB90F357TA	MB90F356AS, MB90F357AS	MB90F356TAS, MB90F357TAS
CPU	F^2MC-16LX CPU			
System clock	On-chip PLL clock multiplier (×1, ×2, ×3, ×4, ×6, 1/2 when PLL stops) Minimum instruction execution time : 42 ns (oscillation clock 4 MHz, PLL × 6)			
ROM	Dual operation flash memory 64Kbytes : MB90F356A(S), MB90F356TA(S) 128Kbytes : MB90F357A(S), MB90F357TA(S)			
RAM	4 Kbytes			
Emulator-specific power supply*1	—			
Sub clock pin (X0A, X1A)	Yes		No (internal CR oscillation can be used as sub clock)	
Clock monitor function	Yes			
Low voltage/CPU operation detection reset	No	Yes	No	Yes
Operating voltage range	3.5 V to 5.5 V : at normal operating (not using A/D converter) 3.5 V to 5.5 V : at using A/D converter/Flash programming 3.5 V to 5.5 V : at using external bus			
Operating temperature range	–40 °C to +125 °C			
Package	LQFP-64			
UART	2 channels			
	Wide range of baud rate settings using a dedicated reload timer Special synchronous options for adapting to different synchronous serial protocols LIN functionality working either as master or slave LIN device			
I^2C (400 Kbps)	1 channel			
A/D Converter	15 channels			
	10-bit or 8-bit resolution Conversion time : Min 3 µs includes sample time (per one channel)			
16-bit Reload Timer (4 channels)	Operation clock frequency : fsys/2^1, fsys/2^3, fsys/2^5 (fsys = Machine clock frequency) Supports External Event Count function.			
16-bit I/O Timer (2 channels)	I/O Timer 0 (clock input FRCK0) corresponds to ICU 0/1. I/O Timer 1 (clock input FRCK1) corresponds to ICU 4/5/6/7, OCU 4/5/6/7.			
	Signals an interrupt when overflowing. Supports Timer Clear when a match with Output Compare (Channel 0, 4) . Operation clock frequency : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4, fsys/2^5, fsys/2^6, fsys/2^7 (fsys = Machine clock frequency)			
16-bit Output Compare	4 channels			
	Signals an interrupt when 16-bit I/O Timer matches with output compare registers. A pair of compare registers can be used to generate an output signal.			

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■ PRODUCT LINEUP 4

Part Number / Parameter	MB90356A, MB90357A	MB90356TA, MB90357TA	MB90356AS, MB90357AS	MB90356TAS, MB90357TAS	MB90V340A-103	MB90V340A-104
CPU	F²MC-16LX CPU					
System clock	On-chip PLL clock multiplier (×1, ×2, ×3, ×4, ×6, 1/2 when PLL stops) Minimum instruction execution time : 42 ns (oscillation clock 4 MHz, PLL × 6)					
ROM	MASK ROM 64Kbytes : MB90356A(S), MB90356TA(S) 128Kbytes : MB90357A(S), MB90357TA(S)				External	
RAM	4 Kbytes				30 Kbytes	
Emulator-specific power supply*	—				Yes	
Sub clock pin (X0A, X1A)	Yes		No (internal CR oscillation can be used as sub clock)		No (internal CR oscillation can be used as sub clock)	Yes
Clock monitor function	Yes					
Low voltage/CPU operation detection reset	No	Yes	No	Yes	No	
Operating voltage range	3.5 V to 5.5 V : at normal operating (not using A/D converter) 4.0 V to 5.5 V : at using A/D converter 4.5 V to 5.5 V : at using external bus				5 V ± 10%	
Operating temperature range	−40 °C to +125 °C				—	
Package	LQFP-64				PGA-299	
UART	2 channels				5 channels	
	Wide range of baud rate settings using a dedicated reload timer Special synchronous options for adapting to different synchronous serial protocols LIN functionality working either as master or slave LIN device					
I²C (400 Kbps)	1 channel				2 channels	
A/D Converter	15 channels				24 channels	
	10-bit or 8-bit resolution Conversion time : Min 3 µs includes sample time (per one channel)					
16-bit Reload Timer (4 channels)	Operation clock frequency : fsys/2^1, fsys/2^3, fsys/2^5 (fsys = Machine clock frequency) Supports External Event Count function.					
16-bit I/O Timer (2 channels)	I/O Timer 0 (clock input FRCK0) corresponds to ICU 0/1. I/O Timer 1 (clock input FRCK1) corresponds to ICU 4/5/6/7, OCU 4/5/6/7.				I/O Timer 0 corresponds to ICU 0/1/2/3, OCU 0/1/2/3. I/O Timer 1 corresponds to ICU 4/5/6/7, OCU 4/5/6/7.	
	Signals an interrupt when overflowing. Supports Timer Clear when a match with Output Compare (Channel 0, 4) . Operation clock frequency : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4, fsys/2^5, fsys/2^6, fsys/2^7 (fsys = Machine clock frequency)					

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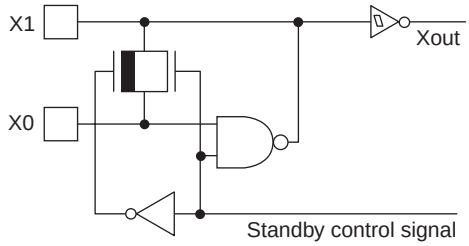
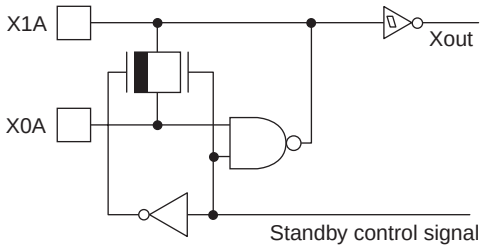
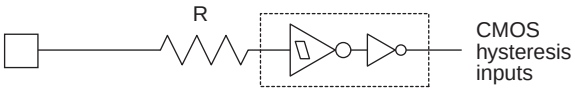
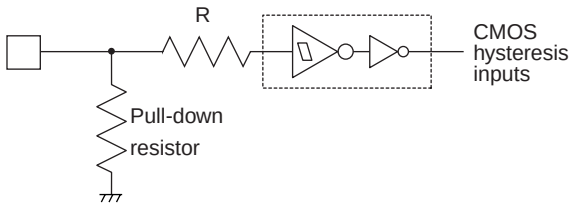
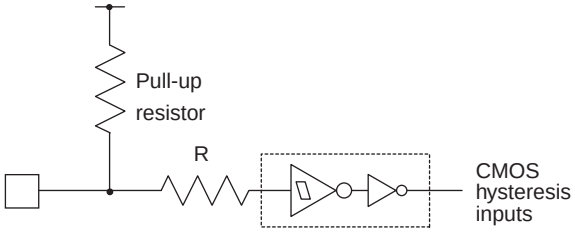
Parameter \ Part Number	MB90356A, MB90357A	MB90356TA, MB90357TA	MB90356AS, MB90357AS	MB90356TAS, MB90357TAS	MB90V340A-103	MB90V340A-104
16-bit Output Compare	4 channels				8 channels	
	Signals an interrupt when 16-bit I/O Timer matches with output compare registers. A pair of compare registers can be used to generate an output signal.					
16-bit Input Capture	6 channels				8 channels	
	Retains freerun timer value by (rising edge, falling edge or rising & falling edge), signals an interrupt.					
8/16-bit Programmable Pulse Generator	6 channels (16-bit)/10 channels (8-bit) 8-bit reload counters × 12 8-bit reload registers for L pulse width × 12 8-bit reload registers for H pulse width × 12				8 channels (16-bit)/16 channels (8-bit) 8-bit reload counters × 16 8-bit reload registers for L pulse width × 16 8-bit reload registers for H pulse width × 16	
	Supports 8-bit and 16-bit operation modes. A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler + 8-bit reload counter. Operation clock frequency : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4 or 128 µs@fosc = 4 MHz (fsys = Machine clock frequency, fosc = Oscillation clock frequency)					
CAN Interface	1 channel				3 channels	
	Conforms to CAN Specification Version 2.0 Part A and B. Automatic re-transmission in case of error Automatic transmission responding to Remote Frame Prioritized 16 message buffers for data and ID Supports multiple messages. Flexible configuration of acceptance filtering : Full bit compare/Full bit mask/Two partial bit masks Supports up to 1 Mbps.					
External Interrupt	8 channels				16 channels	
	Can be used rising edge, falling edge, starting up by H/L level input, external interrupt, extended intelligent I/O services (EI^{2}OS) and DMA.					
D/A converter	—				2 channels	
I/O Ports	Virtually all external pins can be used as general purpose I/O port. All push-pull outputs Bit-wise settable as input/output or peripheral module signal Settable as CMOS schmitt trigger/ automotive inputs TTL input level settable for external bus (only for external bus pin)					
Flash Memory	—					
Corresponding EVA name	MB90V340A-104		MB90V340A-103		—	

* : It is setting of Jumper switch (TOOL VCC) when Emulator (MB2147-01) is used.
Please refer to the Emulator hardware manual about details.

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		Oscillation circuit • High-speed oscillation feedback resistor = approx. 1 MΩ
B		Oscillation circuit • Low-speed oscillation feedback resistor = approx. 10 MΩ
C		Mask ROM device: • CMOS hysteresis input pin Flash memory device: • CMOS input pin
D		Mask ROM device: • CMOS hysteresis input pin • Pull-down resistor value: approx. 50 kΩ Flash memory device: • CMOS input pin • No Pull-down
E		CMOS hysteresis input pin • Pull-up resistor value: approx. 50 kΩ

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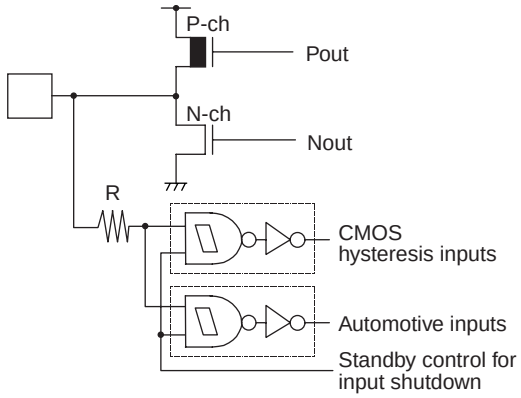
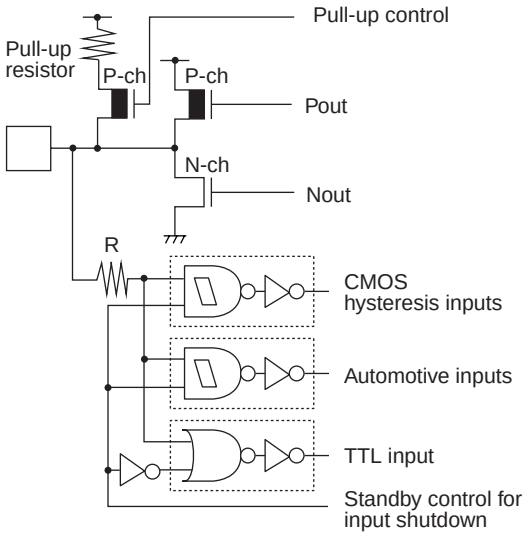
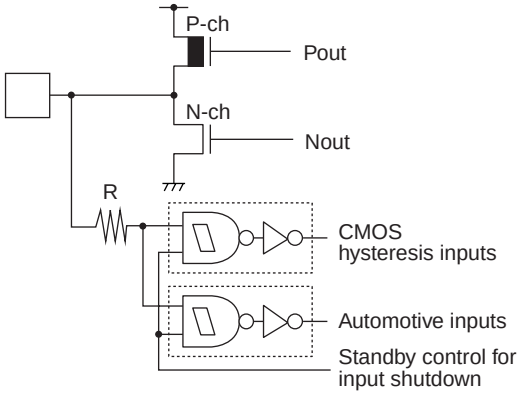
Type	Circuit	Remarks
F		• CMOS level output (I_{OL} = 4 mA, I_{OH} = –4 mA) • CMOS hysteresis inputs (With the stand-by-time input shutdown function) • Automotive input (With the standby-time input shutdown function)
G		• CMOS level output (I_{OL} = 4 mA, I_{OH} = –4 mA) • CMOS hysteresis inputs (With the stand-by-time input shutdown function) • Automotive input (With the standby-time input shutdown function) • TTL input (With the standby-time input shutdown function) • Programmable pull-up resistor: approx. 50 kΩ
H		• CMOS level output (I_{OL} = 3 mA, I_{OH} = –3 mA) • CMOS hysteresis inputs (With the stand-by-time input shutdown function) • Automotive input (With the standby-time input shutdown function)

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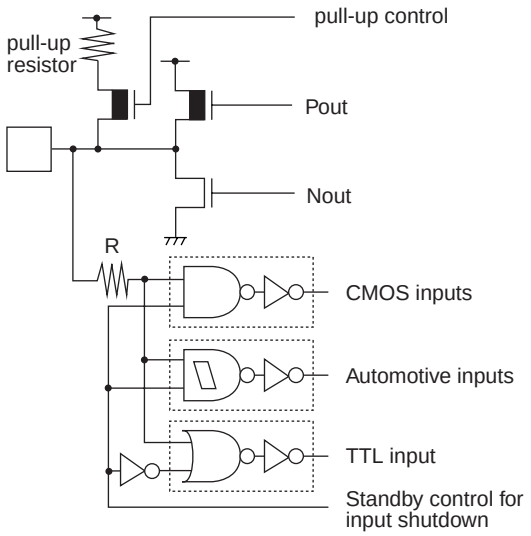
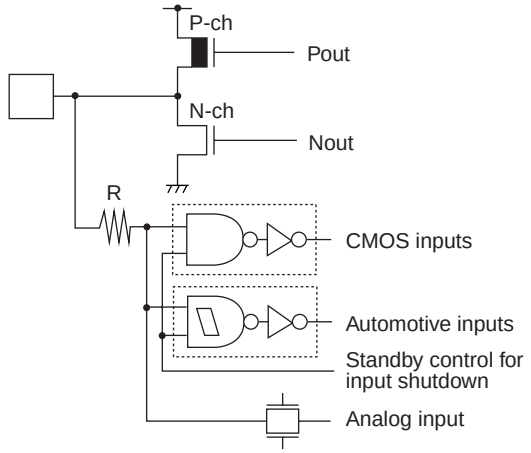
Type	Circuit	Remarks
N		• CMOS level output (I_{OL} = 4 mA, I_{OH} = –4 mA) • CMOS inputs (With the standby-time input shutdown function) • Automotive input (With the standby-time input shutdown function) • TTL input (With the standby-time input shutdown function) • Programmable pull-up resistor: approx. 50 kΩ
O		• CMOS level output (I_{OL} = 4 mA, I_{OH} = –4 mA) • CMOS inputs (With the standby-time input shutdown function) • Automotive input (With the standby-time input shutdown function) • A/D analog input

9. Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs

Make sure to turn on the A/D converter power supply (AV_{CC}, AVRH) and analog inputs (AN0 to AN14) after turning-on the digital power supply (V_{CC}) .

Turn-off the digital power after turning off the A/D converter power supply and analog inputs. In this case, make sure that the voltage does not exceed AVRH or AV_{CC} (turning on/off the analog and digital power supplies simultaneously is acceptable).

10. Connection of Unused Pins of A/D Converter if A/D Converter is used

Connect unused pins of A/D converter to $AV_{CC} = V_{CC}$, $AV_{SS} = AVRH = V_{SS}$.

11. Notes on Energization

To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during energization at 50 µs or more (0.2 V to 2.7 V) .

12. Stabilization of power supply voltage

A sudden change in the power supply voltage may cause the device to malfunction even within the specified V_{CC} power supply voltage operating range. Therefore, the V_{CC} power supply voltage should be stabilized.

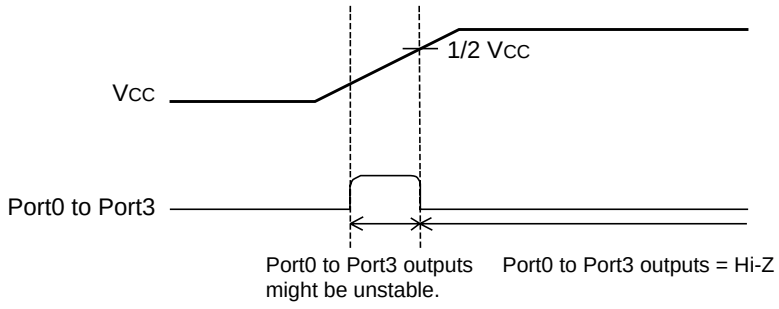
For reference, the power supply voltage should be controlled so that V_{CC} ripple variations (peak-to-peak value) at commercial frequencies (50 Hz to 60 Hz) fall below 10% of the standard V_{CC} power supply voltage and the coefficient of fluctuation does not exceed 0.1 V/ms at instantaneous power switching.

13. Initialization

In the device, there are internal registers which are initialized only by a power-on reset. To initialize these registers, turn on the power again.

14. Port 0 to port 3 output during Power-on (External-bus mode)

As shown below, when power is turned on in external-bus mode, there is a possibility that output signal of Port 0 to Port 3 might be unstable.



15. Notes on using CAN Function

To use CAN function, please set “1” to DIRECT bit of CAN direct mode register (CDMR).
If DIRECT bit is set to “0” (initial value), wait states will be performed when accessing CAN registers.

Note : Please refer to section “22.15 CAN Direct Mode Register” in Hardware Manual of MB90350 series for detail of CAN direct mode register.

Address	Register	Abbreviation	Access	Resource name	Initial value
3C$_H$	PPG 6 Operation Mode Control Register	PPGC6	W, R/W	16-bit Programmable Pulse Generator 6/7	0X000XX1$_B$
3D$_H$	PPG 7 Operation Mode Control Register	PPGC7	W, R/W		0X000001$_B$
3E$_H$	PPG 6/7 Count Clock Select Register	PPG67	R/W		000000X0$_B$
3F$_H$	Reserved				
40$_H$	PPG 8 Operation Mode Control Register	PPGC8	W, R/W	16-bit Programmable Pulse Generator 8/9	0X000XX1$_B$
41$_H$	PPG 9 Operation Mode Control Register	PPGC9	W, R/W		0X000001$_B$
42$_H$	PPG 8/9 Count Clock Select Register	PPG89	R/W		000000X0$_B$
43$_H$	Reserved				
44$_H$	PPG A Operation Mode Control Register	PPGCA	W, R/W	16-bit Programmable Pulse Generator A/B	0X000XX1$_B$
45$_H$	PPG B Operation Mode Control Register	PPGCB	W, R/W		0X000001$_B$
46$_H$	PPG A/B Count Clock Select Register	PPGAB	R/W		000000X0$_B$
47$_H$	Reserved				
48$_H$	PPG C Operation Mode Control Register	PPGCC	W,R/W	16-bit Programmable Pulse Generator C/D	0X000XX1$_B$
49$_H$	PPG D Operation Mode Control Register	PPGCD	W,R/W		0X000001$_B$
4A$_H$	PPG C/D Count Clock Select Register	PPGCD	R/W		000000X0$_B$
4B$_H$	Reserved				
4C$_H$	PPG E Operation Mode Control Register	PPGCE	W,R/W	16-bit Programmable Pulse Generator E/F	0X000XX1$_B$
4D$_H$	PPG F Operation Mode Control Register	PPGCF	W,R/W		0X000001$_B$
4E$_H$	PPG E/F Count Clock Select Register	PPGEF	R/W		000000X0$_B$
4F$_H$	Reserved				
50$_H$	Input Capture Control Status Register 0/1	ICS01	R/W	Input Capture 0/1	00000000$_B$
51$_H$	Input Capture Edge Register 0/1	ICE01	R/W, R		XXX0X0XX$_B$
52$_H$, 53$_H$	Reserved				
54$_H$	Input Capture Control Status Register 4/5	ICS45	R/W	Input Capture 4/5	00000000$_B$
55$_H$	Input Capture Edge Register 4/5	ICE45	R		XXXXXXXX$_B$
56$_H$	Input Capture Control Status Register 6/7	ICS67	R/W	Input Capture 6/7	00000000$_B$
57$_H$	Input Capture Edge Register 6/7	ICE67	R/W, R		XXX000XX$_B$
58$_H$ to 5B$_H$	Reserved				
5C$_H$	Output Compare Control Status Register 4	OCS4	R/W	Output Compare 4/5	0000XX00$_B$
5D$_H$	Output Compare Control Status Register 5	OCS5	R/W		0XX00000$_B$

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Address	Register	Abbrevia-tion	Access	Resource name	Initial value
$A4_H$	DMA Stop Status Register	DSSR	R/W	DMA	00000000_B
$A5_H$	Automatic Ready Function Selection Register	ARSR	W	External Memory Access	$0011XX00_B$
$A6_H$	External Address Output Control Register	HACR	W		00000000_B
$A7_H$	Bus Control Signal Selection Register	ECSR	W		$0000000X_B$
$A8_H$	Watchdog Control Register	WDTC	R,W	Watchdog Timer	$XXXXX111_B$
$A9_H$	Timebase Timer Control Register	TBTC	W,R/W	Timebase timer	$1XX00100_B$
AA_H	Watch Timer Control Register	WTC	R,R/W	Watch Timer	$1X001000_B$
AB_H	Reserved				
AC_H	DMA Enable Register L	DERL	R/W	DMA	00000000_B
AD_H	DMA Enable Register H	DERH	R/W		00000000_B
AE_H	Flash Control Status Register (Flash Devices only. Otherwise reserved)	FMCS	R,R/W	Flash Memory	$000X0000_B$
AF_H	Reserved				
$B0_H$	Interrupt Control Register 00	ICR00	W,R/W	Interrupt Control	00000111_B
$B1_H$	Interrupt Control Register 01	ICR01	W,R/W		00000111_B
$B2_H$	Interrupt Control Register 02	ICR02	W,R/W		00000111_B
$B3_H$	Interrupt Control Register 03	ICR03	W,R/W		00000111_B
$B4_H$	Interrupt Control Register 04	ICR04	W,R/W		00000111_B
$B5_H$	Interrupt Control Register 05	ICR05	W,R/W		00000111_B
$B6_H$	Interrupt Control Register 06	ICR06	W,R/W		00000111_B
$B7_H$	Interrupt Control Register 07	ICR07	W,R/W		00000111_B
$B8_H$	Interrupt Control Register 08	ICR08	W,R/W		00000111_B
$B9_H$	Interrupt Control Register 09	ICR09	W,R/W		00000111_B
BA_H	Interrupt Control Register 10	ICR10	W,R/W		00000111_B
BB_H	Interrupt Control Register 11	ICR11	W,R/W		00000111_B
BC_H	Interrupt Control Register 12	ICR12	W,R/W		00000111_B
BD_H	Interrupt Control Register 13	ICR13	W,R/W		00000111_B
BE_H	Interrupt Control Register 14	ICR14	W,R/W		00000111_B
BF_H	Interrupt Control Register 15	ICR15	W,R/W		00000111_B
$C0_H$ to $C9_H$	Reserved				

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
7908H	Reload Register L4	PRLL4	R/W	16-bit Programmable Pulse Generator 4/5	XXXXXXXXB
7909H	Reload Register H4	PRLH4	R/W		XXXXXXXXB
790AH	Reload Register L5	PRLL5	R/W		XXXXXXXXB
790BH	Reload Register H5	PRLH5	R/W		XXXXXXXXB
790CH	Reload Register L6	PRLL6	R/W	16-bit Programmable Pulse Generator 6/7	XXXXXXXXB
790DH	Reload Register H6	PRLH6	R/W		XXXXXXXXB
790EH	Reload Register L7	PRLL7	R/W		XXXXXXXXB
790FH	Reload Register H7	PRLH7	R/W		XXXXXXXXB
7910H	Reload Register L8	PRLL8	R/W	16-bit Programmable Pulse Generator 8/9	XXXXXXXXB
7911H	Reload Register H8	PRLH8	R/W		XXXXXXXXB
7912H	Reload Register L9	PRLL9	R/W		XXXXXXXXB
7913H	Reload Register H9	PRLH9	R/W		XXXXXXXXB
7914H	Reload Register LA	PRLLA	R/W	16-bit Programmable Pulse Generator A/B	XXXXXXXXB
7915H	Reload Register HA	PRLHA	R/W		XXXXXXXXB
7916H	Reload Register LB	PRLLB	R/W		XXXXXXXXB
7917H	Reload Register HB	PRLHB	R/W		XXXXXXXXB
7918H	Reload Register LC	PRLLC	R/W	16-bit Programmable Pulse Generator C/D	XXXXXXXXB
7919H	Reload Register HC	PRLHC	R/W		XXXXXXXXB
791AH	Reload Register LD	PRLLD	R/W		XXXXXXXXB
791BH	Reload Register HD	PRLHD	R/W		XXXXXXXXB
791CH	Reload Register LE	PRLLE	R/W	16-bit Programmable Pulse Generator E/F	XXXXXXXXB
791DH	Reload Register HE	PRLHE	R/W		XXXXXXXXB
791EH	Reload Register LF	PRLLF	R/W		XXXXXXXXB
791FH	Reload Register HF	PRLHF	R/W		XXXXXXXXB
7920H	Input Capture Register 0	IPCP0	R	Input Capture 0/1	XXXXXXXXB
7921H	Input Capture Register 0	IPCP0	R		XXXXXXXXB
7922H	Input Capture Register 1	IPCP1	R		XXXXXXXXB
7923H	Input Capture Register 1	IPCP1	R		XXXXXXXXB
7924H to 7927H	Reserved				
7928H	Input Capture Register 4	IPCP4	R	Input Capture 4/5	XXXXXXXXB
7929H	Input Capture Register 4	IPCP4	R		XXXXXXXXB
792AH	Input Capture Register 5	IPCP5	R		XXXXXXXXB
792BH	Input Capture Register 5	IPCP5	R		XXXXXXXXB

(Continued)

List of Message Buffers (ID Registers)

Address CAN1	Register	Abbreviation	Access	Initial Value
$007C00_H$ to $007C1F_H$	General-purpose RAM	—	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007C20_H$	ID register 0	IDR0	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007C21_H$				
$007C22_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007C23_H$				
$007C24_H$	ID register 1	IDR1	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007C25_H$				
$007C26_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007C27_H$				
$007C28_H$	ID register 2	IDR2	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007C29_H$				
$007C2A_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007C2B_H$				
$007C2C_H$	ID register 3	IDR3	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007C2D_H$				
$007C2E_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007C2F_H$				
$007C30_H$	ID register 4	IDR4	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007C31_H$				
$007C32_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007C33_H$				
$007C34_H$	ID register 5	IDR5	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007C35_H$				
$007C36_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007C37_H$				
$007C38_H$	ID register 6	IDR6	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007C39_H$				
$007C3A_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007C3B_H$				
$007C3C_H$	ID register 7	IDR7	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007C3D_H$				
$007C3E_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007C3F_H$				

(Continued)

(Continued)

Address CAN1	Register	Abbreviation	Access	Initial Value
007C40H	ID register 8	IDR8	R/W	XXXXXXXXB XXXXXXXXB
007C41H				
007C42H				XXXXXXXXB XXXXXXXXB
007C43H				
007C44H	ID register 9	IDR9	R/W	XXXXXXXXB XXXXXXXXB
007C45H				
007C46H				XXXXXXXXB XXXXXXXXB
007C47H				
007C48H	ID register 10	IDR10	R/W	XXXXXXXXB XXXXXXXXB
007C49H				
007C4AH				XXXXXXXXB XXXXXXXXB
007C4BH				
007C4CH	ID register 11	IDR11	R/W	XXXXXXXXB XXXXXXXXB
007C4DH				
007C4EH				XXXXXXXXB XXXXXXXXB
007C4FH				
007C50H	ID register 12	IDR12	R/W	XXXXXXXXB XXXXXXXXB
007C51H				
007C52H				XXXXXXXXB XXXXXXXXB
007C53H				
007C54H	ID register 13	IDR13	R/W	XXXXXXXXB XXXXXXXXB
007C55H				
007C56H				XXXXXXXXB XXXXXXXXB
007C57H				
007C58H	ID register 14	IDR14	R/W	XXXXXXXXB XXXXXXXXB
007C59H				
007C5AH				XXXXXXXXB XXXXXXXXB
007C5BH				
007C5CH	ID register 15	IDR15	R/W	XXXXXXXXB XXXXXXXXB
007C5DH				
007C5EH				XXXXXXXXB XXXXXXXXB
007C5FH				

(Continued)

Address CAN1	Register	Abbreviation	Access	Initial Value
007CF0H to 007CF7H	Data register 14 (8 bytes)	DTR14	R/W	XXXXXXXXB to XXXXXXXXB
007CF8H to 007CFFH	Data register 15 (8 bytes)	DTR15	R/W	XXXXXXXXB to XXXXXXXXB

(Continued)

Interrupt cause	EI²OS corre-sponding	DMA ch number	Interrupt vector		Interrupt control register	
			Number	Address	Number	Address
UART 2 RX	Y2	14	#39	FFFF60H	ICR14	0000BEH
UART 2 TX	Y1	15	#40	FFFF5CH		
Flash Memory	N	—	#41	FFFF58H	ICR15	0000BFH
Delayed interrupt	N	—	#42	FFFF54H		

Y1 : Usable

Y2 : Usable, with EI²OS stop function

N : Unusable

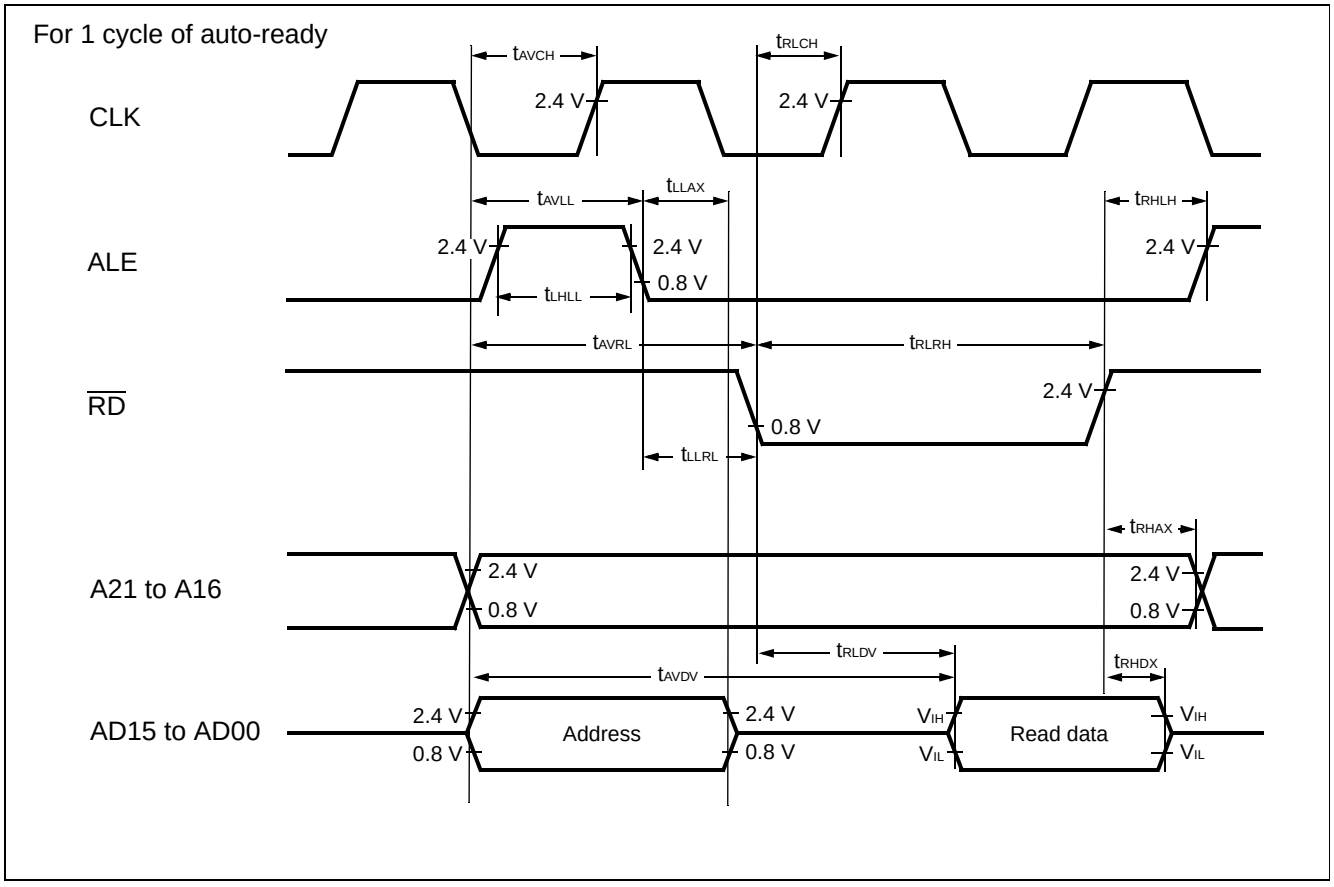
Notes :
- The peripheral resources sharing the ICR register have the same interrupt level.
- When two peripheral resources share the ICR register, only one can use EI²OSat a time.
- When either of the two peripheral resources sharing the ICR register specifies EI²OS, the other one cannot use interrupts.

(5) Bus Timing (Read)

(T_A = –40°C to +105°C, V_{CC} = 5.0 V ± 10 %, V_{SS} = 0.0 V, f_{CP} ≤ 24 MHz)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
ALE pulse width	t_{LHLL}	ALE	—	$t_{CP}/2 - 10$	—	ns	
Valid address ⇒ ALE ↓ time	t_{AVLL}	ALE, A21 to A16, AD15 to AD00		$t_{CP}/2 - 20$	—	ns	
ALE ↓ ⇒ Address valid time	t_{LLAX}	ALE, AD15 to AD00		$t_{CP}/2 - 15$	—	ns	
Valid address ⇒ $\overline{RD}$ ↓ time	t_{AVRL}	A21 toA16, AD15 to AD00, $\overline{RD}$		$t_{CP} - 15$	—	ns	
Valid address ⇒ Valid data input	t_{AVDV}	A21 to A16, AD15 to AD00		—	$5\ t_{CP}/2 - 60$	ns	
$\overline{RD}$ pulse width	t_{RLRH}	$\overline{RD}$		$(n^*+3/2)\ t_{CP} - 20$	—	ns	
$\overline{RD}$ ↓ ⇒ Valid data input	t_{RLDV}	$\overline{RD}$, AD15 to AD00		—	$(n^*+3/2)\ t_{CP} - 50$	ns	
$\overline{RD}$ ↑ ⇒ Data hold time	t_{RHDX}	$\overline{RD}$, AD15 to AD00		0	—	ns	
$\overline{RD}$ ↑ ⇒ ALE ↑ time	t_{RHLH}	$\overline{RD}$, ALE		$t_{CP}/2 - 15$	—	ns	
$\overline{RD}$ ↑ ⇒ Address valid time	t_{RHAX}	$\overline{RD}$, A21 to A16		$t_{CP}/2 - 10$	—	ns	
Valid address ⇒ CLK ↑ time	t_{AVCH}	A21 to A16, AD15 to AD00, CLK		$t_{CP}/2 - 16$	—	ns	
$\overline{RD}$ ↓ ⇒ CLK ↑ time	t_{RLCH}	$\overline{RD}$, CLK		$t_{CP}/2 - 15$	—	ns	
ALE ↓ ⇒ $\overline{RD}$ ↓ time	t_{LLRL}	ALE, $\overline{RD}$		$t_{CP}/2 - 15$	—	ns	

* : n: number of ready cycles


For 1 cycle of auto-ready
CLK
ALE
RD
A21 to A16
AD15 to AD00
tAVCH
tRLCH
2.4 V
tAVLL
tLLAX
tRHLH
0.8 V
tLHLL
tAVRL
tRLRH
tLLRL
tRHAX
tRLDV
tRHDX
tAVDV
Address
Read data
VIH
VIL

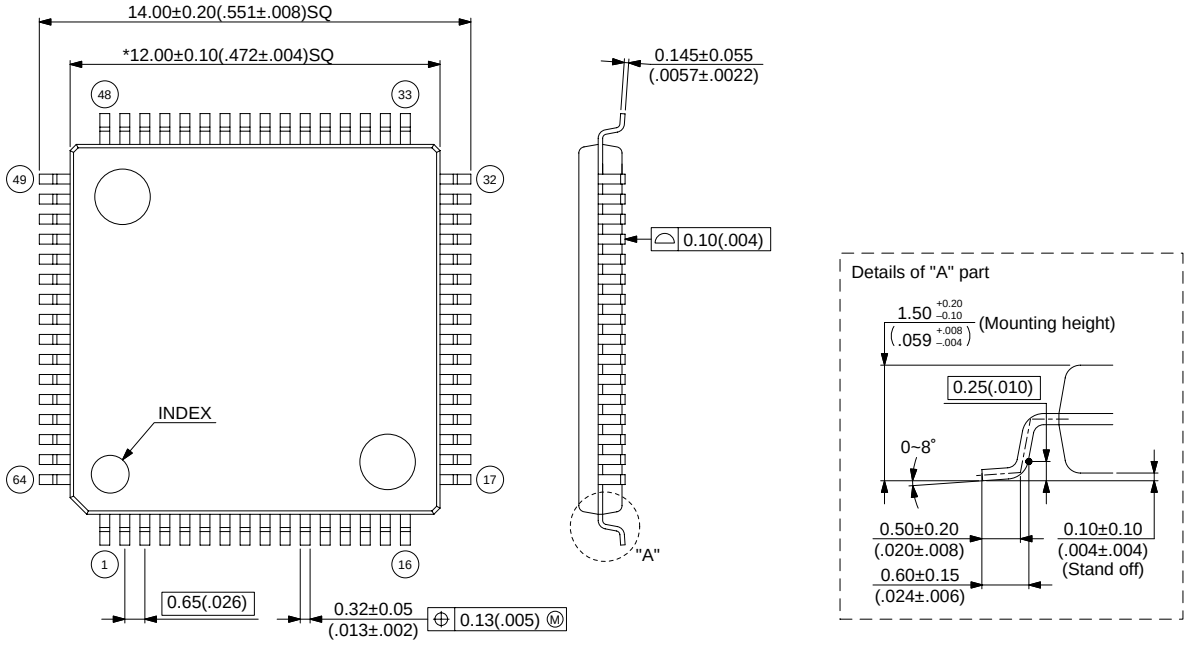
(Continued)

Part number	Package	Remarks
MB90F351APMC1	64-pin plastic LQFP FPT-64P-M24 10 mm □, 0.50 mm pitch	Dual operation Flash memory products* (64 Kbytes)
MB90F351ASPMC1		
MB90F351TAPMC1		
MB90F351TASPMC1		
MB90F356APMC1		
MB90F356ASPMC1		
MB90F356TAPMC1		
MB90F356TASPMC1		
MB90F352APMC1	64-pin plastic LQFP FPT-64P-M24 10 mm □, 0.50 mm pitch	Dual operation Flash memory products* (128 Kbytes)
MB90F352ASPMC1		
MB90F352TAPMC1		
MB90F352TASPMC1		
MB90F357APMC1		
MB90F357ASPMC1		
MB90F357TAPMC1		
MB90F357TASPMC1		
MB90351APMC1	64-pin plastic LQFP FPT-64P-M24 10 mm □, 0.50 mm pitch	MASK ROM products* (64 Kbytes)
MB90351ASPMC1		
MB90351TAPMC1		
MB90351TASPMC1		
MB90356APMC1		
MB90356ASPMC1		
MB90356TAPMC1		
MB90356TASPMC1		
MB90352APMC1	64-pin plastic LQFP FPT-64P-M24 10 mm □, 0.50 mm pitch	MASK ROM products* (128 Kbytes)
MB90352ASPMC1		
MB90352TAPMC1		
MB90352TASPMC1		
MB90357APMC1		
MB90357ASPMC1		
MB90357TAPMC1		
MB90357TASPMC1		
MB90V340A-101	299-pin ceramic PGA PGA-299C-A01	Device for evaluation
MB90V340A-102		
MB90V340A-103		
MB90V340A-104		

* : These devices are under development.

64-pin plastic LQFP
(FPT-64P-M23)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches) .
Note : The values in parentheses are reference values.

(Continued)